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(54) Video signal output circuit comprising semiconductor integrated circuit

Videosignalausgabeschaltung mit integrierter Halbleiterschaltung

Circuit de sortie de signal vidéo avec circuit intégré à semi-conducteur

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates to a semiconductor integrated circuit and a video signal output circuit which are arranged to amplify and output a video signal,

2. Description of the Related Art

[0002] Conventionally, a video signal output circuit which amplifies and outputs a video signal, such as an NTSC (National Television Standards Committee) signal, is known. The video signal is made up of composite signals including a vertical synchronizing signal with a low frequency (for example, 60 Hz), a luminance signal with a frequency up to several MHz, etc. Video signal output circuits according to the related art have been improved to allow transmission of the video signal including these component signals without distortion of the waveform of the video signal.

[0003] FIG. 10 illustrates the composition of a video signal output circuit according to the related art. In the video signal output circuit 10 of FIG. 10, an operational amplifier 1 includes a non-inverted input terminal T1 and an inverted input terminal T2. A video signal is input to the non-inverted input terminal T1 of the operational amplifier 1, and the inverted input terminal T2 of the operation amplifier 1 is connected to an output terminal To of the operational amplifier 1. The video signal amplified by the operational amplifier 1 is output from the output terminal To. Moreover, a capacitor C1 which is provided for removing the direct-current component contained in the video signal output is connected to the output terminal To.

[0004] In the video signal output circuit 10 of FIG. 10, a capacitor with a large capacitance is used as the capacitor C1 in order to eliminate distortion of the waveform of the video signal output. However, if the capacitance of the capacitor C1 is increased, the capacitor C1 is increased in volume (size) and the mounting area of the capacitor C1 is increased. This is not appropriate for the video signal output circuit from a viewpoint of miniaturization of products.

[0005] FIG. 11 illustrates the composition of another video signal output circuit according to the related art. In the video signal output circuit 20 of FIG. 11, a circuit which is provided for compensating distortion (sag) of the waveform of a video signal is arranged so that the capacitance of the capacitor C1 is decreased.

[0006] In the video signal output circuit 20 of FIG. 11, the operational amplifier 1 is provided with a sag compensation terminal Ts in addition to the output terminal To. The sag compensation terminal Ts is connected to both the inverted input terminal T2 of the operational amplifier 1 and one end of a resistor R1. The other end of the resistor R1 is connected to the output terminal To of the operational amplifier 1.

[0007] In the video signal output circuit 20 of FIG. 11, a capacitor C2 is arranged between one end of the capacitor C1 and the sag compensation terminal Ts of the operational amplifier 1, and this capacitor C2 is connected in parallel with the capacitor C1. The video signal that is output from the operational amplifier 1 and passed through the capacitor C1 is returned back to the sag compensation terminal Ts.

[0008] In the video signal output circuit 20 of FIG. 11, the capacitance of the capacitor C1 can be reduced by this composition, and distortion of the waveform of the video signal output can be compensated (sag compensation). For example, Japanese Laid-Open Patent Publication No. 2004-274434 discloses a video signal output circuit which performs sag compensation for a video signal.

[0009] However, the use of a lowered supply voltage in recent years makes it difficult for the video signal output circuit to perform sag compensation. For example, if the supply voltage to the operational amplifier 1 as illustrated in FIG. 11 is changed to a lowered supply voltage, the dynamic range of the operational amplifier 1 will be insufficient for the amplitude of the video signal, which will make it difficult to perform sag compensation for the video signal effectively. As a result, a lack of a synchronizing signal in the video signal will take place and detecting a synchronizing signal in the video signal will be impossible.

[0010] US 2005/0105364 and US 2006/0280436 disclose a video amplifier with a DC blocking capacitor and a feedback network to perform sag compensation.

SUMMARY OF THE INVENTION

[0011] In one aspect of the invention, the present disclosure provides a semiconductor integrated circuit and a video signal output circuit which can prevent a lack of a synchronizing signal in a video signal output from the semiconductor integrated circuit or the video signal output circuit and can contribute to the miniaturization of products with low cost.

[0012] The present invention provides a semiconductor integrated circuit according to appended claim 1.

[0013] Other objects, features and advantages of the invention will be apparent from the following detailed description

when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

FIG. 1 is a diagram illustrating the composition of a video signal output circuit of an embodiment of the invention.
FIG. 2 is a diagram for explaining a sag ratio of a video signal.
FIG. 3 is a diagram for explaining setting of capacitance values of a capacitor C10 and a capacitor C20.
FIG. 4 is a diagram for explaining setting of the capacitance values of the capacitor C10 and the capacitor C20.
FIG. 5A and FIG. 5B are diagrams for explaining a video signal for which sag compensation is performed by the video signal output circuit of the present embodiment in comparison with a video signal for which sag compensation is performed by the video signal output circuit according the related art.
FIG. 6 is a diagram illustrating the composition of a first modification of the video signal output circuit of the present embodiment.
FIG. 7 is a diagram illustrating the composition of a second modification of the video signal output circuit of the present embodiment.
FIG. 8 is a diagram illustrating the composition of a third modification of the video signal output circuit of the present embodiment.
FIG. 9 is a diagram illustrating the composition of a fourth modification of the video signal output circuit of the present embodiment.
FIG. 10 is a diagram illustrating the composition of a video signal output circuit according to the related art.
FIG. 11 is a diagram illustrating the composition of another video signal output circuit according to the related art.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0015] A description will now be given of embodiments of the invention with reference to the accompanying drawings.

[0016] FIG. 1 illustrates the composition of a video signal output circuit 100 of an embodiment of the invention.

[0017] As illustrated in FIG. 1, the video signal output circuit 100 of this embodiment includes a semiconductor integrated circuit 110, a capacitor C10, a capacitor C20, a resistor R10, and a resistor R20,

[0018] The semiconductor integrated circuit 110 of this embodiment has an operational amplifier 111, and this operational amplifier 111 amplifies a video signal which is input to the semiconductor integrated circuit 110. The semiconductor integrated circuit 110 includes an external terminal T10, an external terminal Ts, the operational amplifier 111, a resistor R30, and a resistor Rsag.

[0019] In the semiconductor integrated circuit 110, the video signal is input to a non-inverted input terminal T11 of the operational amplifier 111. An inverted input terminal T12 of the operational amplifier 111 is grounded through the resistor R30. The inverted input terminal T12 of the operational amplifier 111 is connected through the resistor Rsag to the external terminal T10 which is an output terminal of the operational amplifier 111.

[0020] The resistor Rsag is a resistor which is provided for performing sag compensation for the video signal. One end of the resistor Rsag is connected to the external terminal T10, and the other end of the resistor Rsag is connected to the external terminal Ts.

[0021] In the video signal output circuit 100 of this embodiment, the capacitor C10 is a capacitor which is provided tor removing the direct-current component contained in the video signal. The resistor R10 and the resistor R20 are provided to constitute an impedance-matching resistor (75Ω). The capacitor C10, the resistor R10, and the resistor R20 are connected in series to constitute a high-pass filter F. One end of the capacitor C10 is connected to the external terminal T10 of the semiconductor integrated circuit 110. One end of the resistor R20 is grounded. The signal output from a junction point H of the capacitor C10 and the resistor R10 is an output signal of the video signal output circuit 100.

[0022] The capacitor C20 is a capacitor which is provided for performing sag compensation for a video signal output from the operational amplifier 111. One end of the capacitor C20 is connected to the external terminal Ts of the semiconductor integrated circuit 110, and the other end of the capacitor C20 is connected to the external terminal T10 of the semiconductor integrated circuit 110.

[0023] Therefore, in the video signal output circuit 100 of this embodiment, the resistor Rsag and the capacitor C20 are connected in parallel between the inverted input terminal T12 and the output terminal of the operational amplifier 111. Namely, in this embodiment, the video signal before being passed through the capacitor C10 is returned back to the non-inverted input terminal T12 of the operational amplifier 111.

[0024] If a resistance of the resistor Rsag, a capacitance of the capacitor C10 and a capacitance of the capacitor C20 in this embodiment are set to optimal values, the video signal output circuit 100 which has the above-described composition can decrease the capacitance values of the capacitor C10 and the capacitor C20 from those of the video signal

output circuit according to the related art, and can prevent a lack of a synchronizing signal in the video signal output.

[0025] In this embodiment, the optimal values of the resistance of the resistor Rsag, the capacitance of the capacitor C10 and the capacitance of the capacitor C20 are determined as follows. The resistance of the resistor Rsag, the capacitance of the capacitor C10 and the capacitance of the capacitor C20 are set to the optimal values which change a sag ratio (which will be described later) of the video signal to be smaller than or equal to a predetermined value so that distortion of the waveform of the video signal output from the video signal output circuit 100 does not influence the quality of the resulting image. Specifically, in this embodiment, the resistance of the resistor Rsag, the capacitance of the capacitor C10, and the capacitance of the capacitor C20 are set to the optimal values which changed the sag ratio of the video signal to be smaller than or equal to 0.5% so that distortion of the waveform of the video signal does not influence equality of the resulting image.

[0026] Next, a description will be given of a sag ratio of a video signal with reference to FIG. 2. FIG. 2 is a diagram for explaining a sag ratio of a video signal.

[0027] The video signal P illustrated in FIG. 2 is an output signal of the video signal output circuit 100. As illustrated in FIG. 2, the sag ratio of the video signal P is represented by A'/A x 100(%) where A denotes an amplitude of the video signal P and A' denotes a distortion of the waveform of the video signal P. Specifically, in this embodiment, the sag ratio is changed to be smaller than or equal to 0.5% by setting the resistance of the resistor Rsag, the capacitance of the capacitor C10 and the capacitance of the capacitor C20 to the optimal values.

[0028] Next, setting of the capacitance values of the capacitor C10 and the capacitor C20 will be described with reference to FIG. 3 and FIG. 4. FIG. 3 is a diagram for explaining setting of the capacitance values of the capacitor and the capacitor C20. FIG. 4 is a diagram for explaining setting of the capacitance values of the capacitor G10 and the capacitor C20.

[0029] In FIG. 3, the relationship between the capacitance value of the capacitor C10 and the sag ratio when the capacitance value of the capacitor C20 is changed are illustrated. Specifically, in FIG. 3, the relationship between the capacitance value of the capacitor C10 and the sag ratio when the value of the capacitor C20 is set to 0 μF is indicated by the curve S1, the relationship between the capacitance value of the capacitor C10 and the sag ratio when the value of the capacitor C20 is set to 1 μF is indicated by the curve S2, the relationship between the capacitance value of the capacitor C10 and the sag ratio when the value of the capacitor C20 is set 2 μF is indicated by the curve S3, and the relationship between the capacitance value of the capacitor C10 and the sag ratio when the value of the capacitor C20 is set to 4 μF is indicated by the curve S4.

[0030] In this embodiment, as illustrated in FIG. 3, when the capacitance of the capacitor C10 is equal to a specific value, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is selected, and the capacitance value of the capacitor C10 and the capacitance value of the capacitor C20 are optimized based on the selected value.

[0031] Specifically, when the capacitance of the capacitor C10 is equal to 47 μF, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is 1 μF (on the curve S2 as illustrated in FIG. 3). Thus, 1 μF is selected as the capacitance value of the capacitor C20.

[0032] Next, when the capacitance of the capacitor C10 is equal to about 100 μF, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is selected similarly. Art this time, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is 1 μF.

[0033] Next, when the capacitance of the capacitor C10 is about 200 μF, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is selected similarly. At this time, the capacitance value of the capacitor C20 with which the sag ratio is the smallest is 2 μF (on the curve S3 as illustrated in FIG. 3), In this manner, the capacitance value of the capacitor C20 with which the sag ratio is the smallest when the capacitance of the capacitor C10 is equal to a specific value is selected.

[0034] FIG. 3 illustrates the measurement data of the sag ratio which is determined from the output signal of the semiconductor integrated circuit 110 when the capacitance value of the capacitor C10 and the capacitance value of the capacitor C20 are changed in the video signal output circuit 100 of this embodiment.

[0035] In FIG. 4, the curve which indicates the relationship between the pickup points of the capacitance value of the capacitor C10 in FIG. 3 and the measurement data of the sag ratio is illustrated. As illustrated in FIG. 4, the points where the sag ratio is smaller than or equal to 0.5% include the point at which the capacitance value of the capacitor C10 is about 220 μF and the capacitance value of the capacitor C20 is 2 μF, the point at which the capacitance value of the capacitor C10 is about 300 μF and the capacitance value of the capacitor C20 is 4 μF, and the point at which the capacitance value of the capacitor C10 is about 500 μF and the capacitance value of the capacitor C20 is 4 μF.

[0036] In this embodiment, the capacitor C10 = 220 μF and the capacitor C20 = 2 μF are selected as the optimal capacitance value of the capacitor C10 and the optimal capacitance value of the capacitor C20 which change the sag ratio to be smaller than or equal to 0.5%. This is because an electric field capacitor can be used as the capacitor C10 and a chip capacitor can be used as the capacitor C20, and at least one of the capacitor C10 and the capacitor C20 can be decreased in size.

[0037] For example, if the capacitor C10 = 300 μF and the capacitor C20 = 4 μF are selected as the optimal capacitance

value of the capacitor C10 and the optimal capacitance value of the capacitor C20 which change the sag ratio to be smaller than or equal to 0.5%, both the capacitor C10 and the capacitor C20 must be an electric field capacitor. In this case, both the capacitor 10 and the capacitor C20 cannot be decreased in size, and it is difficult for the video signal output circuit of this embodiment to contribute to the miniaturization of products.

[0038] Next, setting of the resistance of the resistor Rsag in the video signal output circuit 100 of this embodiment will be described.

[0039] A cut-off frequency fc of the high-pass filter F constituted by the capacitor C10, the resistor R10 and the resistor R20 in the video signal output circuit 100 is determined as follows. The cut-off frequency fc is represented by the following Equation 1.

Equation 1:

$$f_C = \frac{1}{2 \cdot \pi \cdot R_{load} \cdot C10}$$

[0040] In the above Equation 1, R_{load} denotes a combined resistance of the resistor R10 and the resistor R20, and the combined resistance R_{load} of this embodiment is represented by R_{load} = R10 + R20.

[0041] Next, at the cut-off frequency fc, a voltage gain A_v(fc) of the video signal output circuit 100 after sag compensation for the video signal is performed with the resistor Rsag and the capacitor C20 is determined. The voltage gain A_v(fc) is determined by the following Equation 2.

Equation 2:

$$A_V(f_C) = \frac{1}{\beta} + \frac{\left(R_{sag} // \dfrac{1}{\omega_{fc} \cdot C20} \right)}{R30}$$

[0042] β in the above Equation 2 denotes a value which is computed by the following Equation 3.

Equation 3:

$$\beta = \frac{R30}{R30 + 0} = 1$$

[0043] In this embodiment, the resistance of the resistor Rsag can be determined in accordance with the foregoing Equations 1, 2, and 3. In this embodiment, the capacitor C10 = 220 μF and the capacitor C20 = 2 μ F are selected as the optimal capacitance value of the capacitor C10 and the optimal capacitance value of the capacitor C20 which change

the sag ratio to be smaller than or equal to 0.5%. By substituting these values of the capacitors C10 and C20 into the Equations 1 and 2, a resistance value of the resistor Rsag which changes the sag ratio to be smaller than or equal to 0.5% can be determined.

[0044] After the resistance value of the resistor Rsag is determined, it is determined whether a voltage gain $A_V(DC)$, which is determined by the following Equation 4 into which the resistance value of the resistor Rsag determined by the above Equations 1 to 3 is substituted, falls within the dynamic range of the operational amplifier 111.

Equation 4:

$$A_V(DC) = \frac{1}{\beta} + \frac{R_{sag}}{R30}$$

[0045] If the voltage gain $A_V(DC)$ determined by the above Equation 4 does not fall within the dynamic range of the operational amplifier 111, the operational amplifier 111 does not output the video signal correctly. In this case, the capacitance value of capacitor C10 and the capacitance value of capacitor C20 must be adjusted to change the resistance value of the resistor Rsag to be smaller.

[0046] It the voltage gain $A_V(DC)$ falls within the dynamic range of the operational amplifier 111, the resistance of the resistor Rsag can be set to the value determined by the above Equation 4.

[0047] Next, a description will be given of an example in which the resistance of the resistor Rsag is determined in the case of the capacitor C10 = 220 μ F, the capacitor C20 = 2 μF and the resistor R_{load} = 150Ω.

[0048] The following Equation 5 is the same as the above Equation 1 into which the capacitance value of the capacitor C10 and the resistance value of the resistor R_{load} are substituted.

Equation 5:

$$f_c = \frac{1}{2 \cdot \pi \cdot 150 \cdot 220\mu} = 4.8Hz$$

[0049] By the above Equation 5, the cut-off frequency fc of the high pass filter F can be determined as fc = 4.8Hz. The following Equation 6 is the same as the above Equation 2 into which all of the above-mentioned values and the cut-off frequency fc (= 4.8Hz) determined by the above Equation 5 are substituted.

Equation 6:

$$1.571 = 1.258 + \frac{\left(R_{sag} \,//\, \frac{1}{2 \cdot \pi \cdot 4.8 \cdot 2.2\mu} \right)}{12k}$$

[0050] By the above Equation 6, a resistance value of the resistor Rsag can be determined as Rsag = 5kΩ. If the voltage gain $A_V(DC)$ determined by the above Equation 4 into which this resistance value of the resistor Rsag is substituted falls within the dynamic range of the operational amplifier 111, the resistance of the resistor Rsag can be set to 5kΩ. In

this embodiment, the sag ratio can be changed to be smaller than or equal to 0.5% by using the computed resistance value or the resistor Rsag.

[0051] By setting the respective values of the resistor Rsag, the capacitor C10 and the capacitor C20 in the video signal output circuit 100 of this embodiment as described above, it is possible to perform sag compensation for the video signal sufficiently even when a lowered supply voltage is used as the supply voltage to the operational amplifier 111, and it is possible to prevent a lack of a synchronizing signal in the video signal output from the video signal output circuit 100.

[0052] FIG. 5A and FIG. 5B are diagrams for explaining a video signal for which sag compensation is performed by the video signal output circuit 100 in comparison with a video signal for which sag compensation is performed by the video signal output circuit according to the related art. FIG. 5A illustrates the video signal for which sag compensation is performed by the video signal output circuit according to the related art. FIG. 5B illustrates the video signal for which sag compensation is performed by the video signal output circuit 100 of this embodiment.

[0053] As illustrated in FIG. 5A, in order to prevent a lack of a synchronizing signal in a video signal at the time or transition from a white image to a black image, the operational amplifier in the video signal output circuit according to the related art requires the dynamic range of 3.5 Vp-p. However, as illustrated in FIG. 5B, the dynamic range needed for the operational amplifier 111 in the video signal output circuit. 100 of this embodiment can be reduced to 3.1 Vp-p.

[0054] Therefore, in this embodiment, the operational amplifier 111 having a dynamic range narrower than the dynamic range of the operational amplifier in the video signal output circuit according to the related art can be used to perform sag compensation for the video signal without a lack of a synchronizing signal in the video signal.

[0055] Moreover, in this embodiment, the capacitance of the capacitor C10 and the capacitance of the capacitor C20 can be reduced from those in the video signal output circuit according to the related art. In this embodiment, a chip capacitor can be used as the capacitor C20 for sag compensation, and the mounting area of this capacitor can be reduced from that in the video signal output circuit according to the related art, which will enable cost reduction.

[0056] Therefore, the video signal output circuit 100 of this embodiment can prevent a lack of a synchronizing signal in the video signal and can contribute to the miniaturization of products with low cost.

[0057] In the foregoing embodiment, a video signal from an external device is input to the semiconductor integrated circuit 110. However, the semiconductor integrated circuit 110 is not limited to the specifically disclosed embodiment. For example, the semiconductor integrated circuit 110 as illustrated in FIG. 1 may be arranged to include a circuit which processes a video signal.

[0058] In the foregoing embodiment, after the capacitance values of the capacitors C10 and C20 are set, the resistance value of the resistor Rsag is determined based on the set capacitance values. Alternatively, the resistance value of the resistor Rsag may be determined before the capacitance values of the capacitors C10 and C20 are set. In this case, the capacitance values of the capacitors C10 and C20 are set in conformity with the resistance value of the resistor Rsag.

[0059] Next, a description will be given of several modifications of the present embodiment with reference to FIGs. 6 to 9.

[0060] FIG. 6 illustrates the composition of a first modification of the video signal output circuit of the present embodiment.

[0061] In the video signal output circuit 100A of FIG. 6, a semiconductor integrated circuit 110A is arranged to include a voltage source 120 which is disposed between the resistor R30 and the ground to generate reference voltage Vref, and the operating point of the output signal of the video signal output circuit 100A is changed. In the video signal output circuit 100A of FIG. 6, the operating point of the output signal can be adjusted by changing the value of the generated reference voltage Vref.

[0062] FIG. 7 illustrates the composition of a second modification of the video signal output circuit of the present embodiment.

[0063] In the video signal output circuit 100B of FIG. 7, a semiconductor integrated circuit 110B is arranged to include, in addition to the voltage source 120, a resistor R40 which is connected between the resistor Rsag and the resistor R30. In the video signal output circuit 100B, by arranging the resistor R40, it is possible to set the voltage gain to be in a high region.

[0064] In the video signal output circuit 100B of FIG. 7, β in the above Equation 3 can be determined by the following Equation 7.

Equation 7:

$$\beta = \frac{R30}{R30 + R40}$$

[0065] FIG. 8 illustrates the composition of a third modification of the video signal output circuit of the present embodiment.

[0066] The video signal output circuit 100C of FIG. 8 is arranged to include the semiconductor integrated circuit 110B, and a resistor R50 which is disposed outside the semiconductor integrated circuit 110B and connected between the output terminal T10 and the sag compensation terminal Ts. The resistor R50 between the output terminal T10 and the sag compensation terminal Ts is connected in parallel with the capacitor C20. In the video signal output circuit 100C of FIG. 8, the resistor R50 is arranged outside the semiconductor integrated circuit 110B, and the resistance of the resistor Rsag can be adjusted.

[0067] FIG. 9 illustrates the composition of a fourth modification of the video signal output circuit of the present embodiment.

[0068] The video signal output circuit 100D of FIG. 9 is arranged to include the semiconductor integrated circuit 110B, and a resistor R60 which is disposed outside the semiconductor integrated circuit 110B between the sag compensation terminal Ts and one end of the capacitor C20 and connected in series with the capacitor C20. In the video signal output circuit 100D of FIG. 9, the resistor R60 is arranged outside the semiconductor integrated circuit 110B and the resistance of the resistor Rsag can be adjusted.

[0069] According to the semiconductor integrated circuit and the video signal output circuit of the invention, a lack of a synchronizing signal in the video signal output from the semiconductor integrated circuit or the video signal output circuit can be prevented, and the semiconductor integrated circuit and the video signal output circuit of the invention can contribute to the miniaturization of products with low cost.

Claims

1. A video signal output circuit (100B, 100C, 100D) including a first capacitor (C10), a second capacitor (C20), a point (H) for outputting a signal of the video signal output circuit, and a semiconductor integrated circuit (110) arranged to perform sag compensation for a video signal, the semiconductor integrated circuit comprising:

an operational amplifier (111) including a non-inverted input terminal (T11), an inverted input terminal (T12), and an output terminal, in which in use a video signal is inputted to the non-inverted input terminal;
a first resistor (R30) including a first end connected to the inverted input terminal of the operational amplifier and a second end;
a first terminal (T10) to which the output terminal of the operational amplifier is connected;
a second terminal (Ts); and
a second resistor (Rsag) including a first end connected to the output terminal of the operational amplifier and a second end connected to the second terminal (Ts),
wherein the first capacitor (C10) is provided for removing the direct-current component contained in the video signal between the first terminal (T10) and the point (H) for outputting a signal of the video signal output circuit,
wherein the second capacitor (C20) is disposed between the first terminal (T10) and the second terminal (Ts) and connected in parallel to the second resistor (Rsag),

characterized in that the semiconductor integrated circuit (110) further comprises:

a voltage source (120) including a first end connected to the second end of the first resistor (R30) and a second end being grounded; and
a resistor (R40) including a first end connected to the first end of the first resistor (R30) and a second end connected to the second end of the second resistor (Rsag).

2. A video signal output circuit (100B, 100C, 100D) according to claim 1, further comprising a high-pass filter circuit connected to a junction point between the first terminal (T10) and the second capacitor (C20).

3. A video signal output circuit (100B, 100C, 100D) according to claim 2, wherein the high-pass filter circuit (F) includes the first capacitor (C10), a third resistor (R10), and a fourth resistor (R20) which are connected in series, an end of the fourth resistor (R20) being grounded and wherein the point (H) for outputting a signal of the video signal output circuit is the junction point of the first capacitor (C10) and the third resistor (R10).

4. A video signal output circuit (100C) according to any one of claims 1-3, further comprising a fifth resistor (R50) connected in parallel with the second capacitor (C20) between the output terminal of the operational amplifier and the second terminal.

5. A video signal output circuit (100D) according to any one of claims 1-3, further comprising a fifth resistor (R60) connected in series with the second capacitor (C20) between the second terminal and one end of the second capacitor (C20).

Patentansprüche

1. Videosignalausgabeschaltkreis (100B, 100C, 100D), umfassend einen ersten Kondensator (C10), einen zweiten Kondensator (C20), einen Punkt (H) zum Ausgeben eines Signals des Videosignalausgabeschaltkreises und einen integrierten Halbleiter-Schaltkreis (110), der dafür ausgelegt ist, eine Durchhangkompensation für ein Videosignal auszuführen, wobei der integrierte Halbleiter-Schaltkreis Folgendes umfasst:

    - einen Operationsverstärker (111), der einen nicht-invertierten Eingangsanschluss (T11), einen invertierten Eingangsanschluss (T12) und einen Ausgangsanschluss umfasst, wobei während des Gebrauchs ein Videosignal in den nicht-invertierten Eingangsanschluss eingespeist wird;
    - einen ersten Widerstand (R30), der ein erstes Ende, das mit dem invertierten Eingangsanschluss des Operationsverstärkers verbunden ist, und ein zweites Ende umfasst;
    - einen ersten Anschluss (T10), an den der Ausgangsanschluss des Operationsverstärkers angeschlossen ist;
    - einen zweiten Anschluss (Ts); und
    - einen zweiten Widerstand (Rsag), der ein erstes Ende umfasst, das mit dem Ausgangsanschluss des Operationsverstärkers verbunden ist, und ein zweites Ende umfasst, das mit dem zweiten Anschluss (Ts) verbunden ist,

    wobei der erste Kondensator (C10) dafür vorgesehen ist, die Gleichstromkomponente zu entfernen, die in dem Videosignal zwischen dem ersten Anschluss (T10) und dem Punkt (H) zum Ausgeben eines Signals des Videosignalausgabeschaltkreises enthalten ist,
    wobei der zweite Kondensator (C20) zwischen dem ersten Anschluss (T10) und dem zweiten Anschluss (Ts) angeordnet und mit dem zweiten Widerstand (Rsag) parallel geschaltet ist;
    dadurch gekennzeichnet, dass der integrierte Halbleiter-Schaltkreis (110) des Weiteren Folgendes umfasst:

    - eine Spannungsquelle (120), die ein erstes Ende umfasst, das mit dem zweiten Ende des ersten Widerstandes (R30) verbunden ist, und ein zweites Ende umfasst, das geerdet ist; und
    - einen Widerstand (R40), der ein erstes Ende umfasst, das mit dem ers ten Ende des ersten Widerstandes (R30) verbunden ist, und ein zweites Ende umfasst, das mit dem zweiten Ende des zweite Widerstandes (Rsag) verbunden ist.

2. Videosignalausgabeschaltkreis (100B, 100C, 100D) nach Anspruch 1, der des Weiteren einen Hochpassfilterschaltkreis umfasst, der mit einem Knotenpunkt zwischen dem ersten Anschluss (T10) und dem zweiten Kondensator (C20) verbunden ist.

3. Videosignalausgabeschaltkreis (100B, 100C, 100D) nach Anspruch 2, wobei der Hochpassfilterschaltkreis (F) den ersten Kondensator (C10), einen dritten Widerstand (R10) und einen vierten Widerstand (R20) umfasst, die in Reihe geschaltet sind, wobei ein Ende des vierten Widerstandes (R20) geerdet ist und wobei der Punkt (H) zum Ausgeben eines Signals des Videosignalausgabeschaltkreises der Knotenpunkt des ersten Kondensators (C10) und des dritten Widerstandes (R10) ist.

4. Videosignalausgabeschaltkreis (100C) nach einem der Ansprüche 1 bis 3, der des Weiteren einen fünften Widerstand (R50) umfasst, der mit dem zweiten Kondensator (C20) zwischen dem Ausgangsanschluss des Operationsverstärkers und dem zweiten Anschluss parallel geschaltet ist.

5. Videosignalausgabeschaltkreis (100D) nach einem der Ansprüche 1 bis 3, der des Weiteren einen fünften Widerstand (R60) umfasst, der mit dem zweiten Kondensator (C20) zwischen dem zweiten Anschluss und einem Ende des zweiten Kondensators (C20) in Reihe geschaltet ist.

Revendications

1. Circuit de sortie de signal vidéo (100B, 100C, 100D) comprenant un premier condensateur (C10), un deuxième condensateur (C20), un point (H) pour délivrer un signal du circuit de sortie de signal vidéo, et un circuit intégré à semi-conducteurs (110) agencé pour effectuer une compensation d'affaissement pour un signal vidéo, le circuit intégré à semi-conducteurs comprenant :

   un amplificateur opérationnel (111) comprenant une borne d'entrée non inversée (T11), une borne d'entrée inversée (T12), et une borne de sortie, dans lequel en utilisation un signal vidéo est entré dans la borne d'entrée non inversée ;
   une première résistance (R30) comprenant une première extrémité reliée à la borne d'entrée inversée de l'amplificateur opérationnel et une deuxième extrémité ;
   une première borne (T10) à laquelle la borne de sortie de l'amplificateur opérationnel est reliée ;
   une deuxième borne (Ts) ; et
   une deuxième résistance (Rsag) comprenant une première extrémité reliée à la borne de sortie de l'amplificateur opérationnel et une deuxième extrémité reliée à la deuxième borne (Ts),
   dans lequel le premier condensateur (C10) est fourni pour supprimer la composante de courant continu contenue dans le signal vidéo entre la première borne (T10) et le point (H) pour délivrer un signal du circuit de sortie de signal vidéo,
   dans lequel le deuxième condensateur (C20) est disposé entre la première borne (T10) et la deuxième borne (Ts) et relié en parallèle à la deuxième résistance (Rsag),

   caractérisé en ce que le circuit intégré à semi-conducteurs (110) comprend en outre :

   une source de tension (120) comprenant une première extrémité reliée à la deuxième extrémité de la première résistance (R30) et une deuxième extrémité mise à la masse ; et
   une résistance (R40) comprenant une première extrémité reliée à la première extrémité de la première résistance (R30) et une deuxième extrémité reliée à la deuxième extrémité de la deuxième résistance (Rsag).

2. Circuit de sortie de signal vidéo (100B, 100C, 100D) selon la revendication 1, comprenant en outre un circuit de filtre passe-haut relié à un point de jonction entre la première borne (T10) et le deuxième condensateur (C20).

3. Circuit de sortie de signal vidéo (100B, 100C, 100D) selon la revendication 2, dans lequel le circuit de filtre passe-haut (F) comprend le premier condensateur (C10), une troisième résistance (R10), et une quatrième résistance (R20) qui sont reliées en série, une extrémité de la quatrième résistance (R20) étant mise à la masse et dans lequel le point (H) pour délivrer un signal du circuit de sortie de signal vidéo est le point de jonction du premier condensateur (C10) et de la troisième résistance (R10).

4. Circuit de sortie de signal vidéo (100C) selon l'une quelconque des revendications 1 à 3, comprenant en outre une cinquième résistance (R50) reliée en parallèle au deuxième condensateur (C20) entre la borne de sortie de l'amplificateur opérationnel et la deuxième borne.

5. Circuit de sortie de signal vidéo (100D) selon l'une quelconque des revendications 1 à 3, comprenant en outre une cinquième résistance (R60) reliée en série au deuxième condensateur (C20) entre la deuxième borne et une extrémité du deuxième condensateur (C20).

FIG.1

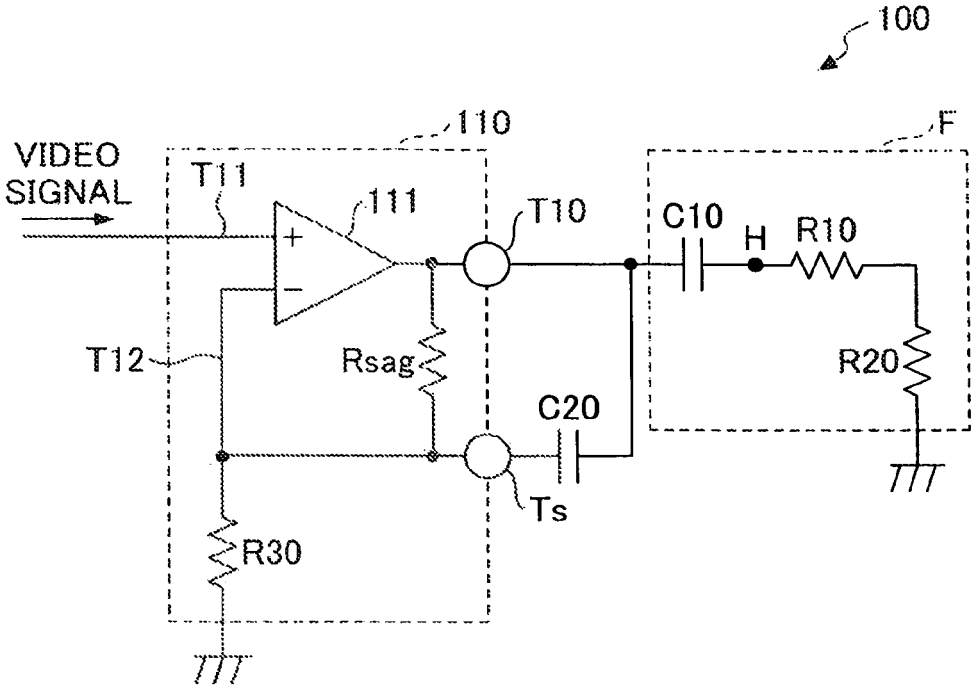
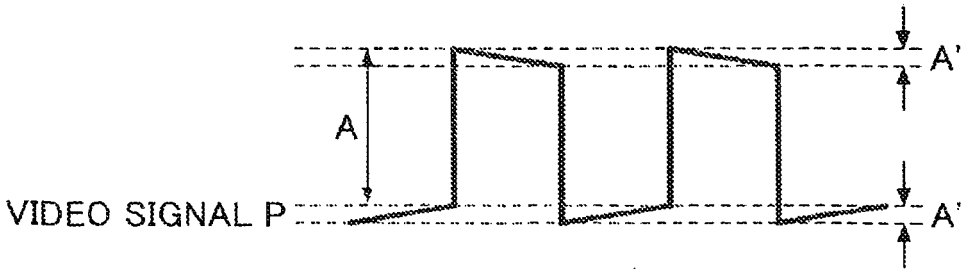


FIG.2



$$\text{SAG RATIO} = \frac{A'}{A} \times 100$$

FIG.3

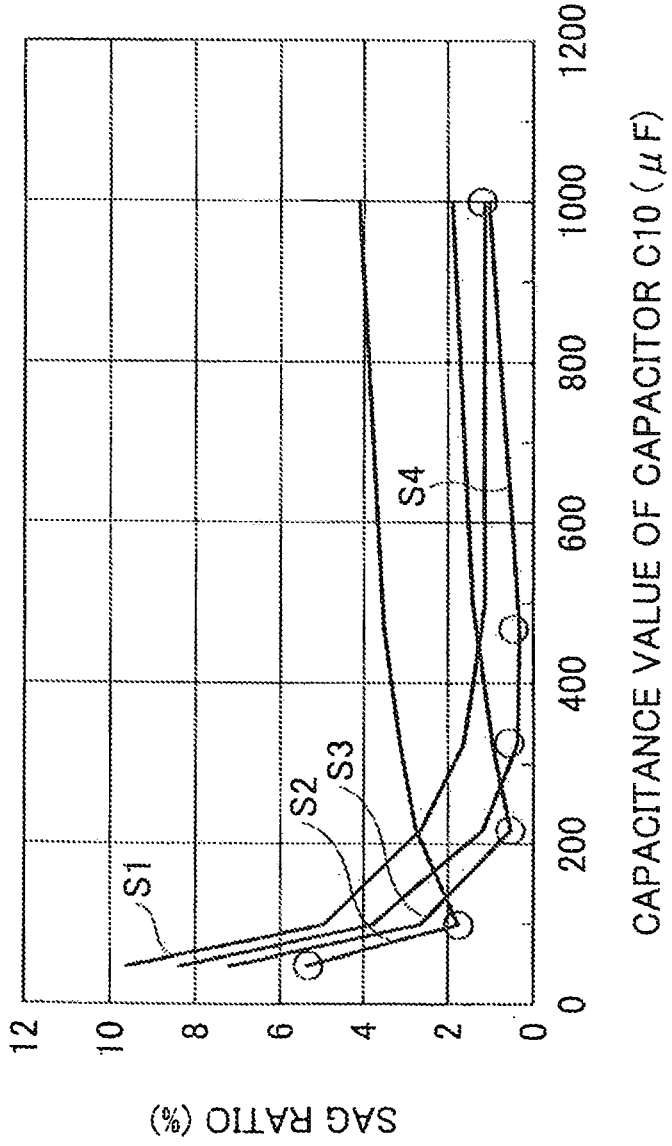

CAPACITANCE VALUE OF CAPACITOR C20
S1→0μF
S2→1μF
S3→2μF
S4→4μF
SAG RATIO (%)
0
2
4
6
8
10
12
0
200
400
600
800
1000
1200
CAPACITANCE VALUE OF CAPACITOR C10 (μF)
S1
S2
S3
S4

FIG.4

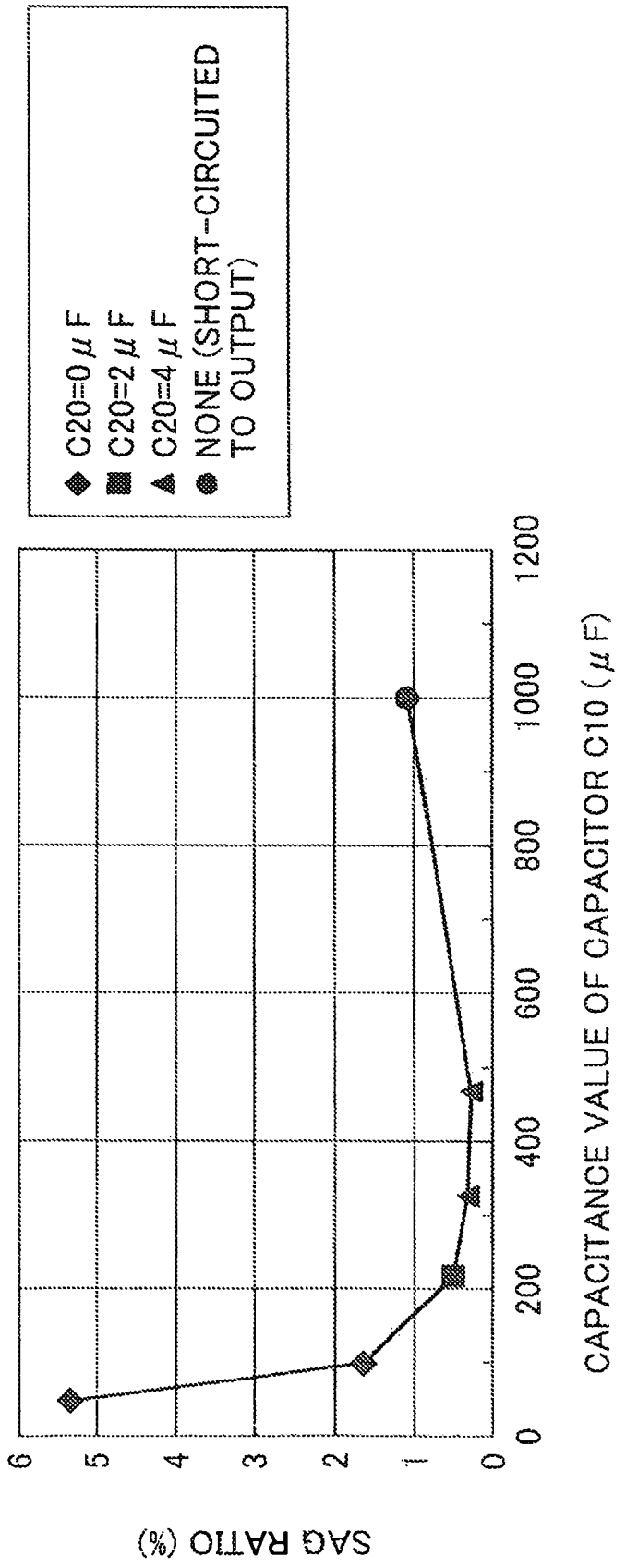

C20=0μF
C20=2μF
C20=4μF
NONE (SHORT-CIRCUITED TO OUTPUT)
SAG RATIO (%)
0
1
2
3
4
5
6
0
200
400
600
800
1000
1200
CAPACITANCE VALUE OF CAPACITOR C10 (μF)

FIG.5A RELATED ART

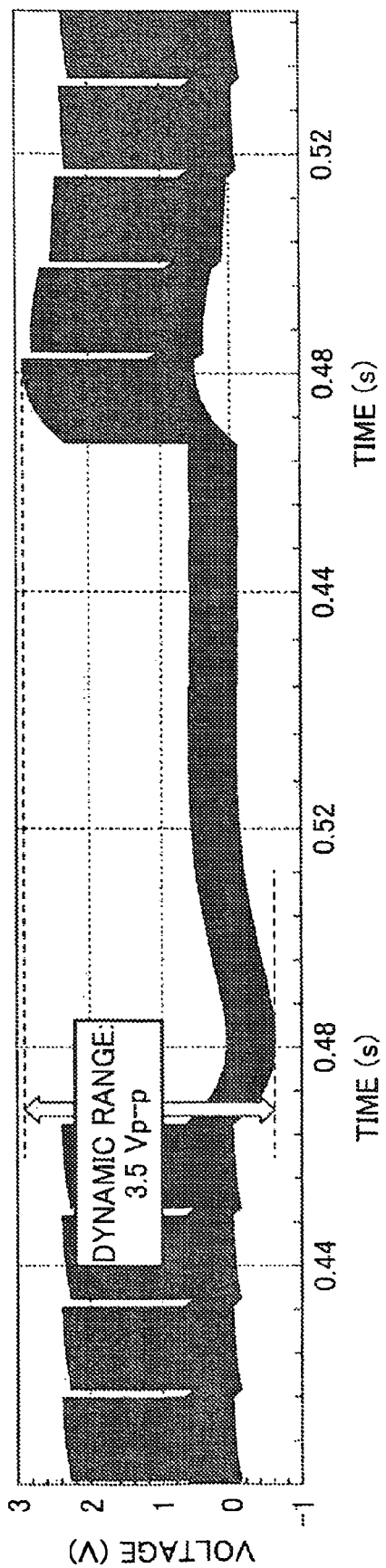


FIG.5B

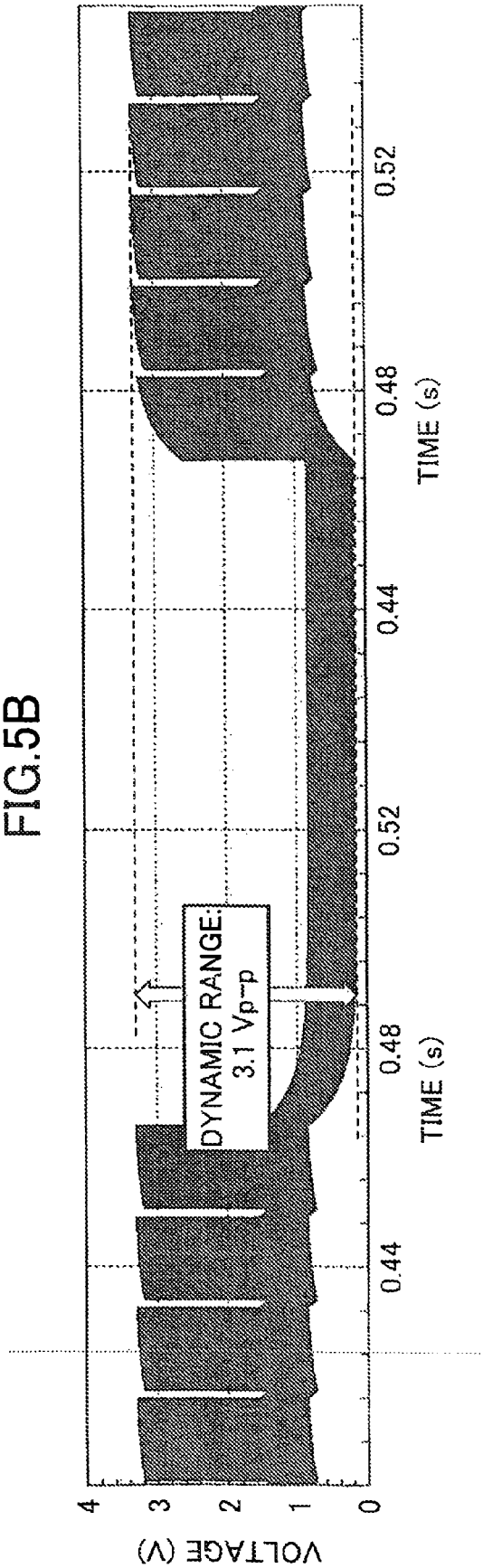


FIG.6

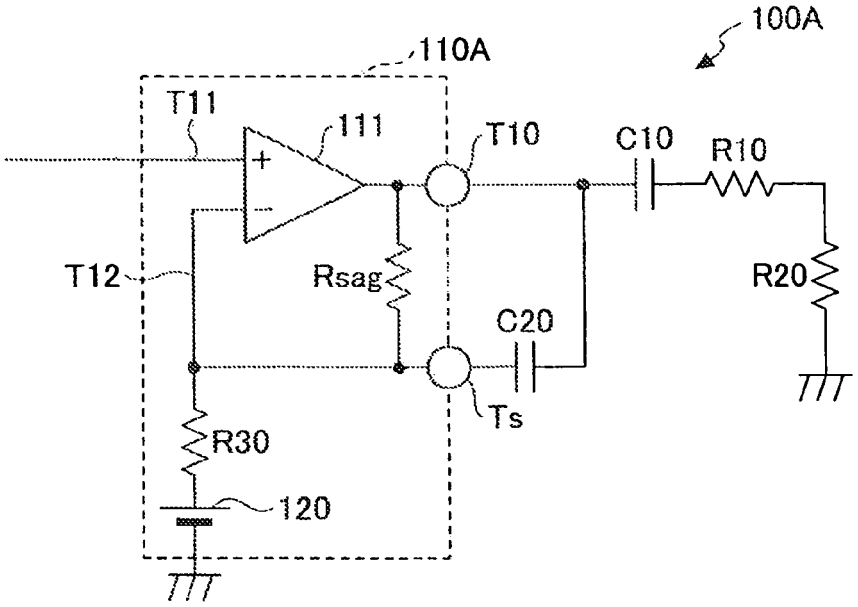

100A
110A
T11
111
T10
C10
R10
T12
Rsag
R20
C20
Ts
R30
120

FIG.7

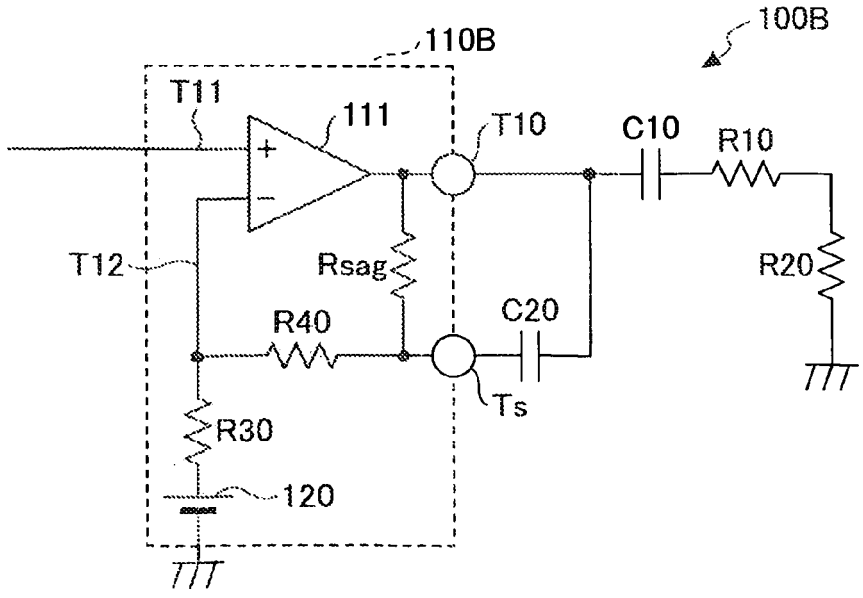

100B
110B
T11
111
T10
C10
R10
T12
Rsag
R20
R40
C20
Ts
R30
120

FIG.8

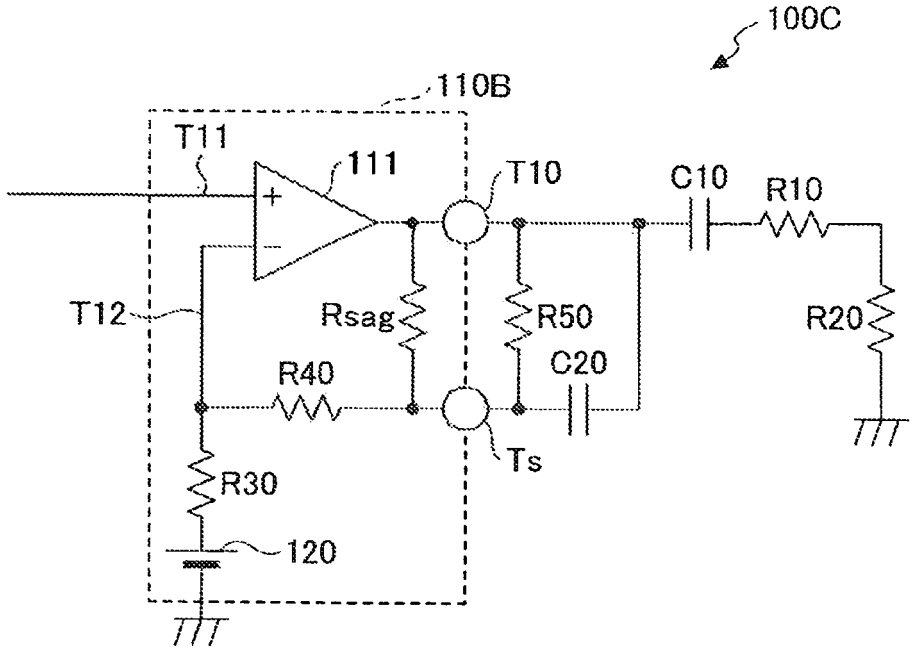

100C
110B
T11
111
T10
C10
R10
T12
Rsag
R50
R20
R40
C20
Ts
R30
120

FIG.9

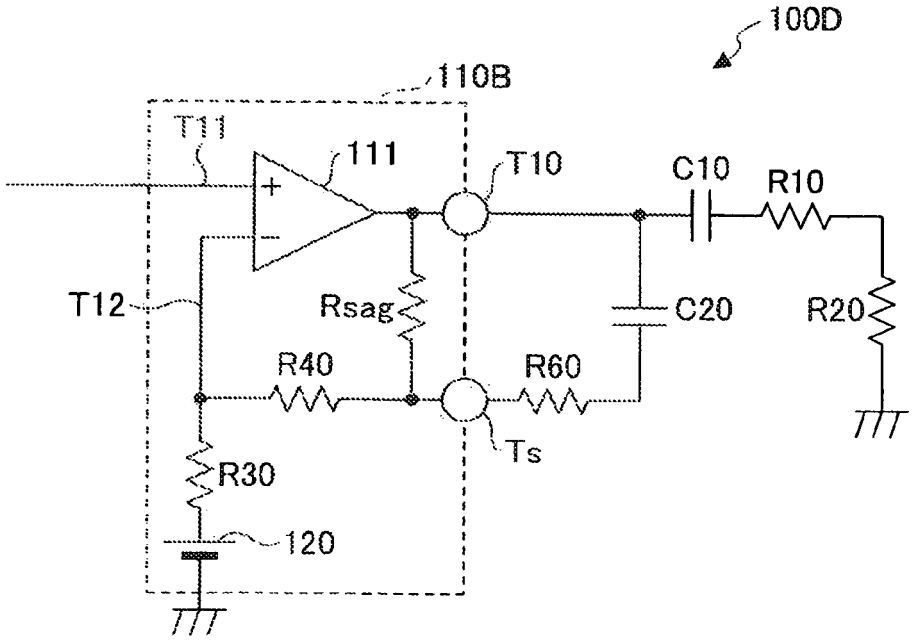

100D
110B
T11
111
T10
C10
R10
T12
Rsag
C20
R20
R40
R60
Ts
R30
120

FIG.10 RELATED ART

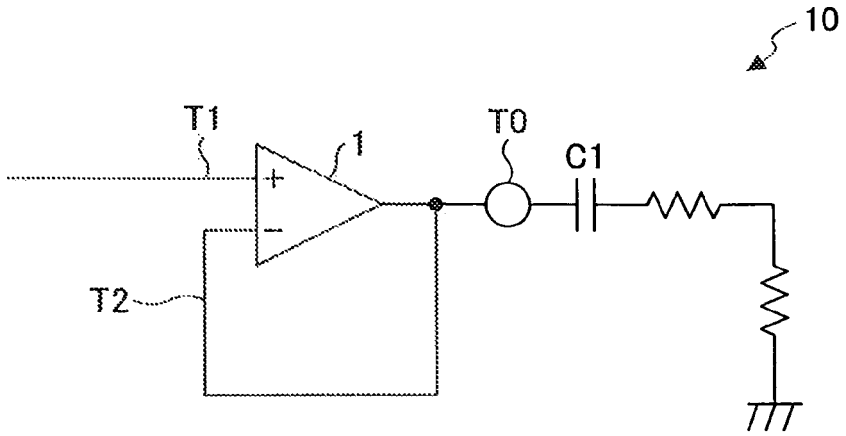
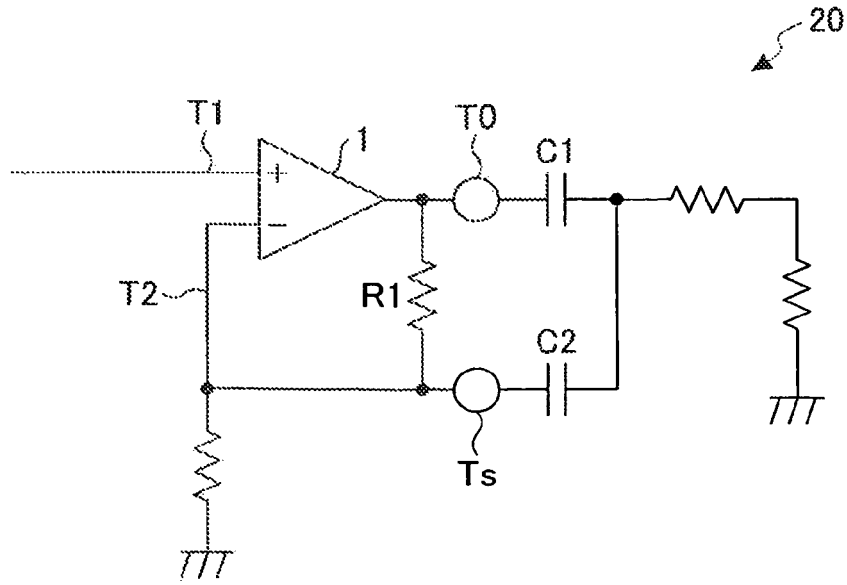


FIG.11 RELATED ART



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 20050105364 A **[0010]**
- US 20060280436 A **[0010]**