



(11)

EP 2 237 253 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
06.10.2010 Bulletin 2010/40

(51) Int Cl.:
G09G 3/32^(2006.01)

(21) Application number: **09157123.2**

(22) Date of filing: **01.04.2009**

(84) Designated Contracting States:
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL
PT RO SE SI SK TR**
Designated Extension States:
AL BA RS

(71) Applicants:
• **ARISTOTLE UNIVERSITY OF THESSALONIKI-
Research Committee
54124 Thessaloniki (GR)**
• **Siskos, Stylianos
54124 Thessaloniki (GR)**
• **Dimitriadis, Charalampos
54124 Thessaloniki (GR)**

• **Pappas, Ilias
54124 Thessaloniki (GR)**

(72) Inventors:
• **Siskos, Stylianos
54124, Thessaloniki (GR)**
• **Pappas, Ilias
54124, Thessaloniki (GR)**
• **Dimitriadis, Charalampos
54124, Thessaloniki (GR)**

(74) Representative: **Petsis, Christos
Attorney at Law
Kyparissias 4-6
54249 Thessaloniki (GR)**

(54) **Pixel circuit, display using the same and driving method for the same**

(57) A pixel circuit including a switching transistor (210) for receiving a control signal and a data voltage, a driving transistor (202), connected to the switching transistor, a first and a second power supply voltage line, a capacitor (204), a current-controlled light emitting means (206), which is connected between the driving transistor and a second power supply voltage line, adapted to generate light so as to display images. The pixel circuit further comprises a threshold voltage variation cancellation cir-

cuit (20) having two terminals, the first terminal whereof is connected to said first power supply voltage line means, and the second terminal is connected to the source terminal of the said driving transistor means, providing an output voltage value to said driving transistor means which is such that a predetermined current is supplied to the light emitting means.

EP 2 237 253 A1

Description**Field of the Invention**

[0001] The present invention is related to the structure and the driving method of a pixel circuit of a display and in particular to driving the pixel circuit and method compensating the threshold voltage variations of driving transistor thereof.

Prior Art

[0002] There has been tremendous growth in information technology during this century and almost all computing devices require varied sizes and high quality displays. For over 50 years, "cathode ray tubes" (CRTs) have been the dominant display technology providing high quality, brightness, contrast ratio, speed and resolution. Although, CRTs are excellent displays, the main disadvantage is their bulkiness. Integration of CRTs into small mobile devices was expensive and difficult. The solution to this problem was the development of Flat Panel Displays (FPDs). Active Matrix Organic Light Emitting Diode (AMOLED) panel displays have emerged as one of the next-generation flat panel displays. AMOLEDs offer many advantages over Liquid Crystal Displays (LCD), such as self-emitting nature, fast response time, light weight, wide viewing angle and thinner devices. AMOLED displays have been implemented with amorphous silicon (a-Si), polycrystalline silicon, organic or other driving backplane.

[0003] Currently most of the AMOLED displays use polysilicon thin-film transistors (poly-Si TFTs) due to their higher carrier mobility, higher current capability, and better switching behavior over other thin-film technologies. On the other hand, a-Si or organic TFTs even with lower mobility, are cost effective solutions.

[0004] TFTs operation can be divided into three working modes: cut-off, linear and saturation modes. For example, the drain current of an n-channel TFT can be represented with the following expressions for each working mode:

$$(1) I_{d_off} = 0, \text{ when } V_{gs} < V_{thn}$$

$$(2) I_{d_linear} = \mu C_{ox} W [V_{eff} V_{ds} - V_{ds}^2/2]/L, \text{ when } 0 < V_{ds} < V_{eff}$$

[0005]

$$(3) I_{d_sat} = [\mu C_{ox} W V_{eff}^2]/2L, \text{ when } V_{eff} < V_{ds}$$

Where μ is the effective surface mobility of the carriers; C_{ox} is the gate oxide capacitance per unit area; W is the effective gate mask width; L is the effective gate mask length; V_{eff} is the effective gate voltage, equal to the difference between the gate to source voltage V_{gs} and the transistor threshold voltage V_{thn} , $V_{eff} = V_{gs} - V_{thn}$; I_{d_off} is the drain current when the TFT is operating in the cut-off mode; I_{d_linear} is the drain current when the TFT is operating in the linear mode; I_{d_sat} is the drain current when the TFT is operating in the saturation mode.

[0006] The above expressions indicate the important role of the threshold voltage in TFT operation. The threshold voltage is determined by the gate and insulator materials, the gate oxide material thickness and the channel doping concentration. The major TFT disadvantage is the threshold voltage variation from device to device due to the channel material structure and fabrication process. In case of polysilicon TFTs, during the fabrication process, the amorphous silicon film is turned to polysilicon film by excimer laser annealing. Annealing process generates grain boundaries (GB) along the TFT channel. The grain boundaries are discontinuities for the carrier transport and their random distribution within the channel cause threshold voltage variation from device to device, even if the devices are implemented on the same wafer. Threshold voltage variation impacts the TFT drain current, since the drain current is a second order function of threshold voltage when the TFT operates in saturation mode and the TFT operation point shifts from the desired position. This means that the output drain current can not be well-controlled. The pixels using such TFT drivers will have irregular display uniformity (mura) due to threshold voltage variation, because driving TFTs supplied with the same data signal will produce different driving current and different OLED luminance. Similar is the behavior of amorphous and organic or other types of TFTs.

[0007] Apart from the threshold voltage variation, mobility variations are also observed in TFT large area electronics.

However, the variation in transistor threshold voltage affects the device performance more seriously than the mobility variation in AMOLED driver circuits, as confirmed with measurements by V. Vaidya et al., "Comparison of pentacene and amorphous silicon AMOLED display driver circuits", IEEE Transactions on Circuits and Systems-I: Regular papers, Vol. 55, NO. 5, June 2008. Therefore, the threshold voltage shift poses a design constrain for the AMOLED backplanes.

[0008] The problem of threshold voltage variations was observed in the first generation of drivers using only two transistors. FIG. 1 shows the configuration of a conventional 2T1C AMOLED pixel 100. AMOLED panel is an array including a plurality of pixels, scan lines and data lines, as well as power supply VDD and VEE as shown in FIG. 2. Scan lines voltages are provided from external row driving circuits and data lines voltages are provided by column driving circuits. The pixels, each one including an organic light emitting diode (OLED) or other electroluminescent device as the light emitting device of the pixel, emits light when a certain amount of current pass through it, are coupled to power supply voltages VDD and VEE, and to external driving circuits via corresponding Scan lines and Data lines. In addition, each pixel includes two TFTs and a storage capacitor as shown in FIG.1. The first TFT 102 is a switch, where the gate and drain/source electrodes are coupled to the Scan Line signal 12 and the Data Line signal 14, respectively. The second TFT 104 is the driving TFT, where the gate electrode is coupled to the switch TFT 102 source/drain path and the source electrode to the power supply voltage VDD. The storage capacitor C_s 106 is coupled between the gate of the driving TFT 104 and the power supply voltage VDD, which keeps the gate voltage of the driving TFT 104 constant until the next frame period. The OLED 108 is coupled between the drain of the driving TFT 104 and the power supply voltage VEE.

[0009] An operation of the conventional AMOLED pixel will be described. FIG. 2 illustrates the pixels array architecture for an AMOLED display. The programming of the pixels array is made by row - at-a time, meaning that refreshing of the pixels configuration is implemented row by row and it is controlled by two external generated signals; a scan signal is generated from row driving circuits and data signal is generated from column driving circuits. The programming procedure includes the steps: First, the scan voltage from the scan line 12 turns "ON" the switch TFT 102. Then, the data signal is delivered via the turned-on switch TFT 102 to the driving TFT 104 gate node and the storage capacitor 106, producing a corresponding to the data signal driving current from the driving TFT 104 to the OLED 108, causing OLED to illuminate in response to the driving current.

[0010] The problem with pixel circuit of prior art is the driving TFT threshold voltage variation and the incapability of pixel circuit to compensate this variation. As a result, the threshold voltage variation causes large variation of current, resulting finally in non uniformity of illumination. To overcome this issue, many pixel circuits have been proposed.

[0011] G.R. Chaji, P. Servati and A. Nathan, [ELECTRONICS LETTERS, 14th April 2005 Vol. 41 No. 8], developed a driving scheme for a-Si AMOLED pixel where two thin film transistors (2T) and one capacitor (1C) are used, which needs a complicated signaling scheme with first three programming cycles before the driving period.

[0012] Similarly in the US Pat. No.7167169 B2, Pub. Date Jan.23, 2007, entitled "Active matrix OLED voltage drive pixel circuit", the 2T1C driving scheme needs a very complicated signaling scheme.

[0013] Also, in the US Pat. No.2005/0105031 A1, Pub. Date May 19, 2005 entitled "Pixel structure of display and driving method thereof" and in US Pat. No. 7,071,932 B2, Pub. Date Jul. 4, 2006, threshold voltage variations are compensated in a pixel with 3T1C driving circuit demanding a complicated signaling scheme.

[0014] Another implementation of a pixel driving circuit using 5T1C, entitled "A New Voltage-Modulated AMOLED Pixel Design Compensating for Threshold Voltage Variation in Poly-Si TFTs", published in IEEE ELECTRON DEVICE LETTERS, VOL. 25, NO. 10, OCTOBER 2004, by Sang-Hoon Jung, Woo-Jin Nam, and Min-Koo Han, in order to compensate the threshold voltage variations needs two Scan signals and a time interval to reset the previous data value stored in the capacitor.

[0015] In prior work, the most common compensation method is the increase of the gate voltage of the driving TFT by one threshold voltage. In this way, the effective gate voltage V_{eff} will be independent of the threshold voltage V_{th} and the produced current will be stable, i.e.

$$\begin{aligned} V_{gs} &= V_{ref} + V_{th} \\ V_{eff} &= V_{gs} - V_{th} = V_{ref} + V_{th} - V_{th} \\ V_{eff} &= V_{ref} \end{aligned}$$

Where V_{gs} is the gate to source voltage of the TFT, V_{ref} is a reference or data voltage.

[0016] In order to achieve this, an additional circuit block coupled to the gate node of the driving TFT was required for producing and adding the threshold voltage to the gate node. The additional circuit part with the control signals is a dynamic component affecting the column and row drivers' architecture of the AMOLED, since complex signaling is needed. Also, more than one capacitors will be included increasing the real silicon area and the response time. Therefore, the prior work pixels and methods for suppressing the threshold voltage variations have many design difficulties, leading

to limited applications and performance.

SUMMARY OF THE INVENTION

[0017] The present invention discloses a pixel circuit, an image display using the same and a driving method thereof, which presents advantages compared to the existing ones for suppressing the threshold voltage variation of thin film transistors and producing a stable threshold - independent current in the pixel.

[0018] The pixel circuit according to the present invention comprises:

a data line means for supplying a data voltage,
 a scan line means for supplying a control signal,
 a switching transistor means for receiving said control signal through its gate terminal and receiving said data voltage through the source-drain current path,
 a driving transistor means, the gate terminal whereof is connected to the source-drain current path of the switching transistor means,
 a first and a second power supply voltage line means, wherein the first one is the more positive one in a p-type implementation, and the second one is the more positive one in a n-type implementation, the implementation type being defined by the type of the driving transistor means,
 a capacitor means having a first terminal and a second terminal, wherein the first terminal is coupled to the gate of the driving transistor and the second terminal is coupled to the more positive power supply voltage line means of the pixel circuit, for maintaining the data voltage supplied to the gate of the driving transistor during a predetermined time,
 a current-controlled light emitting means, for emitting light which brightness corresponds to the current applied, which is connected between the drain terminal of the driving transistor means and a second power supply voltage line means, adapted to generate light so as to display images, wherein it further comprises a threshold voltage variation cancellation circuit means having two terminals, whereof the first terminal is connected to said first power supply voltage line means, and the second terminal connected to the source terminal of the said driving transistor means, providing an output voltage value to said driving transistor means which is such that a predetermined current is supplied to the light emitting means ensuring then that the current through the light emitting means is made independent from the threshold voltage of the driving transistor means.
 According to a preferred embodiment of the invention, the difference between said output voltage value and the opposite sign value of the threshold voltage of the driving transistor means is a constant.

[0019] According to a more preferred embodiment of the invention, the said threshold voltage cancellation circuit comprises :

an opposite sign threshold voltage value extractor means providing at its output terminal a voltage equal to the opposite sign threshold voltage value of said driving transistor means, and
 a buffer means having at least an input terminal which is connected to the output terminal of the opposite sign threshold voltage value extractor circuit means and an output terminal, where said output voltage value is provided, with the difference between said value and the opposite sign value of said threshold voltage of the driving transistor means being a constant.

[0020] According to another preferred embodiment of the invention, the said opposite sign threshold voltage value extractor means comprises an extractor transistor means, providing at its output a voltage value, with the difference between said value and the opposite sign value of said threshold voltage of the driving transistor means being a constant, and the said buffer means having its input terminal coupled to the source output terminal of said extractor transistor means.

[0021] According to a more preferred embodiment of the invention, the said extractor transistor means has the same electrical characteristics than the driving transistor means, with its gate and drain terminals being electrically coupled to said second power supply voltage line means and its source terminal being fed by a bias current.

[0022] According to an even more preferred embodiment of the invention, the said buffer means comprises a buffer transistor means having the gate terminal coupled to the drain terminal of an input transistor means and the source terminal coupled to said first power supply voltage line means of the pixel circuit, said input transistor means having the gate terminal coupled to the output terminal of the opposite sign threshold voltage value extractor means, the drain terminal coupled to a first bias current and the source terminal coupled to the drain terminal of said buffer transistor means. According to another embodiment of the invention, said switching transistor means is either p-channel or n-channel and all other transistors means are of the same type, either p-channel or n-channel, thin film transistors (TFT).

[0023] According to another embodiment of the invention, said transistor means are selected from a list consisting of

a polycrystalline silicon TFT, an amorphous silicon TFT, a nanocrystalline silicon TFT, an organic TFT and an oxide (transparent) TFT.

[0024] The present invention also proposes an image display comprising a scan driver means which is arranged for driving a plurality of scan lines means, a data driver means which is arranged for driving a plurality of data lines means, both said scan lines means and data lines means having intersections, and the pixel circuits arranged at said intersections.

[0025] Finally the present invention proposes a method for driving a light emitting means of a pixel circuit of an image display, the pixel circuit including:

a data line means for supplying a data voltage,

a scan line means for supplying a control signal,

a switching transistor means for receiving said control signal through its gate terminal and receiving said data voltage through the source-drain current path,

a driving transistor means, the gate terminal whereof is connected to the source-drain current path of the switching transistor means,

a first and a second power supply voltage line means, wherein the first one is the more positive one in a p-type implementation, and the second one is the more positive one in a n-type implementation, the implementation type being defined by the type of the driving transistor means,

a capacitor means having a first terminal and a second terminal, wherein the first terminal is coupled to the gate of the driving transistor and the second terminal is coupled to the more positive power supply voltage line means of the pixel circuit, for maintaining the data voltage supplied to the gate of the driving transistor during a predetermined time,

a current-controlled light emitting means, for emitting light which brightness corresponds to the current applied, which is connected between the drain terminal of the driving transistor means and a second power supply voltage line means, adapted to generate light so as to display images,

a threshold voltage variation cancellation circuit means, the method comprising,

conducting the first switching transistor to input the data signal to the gate of the second driving transistor and a first terminal of the capacitance element;

charging the capacitance element to a voltage corresponding to the data signal and fixing the potential of the gate electrode of the second driving transistor;

not conducting the first switching transistor to allow the gate electrode of the second driving transistor to be in a floating state;

supplying current corresponding to potential applied to the gate electrode of the second driving transistor to the light emitting element to emit light;

wherein the threshold voltage variation cancellation circuit fixes at the source electrode of the second driving transistor a potential the difference between said potential voltage value and the opposite sign value of the threshold voltage of the driving transistor means being a constant ensuring that the current through the light emitting means is made independent from the threshold voltage and its variations of the driving transistor means.

[0026] According to another embodiment of the invention, the said potential voltage value is equal to said opposite sign value of the threshold voltage of the driving transistor means.

[0027] According to a more preferred embodiment of the invention, the threshold voltage variation cancellation circuit is continuously in a conducting state.

[0028] According to an even more preferred embodiment of the invention, the loading of the capacitor means comprises fully turning on the switching transistor means and wherein the applying of the voltage to the driving transistor means by the capacitor means comprises fully turning off the switching transistor means.

[0029] According to another preferred embodiment of the invention, said switching transistor means is either p-channel or n-channel and all the rest transistors means are of the same type, either p-channel or n-channel, thin film transistors (TFT), and the TFT is one of a polycrystalline silicon TFT, an amorphous silicon TFT, a nanocrystalline silicon TFT, an organic TFT and an oxide (transparent) TFT.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Fig. 1 shows the prior art pixel driving circuit.

[0031] Fig. 2 shows the prior work AMOLED architecture

[0032] Fig. 3 shows the block diagram of the pixel circuit of an embodiment of the invention

[0033] Fig. 4 shows the p-type implementation of the pixel circuit according to an embodiment of the invention

[0034] Fig. 5 shows the n-type implementation of the pixel circuit according to an embodiment of the invention

[0035] Fig. 6 shows the "threshold voltage variation cancellation circuit" block diagram according to an embodiment

of the invention

[0036] Fig. 7 shows the p-type implementation of the opposite sign threshold voltage value extractor

[0037] Fig. 8 shows the n-type implementation of the opposite sign threshold voltage value extractor

[0038] Fig. 9 shows the p-type implementation of the buffer implemented by a Flipped Voltage Follower circuit

[0039] Fig. 10 shows the n-type implementation of the buffer implemented by a Flipped Voltage Follower circuit

[0040] Fig. 11 shows the complete p-type implementation pixel circuit according to an embodiment of the invention

[0041] Fig. 12 shows the complete n-type implementation pixel driving circuit according to an embodiment of the invention

[0042] Fig. 13 shows an active matrix display architecture using the proposed pixel circuit for p-type (n-type) implementation with I_{bias1} and I_{bias2} (I_{bias11} and I_{bias22}) bias currents.

DETAILED DESCRIPTION OF THE INVENTION

[0043] The main disadvantage of the TFT technology is the variation of the threshold voltage from device to device, even if the devices are implemented on the same wafer. Therefore, the produced drain current is not well-controlled and the analog circuit design is a very difficult task. In order to overcome this disadvantage, the common method used for the design of analog circuits is to increase the TFT gate voltage by one threshold voltage and the produced drain current would be threshold voltage independent.

[0044] For an n-type implementation, the effective voltage V_{eff} of an-channel TFT is equal to:

$$V_{eff} = V_{gs} - V_{thn}$$

[0045] If the TFT is working in the saturation mode, the drain current expression is given by:

$$Id_{satn} = [\mu C_{ox} W V_{eff}^2] / 2L$$

[0046] If the gate voltage is increased by a threshold voltage, the effective gate voltage is equal to:

$$\begin{aligned} V_{eff} &= V_{gs} - V_{thn} \Rightarrow \\ V_{eff} &= V_{ref} + V_{thn} - V_{thn} = V_{ref} \end{aligned}$$

[0047] The drain current Id_{satn} is equal to:

$$Id_{satn} = [\mu C_{ox} W V_{ref}^2] / 2L$$

Where V_{thn} is the TFT threshold voltage, V_{ref} is the reference or data voltage, μ is the mobility of the carriers, C_{ox} is the gate capacitance of the TFT and W and L are the width and length of the TFT respectively.

[0048] From the above expression, it is seen that if the gate voltage is increased by one threshold voltage, the produced drain current will be independent of the threshold voltage. The source voltage is kept constant, not affecting the above expressions.

[0049] Embodiments of the invention are related to a pixel circuit, an image display using the pixel, and a driving method for the pixel, and more particularly, the present invention is related to a pixel circuit, a display using the pixel, and a driving method for the light emitting element of the pixel, in which compensation is made for variation in the threshold voltage (V_{th}) of a drive transistor.

[0050] The invention might be discussed in the context of a general light emitting device (EL device), and for simplicity it will be considered an organic light emitting diode (OLED) as a light emitting device.

In case of an n-channel TFT:

[0051] Instead of increasing the gate voltage as it was described in the prior work, the source voltage is decreased by one threshold voltage V_{thn} , i.e. the voltage at the source node of the TFT is

$$V_s = -V_{thn}$$

[0052] If a voltage V_{ref} is applied to the gate electrode of the TFT, the effective voltage is equal to:

$$V_{eff} = V_{gs} - V_{thn} = [V_{ref} - (-V_{thn})] - V_{thn} = V_{ref}$$

and the drain current is given by:

$$I_{d_satn} = [\mu C_{ox} W V_{ref}^2] / 2L$$

[0053] The above expression shows that the drain current is threshold voltage independent. In a similar way, in case of p-type TFT the above analysis is valid considering that all voltages, V_{eff} , V_{gs} and V_{th} have negative values, the source voltage is increased by one opposite sign threshold voltage, as described in a following embodiment. A pixel circuit is designed thereof.

[0054] FIG. 3 illustrates a pixel circuit according to an embodiment of the invention. Pixel circuit 200 compensates the threshold voltage variations of the driving transistor 202, so that the drain current feeding the OLED 206 is stable and insensitive to the threshold voltage variations. Pixel circuit 200 comprises a switch transistor 210, a driving TFT 202, a threshold voltage variations cancellation circuit 20 and an OLED 206.

[0055] The first terminal of the switch TFT 210 is coupled to the Data Line 14, the second terminal is coupled to the gate electrode of the driving TFT 202 and the third terminal, (its gate), is coupled to the Scan Line 12. The source electrode of the driving TFT 202 is coupled to the first terminal (the output) of the threshold voltage variation cancellation circuit 20 and the drain electrode of the driving TFT 202 is coupled to the first terminal of the OLED 206. The second terminal of the threshold voltage variation cancellation circuit 20 is coupled to a first external power supply, Power Supply 1. The second terminal of the OLED 206 is coupled to a second external power supply, Power Supply 2. The pixel comprises also a storage capacitor 204, with the first terminal coupled to the gate of the driving TFT 202 and the second terminal coupled to the higher external power supply, $V_{supply-high}$, which can be either Power Supply 1 or Power Supply 2.

[0056] Fig. 4 illustrates a p-type implementation of the pixel circuit 200, where all thin film transistors (TFTs) used for the driving circuit are p-channel TFTs according to an embodiment of the invention. The first terminal of the switch TFT 4210 is coupled to the Data Line 14, the second terminal is coupled to the gate of the driving TFT 4202 and the third terminal, (its gate), is coupled to the Scan Line 12. The driving TFT 4202 can include a p-type TFT with the gate electrode coupled to the second terminal of the switch TFT 4210, the source electrode coupled to the threshold voltage variation cancellation circuit 20 and the drain electrode to a first terminal of the OLED 4206. The second terminal of the threshold voltage variation cancellation circuit 20 is coupled to Power Supply 1. The pixel circuit, also, includes a storage capacitor 4204 with the first terminal coupled to the gate electrode of the driving TFT and the second terminal coupled to the Power Supply 1, which corresponds to the higher power line for the p-channel implementation. The first terminal of the OLED 4206 is coupled to the drain of the driving TFT 4202 and the second terminal of the OLED is coupled to the Power Supply 2, which in this p-type implementation can be the lower power supply or ground. OLED 4206 illuminates in response to the current flowing through it.

[0057] When the Scan Voltage (V_{scan}) from the Scan line 12 is pulled low, switch TFT 4210 is turned "ON" and the Data Voltage (V_{data}) from the Data line 14 is being transferred through switch TFT 4210 in the pixel and which in turn is stored in the storage capacitor 4204. When the Data Voltage is stored in the storage capacitor 4204, the Scan Voltage is pulled low and the switch TFT 4210 is turned "OFF". The Data Voltage is then applied to the gate node of the driving

TFT 4202. The storage capacitor 4204 ensures that the gate voltage of the driving TFT 4202 is kept constant during a frame time. Driving TFT 4202 will be working in the saturation mode and the produced drain current will cause the illumination of OLED 4206 and the drain current I_{d_satp} of the TFT is:

$$I_{d_satp} = [\mu C_{ox} W (V_s - V_{data} - |V_{thp}|)]^2 / 2L$$

Where V_{thp} is the threshold voltage of the p-channel TFT 4202 and V_s is the voltage of the source node of the driving TFT 4202.

[0058] The source node of driving TFT 4202 is coupled to the threshold voltage variation cancellation circuit 20, the later providing an output voltage which is the sum of the threshold voltage and a constant given by:

$$V_{out} = V_{ct} + |V_{thp}|$$

where V_{ct} is a constant voltage independent of the TFT_s threshold voltage V_{thp} .

[0059] Since $V_{out} = V_s$, the drain current of the driving transistor 4202 and then the current driving the OLED is given by:

$$I_{OLED} = I_{d_satp} = [\mu C_{ox} W (V_{ct} - V_{data})^2] / 2L$$

[0060] The above expression shows that the current flowing through the OLED device 4206 is independent of the driving TFT threshold voltage, considering that the threshold voltage variation cancellation circuit 20 provides at its output a threshold voltage equal to the threshold voltage of the driving TFT 4202.

[0061] Fig. 5 illustrates an n-type implementation of the pixel driving circuit and the OLED, where all transistors used for the driving circuit are n-channel TFTs according to an embodiment of the invention. Switch TFT 5210 and driving TFT 5202 can include n-type TFTs. The first terminal of the switch TFT 5210 is coupled to the Data Line 14, the second terminal is coupled to the gate of the driving TFT 5202 and the third terminal (gate) is coupled to the Scan Line 12. The driving TFT 5202 has a gate electrode coupled to the second terminal of the switch TFT 5210, a source electrode coupled to the first terminal (output) of the threshold voltage variation cancellation circuit 20 and the drain electrode coupled to the first terminal of the OLED 5206. The pixel circuit, also, includes a storage capacitor 5204 with the first terminal coupled to the gate electrode of the driving TFT and the second terminal coupled to the Power Supply 2, which corresponds to the higher power supply, for the n-type implementation. The first terminal of the OLED 5206 is coupled to the drain of the driving TFT 5202 and the second terminal of the OLED 5206 is coupled to the Power Supply 2. The second terminal of the threshold voltage variation cancellation circuit 20 is coupled to Power Supply 1, which in this n-type implementation can be the lower power supply or ground. OLED 5206 illuminate in response to the current flowing through it.

[0062] When the scan voltage from the Scan Line 12 is pulled high, the switch TFT 5210 is turned "ON" and the data voltage V_{data} from the Data Line 14 is stored to the storage capacitor 5204. The storage capacitor 5204 ensures that the gate voltage of the driving TFT 5202 is kept constant during a frame time. The gate voltage of the driving TFT 5202 will be equal to the stored data voltage V_{data} and the driving TFT will be working in the saturation mode, producing a drain current equal to:

$$I_{d_satn} = [\mu C_{ox} W (V_{gs} - V_{thn})^2] / 2L$$

[0063] The threshold voltage variation cancellation circuit 20 produces an output voltage, which is the sum of the threshold voltage and a constant given by

$$V_{out1} = V_{ct1} - V_{thn}$$

Where V_{ct1} is independent of the threshold voltage V_{thn} .

[0064] Since the output voltage of the threshold voltage variation cancellation circuit 20 is equal to the source voltage of the driving TFT 5202 ($V_{out} = V_s$), the drain current of the driving TFT is:

$$Id_satn = [\mu C_{ox} W (V_{data} - V_{out1} - V_{thn})^2] / 2L$$

$$Id_satn = [\mu C_{ox} W (V_{data} - V_{ct1} + V_{thn} - V_{thn})^2] / 2L$$

$$Id_satn = [\mu C_{ox} W (V_{data} - V_{ct1})^2] / 2L$$

[0065] The above expression shows that the current flowing through the OLED device 5206 is a function of the Data Voltage (V_{data}) and a constant voltage (V_{ct1}) which both are independent of the driving TFT threshold voltage.

[0066] Fig. 6 shows the block diagram of the threshold voltage variation cancellation circuit 20, having two terminals, the first one 170 being connecting at the power supply 1 either positive or negative/ground the second one 70 being its output. This circuit may include an opposite sign threshold voltage extractor 40 and a buffer 30 with high source or sinking current capability depending on the specifications of the used light emitting device. The opposite sign threshold voltage extractor 40 feeds the buffer 30 with a voltage equal to the threshold voltage of opposite sign, which is considered to be equal to the threshold voltage of the driving transistor 202. At the output 70 of the buffer 30 and then of the threshold voltage variation cancellation circuit 20, a linear function of the threshold voltage of opposite sign is obtained.

[0067] Fig. 7 shows the p-type implementation of the opposite sign threshold voltage extractor 40. An opposite sign threshold voltage extractor may include a p-channel TFT 742. TFT 742 is diode-connected, which means that the gate and drain nodes are coupled together to the power supply 2 line, which in case of p-type implementation corresponds to the ground line. Since TFT 742 is diode-connected, it is working in the saturation mode. The TFT 742 source electrode is coupled to a bias current I_{bias1} 750. The bias current I_{bias1} 750 has a small value and the TFT's operation point will be close to the limit of the saturation mode. Therefore, the voltage at the source electrode 760 of the TFT 742 will be equal to the opposite sign value of the threshold voltage of the TFT 742. Considering that transistors TFT 742 and the driving TFT 4202 have equal threshold voltages, since they are very closely located on the same wafer, the voltage at the source electrode 760 of the TFT 742 is equal to the opposite sign value of the driving TFT 4202 threshold voltage.

[0068] Fig. 8 shows the n-type implementation of the opposite sign threshold voltage extractor 40. The diode-connected TFT 842 with its drain and gate electrodes coupled to the Power Supply 2, which in case of n-type implementation corresponds to the higher power supply, represented by V_{DD} and the source electrode coupled to the bias current I_{bias1} , which is small enough so that the operation point of the TFT 842 is near the limit of the saturation mode. Therefore, the voltage at the source electrode 860 (output electrode) of TFT 842 is equal to V_{DD} minus the threshold voltage of TFT 842, $V_{DD} - V_{thn}$. Considering that transistors TFT 842 and the driving TFT 5202 have equal threshold voltages, since they are very closely located on the same wafer, the voltage at the source electrode 860 of the TFT 842 is equal to a the difference between a constant voltage and the opposite sign value of the driving TFT 5202 threshold voltage.

[0069] Fig. 9 shows an example of the p-type implementation of a buffer. The buffer 30 is called "flipped voltage follower" and it is based on the common source amplifier. The buffer 30 includes a p-channel input TFT 932, which is connected as a common source amplifier. The gate electrode of the input TFT 932 is connected to the output electrode 760 of the opposite sign threshold voltage extractor TFT 742, when p-channel transistor is used as shown in fig. 7. Considering that transistors TFT 742 and the driving TFT 4202 have equal threshold voltages, since they are closely located on the same wafer, the input voltage of the buffer 30 is equal to the opposite sign value of the driving TFT 4202 threshold voltage. The drain electrode of TFT 932 is coupled to a dc bias current I_{bias2} 980. This means that the current flowing through the input transistor TFT 932 of the buffer is kept constant and the voltage gain is unity. The buffer 30 could be described as a voltage follower with shunt feedback. The buffer also includes a p-channel TFT 934 with the gate electrode coupled to the drain electrode of input TFT 932, the drain electrode coupled to the source electrode of TFT 932 and the source electrode coupled to Power Supply 1, which is the higher power supply and it has a value equal to V_{DD} . The buffer 30 is able to source a large amount of current. The large sourcing capability is due to the low impedance at the source electrode of the input TFT 932. The output current I_{OLED} of the buffer 30 is equal to the drain current Id_sat of the driving TFT 4202. The current of the TFT 934 is equal to the sum of the Id_sat current and the bias current

I_{bias2} 980. TFT 934 could either working in the saturation mode or in the linear mode without affecting the functionality of the buffer 30. The voltage at the output electrode 970, V_{out} , of the buffer 30 follows the input voltage with a dc level shift V_{ct} , independently of the output current I_{OLED} . Therefore, the voltage at the output electrode 970, V_{out} , of the buffer 30 is the sum of the constant voltage V_{ct} and the absolute value of the threshold voltage of the TFT 4202, i.e.

$$V_{out} = V_{ct} + |V_{thp}|$$

[0070] Fig. 10 shows an example of the n-type implementation of the buffer, ("flipped voltage follower"). The buffer includes an n-type TFT 1032 with the voltage at the gate electrode equal to the voltage at the output electrode 860 of the opposite sign threshold voltage extractor. The drain electrode of the TFT 1032 is coupled to a dc bias current I_{bias22} 1080. This means that the current flowing through TFT 1032 is kept constant and the voltage gain is unity. The buffer 30 could be described as a voltage follower with shunt feedback. The buffer also includes an n-channel TFT 1034 with the gate electrode coupled to the drain electrode of TFT 1032, the drain electrode coupled to the source electrode of TFT 1032 and the source electrode coupled to Power Supply 1, which is the lower power supply having a value equal to V_{EE} or ground. TFT 1032 is connected as a common source follower with constant drain current, since TFT 32 is coupled to a dc bias current I_{bias22} 1080. Therefore, the gain of the buffer is unity. In this case where n-channel TFTs are used, the buffer is able to sink an amount of current, but the sinking capability is restricted from the bias current I_{bias22} 1080. The bias current I_{bias22} is equal to the sum of the I_{d_sat} (or I_{OLED}) plus the drain current I_{EE} of TFT 1034. The output voltage of the buffer is given by the difference of the constant voltage V_{ct1} and the threshold voltage of the TFT 5202, i.e.

$$V_{out1} = V_{ct1} - V_{thn}$$

[0071] From the above description, it is shown that in both p-type and n-type implementations of the threshold voltage cancellation circuit 20, suppress of the threshold voltage variations is static, without needing additional control signals. Therefore, only one phase of operation occurs during the functionality of the pixel. Furthermore, no changes have to be made in the basic AMOLED architecture shown in figure 2.

[0072] Fig. 11 shows the complete p-type implementation of the pixel circuit 200. In this implementation, all transistors are p-channel thin film transistors, Power Supply 1 is the higher supply voltage designated here as V_{DD} , while the lower supply voltage Power Supply 2 is the ground line.

[0073] The first terminal of the switch TFT 11210 is coupled to the Data Line 14, the second terminal is coupled to the gate of the driving TFT 11202 and the third terminal (gate) is coupled to the Scan Line 12. The source electrode of the driving TFT 11202 is coupled to the first terminal (output) 1170 of the threshold voltage variations cancellation circuit and the drain electrode of the driving TFT 11202 is coupled to the first terminal of the OLED 11206. The second terminal of the OLED 11206 is coupled to the ground line.

[0074] The first terminal of the storage capacitor 11204 is coupled to the gate of the driving TFT 11202 and its second terminal is coupled to the higher external power supply V_{DD} . The storage capacitor 11204 ensures that the gate voltage of the driving TFT 11202 is kept constant during a frame time.

[0075] The drain electrode of TFT 1132 is coupled to a dc bias current I_{bias2} 1180. The gate electrode of TFT 1132 is coupled to node 1160, which is the source electrode of TFT 1142. The gate electrode of TFT 1134 is coupled to the drain electrode of TFT 1132, the drain electrode is coupled to the source electrode of TFT 1132 and the source electrode coupled to the higher power supply voltage V_{DD} . TFT 1142 has the drain and gate electrodes coupled to the ground line and the source electrode coupled to the bias current I_{bias1} 1150.

[0076] In this p-type implementation the threshold voltage extractor TFT 1142 provides at its output node 1160 a voltage value equal to the opposite sign of the threshold voltage, $|V_{thp}|$, of TFT 1142. This voltage, which is the input voltage of the buffer, feeds the buffer consisting of the transistors TFT 1132 and TFT 1134. At the output node 1170 of the buffer, a voltage is produced, which is equal to the sum of a constant voltage and the opposite sign of the threshold voltage value $|V_{thp}|$, $V_s = V_{ct} + |V_{thp}|$, where V_{ct} is a constant voltage independent of the TFTs threshold voltage V_{thp} .

[0077] Node 1170 is coupled to the source electrode of the driving transistor 11202. When a scan signal is applied to the gate of the switching TFT 11210, a data voltage V_{data} is charging the capacitor 11204. Then the drain current I_{d_satp} of the driving TFT 11202 is given by

$$I_{d_satp} = [\mu C_{ox} W (V_s - V_{data} - |V_{thp}|)]^2 / 2L$$

[0078] Since $V_s = V_{ct} + |V_{thp}|$, the drain current of the driving transistor 11202 and then the current driving the OLED 11206 is given by

$$I_{OLED} = I_{d_satp} = [\mu C_{ox} W (V_{ct} - V_{data})^2] / 2L$$

[0079] The above expression shows that the current flowing through the OLED device 11206 is independent from the driving TFT threshold voltage and the brightness of the OLED device will be well - controlled.

[0080] In this p-type implementation, in case where an OLED light emitting element is used, the anode of the OLED is driven and the cathode is coupled to the ground line.

[0081] Fig. 12 shows the complete n-type implementation of the pixel circuit 200. In this implementation, all transistors are n-channel thin film transistors, the Power Supply 2 is the higher supply voltage designated here as V_{DD} , where as the lower supply voltage Power Supply 1 is the ground line.

[0082] The first terminal of the switch TFT 12210 is coupled to the Data Line 14, its second terminal is coupled to the gate electrode of the driving TFT 12202 and the third terminal (its gate) with Scan Line 12. The source electrode of the driving TFT 12202 is coupled to the first terminal (output) 1270 of the threshold voltage variations cancellation circuit and the drain electrode of the driving TFT 12202 is coupled to the first terminal of the OLED 12206. The second terminal of the OLED 12206 is grounded.

[0083] The first terminal of the storage capacitor 12204 is coupled to the gate electrode of the driving TFT 12202 and the second terminal is coupled to the higher external power supply V_{DD} . The storage capacitor 12204 ensures that the gate voltage of the driving TFT 12202 is kept constant during a frame time.

[0084] The drain electrode of TFT 1232 is coupled to a dc bias current I_{bias22} 1280. The gate electrode of TFT 1232 is coupled to node 1260, which is the source electrode of TFT 1242. The gate electrode of TFT 1234 is coupled to the drain electrode of TFT 1232, its drain electrode is coupled to the source electrode of TFT 1232 and its source electrode is coupled to the ground line. TFT 1242 has the drain and gate electrodes grounded and its source electrode coupled to the bias current I_{bias11} 1250.

[0085] In this n-type implementation, the threshold voltage extractor TFT 1242 provides at its output node 1260 a voltage value equal to the difference between V_{DD} and the threshold voltage (which is proportional to the opposite sign of the threshold voltage) V_{thn} of TFT 1242. This voltage, which is the input voltage of the buffer, feeds the buffer consisting of the transistors TFT 1232 and TFT 1234. At the output node 1270 of the buffer a voltage V_{s1} is produced, which is equal to the sum of a constant voltage V_{ct1} and the threshold voltage V_{thn} , $V_{s1} = V_{ct1} + |V_{thn}|$, where V_{ct1} is a constant voltage independent of the TFTs threshold voltage V_{thn} .

[0086] Node 1270 is coupled to the source electrode of the driving transistor 12202. When a scan signal is applied to the gate of switching TFT 12210 a data voltage V_{data} is charging the capacitor 12204. Then, the drain current I_{d_satn} of driving TFT 12202 is given by

$$I_{d_satn} = [\mu C_{ox} W (V_{s1} - V_{data} - |V_{thn}|)]^2 / 2L$$

[0087] Since $V_{s1} = V_{ct1} + |V_{thn}|$, the drain current of the driving transistor 12202 and then the current driving the OLED 12206 is given by

$$I_{\text{OLED}} = I_{\text{d_satn}} = [\mu\text{Cox}W(V_{\text{ctl}} - V_{\text{data}})^2]/2L$$

[0088] The above expression shows that the current that flows through OLED device 12206 is independent of the driving TFT threshold voltage, considering that TFT 1242 of the threshold voltage extractor circuit has similar electrical characteristics with those of the driving TFT 12202.

[0089] In this n-type implementation, in case where an OLED light emitting element is used, the cathode of the OLED is driven and its anode is coupled to V_{DD} .

[0090] Fig. 13 shows the AMOLED display architecture using the proposed pixel circuit 200. This architecture has the same simple structure with the basic AMOLED display architecture of the prior work shown in FIG. 2, in terms of scan lines, data lines and power supplies. It is noted that the proposed pixel circuit requires two additional lines for the dc bias currents; first one for the opposite sign threshold voltage extractor and another one for the buffer.

[0091] The pixel circuit of the present invention offers several advantages that are worth noting, considering an AMOLED image display:

(1) The present invention substantially reduces threshold voltage variations and therefore, the undesirable effects of threshold voltage variations on the brightness of a light emitting device.

(2) The present invention uses a small number of components (five transistors and only one capacitor), as well as limited number of control signals thus allowing for small pixels size leading to high resolution.

(3) The present invention uses a threshold voltage variation cancellation unit, which is a static circuit providing at its output continuously a voltage to compensate for the threshold voltage, and therefore only one control signal, the Scan signal, is needed for the AMOLED display. This, results in a very fast response of each pixel leading to a simple and very fast refreshing of the AMOLED display, therefore to a better quality of the produced image.

(4) In the present invention, the pixel circuit can be implemented with both types of TFT, p-channel and n-channel or even in mixed type n-channel and p-channel fabricated in different TFT technologies, polycrystalline silicon, amorphous silicon, nanocrystalline silicon, organic, and oxide (transparent) TFT technologies. It is noted that depending on the quality or the type of TFT produced in each technology, p-type or n-type or mixed type implementation may be used.

(5) In the present invention, commercially available voltage drivers can be used to address the pixel, with threshold voltage independent OLED drive current transformation, furthermore, commercially available current drivers for the dc bias currents can be used to feed the circuits of the opposite sign threshold voltage extractor, as well as the buffer in case of using the aforementioned p-type or n-type implementations.

[0092] It will be understood that when an element or a terminal of an element or a device is referred to as being "connected to" or "coupled to", another element or a terminal of an element or an electrode of an element, it can be directly on the other element or intervening elements may also be present. In addition, it will be understood that when an element or a device is referred to as being "between" two elements, it can be the only elements between the elements, or one or more intervening elements may also be present. Furthermore, when it is described that a device "includes" a constituent element, it means that the device may further include other constituent elements in addition to the element unless specifically referred to the contrary. Like numbers refer to like elements throughout.

[0093] It should also be understood that terms "first," "second," etc. may be used herein to describe various elements, and should not be limited by these terms. These terms are only used to distinguish an element from another element. Thus, a first element discussed herein could be termed a second element without departing from the teachings of example embodiments.

[0094] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, there are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A pixel circuit including:

a data line means for supplying a data voltage,
a scan line means for supplying a control signal,

a switching transistor means for receiving said control signal through its gate terminal and receiving said data voltage through the source-drain current path,

a driving transistor means, the gate terminal whereof is connected to the source-drain current path of the switching transistor means,

a first and a second power supply voltage line means, wherein the first one is the more positive one in a p-type implementation, and the second one is the more positive one in a n-type implementation, the implementation type being defined by the type of the driving transistor means,

a capacitor means having a first terminal and a second terminal, wherein the first terminal is coupled to the gate of the driving transistor means and the second terminal is coupled to the more positive power supply voltage line means of the pixel circuit, for maintaining the data voltage supplied to the gate of the driving transistor during a predetermined time,

a current-controlled light emitting means, for emitting light which brightness corresponds to the current applied, which is connected between the drain terminal of the driving transistor means and a second power supply voltage line means, adapted to generate light so as to display images, wherein it further comprises a threshold voltage variation cancellation circuit means having two terminals, whereof the first terminal is connected to said first power supply voltage line means, and the second terminal connected to the source terminal of the said driving transistor means, providing an output voltage value to said driving transistor means which is such that a predetermined current is supplied to the light emitting means.

2. A pixel circuit according to claim 1, **characterized in that** the difference between said output voltage value and the opposite sign value of the threshold voltage of the driving transistor means is a constant.

3. A pixel circuit according to one of the preceding claims, **characterized in that** said threshold voltage cancellation circuit comprises :

an opposite sign threshold voltage value extractor means providing at its output terminal a voltage equal to the opposite sign threshold voltage value of said driving transistor means, and

a buffer means having at least an input terminal which is connected to the output terminal of the opposite sign threshold voltage value extractor circuit means and an output terminal, where said output voltage value is provided, wherein the difference between said value and the opposite sign value of said threshold voltage of the driving transistor means is a constant.

4. A pixel circuit according to the preceding claim, **characterized in that** said opposite sign threshold voltage value extractor means comprises an extractor transistor means, providing at its output a voltage value, wherein the difference between said value and the opposite sign value of said threshold voltage of the driving transistor means is a constant, and wherein said buffer means has its input terminal coupled to the source output terminal of said extractor transistor means.

5. A pixel circuit according to the preceding claim, **characterized in that** said extractor transistor means has the same electrical characteristics than the driving transistor means, wherein its gate and drain terminals are electrically coupled to said second power supply voltage line means and its source terminal is fed by a bias current.

6. A pixel circuit according to one of the claims 3 to 5, **characterized in that** said buffer means comprises a buffer transistor means having the gate terminal coupled to the drain terminal of an input transistor means and the source terminal coupled to said first power supply voltage line means of the pixel circuit, said input transistor means having the gate terminal coupled to the output terminal of the opposite sign threshold voltage value extractor means, the drain terminal coupled to a first bias current and the source terminal coupled to the drain terminal of said buffer transistor means.

7. A pixel circuit according to one of the preceding claims, **characterized in that** said switching transistor means is either p-channel or n-channel and all other transistor means are p-channel thin film transistors (TFT), wherein said first power supply voltage line is the higher supply voltage of the pixel circuit and said second power supply voltage line is the lower supply voltage of the pixel circuit.

8. A pixel circuit according to one of the preceding claims, **characterized in that** said switching transistor means is either p-channel or n-channel and all other transistor means are n-channel thin film transistors (TFT), wherein said first power supply voltage line is the lower supply voltage of the pixel circuit and said second power supply voltage line is the higher supply voltage of the pixel circuit.

9. A pixel circuit according to one of the preceding claims, **characterized in that** said transistor means are selected from a list consisting of a polycrystalline silicon TFT, an amorphous silicon TFT, a nanocrystalline silicon TFT, an organic TFT and an oxide (transparent) TFT.

10. An image display comprising a scan driver means which is arranged for driving a plurality of scan lines means, a data driver means which is arranged for driving a plurality of data lines means, both said scan lines means and data lines means having intersections, and pixel circuits according to one of the preceding claims, arranged at said intersections.

11. A method for driving a light emitting means of a pixel circuit of an image display, the pixel circuit comprising:

a data line means for supplying a data voltage,
 a scan line means for supplying a control signal,
 a switching transistor means for receiving said control signal through its gate terminal and receiving said data voltage through the source-drain current path,
 a driving transistor means, the gate terminal whereof is connected to the source-drain current path of the switching transistor means,
 a first and a second power supply voltage line means, wherein the first one is the more positive one in a p-type implementation, and the second one is the more positive one in a n-type implementation, the implementation type being defined by the type of the driving transistor means,
 a capacitor means having a first terminal and a second terminal, wherein the first terminal is coupled to the gate of the driving transistor and the second terminal is coupled to the more positive power supply voltage line means of the pixel circuit, for maintaining the data voltage supplied to the gate of the driving transistor during a pre-determined time,
 a current-controlled light emitting means, for emitting light which brightness corresponds to the current applied, which is connected between the drain terminal of the driving transistor means and a second power supply voltage line means, adapted to generate light so as to display images,
 a threshold voltage variation cancellation circuit means,
 the method comprising:
 conducting the first switching transistor to input the data signal to the gate of the second driving transistor and a first terminal of the capacitance element;
 charging the capacitance element to a voltage corresponding to the data signal and fixing the potential of the gate electrode of the second driving transistor;
 not conducting the first switching transistor to allow the gate electrode of the second driving transistor to be in a floating state;
 supplying current corresponding to potential applied to the gate electrode of the second driving transistor to the light emitting element to emit light;
 wherein the threshold voltage variation cancellation circuit fixes at the source electrode of the second driving transistor a potential the difference between said potential voltage value and the opposite sign value of the threshold voltage of the driving transistor means being a constant ensuring that the current through the light emitting means is made independent from the threshold voltage and its variations of the driving transistor means.

12. A method according to claim 11, wherein said potential voltage value is equal to said opposite sign value of the threshold voltage of the driving transistor means.

13. A method according to one of the claims 11 to 12, wherein the threshold voltage variation cancellation circuit is continuously in a conducting state.

14. A method according to one of the claims 11 to 13, wherein the loading of the capacitor means comprises fully turning on the switching transistor means and wherein the applying of the voltage to the driving transistor means by the capacitor means comprises fully turning off the switching transistor means.

15. A method according to one of the claims 11 to 14, wherein said switching transistor means is either p-channel or n-channel and all other transistors means are of the same type, either p-channel or n-channel, thin film transistors (TFT), and wherein the TFT is one of a polycrystalline silicon TFT, an amorphous silicon TFT, a nanocrystalline silicon TFT, an organic TFT and an oxide (transparent) TFT.

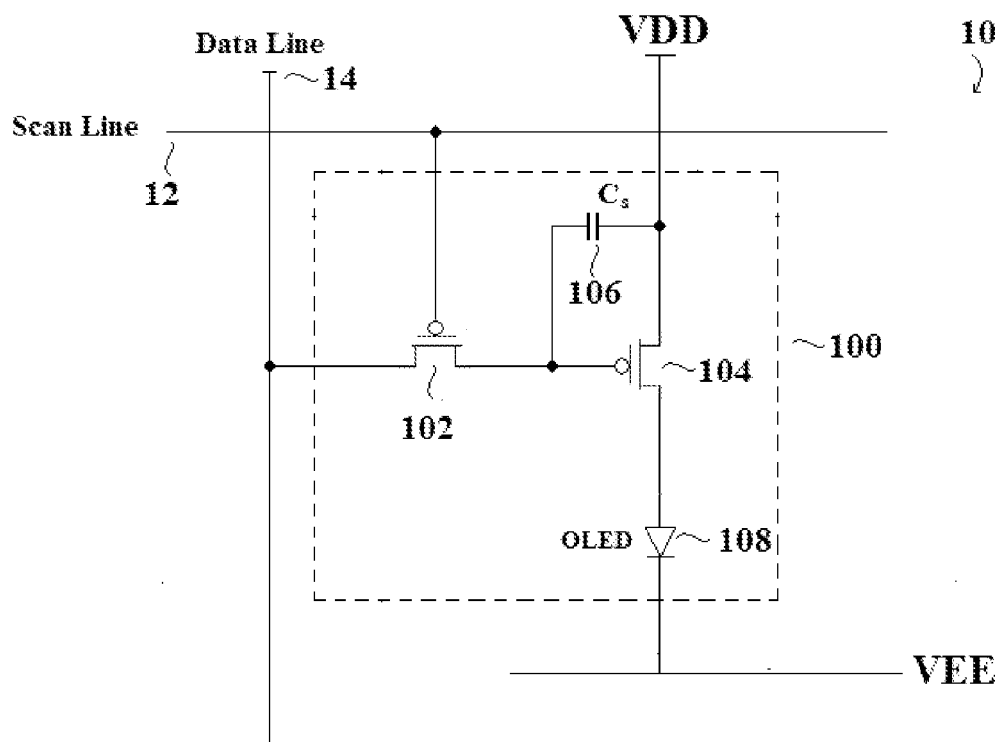


FIG. 1

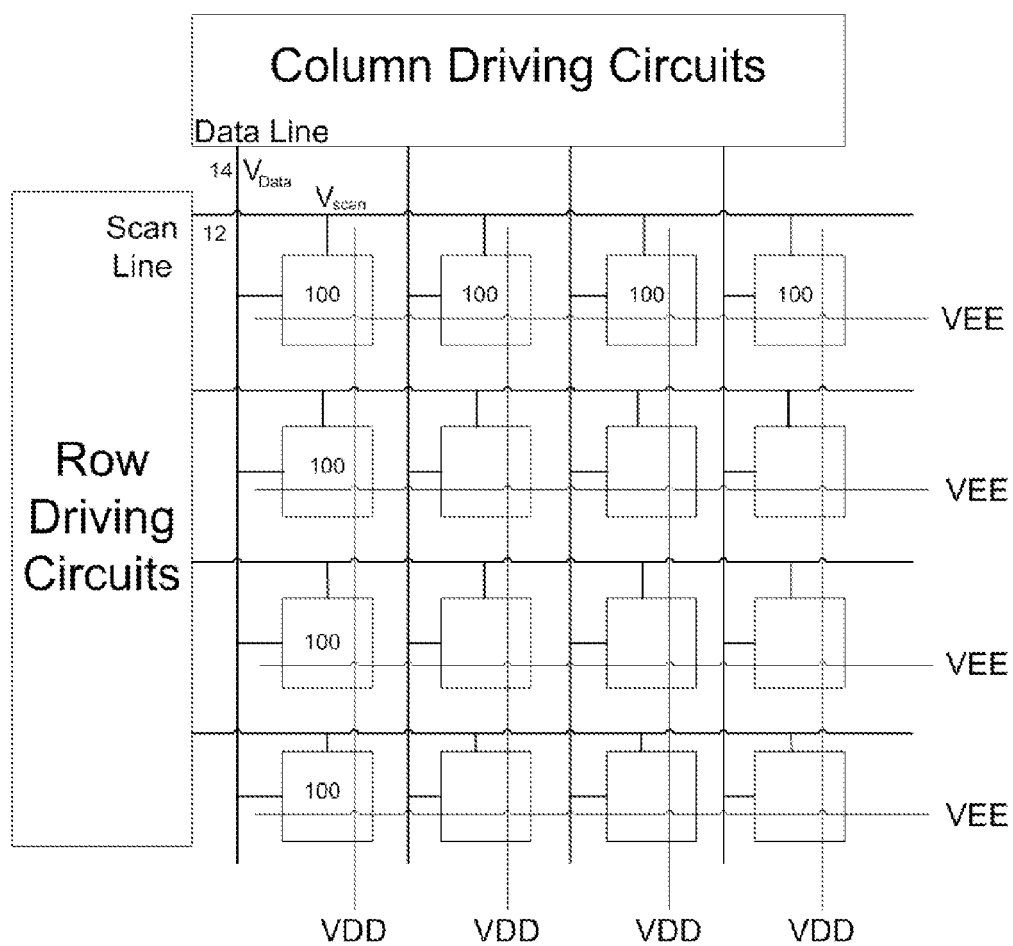


FIG. 2

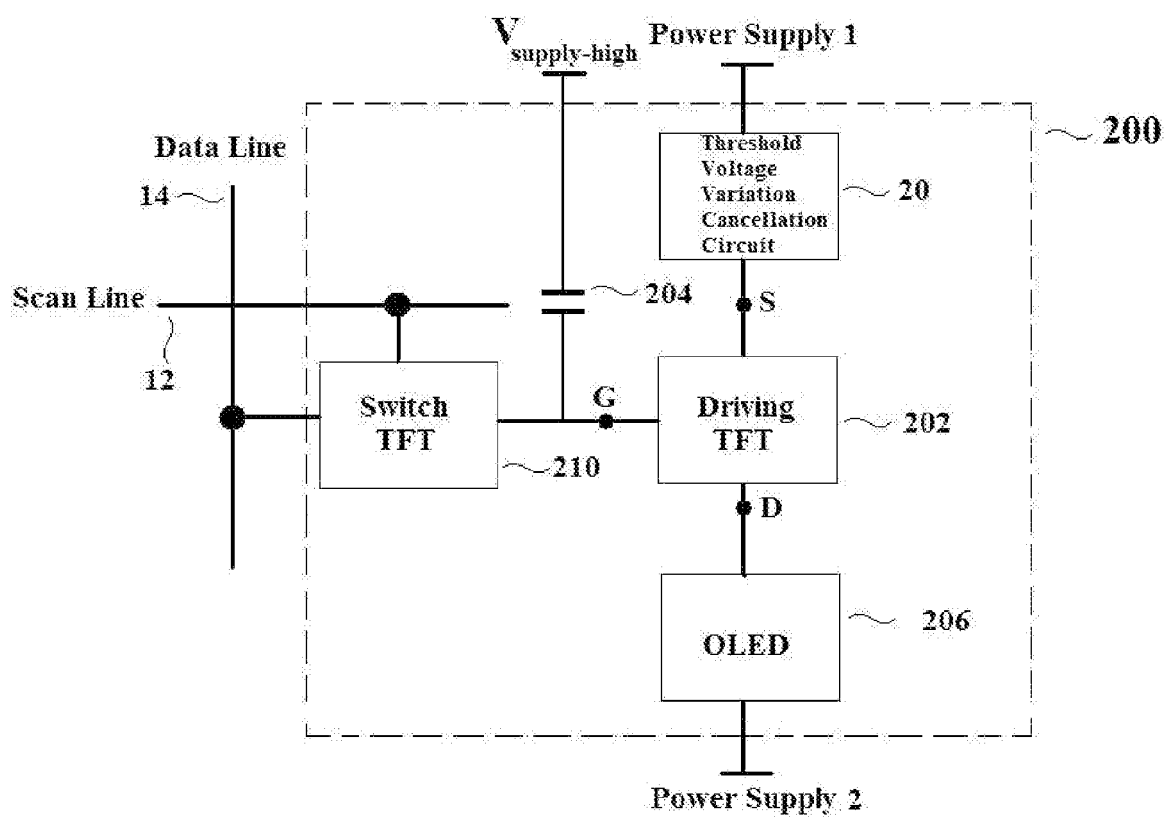


FIG. 3

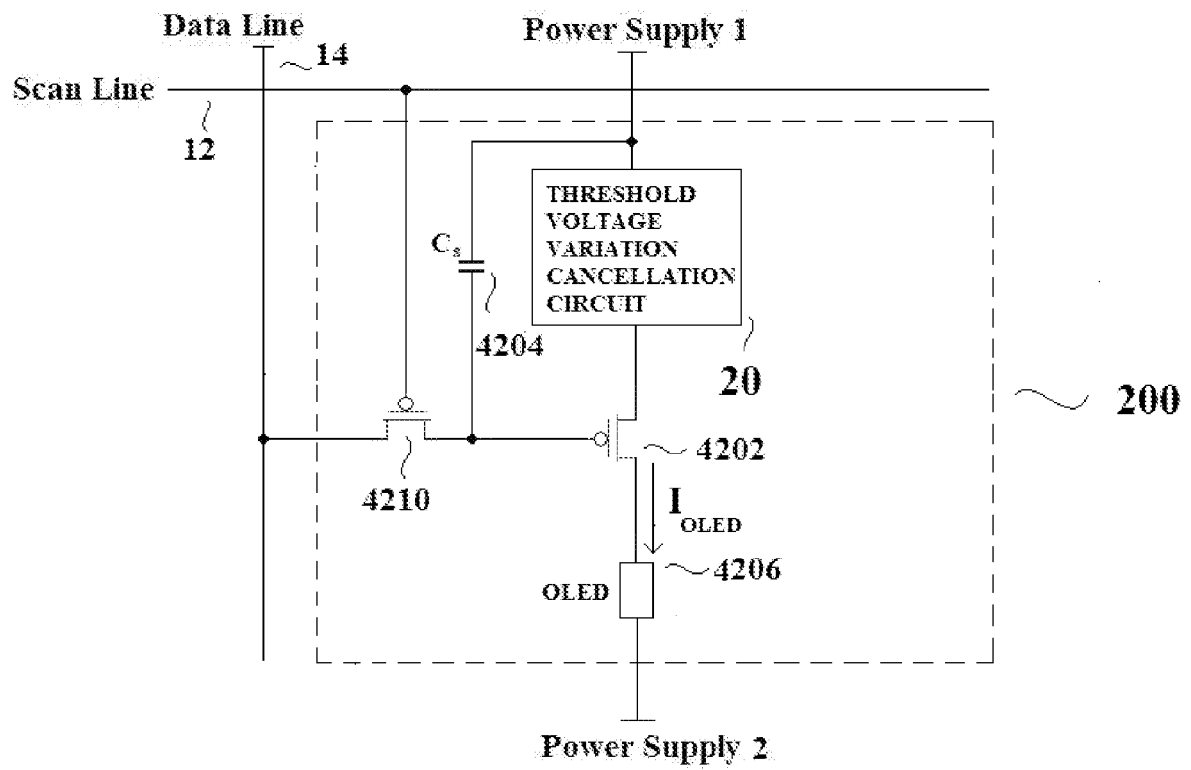


FIG. 4

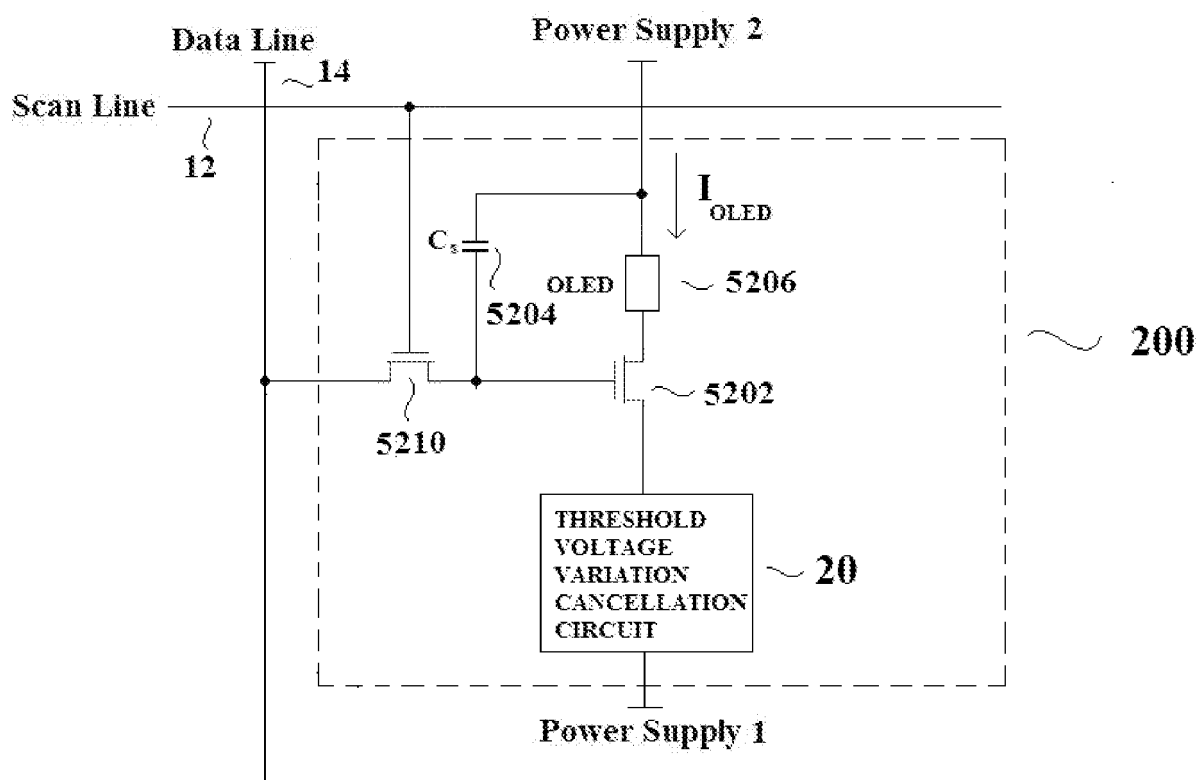


FIG. 5

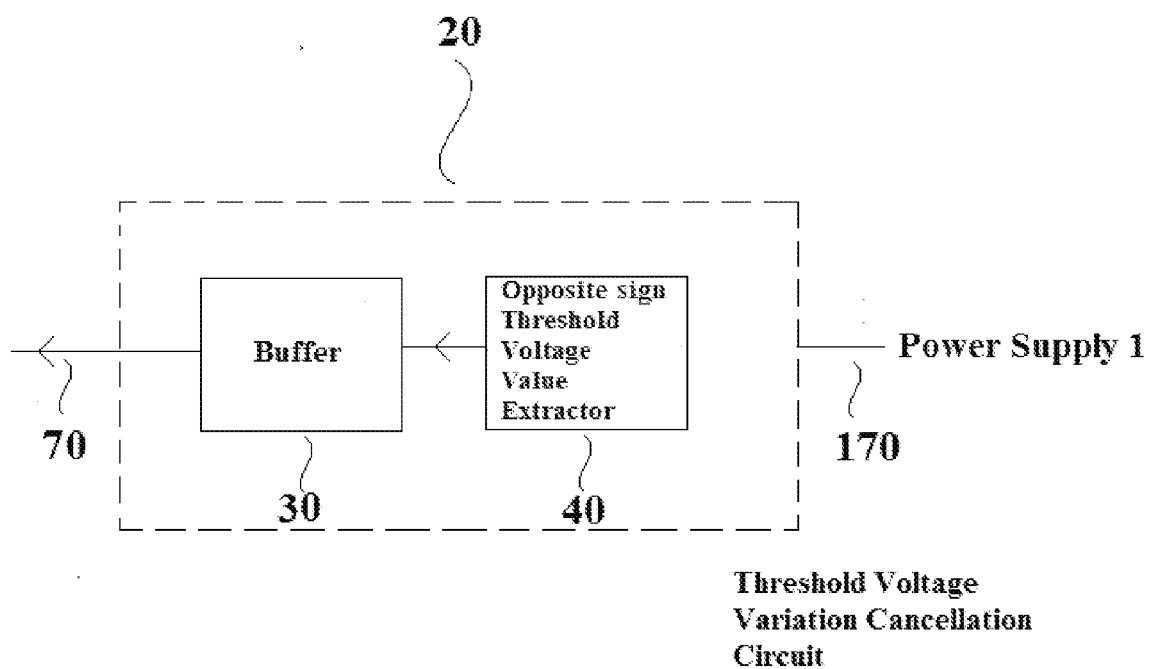


FIG. 6

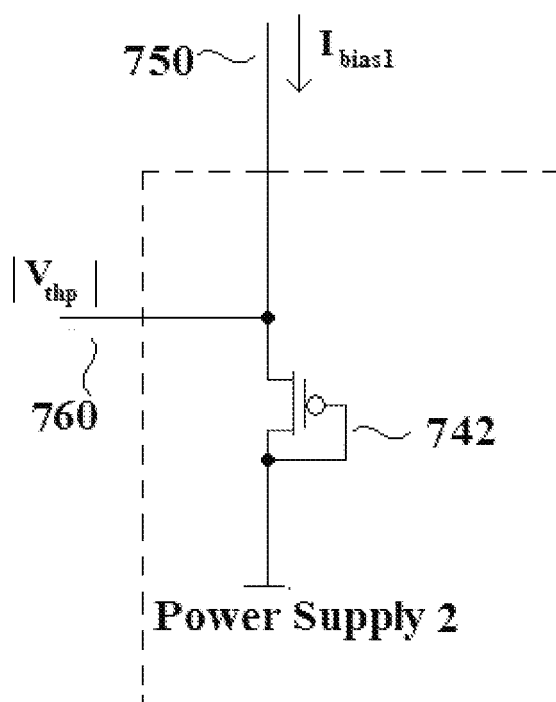


FIG. 7

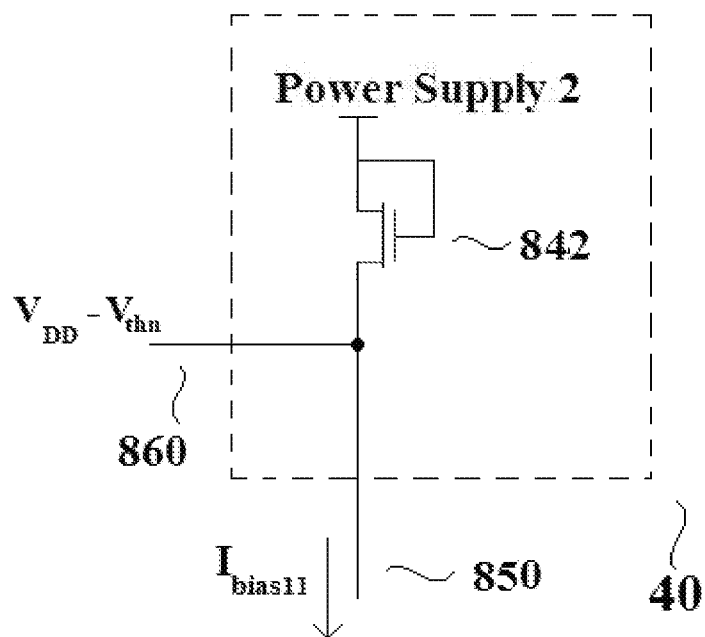


FIG. 8

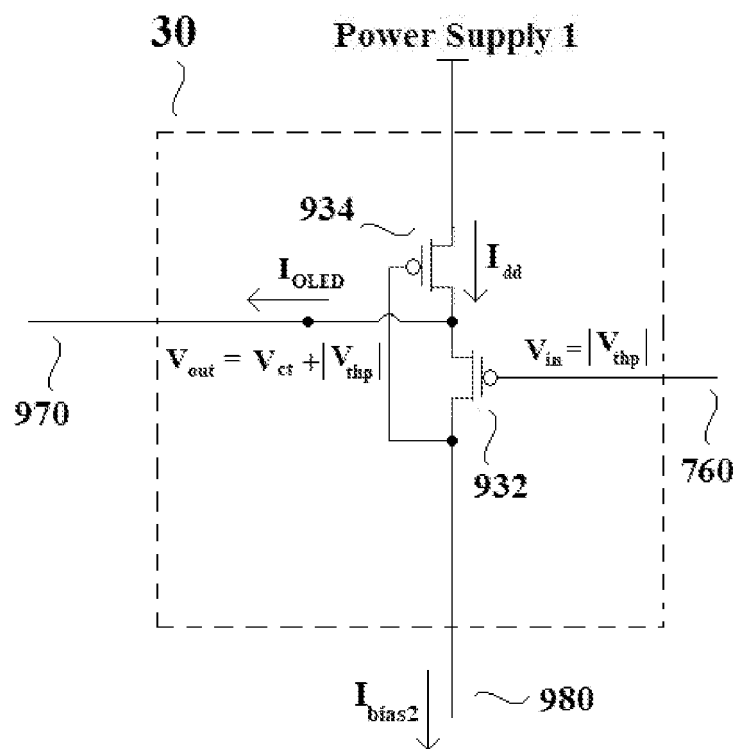


FIG. 9

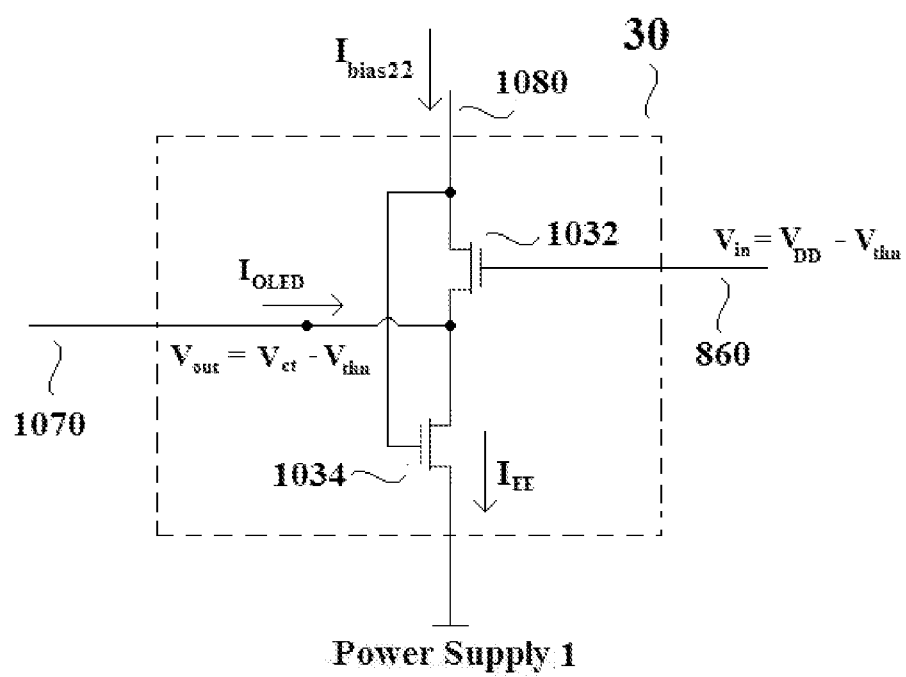


FIG. 10

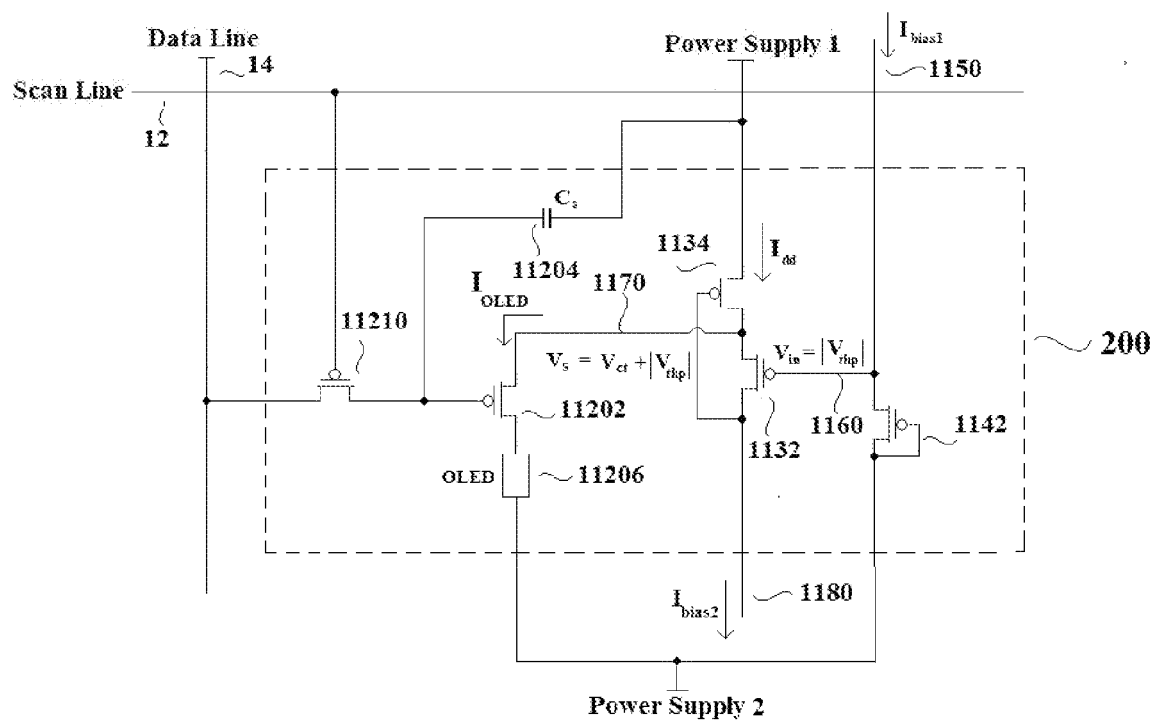


FIG. 11

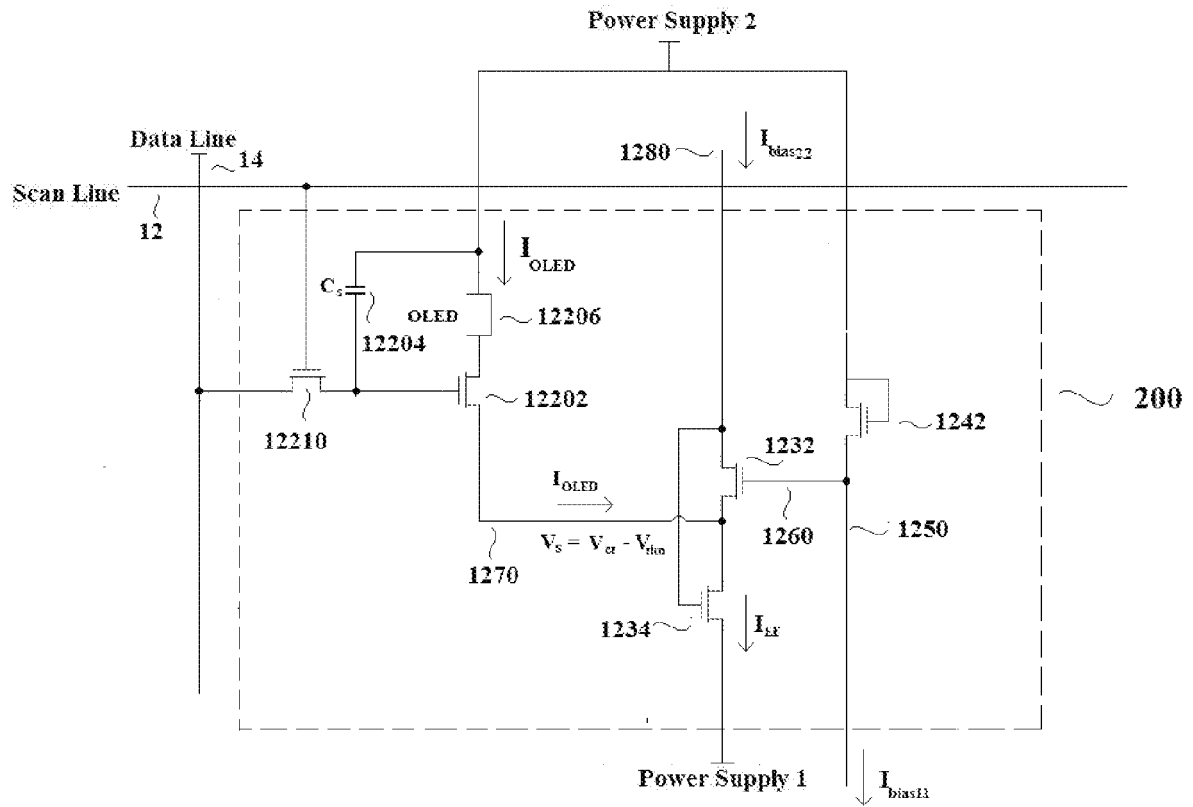


FIG. 12

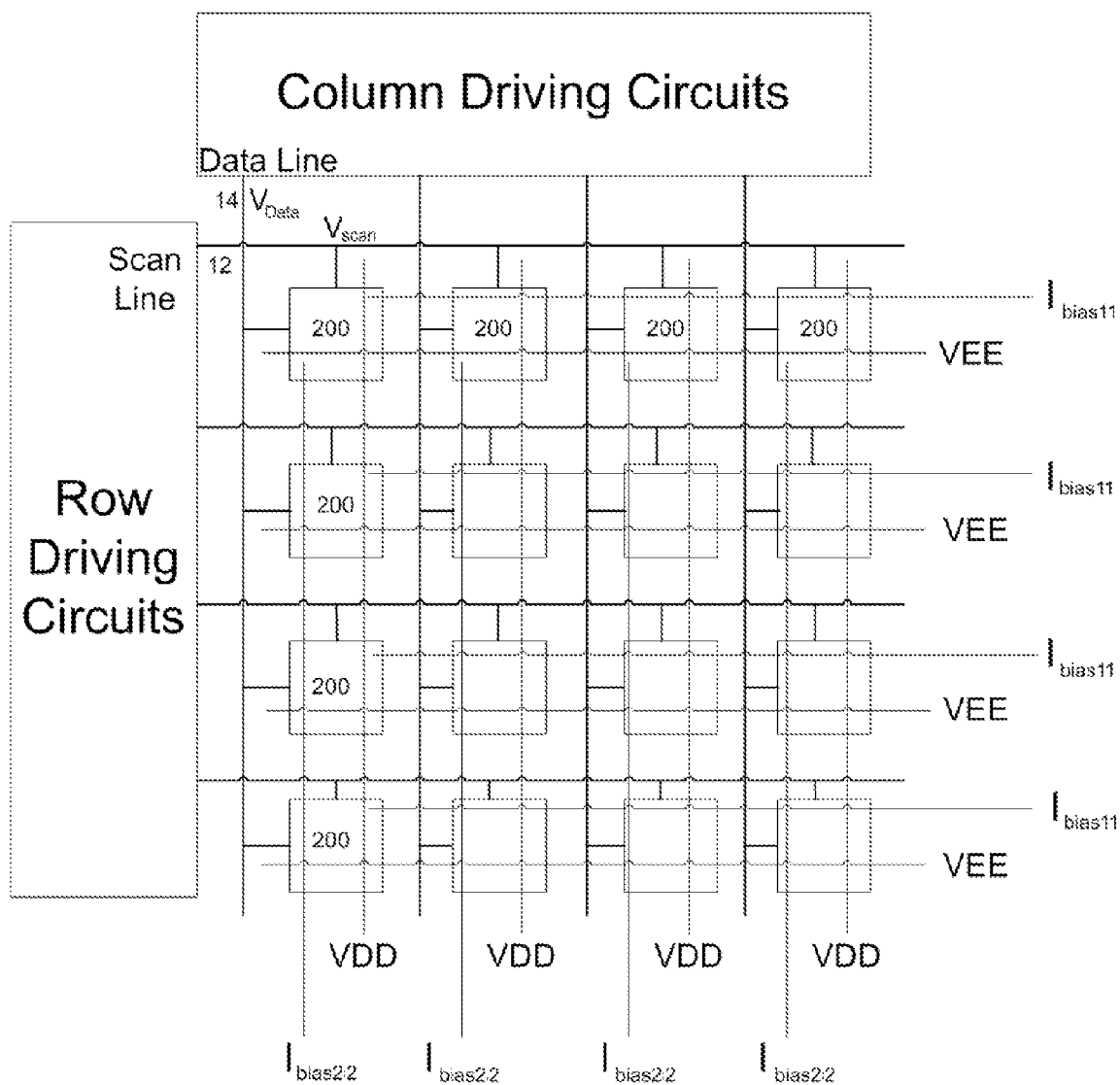


FIG. 13



EUROPEAN SEARCH REPORT

Application Number
EP 09 15 7123

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 1 193 676 A (SANYO ELECTRIC CO [JP]) 3 April 2002 (2002-04-03) * paragraphs [0018], [0059] - [0063]; figures 2,3,5 *	1-5, 7-12,14, 15	INV. G09G3/32
Y	-----	6,13	
Y	US 2005/168415 A1 (NODA TAKESHI [JP] ET AL) 4 August 2005 (2005-08-04) * paragraphs [0014], [0080] - [0096]; figures 2,4,17 *	6,13	
A	----- US 2006/256047 A1 (KIMURA MUTSUMI [JP] ET AL) 16 November 2006 (2006-11-16) * paragraphs [0014] - [0017], [0056] - [0064], [0074] - [0076]; figures 1,3 *	1-15	
A	----- US 2004/183758 A1 (CHEN CHIEN-RU [TW] ET AL) 23 September 2004 (2004-09-23) * paragraphs [0030] - [0038]; figures 4,5 *	1-15	
A	----- EP 1 291 841 A (SEIKO EPSON CORP [JP]) 12 March 2003 (2003-03-12) * paragraphs [0050] - [0063]; figures 2,8 *	1-15	

The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 24 June 2009	Examiner Pichon, Jean-Michel
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

 4
EPO FORM 1503 03.02 (P04C01)



EUROPEAN SEARCH REPORT

Application Number
EP 09 15 7123

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
11 X	EP 1 193 676 A (SANYO ELECTRIC CO [JP]) 3 April 2002 (2002-04-03) * paragraphs [0018], [0059] - [0063]; figures 2,3,5 *	1-5, 7-12,14, 15	INV. G09G3/32
Y	-----	6,13	
7 Y	US 2005/168415 A1 (NODA TAKESHI [JP] ET AL) 4 August 2005 (2005-08-04) * paragraphs [0014], [0080] - [0096]; figures 2,4,17 *	6,13	
7 A	US 2006/256047 A1 (KIMURA MUTSUMI [JP] ET AL) 16 November 2006 (2006-11-16) * paragraphs [0014] - [0017], [0056] - [0064], [0074] - [0076]; figures 1,3 *	1-15	
9 A	US 2004/183758 A1 (CHEN CHIEN-RU [TW] ET AL) 23 September 2004 (2004-09-23) * paragraphs [0030] - [0038]; figures 4,5 *	1-15	
11 A	EP 1 291 841 A (SEIKO EPSON CORP [JP]) 12 March 2003 (2003-03-12) * paragraphs [0050] - [0063]; figures 2,8 *	1-15	

The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 24 June 2009	Examiner Pichon, Jean-Michel
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

EPO FORM 1503 03.92 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 09 15 7123

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

24-06-2009

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 1193676	A	03-04-2002	CN 1367537 A	04-09-2002
			JP 2002175029 A	21-06-2002
			KR 20020025842 A	04-04-2002
			KR 20040049300 A	11-06-2004
			KR 20050012702 A	02-02-2005
			TW 526676 B	01-04-2003
			US 2002074580 A1	20-06-2002
			US 2002075254 A1	20-06-2002
			US 2002084746 A1	04-07-2002
			US 2002101394 A1	01-08-2002
US 2005168415	A1	04-08-2005	CN 1652186 A	10-08-2005
			KR 20050077765 A	03-08-2005
US 2006256047	A1	16-11-2006	NONE	
US 2004183758	A1	23-09-2004	JP 2004287376 A	14-10-2004
			TW 228696 B	01-03-2005
EP 1291841	A	12-03-2003	CN 1405750 A	26-03-2003
			CN 1645460 A	27-07-2005
			DE 60224624 T2	21-05-2008
			JP 4075505 B2	16-04-2008
			JP 2004054188 A	19-02-2004
			KR 20030022693 A	17-03-2003
			TW 571273 B	11-01-2004
			US 2003062844 A1	03-04-2003

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 7167169 B2 [0012]
- US 20050105031 A1 [0013]
- US 7071932 B2 [0013]

Non-patent literature cited in the description

- **V. Vaidya et al.** Comparison of pentacene and amorphous silicon AMOLED display driver circuits. *IEEE Transactions on Circuits and Systems-I: Regular papers*, June 2008, vol. 55 (5 [0007]
- **G.R. Chaji ; P. Servati ; A. Nathan.** *ELECTRONICS LETTERS*, 14 April 2005, vol. 41 (8 [0011]
- A New Voltage-Modulated AMOLED Pixel Design Compensating for Threshold Voltage Variation in Poly-Si TFTs. *IEEE ELECTRON DEVICE LETTERS*, October 2004, vol. 25 (10 [0014]