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(54) **Capacitive switch with enhanced lifetime**

(57) Reducing the negative effects of charging of a capacitive switch enhances the reliability and the lifetime of the capacitive switch. Therefore, a first dielectric layer

is located on the upper surface of a first electrode facing the second electrode, and a second dielectric layer is located on the bottom surface of the second electrode facing the first electrode.

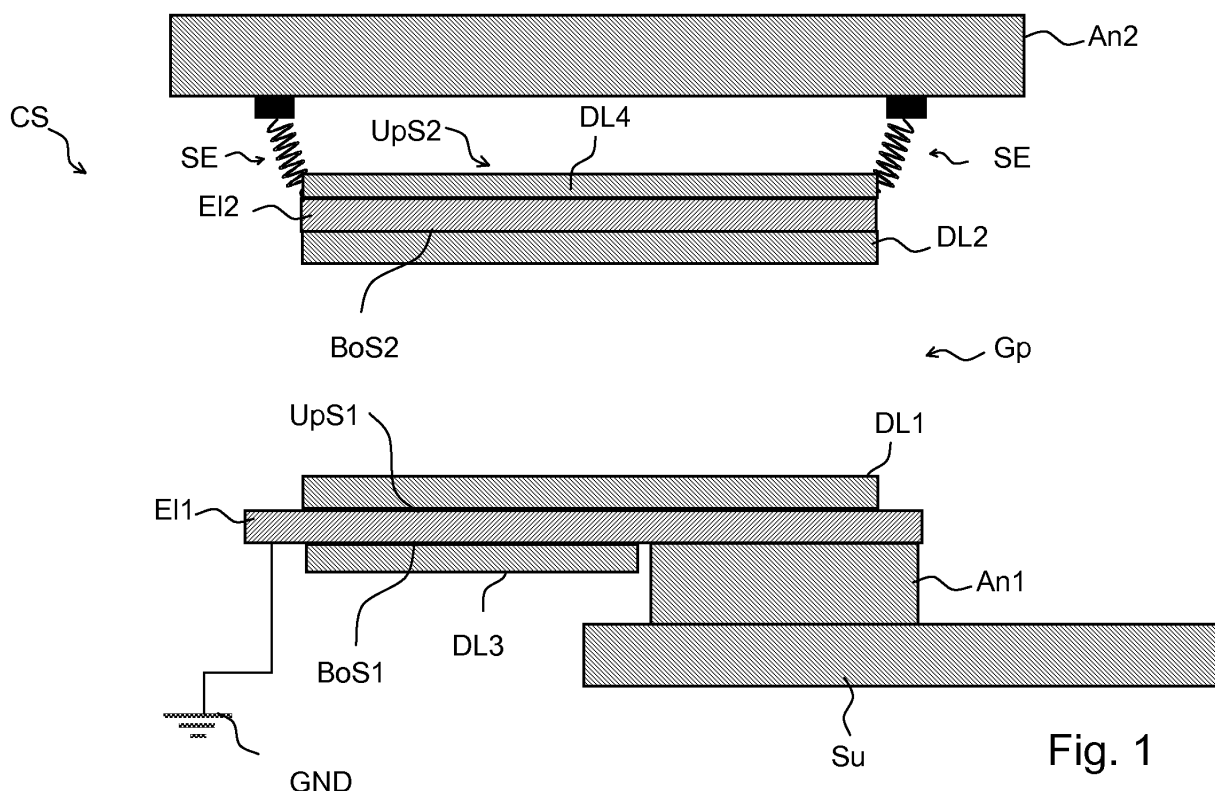


Fig. 1

Description

Field of the invention

- 5 **[0001]** The present invention relates to capacitive switches with enhanced lifetime and reliability by reduced charging effects. The capacitive switches may be MEMS-switches (MEMS = micro electro-mechanical system).

Description of the related art

- 10 **[0002]** Capacitive switches are capacitors comprising two electrodes where at least one electrode is suspended by spring elements and therefore movable. When a voltage that exceeds a certain "pull-in voltage" / "activation voltage" is supplied to the electrodes of the capacitor, the electrostatic force ("pull-in force") leads to a movement of the suspended electrode towards the other electrode; the capacitive switch is in its "closed" state. The other electrode can have a fixed position. When the applied voltage falls below a certain "release voltage" the mechanical force applied by the spring elements separates the electrodes; the capacitive switch is again in its "open" state. Thus, applied voltages can be converted into mechanical movement.

[0003] Such capacitive switches can be used as ON/OFF switches as they can provide the ability of establishing and abandoning galvanic contact between two electrodes (that not necessarily have to be the electrodes of the capacitor).

- 20 **[0004]** Such capacitive switches can also be capacitive elements having a variable capacity: as the capacity of a capacitor depends on the distance of the respective electrodes, a variable distance of the electrodes results in a variable capacity. A capacitive switch has at least two different values of capacitance, i.e. its open and its closed state.

[0005] In order to not short-circuit both electrodes, a dielectric can be located between the electrodes. In "RF-MEMS Switches and Switch Circuits" (IEEE Microwave Magazine, December 2001, page 59), MEMS capacitive switches are disclosed.

- 25 **[0006]** The reliability of capacitive switches is restricted by the effect of charge being injected from an electrode into the dielectric and being trapped in there. Trapped charge can e.g. lead to the situation that a closed capacitive switch cannot be released by decreasing the applied voltage below the activation voltage; the system remains in the closed state.

- 30 **[0007]** As the amount of charge injection into the dielectric is exponential with voltage, it is known that charge injection can effectively be reduced by reducing the activation voltage of a capacitive switch. However, reducing the activation voltage can lead to situations where the closed state cannot be reached at all or where the transition time from the open state to the closed state is undesirable long.

[0008] What is needed is a capacitive switch that is less susceptible to the negative effects of charging and a method for driving such a capacitive switch where the necessity to use a lower activation voltage is avoided.

- 35 Summary of the invention

- [0009]** The present invention provides a capacitive switch that comprises a first electrode, a second electrode, a first dielectric layer, and a second dielectric layer. The first electrode has a bottom surface and an upper surface. The second electrode has an upper surface and a bottom surface where the second electrode is located above the first electrode's upper surface and the second electrode's bottom surface faces the first electrode's upper surface. The first dielectric layer has a first thickness d_1 and is physically attached to the first electrode's upper surface. The second dielectric layer has a second thickness d_2 and is physically attached to the second electrode's bottom surface. In an equilibrium state that may be the open state, a gap is located between the first dielectric layer and the second dielectric layer.

- 45 **[0010]** Although the effort to produce such a capacitive switch is enhanced (one dielectric layer has to be attached to each of the respective electrodes), such a capacitive switch has advantages over known capacitive switches:

- In applications where a certain overall thickness of the dielectric between the two electrodes is necessary, splitting up the dielectric into two distinct layers results in a lower layer thickness of each single layer. Each layer is physically attached to its respective electrode. As a result, the maximum injection depth of negative or positive charge is reduced because electrons cannot be implanted in a deeper depth than the respective thickness of the layer.
- A second advantage arises from the fact that overall charging effects of the respective dielectric layers can cancel each other or can at least be reduced by electrostatic interaction of the charged dielectrics.

- 55 **[0011]** For example: It is possible that charging at the metal/dielectric interface no longer has a negative effect on the properties of the capacitive switch since interface charging can be compensated by influence charge at both interfaces. This is in contrast to known capacitive switches whose dielectric's charge can be transferred from the surface touching the metal electrode to the opposite surface and can be trapped there more effective than in a thinner dielectric.

[0012] Thus, depending on the vertical distribution of the charge density, the lower thickness and the negative sign can decrease the effect of trapped charge.

[0013] In one embodiment of the present invention, the first electrode is physically attached to a substrate.

[0014] A capacitive switch wherein the first electrode is physically attached to the substrate can easily be produced by providing a substrate, depositing a metal or a combination of metals (e.g. an alloy or distinct sub-layers) onto the substrate, and structuring the metal layer in order to get the first electrode.

[0015] In an alternative embodiment, the first electrode is physically attached to a first anchor that itself is physically attached to the substrate and that physically attaches the first electrode to the substrate. If there is only a partial spatial overlap of the electrode and the first anchor, there can be an additional dielectric layer located on the bottom side of the first electrode which may be advantageous with respect to thermal induced stress.

[0016] In one embodiment of the present invention, the second electrode is suspended by at least one spring element to a second anchor. The at least one spring element can - for instance - be a flexible lever or a flexible beam. A flexible lever can be fixed at one distal end to a substrate while the respective other distal end can be the support to which the second electrode is attached to. a flexible beam can be attached to a substrate with both ends while the second electrode is attached to a centered area of the beam.

[0017] In a further embodiment, the ratio $d1 / d2$ of the thickness of the two dielectric layers is in-between 0,2 and 0,95.

[0018] In an alternative embodiment, the ratio of the thicknesses $d1 / d2$ is in-between 0,95 and 1,05.

[0019] In still another alternative embodiment, the ratio of the thicknesses $d1 / d2$ is in-between 1,05 and 5.

[0020] The inventors found out that a capacitive switch whose first and second dielectric layer each have a thickness that is optimized in such a way that the combination of the thicknesses provides a capacitive switch where the dielectric layers' electrostatic charging effects cancel each other fully or at least partially, such that the lifetime and the reliability of the capacitive switch is strongly enhanced.

[0021] In one embodiment of the invention, a third dielectric layer is physically attached to the first electrode's bottom surface (e.g. when the first electrode and a respective anchor do not overlap completely). In another embodiment a fourth dielectric layer is physically attached to the second electrode's upper surface. Further, In still another embodiment the third and the fourth dielectric layer simultaneously are attached to the respective electrode.

[0022] As already mentioned above, an electrode layer having a dielectric physically attached to the underside and another dielectric layer physically attached to the upper side, stress - e. g. thermal induced stress caused by different thermal coefficients of expansion - in the electrode and the attached layers can be reduced. Especially bending of the respective electrode due to the bi-material effect (analog to the bimetal-effect) is effectively reduced. It is, however, possible to chose materials for the electrodes and the dielectrics having similar or identical thermal coefficients of expansion.

[0023] Either the first or the second electrode can be electrically connected to a ground terminal or to ground.

[0024] In situations where the capacitive switch is not in use, i.e. is inactive, the electrical connection to ground enables de-charging of the respective dielectric layer from charge that has been accumulated during its active period. Because the respective dielectric is thinner compared to known capacitive switches the time needed for de-charging is reduced.

[0025] The capacitive switch can be a MEMS-device i.e. a MEMS capacitive switch. It can provide switching capabilities where galvanic connections are established or abandoned with all the advantages of MEMS switches over e. g. PIN diodes or FET switches. Among these are: Near-zero power consumption, very high isolation, very low insertion losses.

[0026] Alternatively, it can be used as a switchable capacitive element having two distinct states (open / close) or that can be driven with a continuously variable voltage in order to provide a capacitive element that has a continuously variable capacity depending on the continuously variable voltage.

[0027] In a preferred embodiment, the capacitive switch is part of a radio frequency (RF-) circuit. Then, the first or the second electrode is electrically connected to the signal path of the radio frequency circuit. Such a capacitive switch can be part of an impedance matching circuit. The capacitive switch can be one out of a group of elements of a capacitive switch array. Such arrays can be used in order to match the impedance of a signal path to the variable impedance of an antenna.

[0028] Each of the first electrode and the second electrode can independently comprise aluminum, tungsten, gold, nickel, copper, AlCu, or an alloy of these metals. Each electrode can further comprise additional elements. Each electrode can consist only of a single element and each electrode can consist of an alloy of different metals.

[0029] Both, the first and the second dielectric layer can comprise silicon oxide (e.g. SiO_2), silicon nitride, a silicon oxy-nitride (e.g. SiON), aluminum nitride, alumina (Al_2O_3), or silicon carbide.

[0030] Each of the third and the fourth dielectric layer also can comprise silicon oxide (e.g. SiO_2), silicon nitride, a silicon oxy-nitride (e.g. SiON), aluminum nitride, alumina (Al_2O_3), or silicon carbide.

[0031] A method for manufacturing a capacitive switch can comprise the steps:

- depositing a first metal layer on a substrate,
- forming the first electrode (E11) by structuring the first metal layer,

- depositing a first dielectric layer (DL1) onto the first electrode (EI1),
- depositing a sacrificial layer onto the first dielectric layer (DL1),
- structuring the sacrificial layer,
- depositing a second dielectric layer (DL2),
- depositing a second metal layer,
- forming a second electrode (EI2) by structuring the second metal layer,
- removing the sacrificial layer by etching.

[0032] In one embodiment of the method, the sacrificial layer or the residual parts of the structured sacrificial layer is / are removed before the second dielectric layer is deposited.

[0033] Each of the layers can be deposited by means of atomic layer deposition, vapor deposition or chemical vapor deposition.

[0034] A method for driving a capacitive switch comprises the steps:

- starting from an equilibrium state where a gap (GP) is located between the first dielectric layer (DL1) and the second dielectric layer (DL2) of the capacitive switch
- bringing into contact the first (DL1) and the second (DL2) dielectric layer by applying a DC voltage across the gap (GP) between first (EI1) and second (EI2) electrode, where the first electrode is part of a moving structure
- separating the first (DL1) from the second (DL2) dielectric layer by decreasing or releasing the DC voltage.

[0035] A method for driving also can comprise the steps:

- starting from an equilibrium state where a gap (GP) is located between the first dielectric layer (DL1) and the second dielectric layer (DL2)
- bringing into contact the first (DL1) and the second (DL2) dielectric layer by applying a AC voltage across the gap (GP) between first (EI1) and second (EI2) electrode, where the first electrode is part of a moving structure and where cycle duration of the AC voltage is bigger than the relaxation time of the moving element and the AC cycle duration is shorter than twice the relaxation time of the moving element,
- separating the first (DL1) from the second (DL2) dielectric layer by releasing the AC voltage.

[0036] Here, AC cycle duration is understood to be the average time needed to change the sign of the polarization of one electrode. In other words: the transition time from one polarity to the opposite polarity is shorter than the relaxation time of the moving element.

[0037] In one method for driving the capacitive switch the period of time when a positive voltage is applied is equal to the period of time when a negative voltage is applied.

Brief description of the drawings

[0038] The present invention will become fully understood from the detailed description given herein below and the accompanying drawings. In the drawings,

FIG. 1 illustrates a cross-section of a capacitive switch,

FIG. 2 illustrates an equivalent circuit diagram of an impedance matching circuit where a capacitive switch is used as a capacitive element with variable capacity.

Detailed description of the embodiments

[0039] FIG. 1 illustrates a capacitive switch CS having a first electrode E11 and a second electrode E12. A first dielectric layer DL1 is located on the upper surface UpS1 of the first electrode and physically attached to the surface. A second dielectric layer DL2 is located at the underside of the second electrode BoS2 and physically attached to the surface. The first electrode E11 is physically attached to a first anchor An1 which itself is physically attached to a substrate Su. The first electrode E11 and the first anchor An1 do not completely overlap. Opposite to the first dielectric layer DL1, a third dielectric layer DL3 is located on the area of the bottom surface BoS1 of the first electrode E11 where the first electrode E11 and the first anchor An1 do not overlap.

[0040] The second electrode E12 is suspended by spring elements SE. The spring elements physically attach the second electrode E12 to a second anchor An2.

[0041] The second electrode E12 can be electrically connected to an external switching environment (not shown). In

FIG. 1, the first electrode E11 is electrically connected to ground GND.

[0042] A gap Gp separates the first dielectric layer DL1 from the second dielectric layer DL2. The upper surface UpS1 of the first electrode E11 faces the bottom surface BoS2 of the second electrode E12.

[0043] FIG. 2 illustrates one possible application of a capacitive switch CS where the capacitive switch CS is part of an impedance matching circuit IMC. The impedance matching circuit is electrically connected to a signal path SP - e.g. as part of the electrical environment of a mobile communication device. The impedance matching circuit IMC further comprises capacitive elements CE and inductive elements IE that are electrically connected to the capacitive switch CS and the signal path SP.

[0044] The capacitive switch of the present invention can be mounted in any arbitrary spatial position. The phrases "upper" and "lower" surface refer to the position of the respective elements relative to other elements of the capacitive switch. The wording does not refer to the absolute position of the elements.

[0045] The present invention comprises electrodes and dielectric layers. The basic concept does not depend on details concerning the dimensions of the components/elements building the capacitive switch further. The invention is not restricted by the embodiments or the accompanying figures. Embodiments based on combinations of presented features or embodiments that further comprise additional elements are also possible.

[0046] Thus, numerous variations departing from the figures are possible without departing from the scope of the invention.

List of reference signs

[0047]

AN1, AN2:	first anchor, second anchor
BOS1:	bottom surface of first electrode
BOS2:	bottom surface of second electrode
CE:	capacitive element
CS:	capacitive switch
DL1, DL2, DL3, DL4:	first, second, third and fourth dielectric layer
EL1, EL2:	first, second electrode
GND:	ground
IE:	inductive element
IMC:	impedance matching circuit
SE:	spring element
SP:	signal path
SU:	substrate
UPS1:	upper surface of first electrode
UPS2:	upper surface of second electrode

Claims

1. A capacitive switch (CS), comprising:

- a first electrode (E11) having an bottom surface (BoS1) and an upper surface (UpS1),
- a second electrode (E12) being located above the first electrode's upper surface (UpS1) and having an upper surface (UpS2) and an bottom surface (BoS2), the bottom surface (BoS2) of the second electrode (E12) facing the first electrode's upper surface (UpS1),
- a first dielectric layer (DL1) having a first thickness d1 and being physically attached to the first electrode's upper surface (UpS1),
- a second dielectric layer (DL2) having a second thickness d2 being physically attached to the second electrode's bottom surface (BoS2),

where

- in an equilibrium state a gap (GP) is located between the first dielectric layer (DL1) and the second dielectric layer (DL2).

2. The capacitive switch of claim 1, where the first electrode (E11) is physically attached to a substrate.

3. The capacitive switch of claim 1, where the first electrode (EI1) is physically attached to a first anchor (An1) that physically attaches the first electrode to a substrate (Su).
- 5 4. The capacitive switch of one of the previous claims, where the second electrode (EI2) is suspended by at least one spring element to a second anchor (An2).
5. The capacitive switch of one of the previous claims, where the ratio $d1 / d2$ of the thicknesses is in between 0,2 and 0,95 or in between 0,95 and 1,05 or in between 1,05 and 5.
- 10 6. The capacitive switch of one of the previous claims, further comprising
 - a third dielectric (DL3) layer being physically attached to the first electrode's bottom surface (BoS1) or
 - a fourth dielectric layer (DL4) being physically attached to the second electrode's upper surface (UpS2).
- 15 7. The capacitive switch of one of the previous claims, wherein one of the first (EI1) and the second (EI2) electrode is electrically connected to a ground terminal (GND) or wherein one of the first (EI1) and second (EI2) electrode is electrically connected to the signal path (SP) of a RF-circuit.
- 20 8. The capacitive switch of one of the previous claims, formed as a MEMS device.
9. The capacitive switch of one of the previous claims, wherein
 - the first electrode (EI1) comprises one of Al, W, Au, AlCu, Ni,
 - 25 - the second electrode (EI2) comprises one of Al, W, Au, AlCu, Ni,
 - the first dielectric layer (DL1) comprises one of SiO₂, SiN, SiON, AlN, Al₂O₃, SiC,
 - the second dielectric layer (DL2) comprises one of SiO₂, SiN, SiON, AlN, Al₂O₃, SiC.
- 30 10. The capacitive switch of one of claims 6 to 9, where
 - the third dielectric layer (DL3) comprises one of SiO₂, SiN, SiON, AlN, Al₂O₃, SiC, and
 - the fourth dielectric layer (DL4) comprises one of SiO₂, SiN, SiON, AlN, Al₂O₃, SiC.
- 35 11. Method for manufacturing a capacitive switch of one of the previous claims comprising the steps:
 - depositing a first metal layer on a substrate,
 - building the first electrode (EI1) by structuring the first metal layer,
 - depositing the first dielectric layer (DL1) onto the first electrode (EI1),
 - depositing a sacrificial layer onto the first dielectric layer (DL1),
 - 40 - structuring the sacrificial layer,
 - depositing the second dielectric layer (DL2),
 - depositing a second metal layer,
 - building the second electrode (EI2) by structuring the second metal layer,
 - removing the sacrificial layer by etching.
- 45 12. Method according to the previous claim where the sacrificial layer is removed before the second dielectric layer is deposited.
- 50 13. Method for manufacturing a capacitive switch of one of the previous claims where the dielectric layers are deposited by means of an atomic layer deposition method.
- 55 14. Method for driving a capacitive switch of one of claims 1 to 11, comprising the steps:
 - starting from an equilibrium state where a gap (GP) is located between the first dielectric layer (DL1) and the second dielectric layer (DL2)
 - bringing into contact the first (DL1) and the second (DL2) dielectric layer by applying a DC voltage across the gap (GP) between first (EI1) and second (EI2) electrode, where the first electrode is part of a moving structure
 - separating the first (DL1) from the second (DL2) dielectric layer by releasing the DC voltage.

15. Method for driving a capacitive switch of one of claims 1 to 11, comprising the steps:

- starting from an equilibrium state where a gap (GP) is located between the first dielectric layer (DL1) and the second dielectric layer (DL2)
- bringing into contact the first (DL1) and the second (DL2) dielectric layer by applying an AC voltage across the gap (GP) between first (EI1) and second (EI2) electrode, where the first electrode is part of a moving structure and where cycle duration of the AC voltage is bigger than the relaxation time of the moving element and the AC cycle duration is shorter than twice the relaxation time of the moving element,
- separating the first (DL1) from the second (DL2) dielectric layer by releasing the AC voltage.

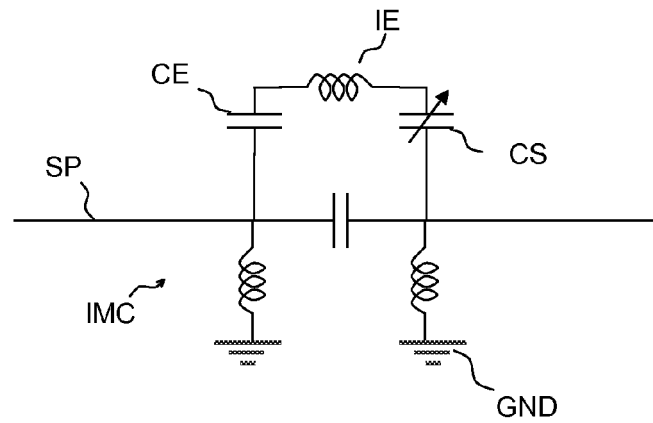
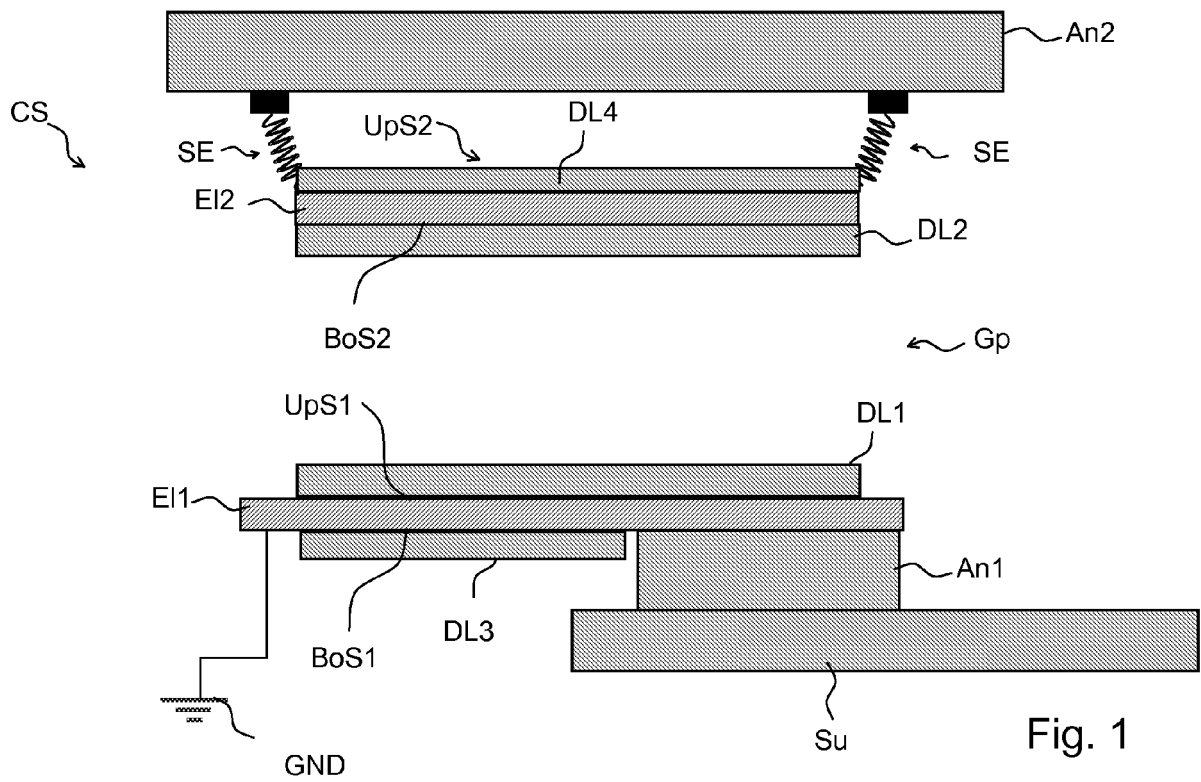


Fig. 2



EUROPEAN SEARCH REPORT

 Application Number
 EP 09 15 8852

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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