(12)

# (11) EP 2 267 184 A1

## EUROPEAN PATENT APPLICATION

(43) Date of publication:

29.12.2010 Bulletin 2010/52

(51) Int Cl.:

C23C 18/30 (2006.01)

C23C 18/20 (2006.01)

(21) Application number: 09163423.8

(22) Date of filing: 22.06.2009

(84) Designated Contracting States:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK TR

**Designated Extension States:** 

**AL BA RS** 

(71) Applicant: THALES NEDERLAND B.V. 7550 GD Hengelo (NL)

(72) Inventors:

 Legtenberg, Rob 7557 HC, HENGELO (NL) Adelaar, Hans
 7558 ST, HENGELO (NL)

(74) Representative: Lucas, Laurent Jacques Marks & Clerk France Conseils en Propriété Industrielle Immeuble "Visium " 22, avenue Aristide Briand 94117 Arcueil Cedex (FR)

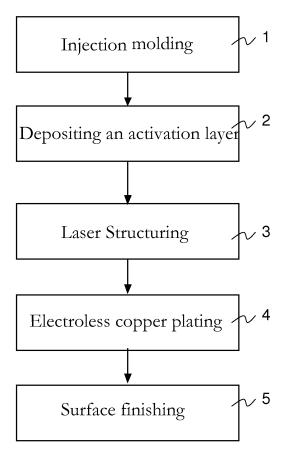
### (54) A method for plating a copper interconnection circuit on the surface of a plastic device

(57) There is disclosed a method for plating a copper interconnection circuit on the surface of a plastic device.

The method comprises a step of depositing an activation layer on the outer surface of the plastic device and a step of plating with copper the outer surface of the plastic device, the activation layer activating plating where copper is needed.

The method comprises a step of laser structuring the outer surface of the plastic device, in order to remove the activation layer locally where copper is not needed.

Application: highly integrated electronics



2 267 184

#### Description

20

30

35

40

45

50

55

**[0001]** The present invention relates a method for plating a copper interconnection circuit on the outer surface of a plastic device. For example, the invention is particularly applicable to the three-dimensional (3D) Moulded Interconnect Device (MID) technologies.

**[0002]** The 3D MID technologies are based on plastic moulding and subsequent metallization techniques, which result in an interconnection circuit on the 3D outer surface of a moulded body.

**[0003]** A flexible way to write an interconnection circuit on the 3D outer surface of a plastic device is by means of laser, such as the Laser Direct Structuring (LDS) technology distributed by the German manufacturer LPKF. The LPKF-LDS process is the most widely used 3D laser structuring technology. It involves three main steps: injection moulding, laser structuring and electroless plating. At the heart of the LPKF-LDS process is a plastic compounded with a special laser-sensitive metal complex developed by LPKF. When the polymer is exposed to the laser, the metal complex is broken down into elemental metal and residual organic groups. The laser draws the circuit pattern onto the part and leaves behind a roughened surface containing embedded metal particles. These particles act as nuclei for the crystal growth during subsequent electroless plating with copper.

**[0004]** Unfortunately, the LPKF-LDS process requires special moulding compounds, which are available in limited materials, types and grades. In addition, the additive metal-complex negatively affects compound properties, especially by modifying its dielectric loss properties.

**[0005]** Moreover, the LPKF-LDS process is an additive technique, which requires laser structuring of the parts of the surface to be plated. In case of design where most of the surface has to be metal plated, this requires that most areas of the surface must be laser structured, hereby inducing longer laser structuring time. The LPKF-LDS process may even require more than one set-up of the laser, in order to laser structure complex 3D shaped geometries, thus leading to higher cost and lower yield.

[0006] Another technique to write an interconnection circuit on the 3D outer surface of a plastic device is the Laser Subtractive Structuring (LSS) process. The LSS process is a subtractive technique, which had been originally developed for Printed Circuit Board (PCB) prototyping. Indeed, for specific applications where a high metallization percentage of the surface is needed or with complex 3D shapes, a subtractive process has advantages with respect to an additive process. The LSS process has been recently applied to MID by E.Beyne et al ("The polymer stud grid array package", Proc. IEPS, Sept. 30 -Oct. 1, 1996, Austin Texas, U.S.A) and W.Falinski et al ("Laser structuring of fine line printed circuit boards", 28th spring seminar on electronics technology, pp. 182-187). First, a copper layer is plated on the surface of a plastic part. Then a tin layer is plated above the copper layer. The tin layer is then subtracted by laser structuring. Afterwards, the underlying copper layer is etched by a wet etchant, whereas the remaining tin layer acts as a mask. Finally, the remaining tin layer is stripped, thus creating a copper circuit.

[0007] Unfortunately, the LSS process involves many additional steps, thus leading to higher cost and lower yield.

**[0008]** The present invention aims to provide a subtractive technique involving a very few steps, which may be used to achieve an interconnection circuit on the outer surface of a plastic device at low cost and high yield. At its most general, the invention proposes a method for plating a copper interconnection circuit on the surface of a plastic device. The method comprises a step of depositing an activation layer on the outer surface of the plastic device and a step of plating with copper the outer surface of the plastic device, the activation layer activating plating where copper is needed. The method comprises a step of laser structuring the outer surface of the plastic device, in order to remove the activation layer locally where copper is not needed.

**[0009]** In a preferred embodiment, the step of plating may comprise a step of electroless copper plating, so as to deposit copper selectively where the activation layer has not been removed.

**[0010]** Advantageously, the method may also comprise a step of surface finishing, for example a step of electroless nickel-gold finishing.

**[0011]** In a preferred embodiment, the step of depositing the activation layer may comprise a step of applying one or a plurality of conditioning substances.

[0012] For example the plastic device may be a three-dimensional moulded plastic device.

**[0013]** Thus, an advantage provided by the present invention in any of its aspects is that all available metallizable mould compounds can be used. Moreover, it is compatible with all existing conventional plastic plating processes.

**[0014]** Non-limiting examples of the invention are described below with reference to the accompanying figure 1, which schematically illustrates an exemplary sequence of steps according to the invention.

**[0015]** The exemplary sequence of steps illustrated by Figure 1 may comprise a step 1 of injection moulding, during which a conventional plastic material is used to form a 3D structure. The exemplary sequence comprises a step 2 of depositing an activation layer, during which one or a plurality of substances are applied on the whole outer surface of the 3D structure. As illustrated below, the step 2 may be a complex process of applying various substances, these substances being chosen based on their ability, alone or in combination, to activate copper platting. The exemplary sequence comprises also a step 3 of laser structuring, during which the activation layer is locally removed where copper

#### EP 2 267 184 A1

is not needed, hereby creating a circuit pattern. Advantageously, the exemplary sequence may also comprises a step 4 of electroless copper plating, so as to deposit a copper layer selectively where the activation layer has not been removed, hereby creating a copper interconnection circuit on a MID. The exemplary sequence may advantageously comprise also a step 5 of surface finishing, during which the outer surface of the MID is finished.

[0016] The following table 1 illustrates a detailed exemplary sequence of steps according to the invention, including time and temperature settings. In the present example, the Ultem 2312 resin is used as plastic material to form a 3D structure. However, many other plastic materials may be used. In the present example, sub-steps 2a to 2s of depositing an activation layer on the outer surface of the 3D structure involve applying a few substances, in order to activate copper plating on Ultem 2312. However, many other substances may be applied depending on the plastic material. Anyway, the basic steps for depositing an activation layer according to the invention are the following: conditioner, etch, neutralizer, glass etch for glass filled compound, promoter, pre-dip, activator, dry. In the present example, the step 5 of surface finishing may advantageously comprise a step of electroless nickel-gold plating. However, many other surface finish processes may be applied.

Table 1

Process flow Ultem 2312 metallization				
Step nr.	Process	settings		
1	Injection moulding / Ultem 2312			
2a	Conditioner	10 min. / 80-84 °C.		
2b	Rinse	3 min. / RT		
2c	Sulfuric acid dip	1 min. / RT		
2d	Rinse	2 min. / RT		
2e	Permanganate	9 min. /80 °C.		
2f	Rinse	4 min. / RT		
2g	Neutraliser	3 min. / 45 °C.		
2h	Rinse	3 min. / RT		
2i	Glass etch	2 min. / 43 °C.		
2j	Sulfuric acid dip	5 min. / RT		
2k	Rinse	3 min. / RT		
21	Conditioner	6 min. / 35 °C.		
2m	Rinse	4 min. / RT		
2n	Predip	1 min. / 27 °C.		
20	Activator	6 min. / 32.5 °C.		
2p	Rinse 1st cascade	1 min. / RT		
2q	Rinse 2nd cascade	1 min. / RT		
2r	Accelerator	3 min. / 49 °C.		
2s	Dry			
3	Laser structuring			
4	Electroless copper plating			
5	Final finish electroless nickel-gold			

**[0017]** As illustrated by the following table 2, the present invention involves a very few steps in comparison with the LSS process known from the prior art:

#### EP 2 267 184 A1

#### Table 2

Proces step	LSS	Laser Activated Surface Removal (invention)	
1	Injection molding	Injection molding	
2	Electroless copper	Surface activation	
3	Full-build electroplate copper	Laser structuring	
4	Electroless tin	Electroless copper	
5	Laser structuring of tin layer	Surface finishing	
6	Etch copper		
7	Strip tin layer		
8	Surface finishing		

**[0018]** Yet a further advantage provided by the present invention is that it requires only conventional plastic plating processes. In particular, no specific catalyst material must be added in the plastic material and no special laser structuring technique is required. Moreover, the present invention provides a subtractive technique, which offers advantages compared to additive techniques, especially for designs in which a high surface coverage is needed or for designs in which the 3D shape is complex or for designs that include through holes.

#### **Claims**

5

10

15

20

25

30

50

55

- 1. A method for plating a copper interconnection circuit on the surface of a plastic device, the method comprising:
  - a step (2) of depositing an activation layer on the outer surface of the plastic device;
  - a step (4) of plating with copper the outer surface of the plastic device, the activation layer activating plating where copper is needed;

the method being **characterized in that** it comprises a step (3) of laser structuring the outer surface of the plastic device, in order to remove the activation layer locally where copper is not needed.

- 2. A method as claimed in Claim 1, **characterized in that** the step of plating comprises a step (4) of electroless copper plating, so as to deposit copper selectively where the activation layer has not been removed.
  - 3. A method as claimed in Claim 1, characterized in that it comprises a step (5) of surface finishing.
- **4.** A method as claimed in Claim 3, **characterized in that** the step (5) of surface finishing comprises a step of electroless nickel-gold finishing.
  - **5.** A method as claimed in Claim 1, **characterized in that** the step (2) of depositing the activation layer comprises a step of applying one or a plurality of conditioning substances (2a, 2l).
- **6.** A method as claimed in Claim 1, **characterized in that** the plastic device is a moulded plastic device.
  - 7. A method as claimed in Claim 1, characterized in that the plastic device is a three-dimensional plastic device.

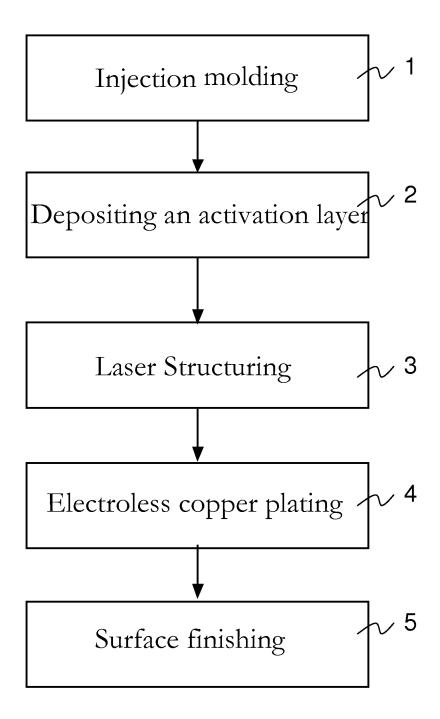


FIG.1



## **EUROPEAN SEARCH REPORT**

Application Number EP 09 16 3423

Category	Citation of document with indicate	tion, where appropriate,	Relevant	CLASSIFICATION OF THE	
Jaiogory	of relevant passages		to claim	APPLICATION (IPC)	
X	ESROM H ET AL: "Modifi with new excimer UV so 15 October 1992 (1992- FILMS, ELSEVIER-SEQUOI LNKD- DOI:10.1016/0046 PAGE(S) 231 - 246, XF ISSN: 0040-6090 [retrieved on 1992-10- * the whole document *	purces" 10-15), THIN SOLID A S.A. LAUSANNE, CH 0-6090(92)90923-Y, 024605386	1-7	INV. C23C18/30 C23C18/20	
X	KOGELSCHATZ U ET AL: "applications of excime sources" 1 October 1991 (1991-1 DESIGN, LONDON, GB LNK DOI:10.1016/0261-3069(251 - 258, XP02415282ISSN: 0261-3069[retrieved on 1991-10-* the whole document *	er ultraviolet .0-01), MATERIALS AND .D- 91)90005-0, PAGE(S) .1 .01]	1-7	TECHNICAL FIELDS SEARCHED (IPC)	
·	The present search report has been	drawn up for all claims			
	Place of search	Date of completion of the search		Examiner	
Munich		23 April 2010	ril 2010 Ramos Flores, Cruz		
CATEGORY OF CITED DOCUMENTS  X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background		E : earlier patent doo after the filing date D : document cited in L : document cited fo	T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons		
A : tech			a : member of the same patent family, corresponding document		

#### EP 2 267 184 A1

#### REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

## Non-patent literature cited in the description

- E.Beyne et al. The polymer stud grid array package. *Proc. IEPS*, 30 September 1996 [0006]
- W.Falinski et al. Laser structuring of fine line printed circuit boards. 28th spring seminar on electronics technology, 182-187 [0006]