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This application was filed on 30-09-2010 as a divisional application to the application mentioned under INID code 62.

(54) **Method and system for hiding refreshes in a dynamic random access memory**

(57) A method and system for refreshing a dynamic random access memory ("DRAM") (40) includes a pair of memory arrays for each of a plurality of banks. The DRAM (40) includes the usual addressing and data path circuitry, as well as a refresh controller (70) that refreshes the arrays in a manner that hides refreshes sufficiently that the DRAM (40) can be used in place of an SRAM as a cache memory (236). Since only one of the arrays in each bank is refreshed at a time, the refresh controller (70) is able to allow data to be written to the array that is not being refreshed. The refresh controller (70) then causes the write data to be temporarily stored so that it can be written to the array of the refresh of the array has been completed. If neither array is being refreshed, the data are written to both arrays. Data are read from the arrays by first checking to determine if any of the arrays is being refreshed. If so, data are read from the array that is not being refreshed.

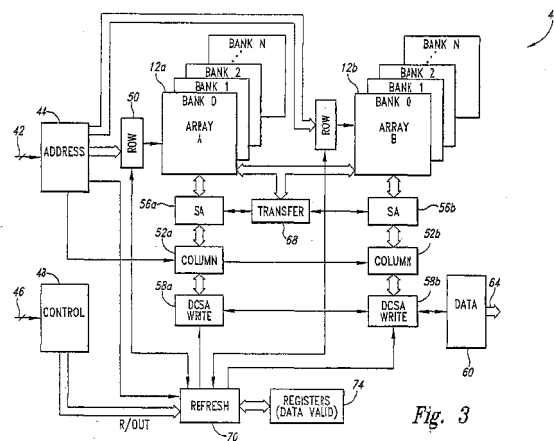


Fig. 3