(11) EP 2 267 832 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:

29.12.2010 Bulletin 2010/52

(51) Int Cl.:

H01P 5/107 (2006.01)

(21) Application number: 09179861.1

(22) Date of filing: 18.12.2009

(84) Designated Contracting States:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

Designated Extension States:

AL BA RS

(30) Priority: 11.06.2009 US 186267 P

(71) Applicants:

• IMEC 3001 Leuven (BE)

 Katholieke Universiteit Leuven 3000 Leuven (BE) (72) Inventors:

- Enayati, Amin 3001 Leuven (BE)
- Brebels, Steven
 3940 Hechtel-Eksel (BE)
- De Raedt, Walter 2547 Lint (BE)
- Vandenbosch, Guy 2830 Heindonk (Willebroek) (BE)
- (74) Representative: Hertoghe, Kris Angèle Louisa et al DenK iP bvba Hundelgemsesteenweg 1114
 9820 Merelbeke (BE)

(54) Integrated system comprising waveguide to microstrip coupling apparatus

(57) The present invention provides an integrated system comprising an RF chip (1), an antenna (2) and a transition element for providing signal coupling between a waveguide (5) and a microstrip line (6). The transition element and the antenna (2) are integrated in a multilayer system (3). The antenna (2) and the RF chip (1) are each located at opposite sides of the multilayer system (3). It is an advantage of embodiments of the present invention that interference between chip (1) and antenna (2) is reduced compared to prior art solutions.

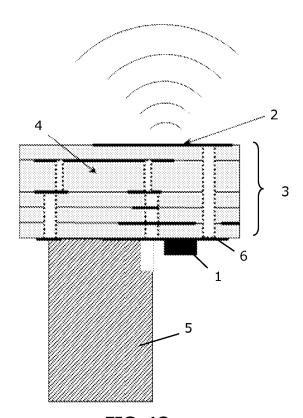


FIG. 12a

EP 2 267 832 A1

20

40

Technical field of the invention

[0001] The present invention relates to a device incorporating signal coupling between a waveguide and a microstrip.

1

Background of the invention

[0002] Increasing demand for higher bandwidths has made greater efforts among researchers to investigate communication systems at higher frequencies. As the frequency of operation increases towards the millimeter and sub-millimeter wavelengths (such as satellite transceivers, RF frontend measurements, collision avoidance radars and novel multi-gigabit millimeter-wave wireless connections), different sorts of measurement problems show up. One of these measurement problems originates from the coaxial nature of the measurement devices commercially available on one side and the planar multi-layer architecture of the devises under test on the other side. Although coaxial-to-planar (Ground-Signal-Ground GSG) probes up to 110 GHz are commercially available, they are expensive and mechanically fragile. Some of the current microstrip to waveguide transitions (or vice versa) are bulky and use several independent pieces that must be assembled in various steps.

[0003] Two elegant solutions to the above measurement problem are as follows. A first solution proposes to design and manufacture all of the needed components in waveguides as the main transmission line. In a second solution, one can design and fabricate different components in a multilayer planar process and afterwards connect them to a waveguide using a suitable transition element. In the latter case where a well-known low cost planar technology is used, the transition from the planar transmission line to the waveguide port plays an important role. Since the dominant mode of a general rectangular waveguide is TE10 mode (transverse electric mode - an electromagnetic field pattern of radiation is measured in a plane perpendicular to the propagation direction of the beam) while the mode of a microstrip line is quasi-TEM mode (transverse electromagnetic mode - a transverse mode in electromagnetic transmission in which there is no electric nor magnetic field in the direction of propagation), the waveguide and the microstrip line need to be connected through a mode converter for impedance matching. FIG. 1 shows a symbolic view of an RF frontend (b), an antenna (c) and a mode converter (microstripto-waveguide transition element) (a).

[0004] The transition elements from microstrip to waveguide can be categorized in three main groups:

- 1- Transition elements longitudinal to the wave propagation direction;
- 2- Transition elements using a slot in one of the waveguide walls to couple the energy from or to the

microstrip line;

3- Transition elements using a microstrip line as a probe inserted into the waveguide and transverse to the wave propagation direction (similar to coax-WG transitions). Such transition elements require electrical coupling providing transition between a microstrip line and a perpendicularly oriented waveguide.

[0005] In "Millimeter-wave Microstrip-to-Waveguide Transition Operating over Broad Frequency Bandwidth", Y. Deguchi et al., IEEE 2005 a microstrip to waveguide transition single-layer, millimeter-wave RF module using a microstrip antenna is disclosed. The transition element connects a microstrip line and a perpendicular waveguide. A probe at one end of the microstrip line is inserted into the waveguide whose one end is short-circuited. It is a disadvantage of this transition element that interaction occurs between the WG and the antenna. This problem could be solved by spatially moving waveguide and antenna away from each other, but this is too expensive in terms of area cost.

Summary of the invention

[0006] It is an object of embodiments of the present invention to provide an integrated system comprising RF chip, antenna and transition element for providing signal coupling between a waveguide and a microstrip line, which integrated element can be used at high frequencies, e.g. frequencies of 40 GHz or higher, for example between 40 GHz and 70 GHz, and is compact.

[0007] The above objective is accomplished by a device according to the present invention.

[0008] The present invention provides an integrated system comprising a waveguide-to-microstrip coupling apparatus providing a transition element for efficient high frequency signal transmission between a local-oscillator and an RF chip, then to an antenna. In accordance with embodiments of the present invention, the transition element and the antenna are integrated in a multilayer system, and the antenna and the RF chip are each located at opposite sides of the multilayer system.

[0009] In particular embodiments, the integrated system reduces interference between the antenna and the RF chip. Embodiments of the present invention are directed to an integrated system that can obtain superior characteristics with the simplicity of its constitution. Embodiments of the present invention allow waveguide to microstrip line conversion (or vice versa) for signals between 40 GHz and 70 GHz, for example for signals of about 60 GHz.

[0010] The multilayer system may comprise a plurality of conductive layers. The plurality of conductive layers may be separated from each other by mean of insulating material, for example layers of insulating material. The multilayer system may for example be any of a multilayer PCB (printed circuit board), LTCC (Low Temperature Cofired Ceramic), MCM (Multi-Chip Module).

40

45

50

[0011] The multilayer system may comprise a first conductive (e.g. metal) layer designed as a microstrip line and a second conductive (e.g. metal) layer designed as ground. The ground layer may be the conductive layer closest to the microstrip line. Including the ground line of the microstrip structure in the multilayer system improves the integration and hence reduces area used.

[0012] In particular embodiments of the present invention, the integrated system furthermore comprises a waveguide, for example perpendicularly connected to the multilayer system. The waveguide may be connected to the multilayer system at the side remote from the antenna. This reduces the scattering effect of the waveguide part on the antenna radiation part.

[0013] The microstrip line may have a resonance with the waveguide encompassing high frequency signals, e.g. signals with a frequency between 40 and 70 GHz, to be conducted by the device. The waveguide may have a top cavity attached to the top layer of the multilayer system. The top layer of the multilayer system is an outer layer of the multilayer system which is located at a side of the multilayer system remote from the side onto which the waveguide is attached. In alternative embodiments of the present invention, the top cavity may be implemented in the multilayer system, for example at a side of the multilayer system remote from the side onto which the waveguide is attached. Hence the top cavity of the waveguide may be provided at a same side of the multilayer structure as where the antenna is provided. The top cavity may be much smaller than the input or output of the waveguide.

[0014] The waveguide may further have a wall opening adjacent the multilayer system through which the microstrip line extends. The multilayer system may comprise a plurality of conductive layers and a plurality of dielectric layers. The plurality of conductive layers may be designed so as to provide impedance matching between a waveguide signal and a signal on the microstrip line. It is an advantage of such impedance matching that it provides better signal transmission.

[0015] To this effect, the conductive layers of the multilayer system may contain openings or irises for matching the signals from the microstrip line to the waveguide and vice versa, thereby reducing effective area of structure, without the requirement of an extra matching device, nor a specific probe design. At least one of the irises in the conductive layers may be designed so as to provide impedance matching between a waveguide signal and a signal on the microstrip line. The design of the conductive layers, in particular for example the design of the irises, may include determining a shape of the irises and/or dimensions of the irises and/or shift of the centre of the irises with respect to the centre of the waveguide and/or shift of the centre of the irises with respect to the centre of the top cavity. The number of available irises, determined by the number of available conductive layers in the multilayer structure, is a design parameter for determining the available bandwidth of the integrated structure.

[0016] The integrated system may further comprise thru metalized vias for connecting different layers of the multilayer system.

[0017] In an embodiment, one of the conductive (e.g. metal) layers of the multilayer system is designed as an antenna, preferably a layer situated on an opposite side of the waveguide. This reduces the scattering effect of the waveguide part on the antenna radiation pattern. In particular embodiments, the antenna is designed in the top conductive layer of the multilayer system.

[0018] In an embodiment, a chip, more particularly for example an RF chip, is attached to the multilayer system (e.g. soldered or wire-bonded) and for example to the bottom layer thereof. This chip may be a transceiver chip for transmitting and receiving high frequency signals.

[0019] In an embodiment, the top cavity of the waveguide is designed in the multilayer structure. In an alternative embodiment, the top cavity is provided separately from the multilayer structure and is connected thereto.

[0020] In an embodiment the multilayer system is a PCB or any other multilayer technology known to a person skilled in the art, e.g. LTCC (Low Temperature Cofired Ceramic) or MCM (Multi-Chip Module).

[0021] The overall integrated device in accordance with embodiments of the present invention provides a low complex device (being mechanically simple) whereby the several components can be implemented in or mounted on the same technology. The overall effective cost is kept to a minimum. Moreover, the proposed design allows the required broadband operation with good performances (low losses, operation ranges, ...)

[0022] The differences of the proposed structure with the available ones are as follows:

- 1. the different position of the microstrip line and its ground plane with respect to the waveguide which allows: a) keeping the microstrip line on the same side as the waveguide part b) having the RF frontend and the antenna on different sides of the multilayer structure c) having the waveguide cavity which is much smaller than the input/output waveguide and the antenna on the same side to reduce the scattering effect of the waveguide part on the antenna radiation pattern.
- 2. Traditionally, some quarter wave microstrip lines are used to match the transition on the microstrip port. However, by using the slots in different layers in the proposed structure as inductive and capacitive loads, these matching lines may be omitted and the transition is matched on the microstrip port plane. This results in a reduction in the area needed for the transition on the microstrip layer.

[0023] By using a multilayer structure, e.g. PCB, the design parameters are increased and consequently design capabilities may be expanded. Moreover, the pro-

10

20

40

50

posed design allows the required broadband operation with good performances (low losses, operation ranges...).

[0024] Further, using the multilayer structure, e.g. PCB, can increase the working bandwidth of the probefed waveguide-to-microstrip transition device, i.e. the waveguide-to-microstrip transition device where the microstrip line is introduced into a slot in the waveguide. [0025] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims. [0026] For purposes of summarizing the invention and the advantages achieved over the prior art, certain objects and advantages of the invention have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the invention. Thus, for example, those skilled in the art will recognize that the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other objects or advantages as may be taught or suggested herein.

Brief description of the drawings

[0027] The invention will be further elucidated by means of the following description and the appended figures.

FIG. 1 shows the three main parts to be integrated on the same structure.

FIG. 2 shows an integrated system according to an embodiment of the present invention.

FIG. 3 shows a cross section of the transition element illustrated as part of the integrated system of FIG. 2. FIG. 4 shows a top view of the multilayer structure used according to embodiments of the present invention.

FIG. 5 shows a plot of a simulation result.

FIG. 6 shows a first sensitivity analysis plot.

FIG. 7 shows a second sensitivity analysis plot.

FIG. 8 shows a third sensitivity analysis plot.

FIG. 9 shows the different mechanical parts of a transition element as may be used in an integrated system according to embodiments of the present invention.

FIG. 10(a) schematically illustrates a waveguide and a transition element integrated in a multilayer system according to embodiments of the present invention, and FIG. 10(b) illustrates the corresponding circuit model.

FIG. 11a schematically illustrates a transition element according to embodiments of the present invention where the end cavity of a waveguide is fab-

ricated in PCB technology.

FIG. 11b schematically illustrates a transition element according to alternative embodiments of the present invention where the end cavity of a waveguide is fabricated in LTCC or MCM technology.

FIG. 12a schematically illustrates an integrated system comprising an RF chip, an antenna and a transition element as illustrated in FIG. 11a.

FIG. 12b schematically illustrates an integrated system comprising an RF chip, an antenna and a transition element as illustrated in FIG. 11b.

[0028] The drawings are only schematic and are non-limiting.

[0029] In the different drawings, the same reference signs refer to the same or analogous elements. Any reference signs in the claims shall not be construed as limiting the scope.

Detailed description of illustrative embodiments

[0030] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not necessarily correspond to actual reductions to practice of the invention. [0031] Furthermore, the terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. The terms are interchangeable under appropriate circumstances and the embodiments of the invention can operate in other sequences than described or illustrated herein.

[0032] Moreover, the terms top, bottom, over, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. The terms so used are interchangeable under appropriate circumstances and the embodiments of the invention described herein can operate in other orientations than described or illustrated herein.

[0033] The term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It needs to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting of only components A and B. It means that with respect to the present invention, the only relevant components of the device are A

40

45

50

and B. In embodiments of the present invention, the three main parts of an integrated system (RF chip, antenna and transition element) are connected using multilayer technology. The multilayer system comprises a plurality of conductive layers, such as metal layers, and a plurality of dielectric layers. In the following, if the simple mentioning of "layer" is used, a conductive layer is meant. The three main parts are connected in such a way that: 1) the antenna and the microstrip to waveguide transition element may be implemented in one multilayer technology; 2) an RF frontend chip can be mounted in or on the same technology; and 3) the interaction between the antenna radiation pattern, the microstrip to waveguide transition element and the RF frontend chip be reduced as much as possible.

[0034] In embodiments of the present invention, the transition element and the antenna are integrated in a multilayer system. A first layer of the multilayer system may be designed as a microstrip line, and a second layer of the multilayer system may be designed as ground. The antenna and the RF chip are each located at opposite sides of the multilayer system. This way, interference between the antenna and the RF chip is reduced, even if both are placed on a small footprint, especially in view of conductive layers being present between the RF chip and the antenna. Hence this solution is cost effective (area cost).

[0035] The waveguide to microstrip transition element, part of an integrated system of embodiments of the present invention, may comprise a waveguide port for connecting, for example perpendicularly, a waveguide to the multilayer system. In particular embodiments, the multilayer system may be a PCB multilayer.

[0036] A waveguide connected to the transition element may have a top cavity attached to the multilayer system, for example to a top layer thereof, and a wall opening adjacent the multilayer system through which a microstrip line extends. In particular embodiments of the present invention, the microstrip line may be implemented in a bottom layer of the multilayer system, hence the waveguide may be connected to the side of the multilayer structure where the microstrip line is provided.

[0037] The transition element may further comprise thru metalized vias for connecting the top and bottom layers of the multilayer system. By the integration of the antenna in the multilayer system, one of the layers of the multilayer system is designed as a (microstrip) antenna, preferably the top layer of multilayer system. In such cases, the top cavity of the waveguide may be applied at the side of the multilayer system where the antenna is provided. An RF front-end chip may then be attached to the bottom layer of the multilayer system, so that antenna and RF front-end chip are located at opposite sides of the multilayer system. By placing the top cavity of the waveguide at the side of the multilayer system where the antenna is provided, interference between waveguide and antenna is reduced.

[0038] FIG. 2 shows an integrated system according

to a first embodiment of the present invention. In FIG. 2 (a) the RF frontend chip (1) and the antenna (2) are on different sides of the multilayer structure (3). So the interaction of the antenna radiation pattern and the RF frontend chip is minimized. On the other hand, FIG. 2(b) shows the exact build up which contains two waveguide parts (4) and (5) and a multilayer structure (3) with 4 conductive layers. The top waveguide part (4) acts as a cavity to reflect the wave into the microstrip line (6) while the bottom waveguide part (5) carries the wave in and out of the transition element (7). As the multilayer part (3) is enclosed with metalized thru vias (8) to prevent the wave from coupling to unwanted layers, the waveguide opening (9) allows the wave to couple to the microstrip line (6) which is patterned on layer 4 of the multilayer structure (3). For the sake of signal matching there are slots (10) in layer 1 and 2 that act as inductive and capacitive loads for the guided mode of the waveguide. The slots (10) are designed so as to provide matching between a waveguide signal and a signal on the microstrip line or vice versa. Finally, layer 3 not only does contain a slot to help the matching procedure, but also it plays the role of the ground plane (11) of the microstrip line which shields the RF frontend chip (1) from the antenna (2) as well, hence reducing interference between these components.

[0039] As explained before, a microstrip line is used in the waveguide to guide the electromagnetic wave from the waveguide to the microstrip line. The microstrip line is manufactured on the multilayer structure, such as for example a multilayer PCB. This multilayer PCB is sandwiched between two conductive, e.g. metallic, waveguide parts (4) and (5).

[0040] FIG. 3 shows a cross section of the waveguide parts (4) and (5), along with the layers of the multilayer PCB (3). The transition element shown in this figure is composed of a waveguide part at the bottom. The waveguide (5) used in this example is the V-band waveguide with the standard name WR-15 and the dimensions of 3.759 mm x 1.880 mm. This part obviously caries the electromagnetic wave through the first waveguide mode towards the microstrip line (6). In order to allow the microstrip line (6) to enter the waveguide (5), an opening is made in the wall of the waveguide with transverse dimensions of 1 mm x 1 mm. This opening is small enough that the cut-off frequency of the first electromagnetic mode in rectangular waveguide resulted within this opening is well above the highest operation frequency. Consequently, the energy coupled to the microstrip line will have a purely microstrip mode distri-

[0041] The microstrip line is manufactured in a multi-layer technology, such as e.g. a PCB technology (3). The base material used for the multilayer PCB in the example described is nelco4000. This material has a permittivity of 3.9 ± 0.2 and a loss tangent of 0.03 ± 0.005 at 60GHz. In Fig. 3, the black bold lines represent the metallic patterned layers in the PCB build-up. From bottom to top

40

45

50

there are 3 layers (21), (22) and (23), the first of which is the microstrip line (21). The substrate layer on which the microstrip line is patterned is a nelco4000 substrate with a thickness of $75\mu m$ (26). As a result, this microstrip line should have a width of 150um in order to yield a 50-ohm characteristic impedance. The microstrip line is placed perpendicular to the width of the waveguide. So its position can be shifted along the width of the waveguide. This shifting parameter along with the length of the microstrip line that goes in the waveguide are two of the design parameters in the PCB part of the transition element.

[0042] The upper 2 conductive layers (22) and (23) in the PCB build-up (for example thickness (25) of 504 μm in the example illustrated) contain openings, also called irises, for example rectangular or circular openings, transverse to the direction of wave propagation. The functionality of these openings in the two upper layers is to load the electromagnetic wave with capacitive and inductive impedances so as to obtain impedance matching between the waveguide and the microstrip line. The number of irises determines the available bandwidth: the more irises are present, the higher the functional bandwidth that can be obtained, if the irises are designed properly. The irises can be designed based on formulae known for irises for impedance matching of coupled waveguides, as for example described in the handbook "Foundations for Microwave Engineering", Robert E. Collin (2001, John Wiley and Sons, Second Edition). From these formulae, suitable dimensions of the irises can be calculated. A combination of capacitive and inductive irises can be considered an LC tank, as illustrated in FIG. 10. FIG. 10(a) schematically illustrates a transition element (7) and a microstrip line (6) integrated in a multilayer system, as well as a waveguide (5) and end cavity (4) with back short (100).

[0043] In particular embodiments of the present invention the end cavity (4) and the back short (100) may be integrated into the multilayer system, as for example illustrated in FIG. 11a and FIG. 11b. FIG. 11a illustrates an embodiment where the end cavity (4) is fabricated in PCB technology. FIG. 11b illustrates an embodiment where the end cavity (4) is fabricated in LTCC or MCM technology. Also the microstrip port (110) and the waveguide port (111) are illustrated in FIG. 11a and FIG. 11(b). In alternative embodiments, as illustrated in FIG. 10(a) the end cavity (4) and the back short (100) may be external to the multilayer system.

[0044] One of the layers of the multilayer system acts as ground layer for the microstrip line, i.e. the metal layer closest to the microstrip line. In FIG. 11a and FIG. 11b this is the metal layer indicated with an encircled reference number 2.

[0045] FIG. 10(b) illustrates the circuit model corresponding to the device schematically illustrated in FIG. 10(a), for use with the formulae known for irises for impedance matching of coupled waveguides as described in the book by Collin above. The open rectangles in the

circuit model represent transmission lines for the waveguide parts, while the filled rectangles illustrate transmission lines for the microstrip parts. Also the microstrip input port (110) and the waveguide port (111) are illustrated. The transmission lines for the waveguide parts take into account the distance between the conductive layers of the multilayer structure. The top iris is represented by the LC tank L10C10, and the bottom iris is represented by the LC tank L11C11.

[0046] The microstrip probe (6) is represented in the circuit model by the inductance L3. It is clear from the circuit model of FIG. 10(b) that supplementary degrees of freedom for matching are added and/or a broader bandwidth can be obtained for the system by adding extra layers in the multilayer system (more d_i's and more LC tanks).

[0047] It is advantageous for bandwidth behavior if the irises are centered in the direction transverse to the microstrip line direction while they can be shifted from the centre point in the longitudinal direction of the microstrip line. As the thickness of the different substrate layers may be chosen before the actual design is performed (hence the parameters d_i in FIG. 10(a) and FIG. 10(b) are fixed), the main design parameters in the PCB buildup may be the width and the length of the irises in the conductive layers of the multilayer structure, in the example given in FIG. 10(a) the two upper PCB layers. Moreover, two other design parameters come from shifting these irises from the centre point tangential to the microstrip-line direction.

[0048] The last objects used on the multilayer, e.g. PCB, part of the transition element are some metalized thru vias (8), illustrated in FIG. 2 and FIG. 4. These vias (8) which connect the top and the bottom conductive layers of the multilayer structure to each other act as a continuum for the waveguide walls in the dielectric material of the multilayer structure. The functionality of these vias is to prevent the electromagnetic wave from penetrating to the dielectric substrate surrounding the irises in different conductive layers of the multilayer structure. The centers of the thru vias determine a shape, such as for example but not necessarily limited thereto, a shape similar to or corresponding to the waveguide shape, e.g. a rectangle or a circle or an oval. If the shape is corresponding to the waveguide shape, this shape may have the same dimensions as the waveguide. In alternative embodiments, dimensions slightly larger or slighter smaller than the waveguide dimensions are also possible. With slightly larger or slightly smaller is meant not more than a quarter wavelength difference. Dimensions which are slightly smaller or slightly larger are advantageous in terms of matching (an extra design parameter is available in the circuit model). The diameter and centre-to-centre spacing of these thru vias in the embodiment described are 150μm and 350μm respectively. As these vias are thru vias, to prevent them from short circuiting the microstrip line, there is an opening in the vias' chain just above the microstrip line. The centre-to-centre distance of the two nearest vias in this region is the same as the width of the opening in the waveguide that is 1mm in the embodiment described. Fig. 4 shows a schematic for the multilayer build-up along with the design parameters for different layers. A top view of the multilayer structure is shown containing three layers (21), (22) and (23). The last part of the transition structure which is named Top-Cap (4) in Fig. 3 is a metal box, having a cavity (24) at one of its faces. The depth of the cavity is a design parameter usable for defining working frequency and/or bandwidth. This cavity (24) that is depicted in Fig. 3 has 3 dimensions of length L4 (in transversal direction of the microstrip line), width w4 (in longitudinal direction of the microstrip line) and depth d4 (e.g. about 250 µm). These 3 dimensions along with the value of the displacement of the centre of the cavity with respect to the centre of the waveguide in the direction of the microstrip line, s4, become 4 other design parameters for the transition element.

[0049] By positioning of the microstrip line and its ground plane with respect to the waveguide as in the present invention, allows: a) keeping the microstrip line on the same side as the waveguide part b) having the RF frontend and the antenna on different sides of the multilayer structure c) having the waveguide cavity which is much smaller than the input/output waveguide and the antenna on the same side to reduce the scattering effect of the waveguide part on the antenna radiation pattern. In the prior art, some quarter wave microstrip lines are used to match the transition on the microstrip port. However, by using the slots in different layers in the proposed structure as the inductive and capacitive loads, these matching lines may be omitted and the transition is matched on the microstrip port plane. This results in a reduction in the area needed for the transition on the microstrip layer. Further, by using a multilayer structure, e.g. multilayer PCB, the number of design parameters is increased and consequently design capabilities are expanded. Moreover, the material used for the transition element has better mechanical stability. As a result, the manufacturing procedure including the thru-hole metallization becomes more convenient and less expensive. On the other hand the assembling of the different parts of the transition such as sandwiching of the multilayer structure, e.g. PCB, between the bulky conductive, e.g. metal, parts of the waveguide takes less effort. Further, using the multilayer structure, e.g. PCB, comprising irises can increase the working bandwidth of the probe-fed waveguide-to-microstrip transition device.

[0050] FIG. 12a and FIG. 12b schematically illustrate an integrated system comprising an RF chip (1), an antenna (2) and a transition element. The transition element in FIG. 12a is as illustrated in FIG. 11a, i.e. a transition element where the end cavity of a waveguide is fabricated in PCB technology. The transition element in FIG. 12b is as illustrated in FIG. 11b, i.e. a transition element where the end cavity of a waveguide is fabricated in LTCC or MCM technology. It can be seen from both embodiments

that RF chip (1) and antenna (2) are located at opposite sides of the multilayer structure, thus saving area. Moreover, in the embodiments illustrated, the antenna (2) is placed at a side of the multilayer remote from the waveguide (5), thus reducing interference between antenna signals and waveguide signals.

[0051] In an experiment, based on the described integrated system comprising a transition element integrated in a multilayer structure and the known electromagnetic properties of different parts of the transition element, a first value for each of the design parameters was chosen. These first values where values which for a person skilled in the art were considered to be realistic values. The thickness of the PCB was predetermined. A waveguide with particular dimensions was selected. For a start, the same dimensions were selected for the irises, and, also for a start, the irises were aligned with the waveguide. Also the dimensions of the upper cavity were selected similar to the dimensions of the waveguide. A bottom margin of some of the above parameter values is restricted by the technology used. The accepted return loss for the aforementioned application (60 GHz receiver) was 10dB. So the goal of the design was to reach the highest possible bandwidth for the return loss, with lowest possible insertion loss in that frequency band. The best result which was obtained by tuning the different design parameters is shown in Fig. 5. This figure shows the insertion loss and return loss for optimized transition for the frequency band from 40GHz to 80GHz. These two frequencies are the cut-off frequencies of the 1st and the 2nd modes in the WR-15 waveguide. In Fig. 5 it can be seen that the insertion loss is less than 1dB for the frequency band 45GHz to 69GHz. If the relative bandwidth is defined as the ratio of the absolute bandwidth to the centre frequency, the designed transition has a relative less-than-1dBinsertion-loss bandwidth of 42%. On the other hand, should 10dB be assumed as the accepted return loss, the optimized transition has a relative more-than-10dB return- loss bandwidth of 46%.

[0052] The values of the design parameters for which the transition has the return loss and insertion loss depicted in Fig. 5 are shown in Table I.

Table I

Design Parameter	Optimized Value (mm)		
d1	0		
L1	0.7		
w2	1.48		
L2	2.76		
s2	0.5		
w3	1.48		
L3	3.26		
s3	0.25		

40

45

(continued)

Design Parameter	Optimized Value (mm)		
d4	0.25		
w4	1.68		
L4	3.56		
s4	0.1		

[0053] It is to be noted that in the optimized transition, all different parts have symmetry versus the x axis depicted in Fig.4 while there are structures that have some shift in the direction of x with respect to the origin O.

[0054] After the optimization procedure and having acceptable simulation results a sensitivity analysis on the sensitive parameters of the transition element was done. As the transition element was designed to be used at millimeter wave frequencies and the resulting dimensions were very tiny, it makes sense to study the effect of probable imperfections of the manufacturing and assembling procedure on the measurement results.

[0055] The first parameter under investigation was the misalignment of the Top-Cap with respect to the multi-layer structure, e.g. PCB, and waveguide parts. Fig.6 shows the simulation results for the insertion loss and return loss sensitivities to this misalignment. As can be seen in this figure, the worst case occurs when the missalignment takes place in the -x direction with an amount of 100 μm . So it can be deduced that the transition element will be not highly sensitive to the miss-alignment of the Top-Cap with respect to the two other parts after being manufactured. This is based on the fact that the mechanical alignment of the 3 different parts has an accuracy better than 100 μm .

[0056] The next sensitivity analysis was done on the misalignment of the waveguide with respect to the Top-Cap and the parts of the multilayer structure, e.g. PCB parts. The simulation results are shown in Fig.7 where the waveguide is shifted by two 50μ m steps in $\pm x$ and $\pm y$ directions.

[0057] It is visible from the simulation results shown in Fig.7 that the transition performance is more sensitive to the misalignment of the waveguide, compared to the misalignment of the Top-Cap. Specifically, in the case of a shift of 100 μm in the x direction the insertion loss and the return loss deviate from their optimum value by considerable values. Consequently, in assembling procedure, special care should be taken into the alignment of the waveguide part.

[0058] The last sensitivity analysis done for the transition structure was on the effect of miss-alignment of the PCB part with respect to the Waveguide and Top-Cap parts. This case is the same case as the miss-alignment of the Cap-Top and waveguide simultaneously with respect to the PCB. Fig. 8 shows the simulation results for the insertion loss and return loss when the PCB is shifted by two $50\mu m$ steps in $\pm x$ and $\pm y$ directions.

[0059] As can be seen in Fig. 8, the return loss level of the transition will degrade when PCB shift is 100 μ m in x or y directions. This degradation is in the return loss level as well as its bandwidth, depending on the case.

[0060] As a result of the sensitivity analysis study, it can be deduced that for a higher-than-10dB return loss and a lower than 1dB insertion loss over the complete frequency band of 45GHz to 69GHz the tolerances in the final alignment and assembly procedure should be less than 100 μm . Fig.9 shows different parts of the transition element to be manufactured and assembled. The flange part (41) comprises the waveguide and a standard flange to connect it appropriately to the external waveguide ports. The PCB (42) is sandwiched between flange part (41) and the other two upper parts of Ring (43) and Cap (44). The latter two parts will be manufactured in one sample as the Top-Cap. As shown in the embodiment illustrated in Fig. 9, there are 4 alignment holes (45) and 3 screw holes (46) in each piece.

[0061] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. The invention is not limited to the disclosed embodiments. Variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. It should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to include any specific characteristics of the features or aspects of the invention with which that terminology is associated.

Claims

35

40

45

50

55

- 1. An integrated system comprising an RF chip (1), an antenna (2) and a transition element for providing signal coupling between a waveguide (5) and a microstrip line (6), wherein the transition element and the antenna (2) are integrated in a multilayer system (3), and wherein the antenna (2) and the RF chip (1) are each located at opposite sides of the multilayer system (3).
- An integrated system according claim 1, wherein the multilayer system (3) comprises a plurality of conductive layers.
- 3. An integrated system according to claim 2, wherein the multilayer system (3) comprises a first conductive layer designed as the microstrip line (6) and a second conductive layer designed as ground layer.
- **4.** An integrated system according to any of claims 2 or 3, wherein the plurality of conductive layers are

designed so as to provide impedance matching between a waveguide signal and a signal on the microstrip line (6).

5. An integrated system according to claim 4, wherein at least one of the plurality of conductive layers has an iris, the dimensions of the at least one iris being adapted for impedance matching between the waveguide (5) and the microstrip line (6).

6. An integrated system according to any of the previous claims, furthermore comprising a waveguide (5) connected to the multilayer system at the side remote from the antenna (2).

7. An integrated system according to claim 6, wherein the waveguide (5) comprises a top cavity (4) attached to the top layer of the multilayer system (3).

- **8.** An integrated system according to any of claims 6 20 or 7, wherein the waveguide (5) further has a wall opening (9) adjacent the multilayer system (3) through which the microstrip line (6) extends.
- **9.** An integrated system according to any of claims 6 to 8, wherein the waveguide (5) is coupled substantially perpendicularly to a conductive layer of the multilayer system (3).
- **10.** An integrated system according to any of the previous claims, wherein the transition element furthermore comprises alignment features (45) for aligning the waveguide (5), the top cavity (4) and the multilayer structure (3) with respect to each other.

10

15

35

45

40

50

55

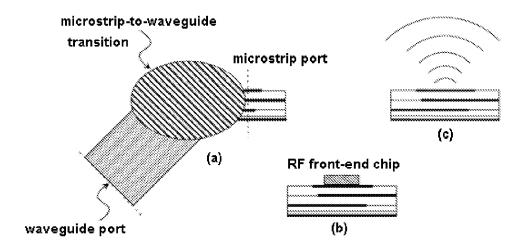


FIG. 1

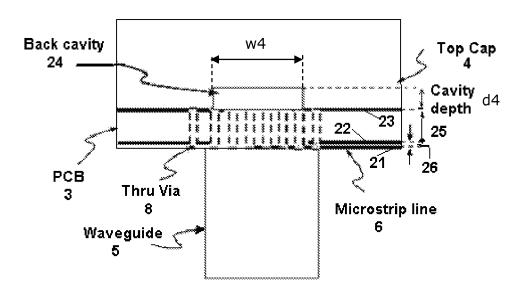
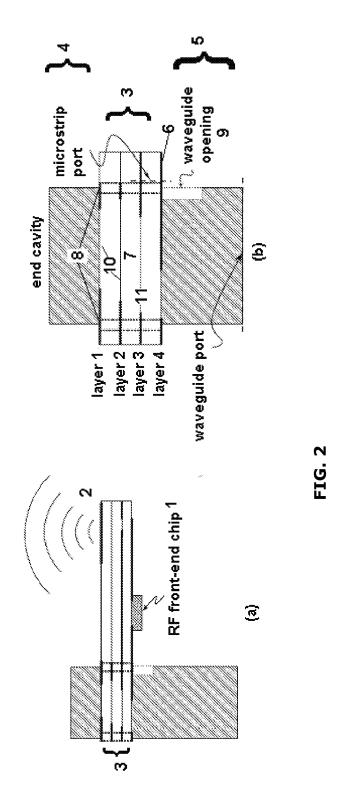


FIG. 3



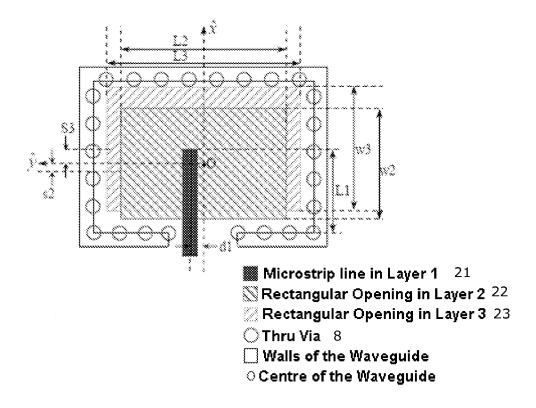
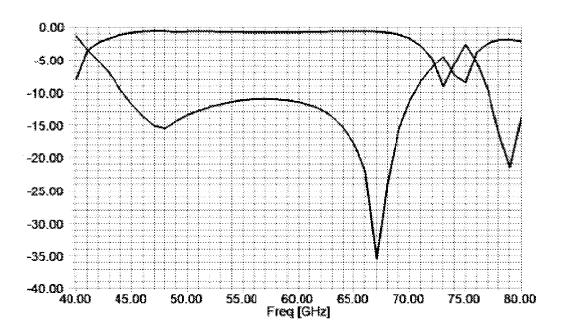


FIG. 4



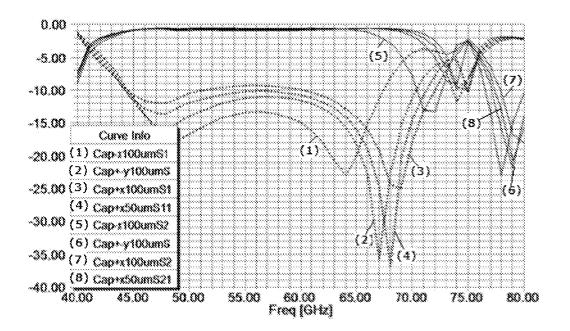


FIG. 6

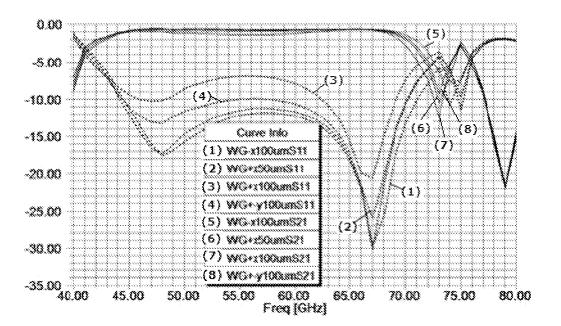


FIG. 7

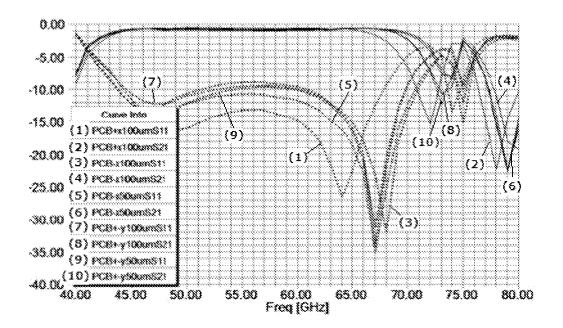


FIG. 8

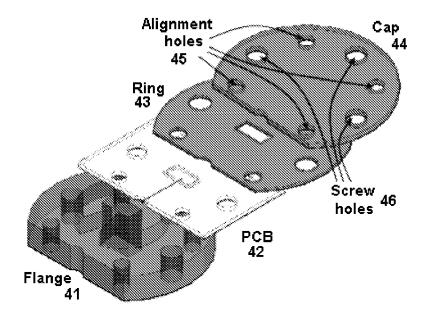
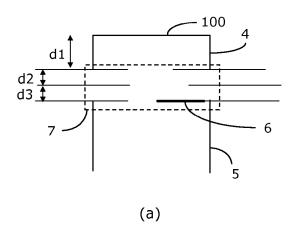


FIG. 9



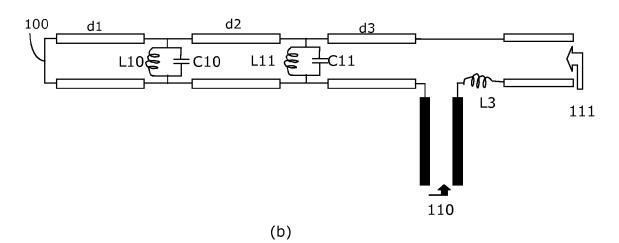


FIG. 10

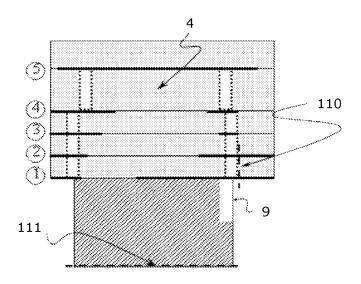


FIG. 11a

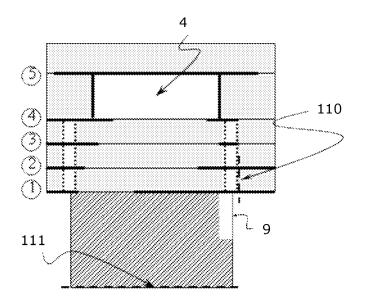


FIG. 11b

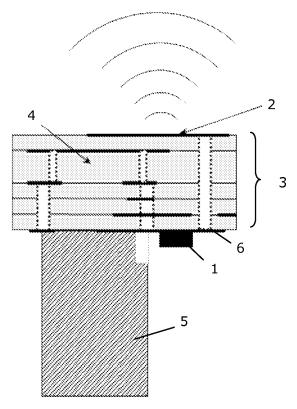


FIG. 12a

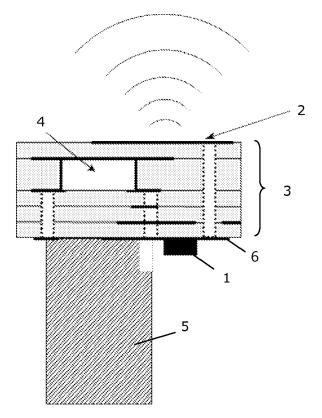


FIG. 12b



EUROPEAN SEARCH REPORT

Application Number EP 09 17 9861

<u> </u>	DOCUMENTS CONSIDERI		T	
Category	Citation of document with indica of relevant passages	tion, where appropriate,	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X Y	EP 1 983 614 A1 (MITSU [JP]) 22 October 2008 * paragraphs [0017],	(2008-10-22)	1-6,8,9 7,10	INV. H01P5/107
'	[0060]; figures 5-1(a)	1-5-2(d) * 	,,10	
Х	US 5 770 981 A (KOIZUM 23 June 1998 (1998-06-	-23)	1-10	
Υ	* abstract; figures 14 * column 3, lines 1-46 * column 4, lines 5-16	A, 1B *) *	7,10	
Х	EP 1 367 668 A1 (SIEME NETWORKS [IT]) 3 December 2003 (2003- * abstract * * paragraph [0020] *		1-10	
Х	EP 1 304 762 A2 (FUJIT SEMICONDUCTOR [US]; FU DEVICES LTD [JP];) 23 April 2003 (2003-04 * abstract; figures 1, * paragraphs [0011], [0025] *	JJITSU QUANTUM 4-23) ,2 *	1-4,6,9	TECHNICAL FIELDS SEARCHED (IPC)
Х	 DP 2009 038696 A (TOYOTA CENTRAL RES & DEV; TOYOTA MOTOR CORP) .9 February 2009 (2009-02-19) f abstract; figures 2,4 *		1-5,9	
Х	JP 2008 252207 A (MITSUBISHI ELECTRIC CORP) 16 October 2008 (2008-10-16) * abstract; figures 1,2 *		1-4,9	
A EP 1 720 213 A1 (MITSUBISHI ELE [JP]) 8 November 2006 (2006-11-* abstract; figures 5,8,9 *		(2006-11-08)	1-4,6,8, 9	
		-/		
	The present search report has been	drawn up for all claims		
	Place of search	Date of completion of the search		Examiner
	Munich	20 April 2010	April 2010 Jäs	
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document		T : theory or principle E : earlier patent doo after the filing dat D : document cited in L : document cited fo	ument, but publi e n the application or other reasons	shed on, or
			& : member of the same patent family, corresponding document	



EUROPEAN SEARCH REPORT

Application Number EP 09 17 9861

Category	Citation of document with in	idication, where appropriate,	Relevant	CLASSIFICATION OF THE
Category	of relevant passa		to claim	APPLICATION (IPC)
A		CHEN MING [US] ET AL L) 008-12-25) *	1,5,7	
				TECHNICAL FIELDS SEARCHED (IPC)
	The present search report has I	peen drawn up for all claims		
	Place of search	Date of completion of the search		Examiner
	Munich	20 April 2010	Jäs	schke, Holger
CA X : parti Y : parti docu A : tech	TEGORY OF CITED DOCUMENTS cularly relevant if taken alone cularly relevant if combined with anotiment of the same category nological background written disclosure	T: theory or princ E: earlier patent o after the filing o D: document cite L: document cite	iple underlying the i document, but publi date d in the application d for other reasons	nvention shed on, or

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 09 17 9861

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

20-04-2010

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
EP 1983614	A1	22-10-2008	CN WO JP US	101395759 2007091470 4394147 2009079648	A1 B2	25-03-2009 16-08-2007 06-01-2010 26-03-2009
US 5770981	Α	23-06-1998	JP JP	2605654 8274513		30-04-1997 18-10-1996
EP 1367668	A1	03-12-2003	NONE			
EP 1304762	A2	23-04-2003	DE JP JP US	60208294 4184747 2003163513 2003076188	B2 A	31-08-2006 19-11-2008 06-06-2003 24-04-2003
JP 2009038696	Α	19-02-2009	NONE			
JP 2008252207	Α	16-10-2008	NONE			
EP 1720213	A1	08-11-2006	WO JP US	2005083832 4176802 2007188258	B2	09-09-2005 05-11-2008 16-08-2007
US 2008316143	A1	25-12-2008	NONE			

FORM P0459

© For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

EP 2 267 832 A1

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Non-patent literature cited in the description

- Y. Deguchi et al. Millimeter-wave Microstrip-to-Waveguide Transition Operating over Broad Frequency Bandwidth, 2005 [0005]
- Robert E. Collin. Foundations for Microwave Engineering. John Wiley and Sons, 2001 [0042]