(54) **Compact FPGA-based digital motor controller**

(57)   A compact field programmable gate array (FP-GA)-based digital motor controller (102), a method, and a design structure are provided. The compact FPGA-based digital motor controller (102) includes a sensor interface (206) configured to receive sensor data from one or more sensors (104) and generate conditioned sensor data. The one or more sensors (104) provide position information for a DC brushless motor (108). The compact FPGA-based digital motor controller (102) also includes a commutation control (210) configured to cre-ate switching commands to control commutation for the DC brushless motor (108). The commutation control (210) generates commutation pulses from the conditioned sensor data of the sensor interface (206). The compact FPGA-based digital motor controller (102) also includes a time inverter (208) configured to receive the commutation pulses. The time inverter (208) converts the commutation pulses into a rotational speed of the DC brushless motor (108) to provide a linear feedback control parameter.
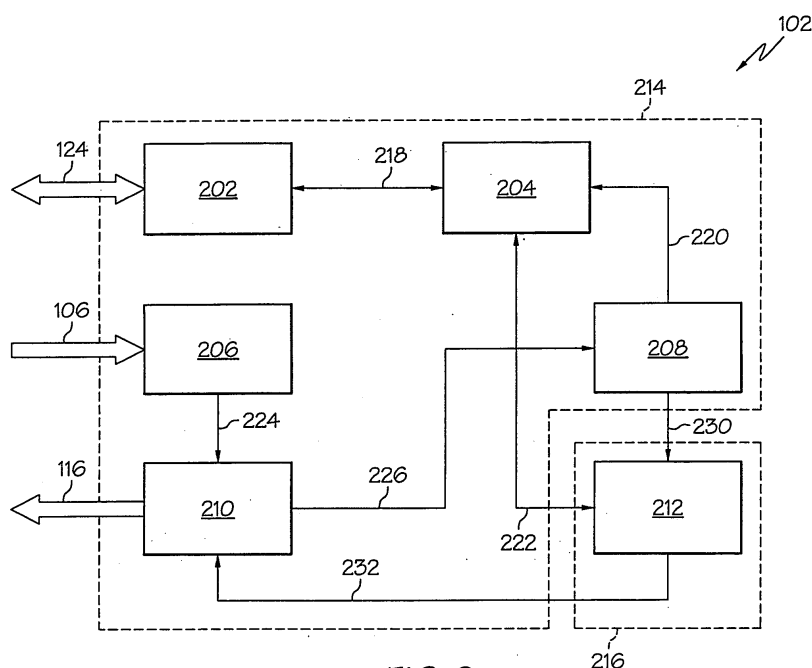
FIG. 2

Description

BACKGROUND OF THE INVENTION

[0001] The subject matter disclosed herein generally relates to digital motor controllers, and more particularly to compact field programmable gate array (FPGA) based digital motor controllers.

[0002] A brushless direct current (DC) motor can use switches to electrically control commutation. One or more sensors can be used to determine position or speed information for feedback control of the brushless DC motor. When sensors are used that provide timing information, commutation control may be non-linear with respect to rotational speed of the motor. Non-linear period information complicates control logic, which can result in demanding mathematical calculations and complex algorithms for accurate control. Such control logic typically requires a microprocessor and accompanying computer system control elements, such as nonvolatile memory, volatile memory, arbitration logic, operating system software, and application software in the motor control loop. The use of a microprocessor and computer system control elements may be unsuitable for certain environments that are geometrically constrained and/or subject to harsh environmental conditions, for instance, high radiation environments.

BRIEF DESCRIPTION OF THE INVENTION

[0003] According to one aspect of the invention, a compact field programmable gate array (FPGA)-based digital motor controller is provided. The compact FPGA-based digital motor controller includes a sensor interface configured to receive sensor data from one or more sensors and generate conditioned sensor data. The one or more sensors provide position information for a DC brushless motor. The compact FPGA-based digital motor controller also includes a commutation control configured to create switching commands to control commutation for the DC brushless motor. The commutation control generates commutation pulses from the conditioned sensor data of the sensor interface. The compact FPGA-based digital motor controller also includes a time inverter configured to receive the commutation pulses. The time inverter converts the commutation pulses into a rotational speed of the DC brushless motor to provide a linear feedback control parameter.

[0004] According to yet another aspect of the invention, a method for an FPGA-based digital motor controller is provided. The method includes receiving sensor data from one or more sensors indicating position information for a DC brushless motor. The method further includes generating conditioned sensor data at a sensor interface implemented in hardware circuitry of the compact FPGA-based digital motor controller. The method also includes generating commutation pulses from the conditioned sensor data at a commutation control implemented in

hardware circuitry of the compact FPGA-based digital motor controller. The method additionally includes converting the commutation pulses into a rotational speed of the DC brushless motor at a time inverter implemented in hardware circuitry of the compact FPGA-based digital motor controller to provide a linear feedback control parameter. The method further includes creating switching commands at the commutation control, to control commutation for the DC brushless motor.

[0005] A further aspect of the invention is design structure for a compact FPGA-based digital motor controller tangibly embodied in a machine-readable medium. The design structure includes a sensor interface configured to receive sensor data from one or more sensors and generate conditioned sensor data, where the one or more sensors provide position information for a DC brushless motor. The design structure further includes a commutation control configured to create switching commands to control commutation for the DC brushless motor, the commutation control generating commutation pulses from the conditioned sensor data of the sensor interface. The design structure additionally includes a time inverter configured to receive the commutation pulses from the commutation control and convert the commutation pulses into a rotational speed of the DC brushless motor to provide a linear feedback control parameter.

[0006] These and other advantages and features will become more apparent from the following description taken in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0008] FIG. 1 is a block diagram of an exemplary embodiment of a system with a compact FPGA-based digital motor controller;

[0009] FIG. 2 depicts a block diagram of a compact FPGA-based digital motor controller; and

[0010] FIG. 3 depicts a process for providing a compact FPGA-based digital motor controller.

[0011] The detailed description explains embodiments of the invention, together with advantages and features, by way of example with reference to the drawings.

DETAILED DESCRIPTION OF THE INVENTION

[0012] FIG. 1 illustrates a block diagram of an exemplary embodiment of a system 100 with a compact field programmable gate array (FPGA)-based digital motor controller 102. The compact FPGA-based digital motor controller 102 receives input data from one or more sensors 104 via sensor data link 106. The one or more sen-

sors 104 may be Hall effect sensors that detect magnetic field changes due to rotation of a direct current (DC) brushless motor 108. In an exemplary embodiment, the one or more sensors 104 produce timing pulses responsive to a rotational position of the DC brushless motor 108. Motor drive transistors 110 switch a drive voltage source 112 onto motor drive link 114, providing switched current to establish commutation for the DC brushless motor 108. Switch commands are driven from the compact FPGA-based digital motor controller 102 to the motor drive transistors 110 using switch command link 116. Mechanical rotation of the DC brushless motor 108 can drive a rotary actuator 118 coupled through mechanical linkage 120. The mechanical linkage 120 may include gearing and other components (not depicted).

[0013]   The compact FPGA-based digital motor controller 102 may receive commands from a system controller 122 through a communication link 124. The system controller 122 can monitor the rotary actuator 118 using system sensors 126. An actuator feedback link 128 provides a feedback path between the rotary actuator 118 and the system sensors 126. A system sensor data link 130 can be used to pass data from the system sensors 126 to the system controller 122. In the embodiment depicted in FIG. 1, the compact FPGA-based digital motor controller 102 performs closed-loop feedback control of the DC brushless motor 108, while the system controller 122 provides closed-loop feedback control of the rotary actuator 118.

[0014]   In an exemplary embodiment, the system controller 122 provides control and configuration commands to the compact FPGA-based digital motor controller 102 and may also read status data from the compact FPGA-based digital motor controller 102. The system controller 122 can communicate with multiple instances of the compact FPGA-based digital motor controller 102 to command multiple instances of the DC brushless motor 108 and the rotary actuator 118 as part of a larger control system.

[0015]   Although the compact FPGA-based digital motor controller 102 is depicted as a single block, it will be understood that the functionality implemented within the compact FPGA-based digital motor controller 102 can be distributed over multiple FPGAs. FPGAs are semiconductor devices that can be configured after manufacturing according to hardware description language (HDL) files. HDL files may be implemented in a variety of formats, such as very high-speed integrated circuit hardware description language (VHDL) and/or Verilog files. As used herein, the term "FPGA" can refer to any programmable logic device capable of performing closed-loop digital motor control absent software execution.

[0016]   FIG. 2 depicts further details of an embodiment of the compact FPGA-based digital motor controller 102. As illustrated in FIG. 2, the compact FPGA-based digital motor controller 102 includes hardware circuitry for a communication interface 202, data registers 204, sensor interface 206, time inverter 208, commutation control

210, and linear digital compensation filter 212. The communication interface 202, data registers 204, sensor interface 206, time inverter 208, commutation control 210, and linear digital compensation filter 212 can be implemented in a single compact FPGA device or distributed between multiple compact FPGA devices. In one embodiment, the communication interface 202, data registers 204, sensor interface 206, time inverter 208, and commutation control 210 are grouped in a first compact FPGA 214, while the linear digital compensation filter 212 is included in a second compact FPGA 216. This configuration may enable a common implementation of the first compact FPGA 214 and customized implementations of multiple instances of the second compact FPGA 216 to support multiple configurations of the DC brushless motor 108 and the rotary actuator 118 of FIG. 1 as part of a larger control system.

[0017]   Both the first compact FPGA 214 and the second compact FPGA 216 can be implemented using antifuse (one-time programmable) technology to decrease susceptibility to radiation, such as alpha particles, which can cause circuits to malfunction. Thus, implementing the compact FPGA-based digital motor controller 102 in antifuse technology may increase overall reliability of the system 100 of FIG. 1, particularly in high-radiation environments. The physical area of the first compact FPGA 214 and the second compact FPGA 216 may be about 1 inch-square (2.54 centimeters-square), where the first compact FPGA 214 and the second compact FPGA 216 contain about 100,000 gates each. It will be understood that the physical dimensions and number of gates for the first compact FPGA 214 and the second compact FPGA 216 can vary within the scope of the invention.

[0018]   The communication interface 202 is coupled to the communication link 124 to provide bidirectional communication with the system controller 122 of FIG. 1. The communication interface 202 may support a variety of communication protocols and standards known in the art, such as RS-485 to support point-to-point and multi-drop bus communication. Data path 218 provides a bidirectional communication link between the communication interface 202 and the data registers 204. The communication interface 202 can perform communication protocol conversion, enabling the system controller 122 of FIG. 1 to read and write values in the data registers 204. The data registers 204 may store a variety of configuration parameters, commands, and status information. For example, the data registers 204 can interface with the time inverter 208 and linear digital compensation filter 212 via data path 220 and data path 222 respectively.

[0019]   The sensor interface 206 receives sensor data from the sensor data link 106 and can provide conditioned sensor data to the commutation control 210 using data path 224. The sensor data received at the sensor interface 206 from the one or more sensors 104 of FIG. 1 may be formatted as digital position data. For example, each of the one or more sensors 104 can generate a pulse as a rotor of the DC brushless motor 108 of FIG. 1 rotates

in close physical proximity to a given sensor of the one or more sensors 104. The sensor interface 206 can use edge detection logic to trigger one or more timers to start, stop, and/or capture time values as transitional edges are detected. Timers may be included in the sensor interface 206 and/or in the commutation control 210.

[0020] The commutation control 210 can convert values received from the sensor interface 206 into commutation pulse data. The commutation pulse data may be formatted as time values indicating elapsed time between a common position and/or multiple positions relative to the DC brushless motor 108 of FIG. 1. The commutation pulse data is sent to the time inverter 208 via data path 226.

[0021] In an exemplary embodiment, the time inverter 208 performs a mathematical inversion of time values from the commutation pulse data and outputs a rotational speed in revolutions-per-minute (RPM). The time inverter 208 is implemented exclusively in hardware circuitry and performs the mathematical inversion of time values (1/time) without software assistance to provide a linear feedback control parameter for controlling the DC brushless motor 108 of FIG. 1. The time inverter 208 may include scalable parameters to control the accuracy of the calculations. In an exemplary embodiment, the accuracy of the time inverter 208 is scalable between 24 and 48 bits. The time inverter 208 may also support additional accuracy ranges. Converting non-linear commutation pulse data to RPM provides linearization to simplify closed loop control logic. Further or alternate scaling, such as unit conversion may be performed prior to passing resulting data values to the data registers 204 on data path 220 and to the linear digital compensation filter 212 on data path 230. Speed data passed to the data registers 204 can be read by the system controller 122 of FIG. 1 using the communication interface 202. Speed data passed to the linear digital compensation filter 212 supplies a linear feedback control parameter to determine an error value for controlling the DC brushless motor 108 of FIG. 1.

[0022] The linear digital compensation filter 212 provides compensation logic for stable control of the DC brushless motor 108 of FIG. 1. The linear digital compensation filter 212 may include one or more digital filter stages, such as an infinite impulse response (IIR) filter or a finite impulse response (FIR) filter. The linear digital compensation filter 212 may also include control loop logic for implementing any combination of proportional, integral, and/or differential control. A commanded speed value can be received from the data registers 204, in addition to one or more gain values and filter coefficients. The values from the time inverter 208 provide control loop feedback for linear digital control. This avoids complexity that may be associated with more advanced control loop designs, such as non-linear state space control. The linear digital compensation filter 212 drives an output on data path 232 that attempts to reduce an error value between a commanded value and the actual value de-

termined by the time inverter 208. In an exemplary embodiment, the output on data path 232 is a compensation command for the commutation control 210, which may be in a pulse-width-modulation (PWM) command.

[0023] The commutation control 210 converts compensation commands from the linear digital compensation filter 212 into switching commands to output on the switch command link 116. The commutation control 210 may issue commands as PWM cycles with an adjustable duty cycle and/or frequency. In an exemplary embodiment, the commutation control 210 implements predictive control to avoid noise induced errors. The predictive control can include filtering self-generated noise. The commutation control 210 may use conditioned sensor data generated by the sensor interface 206 to determine when an error condition likely exists. For example, the commutation control 210 can determine that the rate of change between position data is too fast, indicating that false pulses may be present. The commutation control 210 can maintain a switching sequence from a previous switching cycle or issue no switching commands until the error condition is removed.

[0024] It will be understood that data paths 220-232 may be combined into any combination of shared data path. Sharing data paths can reduce the amount of resources dedicated to routing data paths within the compact FPGA-based digital motor controller 102.

[0025] FIG. 3 depicts a process 300 for providing a compact FPGA-based digital motor controller, such as the compact FPGA-based digital motor controller 102 of FIGs. 1 and 2. At block 302, the sensor interface 206 receives sensor data from one or more sensors 104 indicating position information for DC brushless motor 108. At block 304, the sensor interface 206 generates conditioned sensor data. At block 306, commutation control 210 generates commutation pulses from the conditioned sensor data. At block 308, time inverter 208 converts the commutation pulses into a rotational speed of the DC brushless motor 108 to provide a linear feedback control parameter. At block 310, commutation control 210 creates switching commands to control commutation for the DC brushless motor 108. Data registers 204 can be used to store command and status information, with communication interface 202 providing communication between the data registers 204 and system controller 122 of FIG. 1. Linear digital compensation filter 212 may receive the rotational speed from the time inverter 208 and a speed command from the data registers 204, outputting a compensation command to the commutation control 210 responsive to the rotational speed and the speed command. As previously described, the commutation control 210 can include additional functionality, such as performing predictive control to filter self-generated noise.

[0026] As described above, embodiments of the invention may be embodied in the form of hardware or any processes and/or apparatuses for practicing the embodiments. The invention may also be embodied in the form of a design structure for the compact FPGA-based digital

motor controller 102 of FIGs. 1 and 2 tangibly embodied in a machine-readable medium, such as a floppy diskette, CD ROM, DVD, flash drive, solid-state device, hard drive, or any other computer readable storage medium. One or more HDL files and/or supporting library files stored on one or more machine-readable mediums can provide the functional structure to program one or more FPGA devices to implement the compact FPGA-based digital motor controller 102. The design structure can be encoded in one or more FPGA devices, such as the first compact FPGA 214 and the second compact FPGA 216, by physically modifying the internal resistance of connections in each FPGA device to establish conductive paths for electrical current to flow.

[0027]   Technical effects include a compact FPGA-based digital motor controller. Performing a time inversion of position information for a DC brushless motor in hardware rather than software can avoid use of a microprocessor, computer system components, and software, resulting in a geometrically compact solution for DC brushless motor control. FPGA-based time inversion circuitry enables the use of a digital linear closed loop compensation filter instead of more complex non-linear controls. Converting time data into RPM for closed loop control may further simplify the control logic. The compact FPGA-based digital motor controller can also avoid the use of analog circuits to reduce board area and increase reliability. Implementing the compact FPGA-based digital motor controller in antifuse technology may further enhance reliability in high radiation environments, such as high altitude or space applications.

[0028]   While the invention has been described in detail in connection with only a limited number of embodiments, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the scope of the invention. Additionally, while various embodiments of the invention have been described, it is to be understood that aspects of the invention may include only some of the described embodiments. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

Claims

1.   A compact field programmable gate array (FPGA)-based digital motor controller (102) comprising:

       a sensor interface (206) implemented in hardware circuitry configured to receive sensor data from one or more sensors (104) which provide position information for a direct current (DC) brushless motor (108) and to generate conditioned sensor data;

       a commutation control (210) implemented in hardware circuitry configured to create switching commands to control commutation for the DC brushless motor (108), the commutation control (210) generating commutation pulses from the conditioned sensor data of the sensor interface (206); and
       a time inverter (208) implemented in hardware circuitry configured to receive the commutation pulses from the commutation control (210) and convert the commutation pulses into a rotational speed of the DC brushless motor (108) to provide a linear feedback control parameter.

2.   The compact FPGA-based digital motor controller (102) of claim 1 further comprising:

       data registers (204) configured to store command and status information; and
       a communication interface (202) in communication with the data registers (204) to provide communication with a system controller (122).

3.   The compact FPGA-based digital motor controller (102) of claim 2 further comprising:

       a linear digital compensation filter (212) configured to receive the rotational speed from the time inverter (208) and a speed command from the data registers (204), the linear digital compensation filter (212) outputting a compensation command to the commutation control (210) responsive to the rotational speed and the speed command.

4.   The compact FPGA-based digital motor controller (102) of claim 3 wherein the time inverter (208) is implemented in a first compact FPGA (214) and the linear digital compensation filter (212) is implemented in a second compact FPGA (216).

5.   The compact FPGA-based digital motor controller (102) of claim 1, 2, 3 or 4 wherein accuracy of the time inverter (208) is scalable.

6.   The compact FPGA-based digital motor controller (102) of any preceding claim wherein the commutation control (210) performs predictive control to filter self-generated noise.

7.   The compact FPGA-based digital motor controller (102) of any preceding claim wherein the compact FPGA-based digital motor controller (102) is implemented in antifuse technology.

8.   A method (300) for providing a compact field programmable gate array (FPGA)-based digital motor controller (102) comprising:

receiving (302) sensor data from one or more sensors (104) indicating position information for a direct current (DC) brushless motor (108);
generating (304) conditioned sensor data at a sensor interface (206) implemented in hardware circuitry of the compact FPGA-based digital motor controller (102);
generating (306) commutation pulses from the conditioned sensor data at a commutation control (210) implemented in hardware circuitry of the compact FPGA-based digital motor controller (102);
converting (308) the commutation pulses into a rotational speed of the DC brushless motor (108) at a time inverter (208) implemented in hardware circuitry of the compact FPGA-based digital motor controller (102) to provide a linear feedback control parameter; and
creating (310) switching commands at the commutation control (210) to control commutation for the DC brushless motor (108).

9. The method of claim 8 further comprising:

storing command and status information in data registers (204) of the compact FPGA-based digital motor controller (102); and
providing communication between the data registers (204) and a system controller (122) via a communication interface (202) of the compact FPGA-based digital motor controller (102).

10. The method of claim 9 further comprising:

receiving the rotational speed from the time inverter (208) and a speed command from the data registers (204) at a linear digital compensation filter (212) of the compact FPGA-based digital motor controller (102); and
outputting a compensation command to the commutation control (210) responsive to the rotational speed and the speed command.

11. The method of claim 10 wherein the time inverter (208) is implemented in a first compact FPGA (214) and the linear digital compensation filter (212) is implemented in a second compact FPGA (216).

12. The method of claim 8, 9, 10 or 11 wherein accuracy of the time inverter (208) is scalable.

13. The method of any of claims 8 to 12 wherein the commutation control (210) performs predictive control to filter self-generated noise.

14. The method of any of claims 8 to 13 wherein the compact FPGA-based digital motor controller (102) is implemented in antifuse technology.

15. A design structure for a compact field programmable gate array (FPGA)-based digital motor controller (102) tangibly embodied in a machine-readable medium, the design structure providing the functional structure to program one or more FPGA devices to implement the compact field programmable gate array (FPGA)-based digital motor controller of any of claims 1 to 6.

FIG. 1

FIG. 2

300

RECEIVE SENSOR DATA FROM ONE OR MORE SENSORS INDICATING
POSITION INFORMATION FOR A DC BRUSHLESS MOTOR
— 302

GENERATE CONDITIONED SENSOR DATA AT A SENSOR INTERFACE
IMPLEMENTED IN HARDWARE CIRCUITRY OF A COMPACT
FPGA-BASED DIGITAL MOTOR CONTROLLER
— 304

GENERATE COMMUTATION PULSES FROM THE CONDITIONED SENSOR
DATA AT A COMMUTATION CONTROL IMPLEMENTED IN HARDWARE
CIRCUITRY OF THE COMPACT FPGA-BASED DIGITAL MOTOR CONTROLLER
— 306

CONVERT THE COMMUTATION PULSES INTO A ROTATIONAL SPEED OF
THE DC BRUSHLESS MOTOR AT A TIME INVERTER IMPLEMENTED IN
HARDWARE CIRCUITRY OF THE COMPACT FPGA-BASED DIGITAL MOTOR
CONTROLLER TO PROVIDE A LINEAR FEEDBACK CONTROL PARAMETER
— 308

CREATE SWITCHING COMMANDS AT THE COMMUTATION CONTROL TO
CONTROL COMMUTATION FOR THE DC BRUSHLESS MOTOR
— 310

FIG. 3

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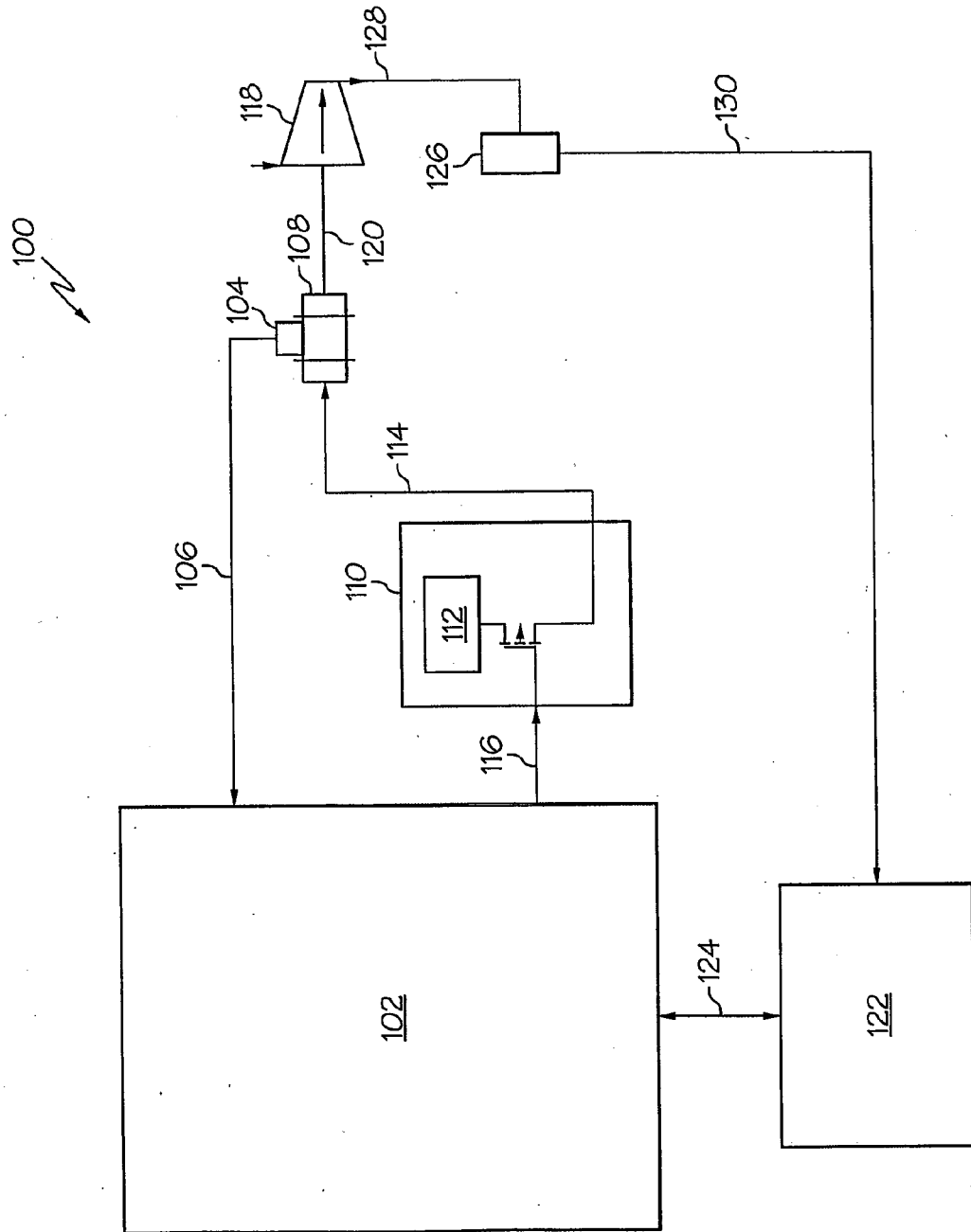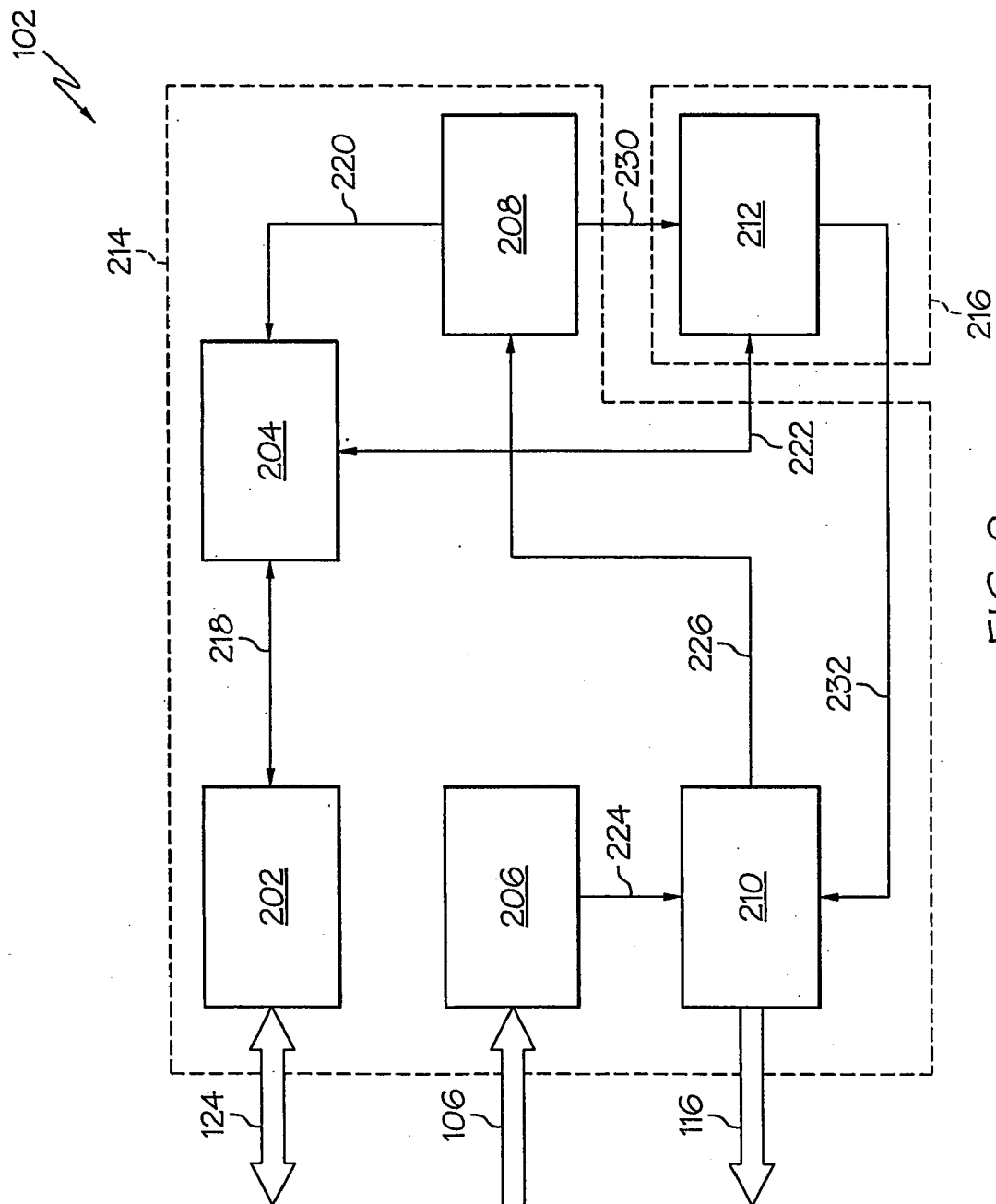Patentamt

European
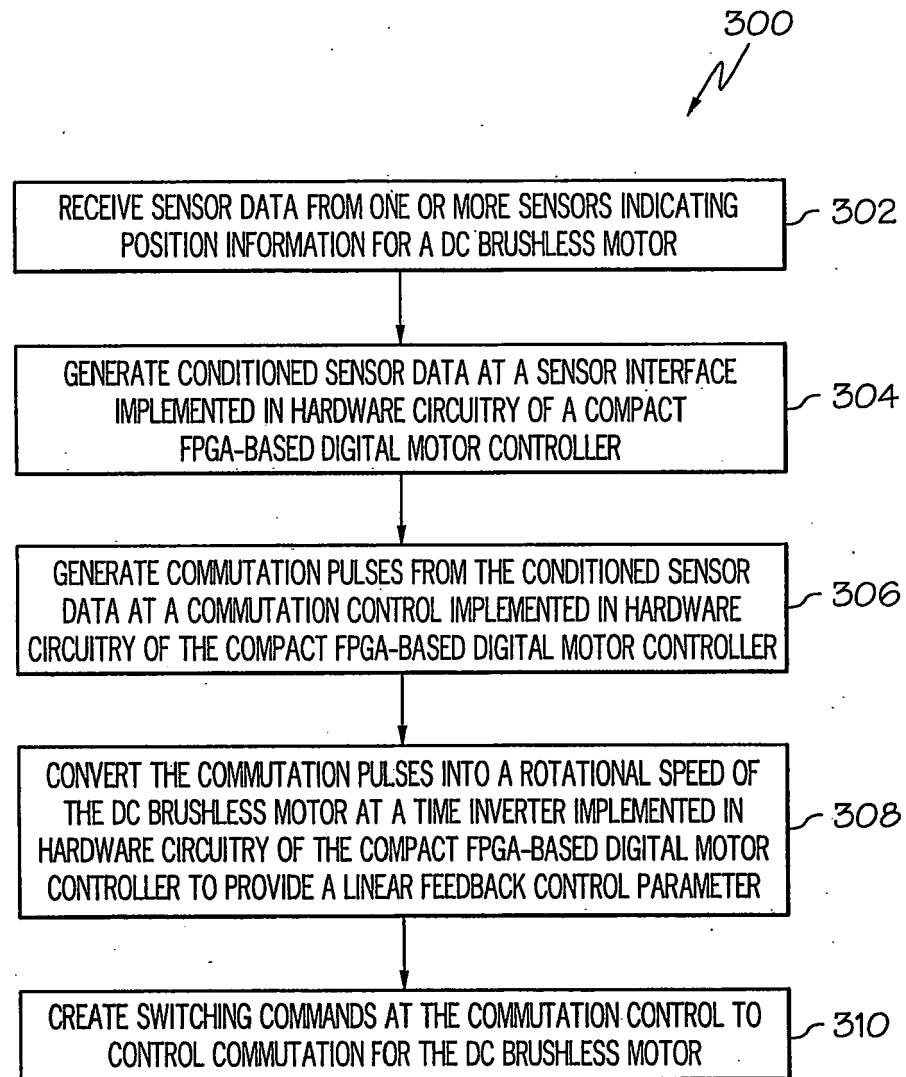Patent Office

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EUROPEAN SEARCH REPORT

Application Number

EP 10 25 1247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	shiva@ishnatek.com: "Implementing a Brushless DC Motor Controller on an IGLOO FPGA" Ishnatek Systems & Services Private limited 2008, XP002600282 Retrieved from the Internet: URL:http://www.eetasia.com/STATIC/PDF/2008 10/EEOL_2008OCT01_PL_AN_01.pdf?SOURCES=DOW NLOAD [retrieved on 2010-09-08] * the whole document * -& "Miniature Motor Control Daughter Card for Actel IGLOO Icicle Kit" ACTEL May 2008 (2008-05), XP002601681 Retrieved from the Internet: URL:http://www.actel.com/products/solution s/motorcontrol/minicard.aspx [retrieved on 2010-09-08] * the whole document * -----	1-15	INV. H02P6/00 H02P6/16
X	Craig Hackney: "FPGA Motor Control Reference Design" XILINX 16 September 2005 (2005-09-16), XP002600283 Retrieved from the Internet: URL:http://www.xilinx.com/support/document ation/application_notes/xapp808.pdf [retrieved on 2010-09-08] * page 1 - page 1 * -----	1-15	TECHNICAL FIELDS SEARCHED (IPC) H02P
A	US 6 351 048 B1 (SCHOB RETO [CH] ET AL) 26 February 2002 (2002-02-26) ----- -/--	1-15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	22 September 2010	Segaert, Pascal

EPO FORM 1503 03.82 (P04C01)

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EUROPEAN SEARCH REPORT

Application Number

EP 10 25 1247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	WO 2004/004109 A2 (XIDEM INC [US]) 8 January 2004 (2004-01-08) -----	1-15	
A	EP 0 812 057 A1 (SMITH CORP A O [US]) 10 December 1997 (1997-12-10) -----	1-15	

TECHNICAL FIELDS
SEARCHED   (IPC)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	22 September 2010	Segaert, Pascal

CATEGORY OF CITED DOCUMENTS

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**   EP 10 25 1247

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22-09-2010

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6351048	B1	26-02-2002	EP	1063753 A1	27-12-2000
			JP	4484320 B2	16-06-2010
			JP	2001016887 A	19-01-2001
WO 2004004109	A2	08-01-2004	AU	2003263769 A1	19-01-2004
EP 0812057	A1	10-12-1997	EP	0812056 A1	10-12-1997

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82