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(54) Preheat cycle control circuit for a fluorescent lamp

(57) A preheat cycle control circuit and method for a fluorescent lamp drive circuit is presented, the fluorescent lamp drive circuit having a low-side switching element and high-side switching element connected in series, a controller adapted to switch the switching elements on and off alternately at a frequency of operation, and a sweep capacitance adapted to control the frequency of operation of the controller. The preheat cycle control circuit comprises an integrator circuit adapted to regulate a current through the low-side switching element; and a switch operable to connect the integrator circuit to the controller in a first configuration and to connect the sweep capacitor to the controller in a second configuration.

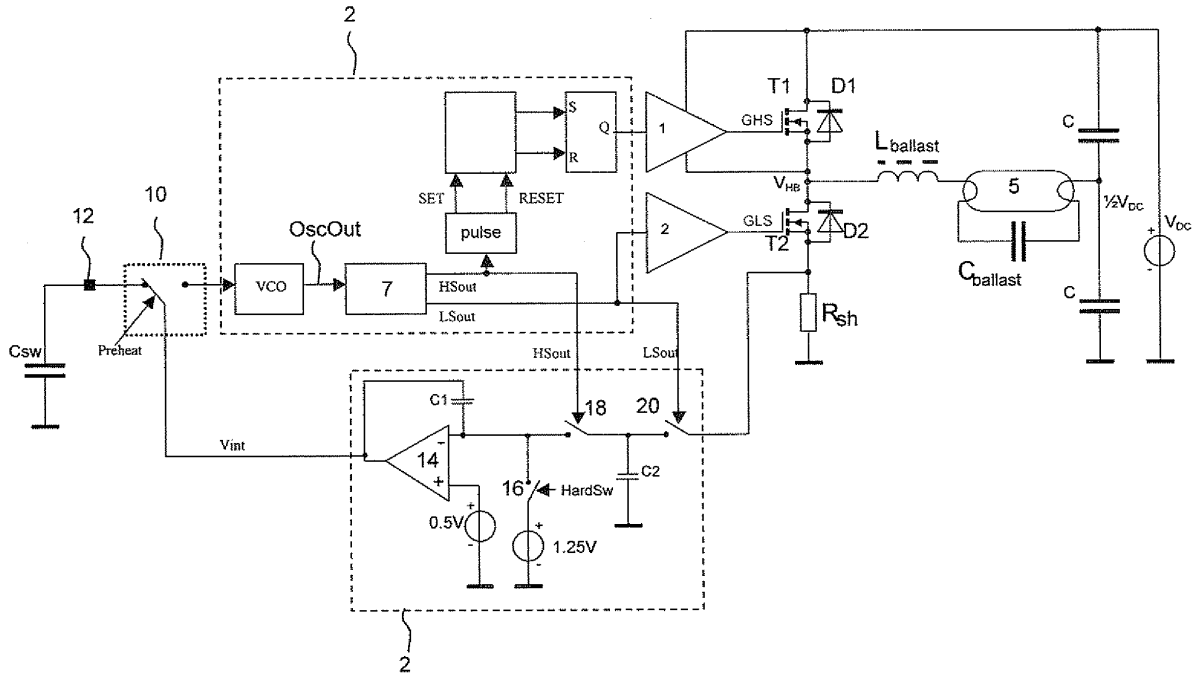


Fig. 1

EP 2 285 192 A1

Description

[0001] The present invention relates to fluorescent lamps, and more particularly to a preheat cycle control circuit for a fluorescent lamp drive circuit.

[0002] A fluorescent lamp or fluorescent tube is a gas-discharge lamp that uses electricity to excite mercury vapor. The excited mercury atoms produce short-wave ultraviolet light that then causes a phosphor to fluoresce, producing visible light.

[0003] Drive circuits are employed to start and operate fluorescent lamps. The choice of drive circuit is based on factors such as mains voltage, tube length, initial cost, long term cost, instant versus non-instant starting, temperature ranges and parts availability, etc.

[0004] A drive circuit may be used to control the voltage and current provided to the fluorescent lamp during startup and operation. Typically, the drive circuit includes a preheat cycle and an operating cycle (comprising an ignition period followed by a burn period). During the preheat cycle, voltage and current are supplied to the lamp to warm the electrodes. Once the electrodes are warmed, a voltage and current may be supplied to the lamp to excite the gas.

[0005] The duration of a preheat cycle prior to the operating cycle may be based on a predetermined period of time, based on a resistor with heating characteristics similar to the lamp, or a current or voltage supplied the lamp.

[0006] An optimal preheat duration maximizes lamp life. However, with all of these types of preheat schemes, the drive circuit uses some form of generic predetermined value of time, current, voltage or resistance to determine the duration of the preheat cycle. Accordingly, the specific type of fluorescent lamp used with the drive circuit must be known and previously tested to determine the predetermined value to be used for the preheat cycle. Furthermore, variations in materials and manufacturing of fluorescent lamps makes the optimal preheat duration of a lamp vary significantly. Thus, an optimal preheat duration for one lamp may be significantly reduce the life or reliability of another similar fluorescent lamp.

[0007] Improvements in Compact Fluorescent Lamps (CFLs) are typically driven by costs and size. The use of cheap packages and less external components is a therefore desirable.

[0008] Embodiments utilize a conventional existing sweep capacitor (which typically sets the frequency of operation of a fluorescent lamp drive circuit) to also control the duration of the preheat cycle. Thus, embodiments can employ existing packages, such as 8-pin DIP8 packages, whilst adding extra functionality like a pre-heat function.

[0009] By using the sweep capacitor to form a switched capacitor filter or integrator circuit during the preheat cycle, embodiments may regulate the internal preheat current through a low-side half-bridge MOSFET of a fluorescent lamp drive circuit in order to define the preheat cycle.

[0010] According to an aspect of the invention, there is provided a preheat control circuit for a fluorescent lamp drive circuit having a low-side switching element and high-side switching element connected in series, a controller adapted to switch the switching elements on and off alternately at a frequency of operation, and a sweep capacitance adapted to control the frequency of operation of the controller, the preheat cycle circuit comprising: an integrator circuit adapted to regulate a current through the low-side switching element; and a switch operable to connect the integrator circuit to the controller in a first configuration and to connect the sweep capacitor to the in a second configuration.

[0011] According to another aspect of the invention, there is provided a preheat cycle control method for use with a fluorescent lamp drive circuit having a low-side switching element and high-side switching element connected in series, a controller adapted to switch the switching elements on and off alternately at a frequency of operation, and a sweep capacitance adapted to control the frequency of operation of the controller, the method comprising the steps of: connecting an integrator circuit to the controller in a first configuration so as to regulate a current through the low-side switching element; and connecting the sweep capacitor to the controller in a second configuration.

[0012] For a better understanding of the invention, embodiments will now be described, purely by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a fluorescent lamp drive circuit according to an embodiment of the invention;
Figure 2 illustrates the output signals of the oscillator arrangement of Figure 1; and
Figure 3 is a plot of voltage across low-side resistor Rsh against elapsed time for the circuit of Figure 1; and
Figure 4 shows the variation of signals in the circuit of Figure 1 plotted against elapsed time T according to an embodiment of the invention;
Figure 5 shows the variation of signals in the circuit of Figure 1 plotted against elapsed time T according to another embodiment of the invention
Figure 6 is a circuit diagram of a preheat cycle control circuit according to an embodiment of the invention.

[0013] Proposed embodiments of the invention arrange a sweep capacitor to have two functions. In this way, during a preheat cycle, the sweep capacitor is used for timing the pre-heat cycle and, during the ignition and burn period (i.e. during the operating period) the frequency is set by the sweep capacitor.

[0014] To control the timing of the preheat cycle, embodiments are arranged to regulate the peak current through a low side half bridge MOSFET. This current determines the preheat current through the electrodes. To regulate the preheat current internally, a switched capacitor filter with a long integration time (in the range of milliseconds) can be employed, because the transient response of the half bridge is also long.

[0015] Turning now to Figure 1, an exemplary embodiment of the invention will now be explained.

[0016] Figure 1 shows a fluorescent lamp drive circuit according to an embodiment of the invention. The circuit comprises a conventional halfbridge arrangement coupled to an oscillator arrangement 2 and a preheat circuit 3 according to an embodiment of the invention.

[0017] Here, the halfbridge arrangement is provided with a pair of MOSFET switching elements T1,T2 connected in series, driver circuits 1,2 for controlling the MOSFET switching elements T1,T2 to switch on and off alternately, and fly wheel diodes D1, D2 connected in inverse parallel with the switching elements T1,T2.

[0018] It is known to limit the current through the low-side MOSFET (T2) by measuring the current through the low-side MOSFET T2 using a resistor Rsh (connected in series between the low-side MOSFET T2 and ground). Here, when the current through the resistor Rsh of the low-side MOSFET T2 becomes too high, a mechanism may be started to turn off the low-side MOSFET T2. Several ways to do this are known and will not be described in any detail here.

[0019] The oscillator arrangement 2 will now be described with reference to Figure 2. An input voltage is provided to a voltage controlled oscillator (VCO). The oscillator frequency is determined by this input voltage. The output (OscOut) of the VCO is provided to a non-overlap circuit 7 which generates the signals, HSout and LSout, that are used drive the gate of the high-side (T1) and the low-side (T2) MOSFETs, respectively.

[0020] As shown in Figure 2, the gate drive signals, HSout and LSout, are generated with non-overlap time, T_{NO}. This non-overlap time T_{NO} can be fixed or variable (in other words, adaptive) according to requirements.

[0021] Referring back to Figure 1, the circuit comprises a switch 10 adapted to connect the SW-pin 12 of the circuit package to the preheat circuit 3 during a pre-heat period, and to connect the SW-pin 12 to the VCO of the oscillator arrangement 2 during an operating period. In this way, during the preheat period, a sweep capacitor Csw (connected to the SW-pin 12) and the preheat circuit 3 form a switched capacitor integrator adapted to regulate a current through the low-side switching MOSFET T2 and to control the duration of the pre-heat period.

[0022] More specifically, during the pre-heat period, the VCO is connected to the output of a switched capacitor filter circuit 3 comprising an amplifier 14. The positive (+) input of the amplifier 14 is connected to a 0.5V voltage source, whereas the negative (-) input of the amplifier 14 is connected to the output of the amplifier 14 via a first filter capacitor C1. The negative (-) input of the amplifier 14 is also connected to a 1.25V voltage source via a first switch 16, and to the resistor Rsh via second 18 and third 20 switches arranged in series. Between the second 18 and third 20 switches there is connected to second filter capacitor C2 to ground.

[0023] The first 16, second 18 and third 20 switches are controlled by a hard switching HardSW, high-side gate drive signal HSout, and low-side gate drive signal LSout, respectively.

[0024] Thus, it will be understood that, during the preheat period, the peak current through the low side MOSFET T2 is regulated by regulating the voltage across Rsh to 0.5V (the plus input of the amplifier). When the low-side MOSFET T2 is turned off, the voltage across Rsh is set on capacitor C1. When the high-side gate drive signal HSout is high, charge from C1 is pushed in C2. In this way the control regulates the peak voltage across Rsh to 0.5V.

[0025] Normally, there is no hard-switching or capacitive mode during the preheat period. Thus, when capacitive mode or hard-switching is detected during the preheat period, it is concluded that there something wrong. In this case, the negative input of the amplifier 14 is forced to 1.25V by closing the first switch 16. This results in the input of VCO going low and the frequency of the VCO output going to its maximum.

[0026] Referring to Figure 3, the voltage across Rsh against elapsed time is plotted. It is seen that the voltage tries to regulate to 0.5V. When the elapsed time equals 3ms, a hard-switch cycle is forced by closing the first switch 16 and the frequency goes to the maximum.

[0027] During the operating period, the sweep capacitor Csw is connected to the VCO of the oscillator arrangement 2 and controls the frequency of operation of the VCO.

[0028] Referring now to Figure 4, the variation of signals in the circuit of Figure 1 is plotted against elapsed time T. During the preheat period (T1), the sweep (SW) pin 12 is connected to the preheat timing circuit 3. The sweep capacitor Csw is used for timing, since the voltage of the SW-pin increases linearly (see dashed line of Figure 3a) to a first reference voltage Vref1 and then decreases linearly. When the voltage of the SW-pin decreases to below the integrator reference voltage value (in this case, the regulation voltage of the integrator (see solid line of Figure 4a), the preheat period is ended. Thus, for the duration of the preheat period T1, the output of the integrator is connected to the input of the VCO (See solid line of Figure 4b).

[0029] After the preheat period (i.e. during the operating period which comprises the lamp ignition period T2 followed by the lamp burn period T3) the sweep capacitor Csw is connected to the VCO, so the sweep capacitor determines the frequency of the VO.

[0030] Figure 5 shows the variation of signals in the circuit of Figure 1 being operated according to an alternative

embodiment. During the preheat period (T1), when the sweep capacitor Csw voltage is below the integrator voltage Vint, the sweep (SW) pin 12 is connected to the input of the VCO. The operating frequency of the VCO is then determined by the sweep capacitor Csw. When the sweep capacitor voltage Csw exceeds the integrator voltage, the integrator voltage Vint determines the input of the VCO. The sweep capacitor Csw is used for timing, since the voltage of the SW-pin increases linearly (see dashed line of Figure 5a) to a first reference voltage Vref1 and then decreases linearly. When the voltage of the SW-pin decreases to below the integrator reference voltage value (in this case, the regulation voltage of the integrator (see solid line of Figure 5a), the preheat period is ended.

[0031] After the preheat period (i.e. during the operating period which comprises the lamp ignition period T2 followed by the lamp burn period T3) the sweep capacitor Csw is connected to the VCO, so the sweep capacitor determines the frequency of the VO. In other embodiments the preheat timing circuit 3 (or integrator circuit) can be implemented in a different way, because the capacitor ratio between C1 and C2 is preferably very large. Such an arrangement may require a small second filter capacitor C2, (which very sensitive to noise), and a large first filter capacitor C1.

[0032] Thus, Figure 6 shows a preheat timing circuit 50 according to an alternative embodiment of the invention wherein the capacitor values are of improved practicality.

[0033] The preheat timing circuit 50 of Figure 6 is an inverting integrator circuit comprising an amplifier 52. The positive (+) input of the amplifier 52 is connected to a 0.5V voltage source, whereas the negative (-) input of the amplifier 52 is connected to a 1.25V voltage source via a first switch 54, and to the sensed Voltage Vsense of a low side resistor (such as Rsh of Figure 1) via a second switch 56. Between the first 54 and second 56 switches there is connected a first capacitor C1 to ground.

[0034] The negative (-) input of the amplifier 52 is also connected to the output of the amplifier 52 via a second capacitor C2. The positive (+) input of the amplifier 52 is also connected to the output of the amplifier 52 via a third switch 58 connected in series with a third capacitor C3, and also connected to the second switch 56 via a fourth switch 60 in series. Finally, the negative (-) input of the amplifier 52 is connected to the third switch 58 via a fifth switch 62.

[0035] The first 54 switch is controlled by a hard switching signal HardSW, the second 56 and third 5 switches are controlled by a low-side gate drive signal LSout, and the fourth 60 and fifth 62 switches are controlled by a high-side gate drive signal HSout.

[0036] Here, the first C1, second C2 and third C3 capacitors have values 2pF, 10pF and 1pF, respectively.

[0037] The voltage step that can be made in every cycle may be represented by equation (1):

$$\Delta V_{out} = -(V_{in} - V_{ref}) \frac{C_1 \cdot C_3}{C_2 \cdot (C_3 + C_2)} \qquad (1)$$

[0038] Thus, it will be appreciated that the voltage step of the circuit of Figure 5 is smaller than the integrator circuit 3 of Figure 1 which may be represented by equation (2):

$$\Delta V_{out} = -(V_{in} - V_{ref}) \frac{C_2}{C_1} \qquad (2)$$

[0039] From the above description it will be understood that embodiments use a packaging pin, which is normally used to control oscillator frequency, to provide it will an additional function during the preheat cycle. During pre-heat cycle, the pin is used for timing the pre-heat cycle.

[0040] During the pre-heat cycle, embodiments control the peak current through the low-side mosfet of the conventional halfbridge arrangement. For this, an integrated switched capacitor integrator may be employed to define the input of the VCO. Further, the positive (+) input of an amplifier employed for the integrator may be set to a required voltage of the peak voltage of the low-side resistor Rsh.

[0041] Also, when a hardswitching or capacitive mode it detected, the preheat circuit may be forced to go a maximum frequency by forcing the minus input of the switched capacitor amplifier.

[0042] While specific embodiments have been described herein for purposes of illustration, various modifications will be apparent to a person skilled in the art and may be made without departing from the scope of the invention.

Claims

1. A preheat cycle control circuit for a fluorescent lamp drive circuit having a low-side switching element and high-side switching element connected in series, a controller adapted to switch the switching elements on and off alternately at a frequency of operation, and a sweep capacitance adapted to control the frequency of operation of the controller, the preheat circuit comprising:

   an integrator circuit adapted to regulate a current through the low-side switching element; and
   a switch operable to connect the integrator circuit to the controller in a first configuration and to connect the sweep capacitor to the controller in a second configuration.

2. The preheat cycle control circuit of claim 1, wherein the switch is adapted to connect the integrator circuit to the controller in a first configuration during a preheat period of the fluorescent lamp drive circuit.

3. The preheat cycle control circuit of claim 1 or 2, wherein the integrator circuit comprises an amplifier and wherein a first input of the amplifier is connected to a first reference voltage source and a second input of the amplifier is connected to the low-side switching element.

4. The preheat cycle control circuit of claim 3, wherein the second input of the amplifier is connected to the low-side switching element via at least one switch controlled by a drive signal for one of the switching elements.

5. The preheat cycle control circuit of claim 3 or 4, wherein the second input of the amplifier is connected to a second reference voltage source via a switch, and wherein the voltage value of the second reference voltage source is greater than the voltage value of the first reference voltage source.

6. The preheat cycle control circuit of any preceding claim, wherein at least one of the low-side switching element and high-side switching element comprises a FET.

7. A power supply circuit for a fluorescent lamp comprising a preheat cycle control circuit according to any preceding claim.

8. A preheat cycle control method for use with a fluorescent lamp drive circuit having a low-side switching element and high-side switching element connected in series, a controller adapted to switch the switching elements on and off alternately at a frequency of operation, and a sweep capacitance adapted to control the frequency of operation of the controller,
   the method comprising the steps of:

   connecting an integrator circuit to the controller in a first configuration so as to regulate a current through the low-side switching element; and
   connecting the sweep capacitor to the controller in a second configuration.

9. The method of claim 8, wherein the step of connecting the integrator circuit to the controller in a first configuration is undertaken during a preheat period of the fluorescent lamp drive circuit.

10. The method of claim 8 or 9, wherein the integrator circuit comprises an amplifier and wherein a first input of the amplifier is connected to a first reference voltage source and a second input of the amplifier is connected to the low-side switching element.

11. The method of claim 10, wherein the second input of the amplifier is connected to the low-side switching element via at least one switch controlled by a drive signal for one of the switching elements.

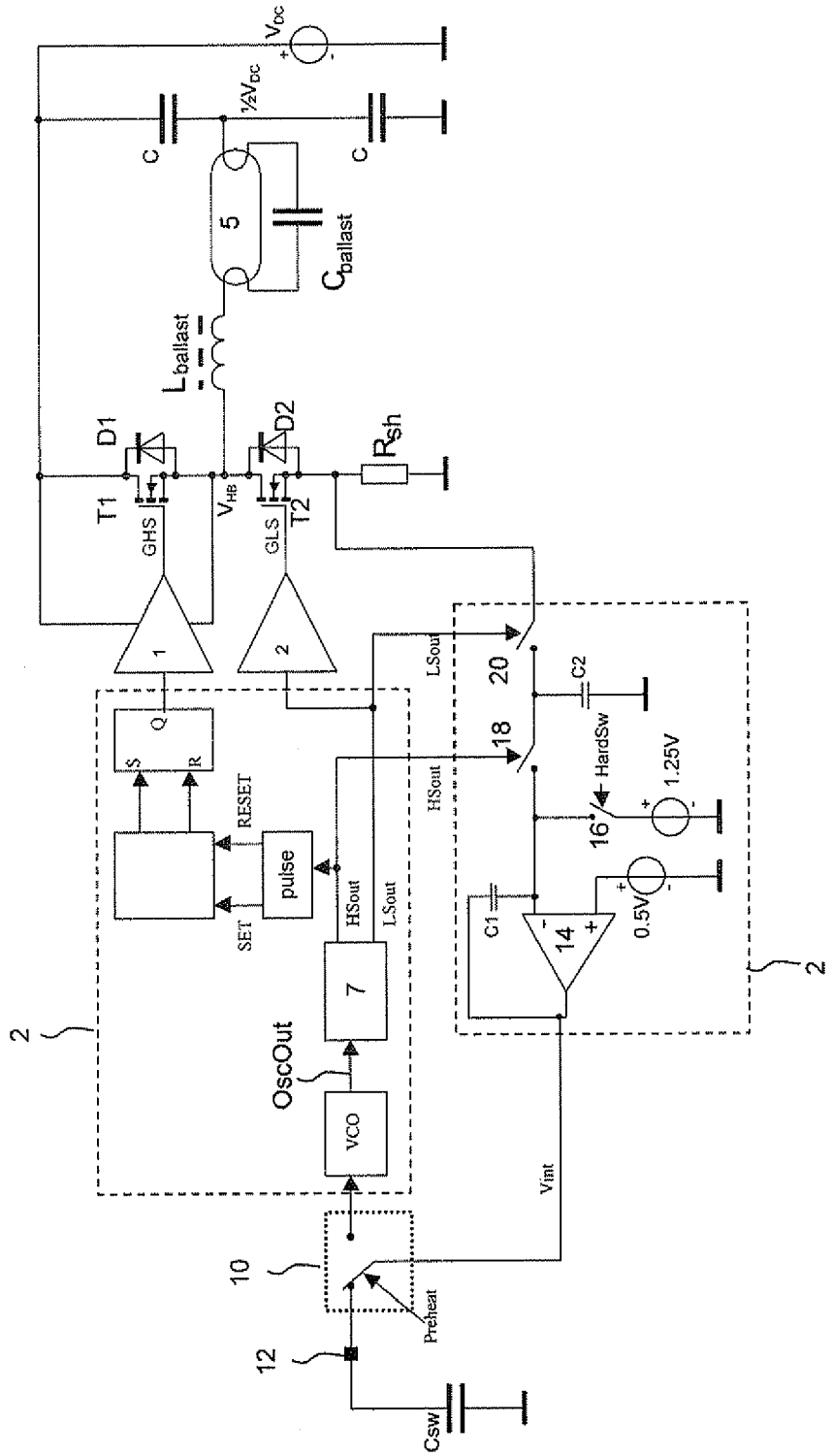
12. The method of any of claims 8 to 11, further comprising the steps of:

    detecting a hardswitching or capacitive mode during the preheat cycle period detected; and
    if a hards witching or capacitive mode is detected during the preheat cycle period, arranging the controller to go to a maximum frequency of operation.

13. A computer program comprising computer program code means adapted to perform all of the steps of any of claims

8 to 12 when said program is run on a computer.

14. A computer program as claimed in claim 13 embodied on a computer readable medium.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C
C
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$L_{ballast}$
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D2
R_{sh}
T1
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GLS
V_{HB}
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Q
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SET
pulse
HSout
LSout
7
OscOut
VCO
Vint
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C1
14
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Fig. 1

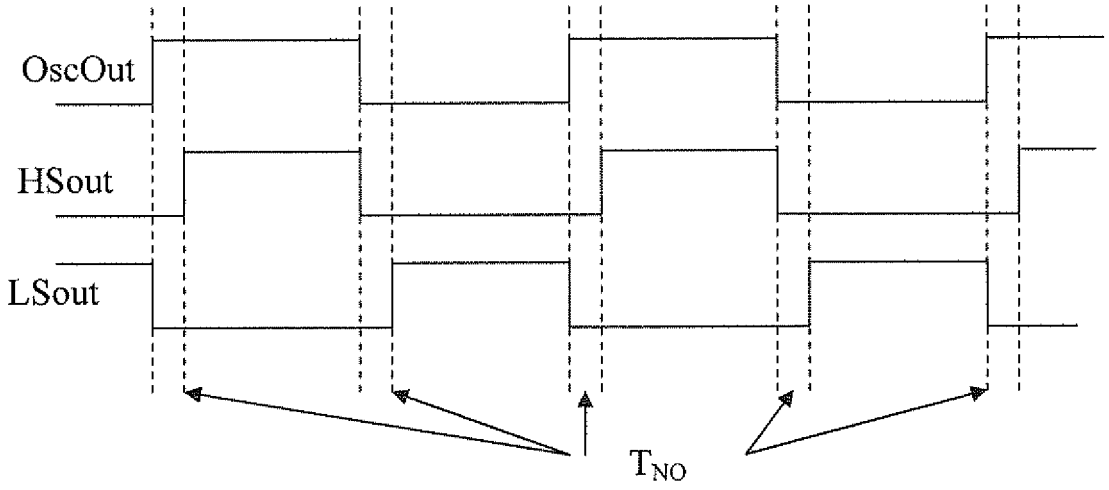


Fig. 2

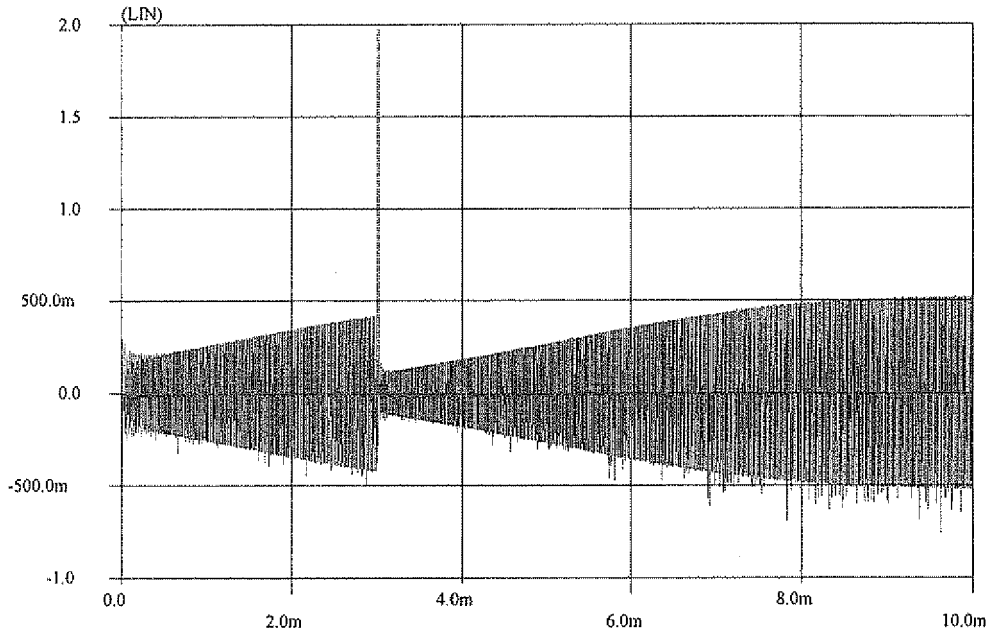
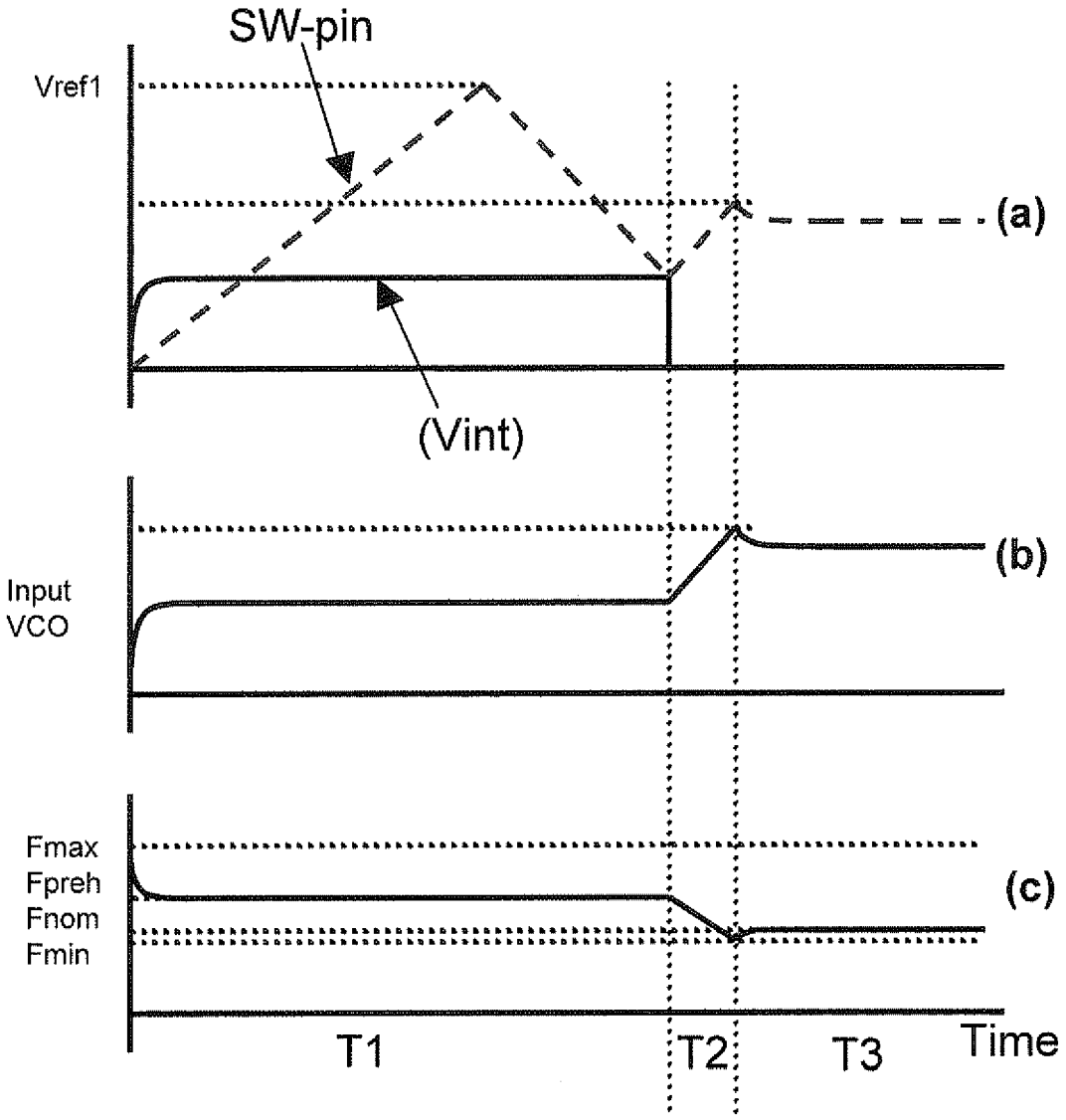


Fig. 3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VCO
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Fpreh
Fnom
Fmin
(c)
T1
T2
T3
Time

Fig. 4

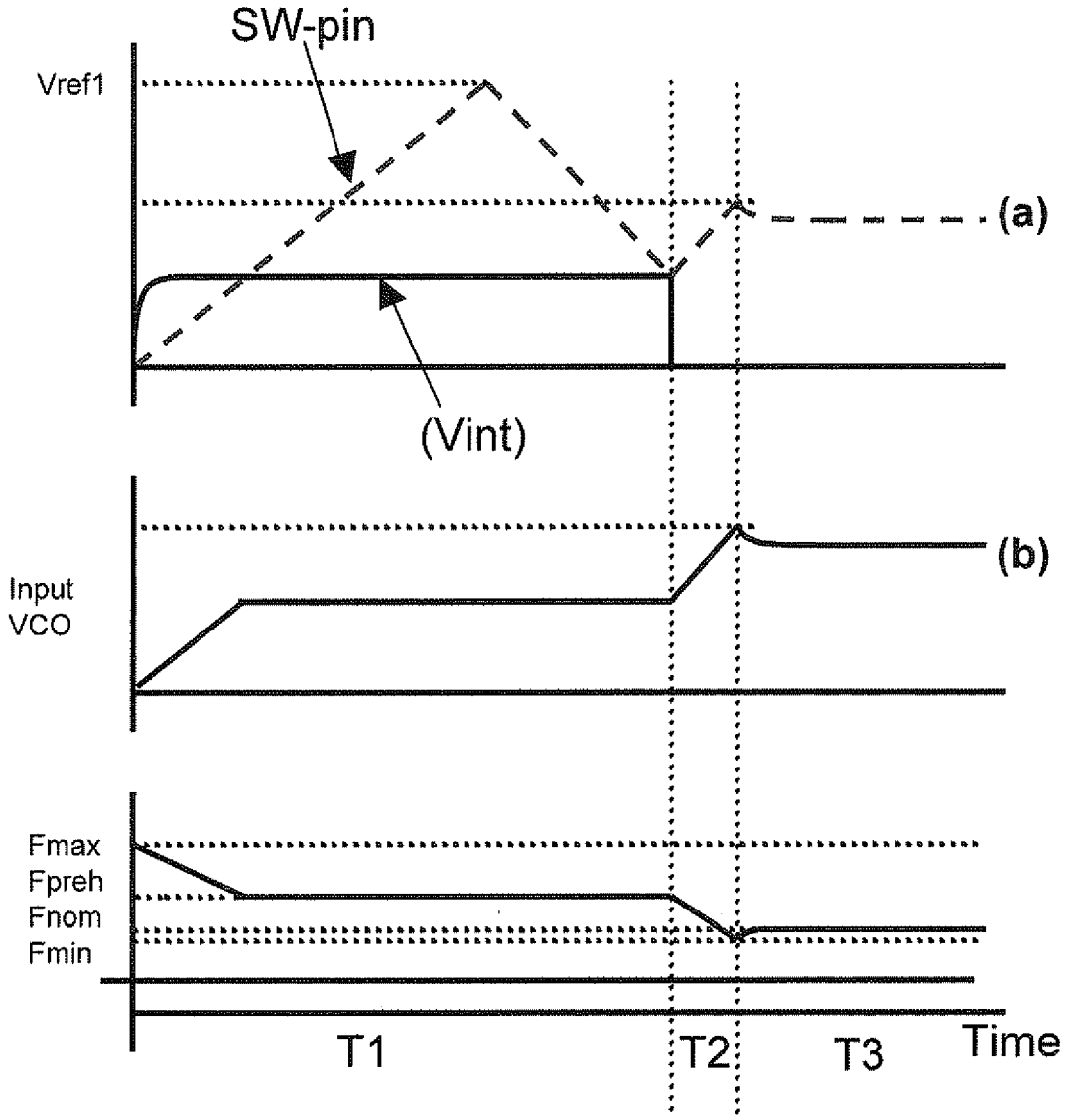
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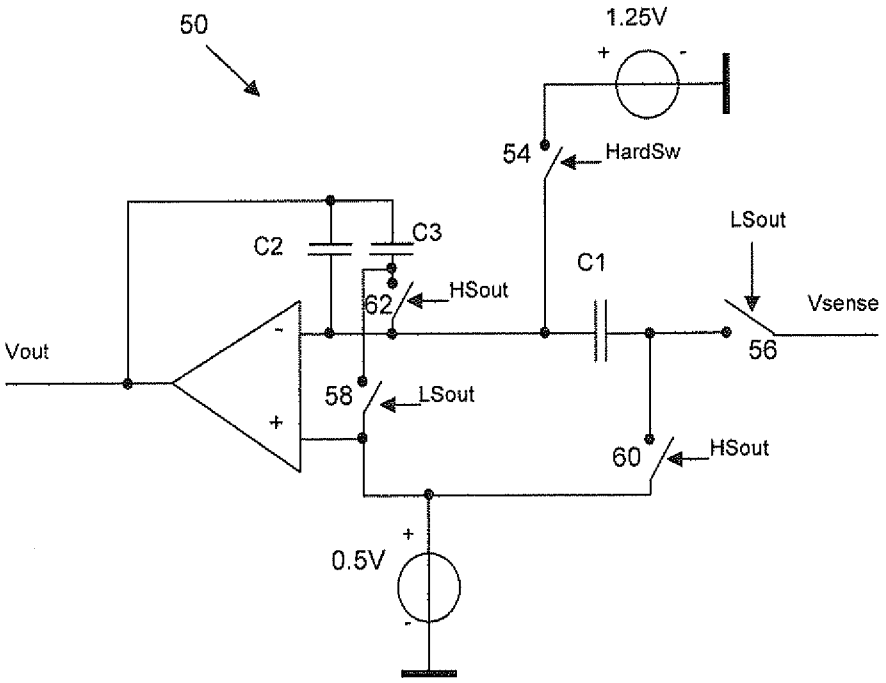
Fig. 5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+
-
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HardSw
C2
C3
C1
LSout
62
HSout
Vsense
Vout
56
58
LSout
60
HSout
+
0.5V
-

Fig. 6

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EUROPEAN SEARCH REPORT

Application Number
EP 09 16 5323

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	26 February 2010	Müller, Uta

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EUROPEAN SEARCH REPORT

Application Number
EP 09 16 5323

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Munich	26 February 2010	Müller, Uta

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