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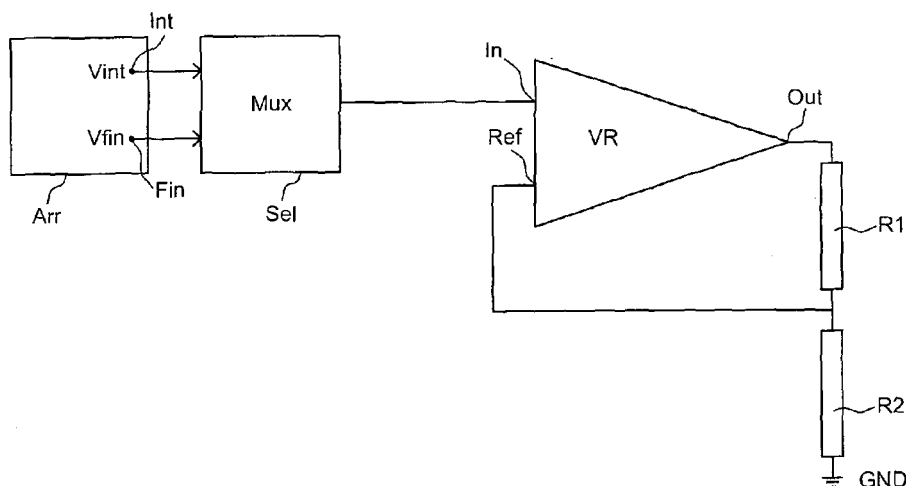
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(54) **Method for voltage regulation and voltage regulator arrangement**

(57) A method for voltage regulation comprises steps of providing a sequence of input voltages of at least one intermediate input voltage (V_{int}) and a target input voltage (V_{fin}), and selecting the at least one intermediate input voltage (V_{int}) from the sequence of input voltages. Next, regulating an output voltage (V_{out}) depending on the at least one intermediate input voltage (V_{int}) such

that the output voltage (V_{out}) reaches a steady-state condition. Furthermore, the method for voltage regulation comprises steps of selecting the target input voltage (V_{fin}) in the sequence of input voltages, and regulating the output voltage (V_{out}) depending on the target input voltage (V_{fin}) such that the output voltage (V_{out}) reaches the steady-state condition.

FIG 2A



Description

[0001] The present invention relates to a method for voltage regulation and a voltage regulator arrangement.

[0002] Nearly all electronic circuits, ranging from simple transistors to complex circuits like microprocessors need one or more reliable sources of stable DC voltage. Voltage regulators achieve that goal and are as diverse as their fields of application. Often voltage regulators like LDOs (low-dropout regulators) face the requirement to not only provide a fast start-up but, at the same time, prevent exceeding voltage overshoot. In turn, combination of fast start-up and low overshoot is detrimental to many applications. Achieving such performance is usually far from being straightforward and, in most cases, goes along with accepting other restrictions like in load and line regulation, high frequency PSSR (power supply rejection ratio) or load transient response.

[0003] The art knows several approaches to improve start-up behaviour of voltage regulators. Some exemplary prior art implementations are depicted in Figures 1A to 1C.

[0004] Figure 1A shows an exemplary embodiment of a voltage regulator arrangement based on a LDO according to prior art. The voltage regulator VR comprises an input terminal In and an output terminal Out. The output terminal Out is coupled to a series connection of a first resistor R1 and a second resistor R2. Furthermore, the output terminal Out feeds back via the first resistor R1 to a reference input terminal Ref of the voltage regulator VR. The second resistor R2 is connected to common ground GND.

[0005] Figure 1B shows an exemplary start-up phase for the voltage regulator VR according to Figure 1A. The graph depicted in Figure 1B shows input voltage and regulated output voltages applied to or provided by the voltage regulator arrangement as a function of time.

[0006] Without any further arrangements to account for possible overshoot, applying an input voltage V_{in} to the input voltage terminal In leads to regulation of an output voltage V_{out} . As apparent from Figure 1B this may cause significant overshoot in the output voltage V_{out} which can easily exceed the value of the applied input voltage V_{in} .

[0007] Generally, input voltage V_{in} and regulated output voltage V_{out} are not equal but scaled with respect to each other by a certain factor, e.g. determined by a ratio of resistances R1, R2 given as $(1 + R1/R2)$.

[0008] In order to prevent significant overshoot during the start-up phase the gain bandwidth of the voltage regulator VR may be reduced according to prior art. The input voltage V_{in} , however, is applied in the same way as before. The black line in Figure 1B represents the reduced output voltage rV_{out} output by a voltage regulator VR with reduced bandwidth. It is apparent from Figure 1B that no significant overshoot in the reduced output voltage rV_{out} occurs. Reducing bandwidth may be achieved by filtering the bias current of the voltage regulator VR, e.g. of a low dropout regulator LDO, by means of τ filters.

[0009] Figure 1C shows the start-up phase of the voltage regulator arrangement of Figure 1A according to prior art. Instead of changing the gain bandwidth of the voltage regulator VR an alternative solution is possible. By ramping up or smoothing the input voltage V_{in} the regulated output voltage V_{out} stays close to the input voltage V_{in} at all times. This way, overshoot is prevented from exceeding the final desired value.

[0010] Moreover, both solutions presented in Figures 1B and 1C have the drawback that additional components have to be implemented. Frequently, an integrated circuit comprises more than one regulated output terminal Out or channel (hereinafter denoted a multi-channel voltage regulator arrangement). Prior art solutions as described above may lead to serious trade-offs between large area requirement and corresponding high noise levels. This is due to the fact that in multi-channel arrangements like components (e.g. filters or intermediate buffers) have to be implemented for each individual channel. In case of very high load capacities and load currents such solutions are not very effective as settling takes place at maximum bandwidth if a long time elapses from power down release.

[0011] It is an object of the present invention to provide a method for voltage regulation and a voltage regulator arrangement achieving an easy and flexible way of implementation combining fast start-up and reduced voltage overshoot.

[0012] The object is solved by a method for voltage regulation according to claim 1, as well as a voltage regulator arrangement according to claim 8. Preferred embodiments are presented in dependent claims.

[0013] According to an aspect of the invention, a method for voltage regulation comprises a step of providing a sequence of input voltages of at least one intermediate input voltage and a target input voltage, and selecting the at least one intermediate input voltage from the sequence of input voltages. Furthermore, regulating an output voltage depending on the at least one intermediate input voltage such that the output voltage reaches a steady-state condition. Moreover, the method comprises a step of selecting the target input voltage in the sequence of input voltages. Next, regulating the output voltage depending on the target input voltage such that the output voltage reaches the steady-state condition is performed.

[0014] In the stepwise approach employed by the method for voltage regulation, overshoot in output voltage is almost proportional to the applied step-size. Hereinafter, the step-size denotes a voltage difference between two consecutively applied input voltages, e.g. the voltage difference between the at least one intermediate input voltage or the target input voltage. Any voltage coupled to an input terminal of the voltage regulator shall be considered an input voltage.

[0015] Hereinafter all voltages like input and output voltages are generally considered as referenced with respect to a reference supply rail. Preferably, such reference may be given as the systems ground potential.

[0016] Advantageously, input voltages and step-sizes can be tailored depending on the application and such that overshoot stays lower than the target input voltage or exceeds this voltage by just a little but tolerable amount. This way, only a final step-size determines the overshoot which can be rather low. Consequently, the method for voltage regulation mitigates the trade-offs between overshooting amplitude and fast start-up times.

[0017] Furthermore, the method for voltage regulation is flexible and can be applied to any kind of voltage regulator, preferably low dropout regulators (LDOs). In particular, the method for voltage regulation is advantageously implemented in dual or multiple channel arrangements. Area requirement and noise level are advantageously reduced due to few components needed for implementing the method e.g. with appropriate components on an integrated circuit. Additionally, performance of the voltage regulator does not depend on load conditions and bandwidth is not modified as no filters are necessary to create increase the voltage regulator's bias current.

[0018] Preferably, the steps of voltage regulation are implemented during a start-up phase. In the following the start-up phase shall be defined as that particular period of time, starting from switching-on the voltage regulator, necessary for the regulated output voltage to reach a value characterized by the desired target input voltage. In turn, the steady-state condition may be used to indicate the end of the start-up phase.

[0019] According to another aspect of the invention the method for voltage regulation comprises a step of selecting a further intermediate input voltage from the sequence of input voltages and is provided between the at least one intermediate input voltage and the target input voltage. Furthermore, it comprises a step of regulating the output voltage depending on the further intermediate input voltage such that the output voltage reaches the steady-state condition.

[0020] Preferably, selecting input voltages follows a step-wise approach, i.e. the at least one input voltage is selected first. In a next step the further intermediate input voltage is selected and so on. Finally, in a last step the target input voltage is selected. Preferably, corresponding step-sizes are chosen so as to increase input voltages up to the target input voltage. Note that in conjunction with each step and selection of input voltages just a single i.e. selected input voltage is coupled to the input terminal.

[0021] Advantageously, choosing more than one intermediate input voltage allows for a more flexible approach to reach the final target input voltage. The number and step-size of each individual intermediate input voltage may be chosen appropriate to a given application. This way, overshoot is further reduced for all intermediate input voltages.

[0022] According to another aspect of the invention, the method for voltage regulation comprises successive selection of a number of N further intermediate input voltages in the sequence of input voltages. Furthermore, it comprises corresponding successive regulation of the output voltage depending on the respective of the N further intermediate input voltages such that the output voltage increases in a step-like fashion until the target input voltage in the sequence of input voltages is selected. Next, the method for voltage regulation comprises a step of regulating the output voltage depending on the target input voltage.

[0023] Advantageously, using a number of N further intermediate input voltages to increase the output voltage in a step-like fashion, the output voltage can be regulated as, approximately, a smooth function without any substantial edges. This way, overshoot is reduced at all times during start-up. Essentially this approach mimics filtering or smoothing of input voltage edges but, however, without using any additional arrangements, e.g. filters for each individual channel as for multi-channel arrangements. Therefore, area requirements and noise level are advantageously reduced.

[0024] According to another aspect of the invention, the method for voltage regulation comprises a steady-state condition which is reached if the input voltage, e.g. intermediate input voltage, further intermediate input voltage or target input voltage equals the regulated output voltage multiplied by a scaling factor. The scaling factor may be defined by system parameters such as resistances.

[0025] Reaching the steady-state condition constitutes a detectable condition. Application of each input voltage, i.e. intermediate input voltage, further intermediate input voltage or target input voltage, leads to respective regulation of the output voltage. As soon as the steady-state condition is reached selection of another input voltage in the start-up phase can follow.

[0026] Advantageously, detecting reaching the steady-state condition using appropriate measuring means can help optimizing start-up times. In practice the steady-state condition may account for experimental tolerances, e.g. noise and other distortions. The steady-state condition may be reached already if the output voltage is regulated within a certain tolerance interval, e.g. $\pm 10\%$.

[0027] According to another aspect of the invention, reaching the steady-state condition is indicated by a steady-state signal.

[0028] Advantageously, by using a steady-state signal to indicate reaching the steady-state condition, start-up phase of a voltage regulator can be further shortened to provide fast start-up times. Preferably, a power ok signal is used for that purpose which, conveniently, is already implemented in many conventional LDO circuits.

[0029] According to another alternative aspect of the invention, the method for voltage regulation comprises a step in which reaching the steady-state condition is indicated by a time period.

[0030] Reaching the steady-state condition takes a certain amount of time. Depending on the application the time to reach steady-state may be within a characteristic time period. Such time period can be employed to indicate steady-state by simple components such as timers. The timer may define a certain amount of time between selection of an input voltage, e.g. at least one intermediate input voltage, further intermediate input voltage or target input voltage, which then is coupled to the input terminal.

[0031] Advantageously, timers are inexpensive and simple components to be integrated into applications where an appropriate time period between selection of input voltages is known or defined by a desired value. Timers may be used as an alternative to appropriate means to indicate the steady-state signal as e.g. the power ok signal.

[0032] According to another aspect of the invention, the method for voltage regulation comprises a step in which the further intermediate input voltage is selected depending on the steady-state signal indicating the steady-state condition.

[0033] According to an aspect of the invention, a voltage regulator arrangement comprises a voltage regulator having an input terminal and an output terminal. Furthermore, the voltage regulator arrangement comprises an arrangement for generating at least one intermediate input voltage and a target input voltage. Next, the voltage regulator arrangement comprises a start-up selection circuit for selecting the at least one intermediate input voltage or the target input voltage.

[0034] The start-up selection circuit selects the at least one intermediate input voltage or the target input voltage and couples the at least one intermediate input voltage or the target input voltage to the input terminal during a start-up phase. Preferably, the at least one intermediate input voltage is smaller than the target input voltage. The at least one intermediate input voltage may preferably be consecutively applied to the voltage regulator in a step-like fashion.

[0035] Advantageously, the voltage regulator arrangement can be implemented with any kind of voltage regulator, preferably low dropout regulators (LDO). In particular, this is an advantage if implemented in dual or multiple channel voltage regulator arrangements as components are shared for each channel. This way, area consumption and noise are advantageously reduced. Furthermore, performance does not depend on load conditions and bandwidth of the voltage regulator, e.g. a LDO, is not modified.

[0036] Another advantage lies in the stepwise approach, i.e. using the start-up selection circuit to consecutively couple the at least one intermediate input voltage or target input voltage to the input terminal. This way, overshoot is almost proportional to the step-size and allows for keeping overshoot comparably low during the entire start-up phase. As a consequence, a step-size associated with selection of the target input voltage leads to an overshoot which can be quite small compared to the target input voltage.

[0037] According to another aspect of the invention, the start-up selection circuit comprises a further intermediate input voltage which is provided between the at least one intermediate input voltage and the target input voltage.

[0038] The start-up selection circuit selects the further intermediate input voltage and couples the further intermediate input voltage to the input terminal. In particular, the start-up selection circuit only selects one input voltage, i.e. either the at least one intermediate input voltage, further intermediate input voltage or target input voltage such that only a single input voltage is coupled to the input terminal at a time.

[0039] Advantageously, by using more than one intermediate input voltage overshoot during the start-up phase can be further reduced by using appropriate step-sizes.

[0040] According to another aspect of the invention, the start-up selection circuit successively selects a number of N increasing further intermediate input voltages. The number of N increasing further intermediate input voltages are provided between the at least one intermediate input voltage and the target input voltage.

[0041] The start-up selection circuit selects a number of N increasing further intermediate input voltages such that it, in a step-like fashion, successively couples the number of N increasing further intermediate input voltages to the input terminal.

[0042] Advantageously, by using a number of N increasing further intermediate input voltages, the regulated output voltage approximately follows a smooth function without any significant edges. In particular, using the start-up selection circuit the voltage regulator arrangement removes the need of an individual input circuit like a filter for each channel.

[0043] According to another aspect of the invention the start-up selection circuit selects the at least one intermediate input voltage, further intermediate input voltage or the target input voltage depending on a steady-state signal indicating a steady-state condition.

[0044] The steady-state condition is reached if the intermediate input voltage, further intermediate input voltage or target input voltage equals a regulated output voltage at the output terminal.

[0045] Advantageously, indicating a steady-state condition allows for improved control of the start-up phase of the voltage regulator arrangement. Depending on the steady-state signal start-up phase can be reduced in time. This is especially important for applications demanding fast start-up times.

[0046] In practice the steady-state condition may account for experimental tolerances, e.g. noise and other distortions. The steady-state condition may be reached already if the output voltage is regulated within a certain tolerance interval, e.g. $\pm 10\%$.

[0047] According to another aspect of the invention, the voltage regulator arrangement comprises a start-up selection circuit selecting the at least one intermediate input voltage, further intermediate input voltage or target input voltage

depending on the steady-state signal.

[0048] Advantageously, using the steady-state signal start-up time of voltage regulation can be tailored appropriate to a given application. Unwanted dead times, i.e. times between reaching the steady-state condition and selection of an input voltage, are advantageously reduced and a next step in voltage regulation, i.e. selecting and coupling of an input voltage by the start-up selection circuit, is only initiated if overshoot has died out. This way the voltage regulator arrangement not only features reduced start-up times but stays functional and overshoot is prevented from adding up. Preferably, the steady-state signal constitutes a power ok signal of a LDO. Such a signal asserts that the LDO has reached the steady-state condition and is conveniently implemented in most commercially available LDO circuits.

[0049] The power ok signal is only applied after a delay depending on the LDO gain bandwidth and phase margin, i.e. the time it takes for the overshoot to die out. Thus, the power ok signal indicates that LDO is ready to settle to a next input voltage again.

[0050] Alternatively, the start-up selection circuit selects the at least one intermediate input voltage, further intermediate input voltage or target input voltage depending on a predetermined time period.

[0051] Preferably, the start-up selection circuit comprises a timer circuit, which usually is already present in commercially available LDOs and implemented into sub-circuits that regulate pre-charging of noise filters.

[0052] According to another aspect of the invention, the voltage regulator arrangement comprises a voltage regulator having a reference input terminal and the output terminal feeds back to the reference input terminal. Preferably, the voltage regulator is a LDO.

[0053] According to another aspect of the invention, the arrangement comprises at least one intermediate input voltage terminal fed by the intermediate input voltage and a target input voltage terminal fed by the target input voltage. Furthermore, the start-up selection circuit may comprise a multiplexer.

[0054] The multiplexer electrically couples the at least one intermediate input voltage terminal or the target input voltage terminal to the input terminal.

[0055] According to another aspect of the invention, the arrangement comprises a variable resistor coupled between the output terminal and the reference input terminal and is connected to common ground. Preferably, the variable resistor comprises taps which are coupled to the reference terminal of the voltage regulator.

[0056] The start-up selection circuit sets the variable resistor such that the at least one intermediate input voltage or the target input voltage terminal is effectively connected to the reference input terminal. In other words, the voltage applied at the input terminal is kept constant and the regulated output at the output terminal changes in steps of resistance set to the variable resistor.

[0057] According to another aspect of the invention, the start-up selection circuit may comprise a multiplexer and the arrangement may comprise a variable resistor coupled between the output terminal and the reference input terminal.

[0058] The following description of figures of exemplary embodiments further illustrates and explains the invention. Devices with the same structure or with the same effect, respectively, appear with like reference numerals. A description of a part of a circuit or a device having the same function in different figures might not be repeated in each of the following figures.

Figures 1A, 1B and 1C outline prior art related to a conventional voltage regulator arrangement,

Figures 2A, 2B and 2C show exemplary embodiments of a voltage regulator arrangement according to the principle presented, and

Figure 3 shows an exemplary embodiment of the start-up selection circuit according to the principle presented.

[0059] Figure 2A shows an exemplary embodiment of a voltage regulator arrangement according to the principle presented. A voltage regulator VR comprises an input terminal In and an output terminal Out. The output terminal Out is connected to a series connection of a first resistor R1 and a second resistor R2. The first resistor R1 is connected to a reference input terminal Ref of the voltage regulator VR. The second resistor R2 is connected to the ground level GND. The input terminal In is connected to a start-up selection circuit Sel which comprises a multiplexer Mux. The start-up selection circuit Sel is coupled to an arrangement Arr for generating at least one intermediate input voltage Vint and a target input voltage Vfin which comprises an intermediate input voltage terminal Int and a target input voltage terminal Fin. The intermediate input voltage terminal Int is coupled to the intermediate input voltage Vint, and the target input voltage terminal Fin is coupled to the target input voltage Vfin.

[0060] During a start-up phase the start-up selection circuit Sel successively selects the intermediate input voltage Vint and the target input voltage Vfin and couples the respectively selected one input voltage to the input voltage terminal of the voltage regulator VR. Preferably, the start-up selection circuit triggers the multiplexer Mux to electrically couple the intermediate input voltage Vint and the target input voltage Vfin, respectively, to the input voltage terminal In of the

voltage regulator VR.

[0061] Figure 2B shows another exemplary embodiment of a voltage regulator arrangement according to the presented principle. In this embodiment the arrangement Arr comprises the first resistor R1 and the second resistor R2, in turn, comprising a variable resistor Rvar. Alternatively, also resistor R1 or both R1 and R2 can be made variable.

[0062] The start-up selection circuit Sel sets the resistance of the variable resistor Rvar. Thereby, the arrangement Arr generates the at least one intermediate input voltage Vint or target input voltage Vfin which is then coupled to the reference input terminal Ref.

[0063] Advantageously, the voltage regulator arrangements according to Figure 2A and 2B can be implemented with any kind of voltage regulator VR, preferably with LDOs, i.e. low dropout regulators. In particular, this is an advantage if implemented in dual or multiple channel voltage regulator arrangements. Area requirements and noise are lowered and performance does not depend on load conditions. Furthermore, bandwidth of the voltage regulator VR, e.g. an LDO, is not modified.

[0064] In a further alternative embodiment (not shown) the start-up selection circuit Sel comprises a logic circuitry to modulate the variable resistor Rvar depending on the target input voltage Vfin.

[0065] Figure 2C shows the start-up phase of the voltage regulator arrangement according to Figures 2A or 2B. Figure 2C shows input voltages and regulated output voltages applied to or provided by the voltage regulator arrangement as a function of time.

[0066] In a first step, the selection circuit Sel couples the at least one intermediate input voltage Vint to the input terminal In or the reference input terminal Ref, respectively. In response, the voltage regulator VR regulates the output voltage Vout. This results in a first overshoot 1 in the output voltage Vout. Next, in a second step, the selection circuit Sel couples the target input voltage Vfin to the input terminal In or the reference input terminal Ref, respectively. In response, the voltage regulator VR regulates the output voltage Vout resulting in a relatively small second overshoot 2.

[0067] Advantageously, by using the start-up selection circuit Sel the at least one intermediate input voltage Vint or target input voltage Vfin is coupled to the input terminal In or reference input terminal Ref, respectively, during the start-up phase in a stepwise approach. This way, overshoot is almost proportional to the step-size and can be tailored to keep overshoot low during the entire start-up phase. As a consequence, a final step-size leads to an overshoot which can be quite small compared to the target input voltage Vfin.

[0068] In a further alternative embodiment (not shown) the arrangement Arr comprises at least one further intermediate input voltage which is provided between the at least one intermediate input voltage Vint and the target input voltage Vfin. Correspondingly the arrangement Arr comprises an at least one further intermediate input voltage terminal.

[0069] The start-up selection circuit Sel selects and couples the further intermediate input voltage to the input terminal In or reference input terminal Ref, respectively.

[0070] In a further alternative embodiment (not shown) the arrangement Arr generates a number of N increasing further intermediate input voltages provided between the at least one intermediate input voltage Vint and the target input voltage Vfin.

[0071] The start-up selection circuit Sel successively selects and couples, in a step like fashion, the number of N increasing further intermediate input voltages to the input terminal In or reference input terminal Ref, respectively.

[0072] Figure 3 shows an exemplary embodiment of the start-up selection circuit according to the presented principle. The start-up selection circuit Sel comprises a multiplexer Mux which is embedded in a first amplification stage of the voltage regulator VR. The multiplexer comprises a first and second source-coupled transistor pair circuit TP1 and TP2 plus a current switch S1a and S1b coupled to transistor pair circuit TP1 and TP2, respectively. Each transistor pair circuit TP1 and TP2 further comprises a first transistor T1 and a second transistor T2 which share the same source terminal. Each first and second transistor T1 and T2 is, at its drain side, coupled to a loading block of the first amplification stage, made up by a first and second load transistor MP1, MP2, respectively, which are connected in a current mirror configuration. It may, however, be understood that such loading block constituted by load transistors MP1, MP2 can be implemented in several other ways known to those expert in the art. A bias current Itail, coupled to a supply rail is deviated into one out of the two common sources of the transistor pair circuits TP1, TP2 by means of the complementary switches S1a and S1b which may be digitally driven by a selection block. The supply rail may either be ground potential GND or any supply-voltage, e.g. Vdd in case the transistor pair circuit is in PMOS.

[0073] In the first transistor pair circuit TP1 the first transistor T1 has a control terminal C1a and the second transistor T2 a control terminal C2a. In the second transistor pair circuit TP2 the first transistor T1 has a control terminal C1b and the second transistor T2 a control terminal C2b. The second control terminal C2a of the first transistor pair circuit TP1 is connected to the first control terminal C1b of the second transistor pair circuit TP2. The at least one input voltage Vint is coupled to the first control terminal C1a of the first transistor pair circuit TP1 and the target input voltage Vfin is coupled to the second control terminal C2b of the second transistor pair circuit TP2. Both control terminals C1a and C2b are coupled to the reference input terminal Ref of the voltage regulator VR.

[0074] By appropriate switching of complementary switches S1a and S1b the bias current Itail is deviated between the first transistor pair circuit TP1 and the second transistor pair circuit TP2. In this way only one of the two transistor

pair circuits TP1, TP2 is effectively connected to the load transistors MP1, MP2 of the first amplification stage of the voltage regulator VR while the other is left in an off-state. Consequently, only one input voltage between Vint and Vfin is effectively coupled to input terminal In of the voltage regulator VR.

[0075] The presence of analog switches in a multiplexer in series to the voltage regulator VR input terminal In might give reason to concerns about noise and dynamic range. However, the above proposed solution, i.e. moving the multiplexer Mux inside the voltage regulator VR, outperforms alternative arrangements where the multiplexer is implemented outside the voltage regulator VR. This is due to the fact that no additional circuitry in an on-state is needed after replacing the input stage of the voltage regulator VR and keeping all the remaining transistors off. Hence, the same noise level and accuracy is achieved as if the multiplexer Mux was implemented outside the voltage regulator VR. Even though such an approach demands some more chip area usually the overall gain in noise and dynamic range renders such approach advantageous. Moreover, final configuration of the voltage regulator VR, e.g. a LDO, remains unaltered. Additionally, switching tail current Itail from one transistor pair circuit to another is so fast that no significant spikes occur at the control terminals C1a, C1b, C2a and C2b of the transistors. In fact, the control terminals are loaded by parasitics such that if tail currents Itail are not fed for fractions of nanoseconds operation of the voltage regulator VR does not fail.

[0076] Instead of moving the multiplexer Mux inside the voltage regulator VR it is just as well possible to externally connect the multiplexer Mux to the input terminal In. The at least one intermediate input voltage Vint and target input voltage Vfin, as well other appropriate input voltages may e.g. be obtained from the arrangement Arr by taking some taps of a resistor string which generates a reference voltage. Such an approach is effective if the final output voltage Vout of the voltage regulator VR stays higher than a minimum common mode voltage.

[0077] In a further alternative embodiment (not shown) the multiplexer Mux comprises series connection of a number of N parallel transistor pair circuits TP to provide N further intermediate input voltages to the voltage regulator VR.

List of Reference Numerals

[0078]

1	first overshoot
2	second overshoot
Arr	arrangement
C1a	first control terminal
C1b	second control terminal
C2a	first control terminal
C2b	second control terminal
Fin	target input voltage terminal
GND	common ground
I	current source
In	input terminal
Int	intermediate input voltage terminal
Itail	bias current
MP1	first load transistor
MP2	second load transistor
Mux	multiplexer
Out	output terminal
R1	first resistor
R2	second resistor
Ref	reference input terminal
Rvar	variable resistor
rVout	reduced output voltage
S1a	switch
S1b	switch
Sel	start-up selection circuit
T1	first transistor
T2	second transistor
TP1	first transistor pair circuit
TP2	second transistor pair circuit
Vfin	target input voltage
Vint	intermediate input voltage
Vout	output voltage

VR voltage regulator
VR2 second amplification stage

5 Claims

1. Method for voltage regulation, comprising:

- providing a sequence of input voltages of at least one intermediate input voltage (V_{int}) and a target input voltage (V_{fin}),
- selecting the at least one intermediate input voltage (V_{int}) from the sequence of input voltages,
- regulating an output voltage (V_{out}) depending on the at least one intermediate input voltage (V_{int}) such that the output voltage (V_{out}) reaches a steady-state condition,
- selecting the target input voltage (V_{fin}) in the sequence of input voltages, and
- regulating the output voltage (V_{out}) depending on the target input voltage (V_{fin}) such that the output voltage (V_{out}) reaches the steady-state condition.

2. Method for voltage regulation according to claim 1, comprising:

- selecting a further intermediate input voltage from the sequence of input voltages provided between the at least one intermediate input voltage (V_{int}) and the target input voltage (V_{fin}), and
- regulating the output voltage (V_{out}) depending on the further intermediate input voltage such that the output voltage (V_{out}) reaches the steady-state condition.

3. Method for voltage regulation according to claim 2, comprising successive selection of a number of N further intermediate voltages in the sequence of input voltages and corresponding successive regulation of the output voltage (V_{out}) depending on the respective of the N further intermediate input voltages such that the output voltage (V_{out}) increases in a steplike fashion until the target input voltage (V_{fin}) in the sequence of input voltages is selected and the output voltage (V_{out}) depending on the target input voltage (V_{fin}) is regulated.

4. Method for voltage regulation according to claim 2 or 3, in which the steady-state condition is reached if the intermediate input voltage (V_{int}), further intermediate input voltage or target input voltage (V_{fin}) multiplied by a scaling factor equals the regulated output voltage (V_{out}).

5. Method for voltage regulation according to one of claims 2 to 4, in which reaching the steady-state condition is indicated by a signal.

6. Method for voltage regulation according to one of claims 2 to 4, in which reaching the steady-state condition is indicated by a time period.

7. Method for voltage regulation according to claim 5, in which the further intermediate input voltage is selected depending on the signal.

8. Voltage regulator arrangement, comprising:

- a voltage regulator (VR) having an input terminal (In) and an output terminal (Out),
- an arrangement (Arr) for generating at least one intermediate input voltage (V_{int}) and a target input voltage (V_{fin}), and
- a start-up selection circuit (Sel) for selecting the at least one intermediate input voltage (V_{int}) or the target input voltage (V_{fin}) and coupling the at least one intermediate input voltage (V_{int}) or the target input voltage (V_{fin}) to the input terminal (In) during a start-up phase.

9. Voltage regulator arrangement according to claim 8, in which the start-up selection circuit (Sel) selects a further intermediate input voltage which is provided between the at least one intermediate input voltage (V_{int}) and the target input voltage (V_{fin}) and couples the further intermediate input voltage to the input terminal (In).

10. Voltage regulator arrangement according to claim 9, in which the start-up selection circuit (Sel) successively selects a number of N increasing further intermediate voltages provided between the at least one intermediate input voltage

(Vint) and the target input voltage (Vfin) and, in a steplike fashion, successively couples the number of N increasing further intermediate input voltages to the input terminal (In).

11. Voltage regulator arrangement according to claim 9 or 10, in which

- the start-up selection circuit (Sel) selects the at least one intermediate input voltage (Vint), further intermediate input voltage or the target input voltage (Vfin) depending on a signal indicating a steady-state condition, and
- the steady-state condition is reached if the intermediate input voltage (Vint), further intermediate input voltage or target input voltage (Vfin) equals a regulated output voltage (Vout) at the output terminal (Out) multiplied by a scaling factor.

12. Voltage regulator arrangement according to claim 9 or 10, in which the start-up selection circuit (Sel) selects the at least one intermediate input voltage (Vint), further intermediate input voltage or the target input voltage (Vfin) depending on a signal or a predetermined time period.

13. Voltage regulator arrangement according to one of claims 8 to 12, in which voltage regulator (VR) further comprises a reference input terminal (Ref), and the output terminal (Out) feeds back to the reference input terminal (Ref).

14. Voltage regulator arrangement according to claim 13, in which

- the arrangement (Arr) comprises at least one intermediate input voltage terminal (Int) fed by the intermediate input voltage (Vint), and a target input voltage terminal (Fin) fed by the target input voltage (Vfin), and
- the start-up selection circuit (Sel) comprises a multiplexer (Mux) for electrically coupling the at least one intermediate input voltage terminal (Int) or the target input voltage terminal (Fin) to the input terminal (In).

15. Voltage regulator arrangement according to claim 13, in which

- the arrangement (Arr) comprises a variable resistor (Rvar) coupled between the output terminal (Out) and the reference input terminal (Ref) and connected to a reference supply rail, and
- the start-up selection circuit (Sel) sets the variable resistor (Rvar) such that the at least one intermediate input voltage (Vint) or the target input voltage (Vfin) is effectively provided at the output terminal (Out).

FIG 1A (Prior Art)

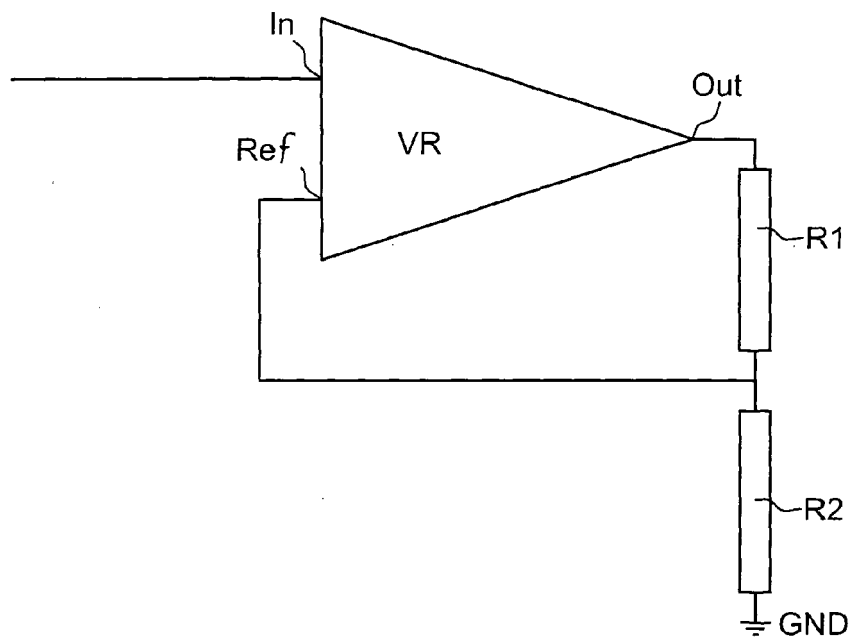


FIG 1B (Prior Art)

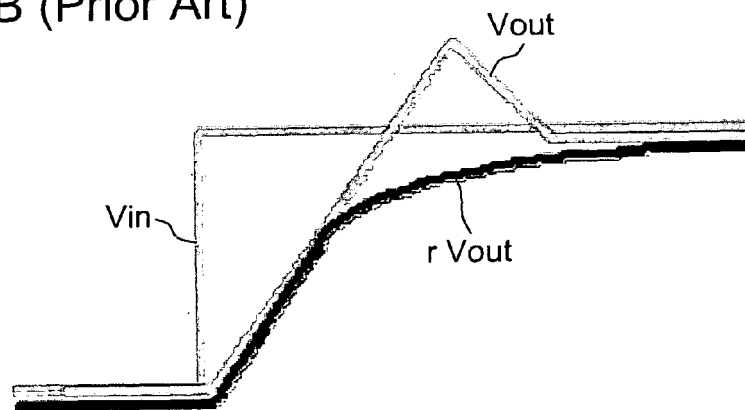


FIG 1C (Prior Art)

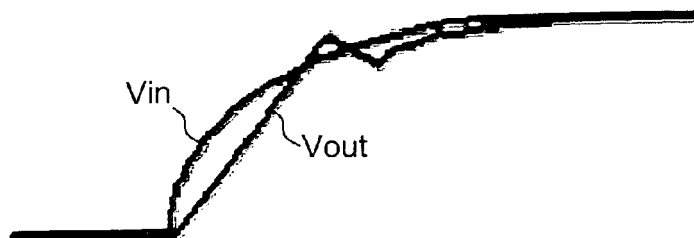


FIG 2A

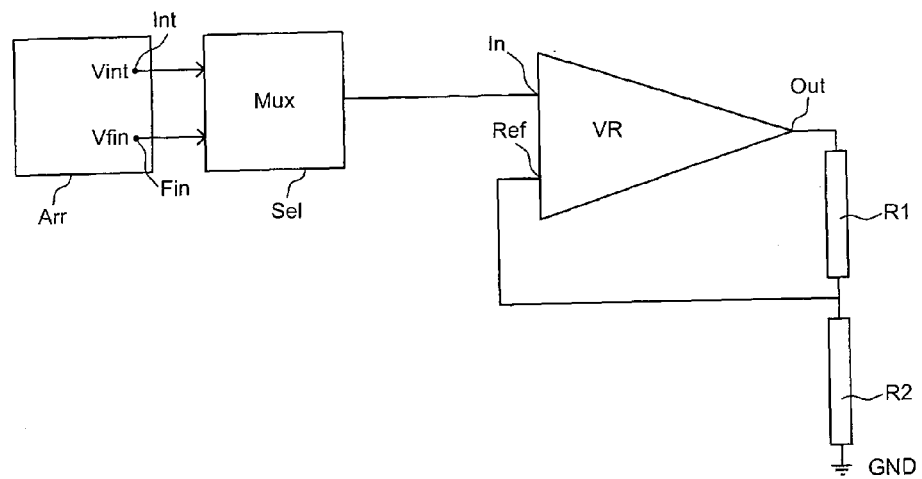


FIG 2B

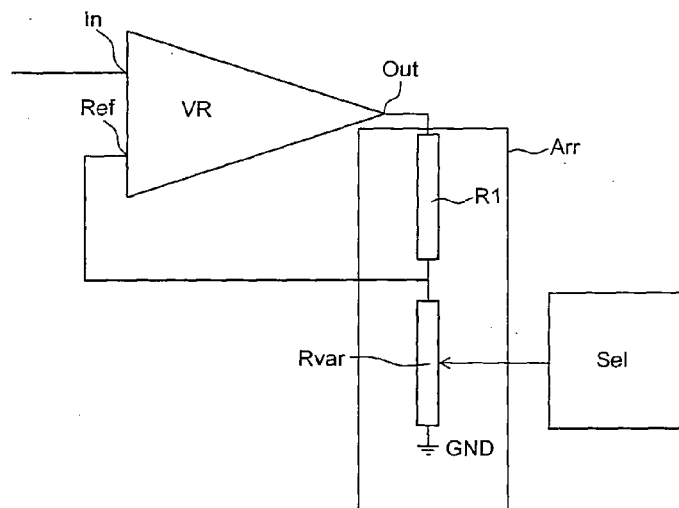


FIG 2C

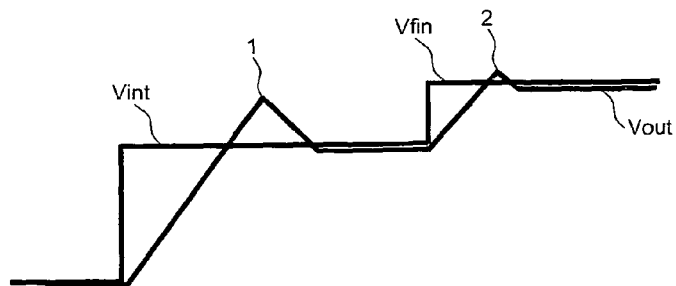
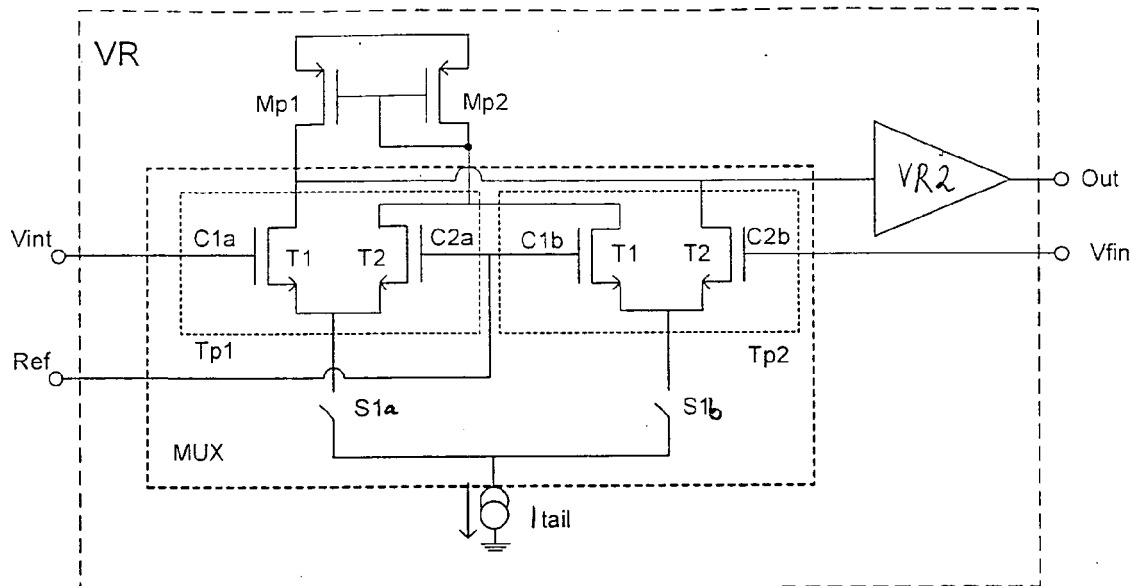


FIG 3





EUROPEAN SEARCH REPORT

Application Number
EP 09 01 3621

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			G05F
Place of search		Date of completion of the search	Examiner
The Hague		17 March 2010	Arias Pérez, Jagoba
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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EPO FORM 1503 03 82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 09 01 3621

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The members are as contained in the European Patent Office EDP file on
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17-03-2010

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