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(54) High-voltage vertical FET and method of manufacturing the same

(57) In one embodiment, a transistor fabricated on a semiconductor die is arranged into sections of elongated transistor segments. The sections are arranged in rows and columns substantially across the semiconductor die. Adjacent sections in a row or a column are oriented such that the length of the transistor segments in a first one of the adjacent sections extends in a first direction, and the length of the transistor segments in a second one of the adjacent sections extends in a second direction, the first direction being substantially orthogonal to the second direction. It is emphasized that this abstract is provided to comply with the rules requiring an abstract that will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure.

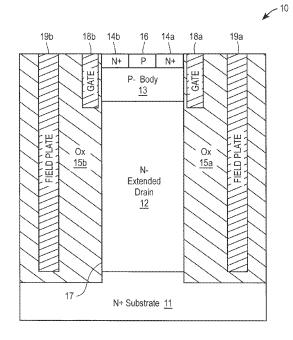
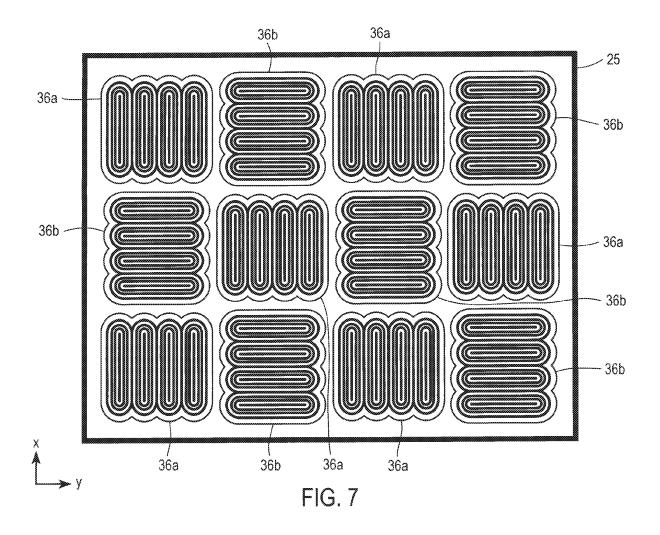


FIG. 1

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EUROPEAN SEARCH REPORT

Application Number EP 11 16 8216

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