(12)

## **EUROPEAN PATENT APPLICATION**

(43) Date of publication:

16.11.2011 Bulletin 2011/46

(51) Int Cl.: H01F 7/18<sup>(2006.01)</sup> H01H 47/00<sup>(2006.01)</sup>

F23N 5/24 (2006.01)

(21) Application number: 10004949.3

(22) Date of filing: 11.05.2010

(84) Designated Contracting States:

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

Designated Extension States:

**BA ME RS** 

(71) Applicant: Honeywell Technologies Sarl 1180 Rolle (CH)

(72) Inventor: Galeazzi, Daniele 20059 Vimercate (MB) (IT)

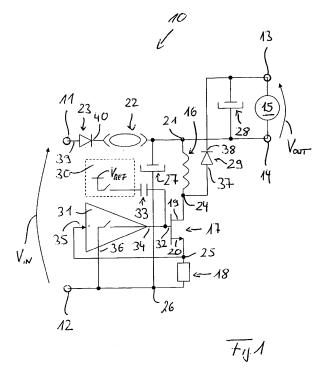
(74) Representative: Sturm, Christoph et al

Quermann Sturm Weilnau Patentanwälte Unter den Eichen 7 65195 Wiesbaden (DE)

(54) Power driver and fail safe circuit for a gas valve

(57) Power driver and fail safe circuit (10) for a gas valve in order to open or close the gas valve, comprising: input contacts (11, 12) to which a power source providing a defined DC input power is connectable; an inductance coil (16), a transistor (17) and a resistor (18) being connected in series in such a way that said inductance coil (16) is connected to the drain (19) and said resistor (18) is connected to the source (20) of the transistor; an input capacitor (27) being connected in parallel to the series connection of said inductance coil (16), said transistor (17) and said resistor (18); an output capacitor (28) being

connected between output contacts (13, 14) to which a coil (15) of the gas valve is connectable; a first diode (29) being connected in series to the parallel connection of the output capacitor (28) and the coil (15) of the gas valve, wherein said series connection is connected in parallel to said inductance coil (16); a micro controller (30) and a peak current detector (31) both being connected to the gate (32) of said transistor so that the transistor can be turned on into a current conducting mode by a signal provided by the micro controller (30) and that the transistor can be turned off into a current blocking mode by a signal provided by the peak current detector (31).



EP 2 387 046 A1

### **Description**

20

30

35

40

45

50

55

[0001] The invention relates to a power driver and fail safe circuit for a gas valve.

[0002] An electric or electronic power driver circuit for a gas valve is connected by input contacts of the same to an electrical power source providing an electrical input power to the power driver circuit. Further on, such a power driver circuit for a gas valve is connected by output contacts of the same to a coil of the gas valve to be operated. The power driver circuit for a gas valve is used to open or close the gas valve. The power driver circuit opens or closes a gas valve in such a way that the gas valve is opened when the coil of the gas valve being connected to output contacts of the power driver circuit is energized with a defined electrical output power of the power driver circuit. The gas valve is closed when said coil of the gas valve is not energized with the defined electrical output power of the power driver circuit.

**[0003]** In order to provide a safe operation of the gas valve, it is necessary to ensure that a gas valve becomes not opened by a failure of one or more components of the power driver circuit. So, it is necessary to ensure that the power driver circuit does not energize the coil of the gas valve with the defined electrical output power in case of a failure of one or more components of the electric or electronic power driver circuit. Such a power driver circuit providing fail safe functionality is called power driver and fail safe circuit.

[0004] Against this background, a novel power driver and fail safe circuit for a gas valve is provided.

**[0005]** According to the present invention the power driver and fail safe circuit for a gas valve comprises input contacts to which an electrical power source providing a defined electrical DC input power level for the power driver and fail safe circuit is connectable. The power driver and fail safe circuit further comprises an inductance coil, a transistor and a resistor being connected in series to each other in such a way that said inductance coil is connected to the drain of the transistor and that said resistor is connected to the source of the transistor. The power driver and fail safe circuit further comprises an input capacitor being connected in parallel to the series connection of said inductance coil, said transistor and said resistor. The power driver and fail safe circuit further comprises an output capacitor being connected between the output contacts of the power driver and fail safe circuit and thereby being connected in parallel to the coil of the gas valve to be operated. The power driver and fail safe circuit comprises further a first diode being connected in series to the parallel connection of the output capacitor and the coil of the gas valve; wherein said series connection is connected in parallel to said inductance coil. The power driver and fail safe circuit comprises further a micro controller and a peak current detector both being connected to the gate of said transistor so that the transistor can be turned on into a current conducting mode by a signal provided by the micro controller and that the transistor can be turned off into a current blocking mode by a signal provided by the peak current detector.

**[0006]** The novel electric or electronic power driver and fail safe circuit ensures that a gas valve becomes not opened by a failure of one or more components of the power driver and fail safe circuit. The power driver and fail safe circuit does not need an extra electrical power. The novel electric or electronic power driver and fail safe circuit has a low power consumption. The power driver and fail safe circuit provides a defined DC output power level being fully controlled by the power driver and fail safe circuit and being independent from the impedance of the coil of the gas valve.

**[0007]** Preferred developments of the invention are provided by the dependent claims and the description which follows. Exemplary embodiments are explained in more detail on the basis of the drawing, in which:

- Figure 1 shows a power driver and fail safe circuit for a gas valve according to a first embodiment;
- Figure 2 shows a power driver and fail safe circuit for a gas valve according to a second embodiment;
  - Figure 3 shows a power driver and fail safe circuit for a gas valve according to a third embodiment; and
  - Figure 4 shows a power driver and fail safe circuit for a gas valve according to a fourth embodiment.

**[0008]** The invention relates to an electric or electronic power driver and fail safe circuit for a gas valve. Such a power driver and fail safe circuit is connected to an electrical power source providing an electrical input power to the power driver and fail safe circuit. Further on, such a power driver and fail safe circuit is connected by to a coil of a gas valve to be operated.

**[0009]** The power driver and fail safe circuit for a gas valve is used to open or close the gas valve. The power driver circuit and fail safe opens or closes the gas valve in such a way that the gas valve is opened when the coil of the gas valve being connected to output contacts of the power driver and fail safe circuit is energized with a defined electrical output power of the power driver and fail safe circuit. The gas valve is closed when said coil of the gas valve is not energized with the defined electrical output power of the power driver and fail safe circuit.

**[0010]** Figure 1 shows a fist preferred embodiment of a power driver and fail safe circuit 10 for a gas valve. The power driver and fail safe circuit 10 has input contacts 11, 12 to which a power source (not shown) is connected.

**[0011]** The power source provides a DC input power V<sub>IN</sub> with a defined DC input power level to the power driver and fail safe circuit 10. The input contact 11 corresponds to positive input contact and the input contact 12 corresponds to the negative input contact which is also often called ground contact. The power driver and fail safe circuit 10 has further output contacts 13, 14 to which a coil 15 of a gas valve is connected. The gas valve is opened when said coil 15 being

connected to output contacts 13, 14 of the power driver and fail safe circuit 10 is energized with a DC output power V<sub>OUT</sub> having a defined DC output power level. The gas valve is closed when said coil 15 is not energized with the defined DC output power level of the circuit 10.

**[0012]** The defined DC output power level  $V_{OUT}$  provided by the circuit 10 is fully controlled by the same and is independent from the impedance of the coil 15 of the gas valve.

**[0013]** The power driver and fail safe circuit 10 comprises an inductance coil 16, a transistor 17 and a resistor 18 being connected in series to each other. These elements 16, 17 and 18 are connected in series in such a way that said inductance coil 16 is connected to the drain 19 of the transistor 17 and that said resistor 18 is connected to the source 20 of the transistor 17.

**[0014]** As shown in the preferred embodiment of figure 1, a first contact 21 of said inductance coil 16 is connected to the first input contact 11 of the power driver and fail safe circuit 10, preferably through a fuse 22 and a diode 23. A second contact 24 of said inductance coil 16 is connected to the drain 19 of the transistor 17.

**[0015]** A first contact 25 of the resistor 18 is connected to the source 20 of the transistor 17. A second contact 26 of the resistor 18 is connected to a second input contact 12 of the power driver and fail safe circuit 10 and thereby to input contact or ground contact.

**[0016]** The power driver and fail safe circuit 10 further comprises an input capacitor 27 being connected in parallel to the series connection of said inductance coil 16, said transistor 17 and said resistor 18. As shown in figure 1, the input capacitor 27 is connected to the first contact 21 of said inductance coil 16 and to the second contact 26 of the resistor 18.

**[0017]** The power driver and fail safe circuit 10 further comprises an output capacitor 28 being connected between the output contacts 13, 14 of the power driver and fail safe circuit 10 and thereby in parallel to the coil 15 of the gas valve. The power driver and fail safe circuit 10 further comprises a diode 29, being connected in series to the parallel connection of the output capacitor 28 and the coil 15 of the gas valve. Said series connection is connected in parallel to said inductance coil 16.

20

30

35

40

45

50

55

**[0018]** The power driver and fail safe circuit 10 further comprises a micro controller 30 and a peak current detector 31 both being connected to the gate 32 of said transistor 17. The micro controller 30 is connected to the gate 32 of the transistor 17 trough a capacitor 33 and provides a dynamic, alternating signal to the gate 32. This signal provided by the transistor 17 depends on a reference DC voltage  $V_{\rm RFF}$ .

**[0019]** The peak current detector 31 is connected with an output contact 34 to the gate 32 of said transistor 17, with a first input contact 35 to the source 20 of said transistor 17 and thereby to the first contact 25 of the resistor 18 and with a second input contact 36 to the input contact or ground contact. The peak current detector 31 provides a dynamic signal to the gate 32 of the transistor 17 depending on the current flow through the resistor 18.

[0020] The transistor 17 can be turned on into a current conducting mode by the signal provided by the micro controller 30. The transistor 17 can be turned off into the current blocking mode by a signal provided by the peak current detector 31.

**[0021]** When the transistor 17 is turned on into the current conducting mode said inductance coil 16 becomes charged and the current across said resistor 18 being connected to the source 20 of the transistor 17 reaches its peak. When the transistor 17 is turned off into the current blocking mode the inductance coil 16 becomes discharged through the diode 29 thereby charging the output capacitor 28. Between these two modes the transistor 17 memorizes the state in its gate source capacitance.

**[0022]** As shown in the preferred embodiment of figure 1, the anode 37 of the diode 29 is connected to the second contact 24 of said inductance coil 16 and to the drain 19 of the transistor 17. The cathode 38 of said diode 29 is connected to the output capacitor 28 and to a first output contact 13 of the power driver and fail safe circuit 10.

**[0023]** Said fuse 22 and the diode 23 being connected between the first contact 21 of said inductance coil 16 and the first input contact 11 of the power driver and fail safe circuit 10 are connected in series to each other, namely in such a way that the anode 39 of said diode 23 is connected to first input contact 11 of the power driver and fail safe circuit 10 and that the cathode 40 of said diode 23 is connected to the fuse 22.

**[0024]** The transistor 17 is preferably a MOSFET transistor. Most preferably the transistor 17 is a n-channel enhancement mode MOSFET transistor being normally turned off into the current blocking mode.

**[0025]** The power driver and fail safe circuit 10 works with a cycle to charge and discharge the inductance coil 16. The signal provided by the micro controller 30 is preferably a signal of type on/off with a defined frequency fixed duty cycle. The power driver and fail safe circuit 10 normally works for a defined time period which depends on the defined frequency, and for the next defined time period it is off. It should be noted that the system could in general work also continuously, whereby in this case the defined off time period would then be zero.

[0026] The micro controller 30 connects quickly capacitor 33 at the positive voltage. The gate-source capacitor of the transistor 17 being an intrinsic component inside the transistor 17 is charging and, by a capacitive partition with capacitor 33, transistor 17 conducts. The transistor 17 conducts till the current over inductance coil 16 or resistor 18 grows up to a maximum value. The peak of the current in the inductance coil 16 or resistor 18 is detected and positive feedback is activated by the peak current detector 31 thereby turning off the transistor 17. The output of the peak current detector 31 switches off the transistor 17, it resets to zero the charge of the capacitor gate-source of transistor 17 and of the

capacitor 33. The capacitor 33 is discharged. The energy of inductance coil 16 is recovered by the diode 29 and the output capacitor 28. The diode 29 turns on when transistor 17 turns off, so output capacitor 28 is charging.

[0027] The power driver and fail safe circuit 10 can not provide any output voltage VOUT to open the gas valve when one component fails. The path to connect the coil 15 of the gas valve to the input voltage  $V_{\text{IN}}$  passes through the diode 29 and transistor 17. The diode 29 and the transistor 17 are able to withstand their failure. A failure of the transistor 17 can not damage the diode 29 and vice versa. If the transistor 17 would fail, the transistor 17 would be is in short. In case of the failure of the transistor 17 the power driver and fail safe circuit 10 can detect the failure because the coil 15 of gas valve can not be energized.

**[0028]** In this case the current would flow from the input power source to the diode 23, to the fuse 22, to the inductance coil 16, to the transistor 17 and than to the resistor 18.

**[0029]** The Fuse 22 works detecting the failure, because current is limited by the impedance but exceeds the fuse rating. Inductance coil 16 is able to withstand the current that breaks the fuse 22. This failure mode shut off the board in safety mode.

**[0030]** Further on, under the hypothesis that the inductance coil 16 would break down in an open circuit, the power driver and fail safe circuit 10 can also not provide any output voltage V<sub>OUT</sub> to the coil 15 to open the gas valve.

**[0031]** Figure 2 shows a second preferred embodiment of a power driver and fail safe circuit 10' having compared to power driver and fail safe circuit 10 according to figure 1 the difference that the input capacitor 27 is connected with a first contact between said fuse 22 and said diode 23 and with a second contact to ground so that the input capacitor 27 is connected in parallel to the fuse 22.

**[0032]** In figure 1 the input capacitor 27 is connected with a first contact between said fuse 22 and said inductance coil 16 and with a second contact to ground so that the input capacitor 27 is connected in series to the fuse 22. However, the failure detection functionality remains the same.

**[0033]** Figure 3 shows a third preferred embodiment of a power driver and fail safe circuit 10" having compared to power driver and fail safe circuit 10 according to figure 1 as additional component a diode 41. Said diode 41 is connected in parallel to said output capacitor 28, whereby the cathode 42 of said diode 41 is connected to the cathode 38 of the diode 29 and whereby the anode 43 of said diode 41 is connected to the first contact 21 of said inductance coil 16.

[0034] In case the diode 29 would fail in short circuits, the electrical current would flow from the input power source to the diode 23, to the fuse 22, to the diode 42, to the diode 29, to the transistor 17 and than to the resistor.

**[0035]** The fuse 22 would work detecting the failure, because current is limited by the impedance of devices but exceeds the fuse rating. Diode 41 is able to withstand the current that breaks the fuse 22. This failure mode shut off the power driver and fail safe circuit 10 in safety mode.

[0036] Figure 4 shows a fourth preferred embodiment of a power driver and fail safe circuit 10" having compared to power driver and fail safe circuit 10" according to figure 3 as additional components the diodes 44 and preferably the diodes 47 and 48. This provides redundancy and a higher reliability of the power driver and fail safe circuit. The diodes 41, 44 are connected in parallel with the coil 15 of the gas valve. The diode 44 is connected in parallel to said output capacitor 28 and said diode 41, whereby the cathode 45 of the diode 44 is connected to the cathode 42 of the diode 41 and whereby the anode 46 of the diode 44 is connected to the anode 43 of the diode 41. The diodes 47 and 48 are connected in series to diode 29, namely in such a way that anode of the diode 47 is connected to the cathode of the diode 48 is connected to the cathode of the diode 47 and that the cathode of the diode 48 is connected to the first output contact 13.

**[0037]** In connection with the embodiments of figures 3 and 4 it is possible to use the connection scheme for the input capacitor 27 as shown in figure 2.

[0038] The power driver and fail safe circuits 10, 10' and 10" are all using a transistor 17 working like a switching operator. The transistor 17 is driven by two commands, one to turn on the transistor 17 and the other to turn off transistor 17. The signal to turn on the transistor 17 is generated by the micro controller 30 and the signal to turn off the transistor 17 is provided by the peak current detector 31. Between the two events the transistor 17 memorizes the state in its gate source capacitance.

**[0039]** In the power driver and fail safe circuits 10, 10' and 10", the control of the power can be done electronically by the control of the energy stored into the inductance coil 16. Current in the inductance coil 16 starts from zero, then the power driver and fail safe circuits 10, 10' and 10"controls the peak of the current and fixes carefully its maximum value. A constant flux of energy is assured by repeating the cycle at a constant frequency.

List of reference signs

## *55* **[0040]**

20

30

35

40

45

50

10, 10', 10", 10"' power driver and fail safe circuit

|    | 11 | input contact                           |
|----|----|---|
|    | 12 | input contact                           |
| 5  | 13 | output contact                          |
|    | 14 | output contact                          |
| 10 | 15 | coil / gas valve                        |
| 10 | 16 | inductance coil                         |
|    | 17 | transistor                              |
| 15 | 18 | resistor                                |
|    | 19 | drain of transistor                     |
| 20 | 20 | source of transistor                    |
| 20 | 21 | first contact of inductance coil        |
|    | 22 | fuse                                    |
| 25 | 23 | diode                                   |
|    | 24 | second contact of inductance coil       |
| 30 | 25 | first contact of resistor               |
| 00 | 26 | second contact of resistor              |
|    | 27 | input capacitor                         |
| 35 | 28 | output capacitor                        |
|    | 29 | diode                                   |
| 40 | 30 | micro controller                        |
|    | 31 | peak current detector                   |
|    | 32 | gate of transistor                      |
| 45 | 33 | capacitor                               |
|    | 34 | output contact of peak current detector |
| 50 | 35 | input contact of peak current detector  |
|    | 36 | input contact of peak current detector  |
|    | 37 | anode                                   |
| 55 | 38 | cathode                                 |
|    | 39 | anode                                   |

|    | 40 | cathode |
|----|----|---------|
|    | 41 | diode   |
| 5  | 42 | cathode |
|    | 43 | anode   |
| 10 | 44 | diode   |
| 70 | 45 | cathode |
|    | 46 | anode   |
| 15 | 47 | diode   |
|    | 48 | diode   |
|    |    |         |

#### 20 Claims

25

30

35

40

50

- 1. Power driver and fail safe circuit (10, 10', 10", 10"') for a gas valve in order to open or close the gas valve in such a way that the gas valve is opened when a coil (15) of the gas valve being connectable to output contacts (13, 14) of the power driver and fail safe circuit (10, 10', 10"') is energized with a defined, fully controlled DC output power level of the power driver and fail safe circuit and that the gas valve is closed when said coil (15) of the gas valve is not energized with the defined DC output power level of the power driver and fail safe circuit, comprising:
  - input contacts (11, 12) to which a power source providing a defined DC input power level for the circuit is connectable:
  - an inductance coil (16), a transistor (17) and a resistor (18) being connected in series to each other in such a way that said inductance coil (16) is connected to the drain (19) of the transistor (17) and that said resistor (18) is connected to the source (20) of the transistor (17);
  - an input capacitor (27) being connected in parallel to the series connection of said inductance coil (16), said transistor (17) and said resistor (18);
  - an output capacitor (28) being connected between the output contacts (13, 14) to which the coil (15) of the gas valve being connectable;
  - a first diode (29) being connected in series to the parallel connection of the output capacitor (28) and the coil (15) of the gas valve; wherein said series connection is connected in parallel to said inductance coil (16);
  - a micro controller (30) and a peak current detector (31) both being connected to the gate (32) of said transistor (17) so that the transistor (17) can be turned on into a current conducting mode by a signal provided by the micro controller (30) and that the transistor (17) can be turned off into a current blocking mode by a signal provided by the peak current detector (31).
- 2. Power driver and fail safe circuit as claimed in claim 1, **characterized in that** when the transistor (17) is turned on into the current conducting mode said inductance coil (16) becomes charged and the current across said resistor (18) being connected to the source (20) of the transistor (17) reaches its peak.
  - 3. Power driver and fail safe circuit as claimed in claim 1 or 2, **characterized in that** when the transistor (17) is turned off into the current blocking mode the inductance coil (16) becomes discharged through the first diode (29) thereby charging the output capacitor (28).
    - **4.** Power driver and fail safe circuit as claimed in one of claims 1 to 3, **characterized in that** said transistor (17) is a MOSFET transistor.
- 55 **5.** Power driver circuit as claimed in claim 4, **characterized in that** the MOSFET transistor is a n-channel MOSFET transistor being normally turned off into the current blocking mode.
  - 6. Power driver and fail safe circuit as claimed in one of claims 1 to 5, characterized in that the anode (37) of said

first diode (29) is connected to said inductance coil (16) and to the drain (19) of the transistor (17), and that the cathode (38) of said first diode (29) is connected to the output capacitor (28) and to a first output contact (13).

7. Power driver and fail safe circuit as claimed in one of claims 1 to 6, **characterized in that** the peak current detector (31) is connected with an output contact (34) to the gate (32) of said transistor (17), with a first input contact (35) to the source (20) of said transistor (17) and to a contact (25) of the resistor (18), and with a second input contact (36) to the other contact (26) of the resistor (18) and to ground.

5

10

15

25

30

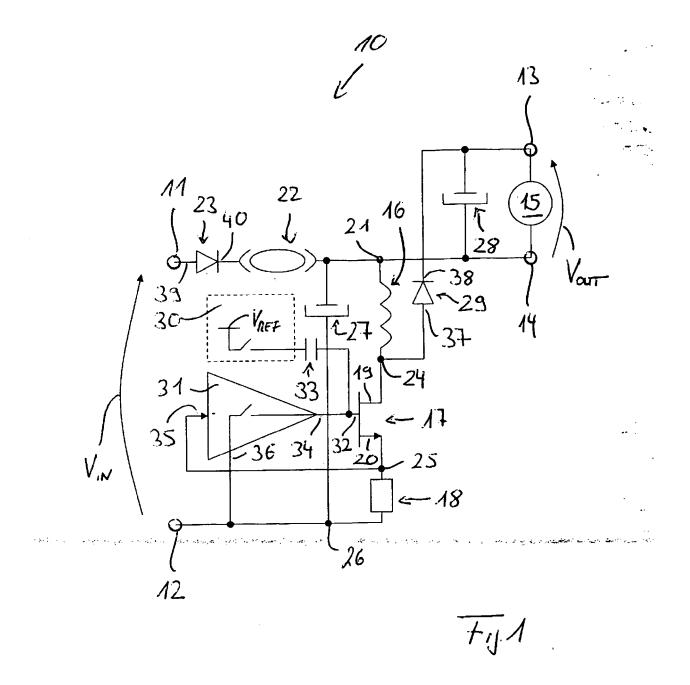
40

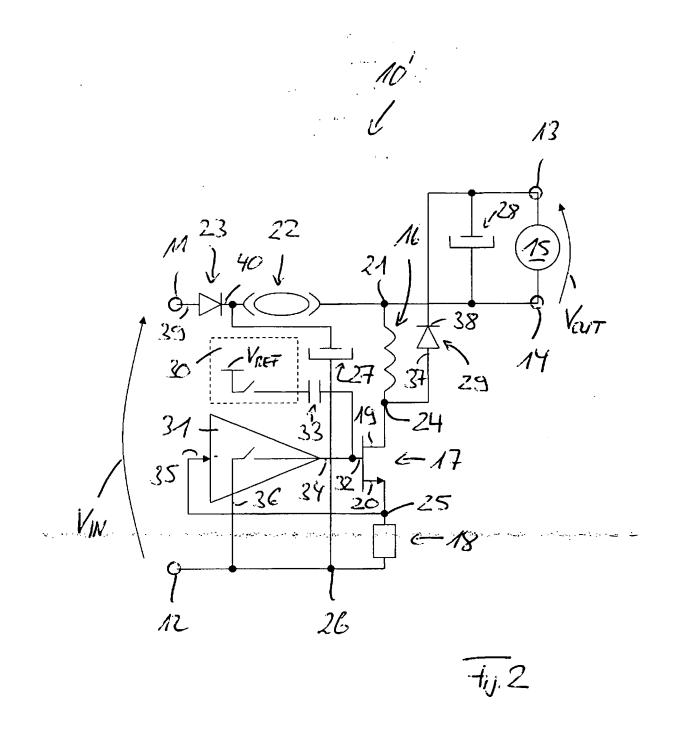
45

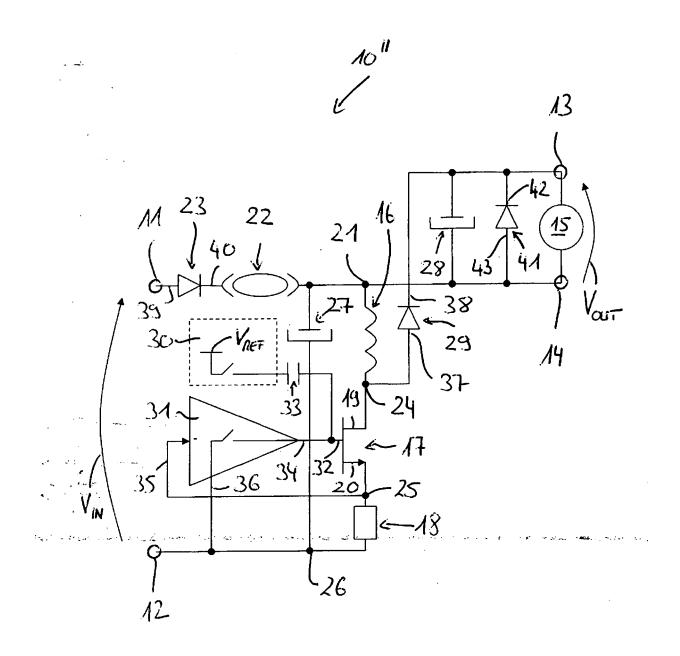
50

55

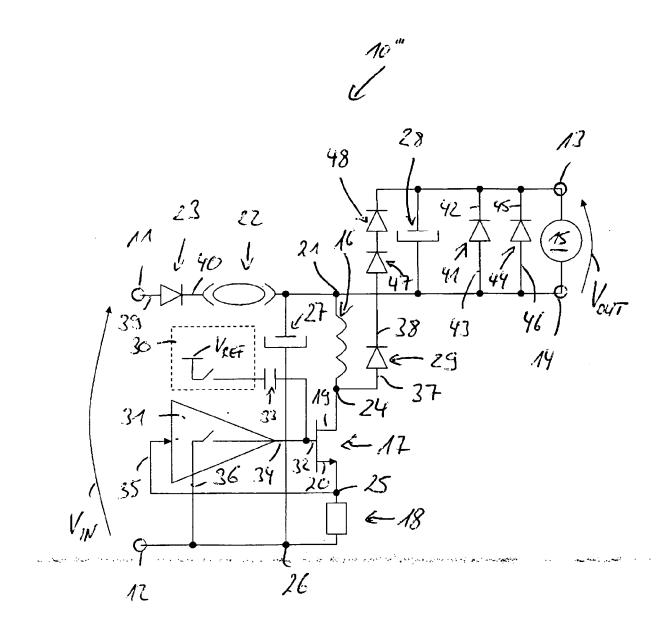
- **8.** Power driver and fail safe circuit as claimed in one of claims 1 to 7, **characterized in that** a fuse (22) is connected to said inductance coil.
- 9. Power driver and fail safe circuit as claimed in claim 8, **characterized in that** a second diode (23) is connected in series to that fuse (22), whereby the anode (39) of said diode (23) is connected to first input contact (11), and whereby the cathode (40) of said diode (23) is connected to the fuse (22).
- **10.** Power driver and fail safe circuit as claimed in claim 8 or 9, **characterized in that** the input capacitor (27) is connected with a first contact between said fuse (22) and said inductance coil (16) and with a second contact to ground so that the input capacitor (27) is connected in series to the fuse (22).
- 20 **11.** Power driver and fail safe circuit as claimed in claim 9, **characterized in that** the input capacitor (27) is connected with a first contact between said fuse (22) and said diode (23) and with a second contact to ground so that the input capacitor. (27) is connected in parallel to the fuse (22).
  - 12. Power driver and fail safe circuit as claimed in one of claims 1 to 11, **characterized in that** a third diode (41) is connected in parallel to said output capacitor (28), whereby the cathode (42) of said third diode (41) is connected to the cathode (38) of the first diode (29) and whereby the anode (43) of said third diode (41) is connected to said inductance coil (16).
  - 13. Power driver and fail safe circuit as claimed in claim 12, **characterized in that** a fourth diode (44) is connected in parallel to said output capacitor (28) and said third diode (41), whereby the cathode (45) of said fourth diode (44) is connected to the cathode (42) of the third diode (41) and whereby the anode (46) of said fourth diode (44) is connected to the anode (43) of the third diode (41).
- 14. Power driver and fail safe circuit as claimed in one of claims 1 to 13, **characterized by** a fifth diode (47) and a sixth diode (48) being connected in series to first diode (29), namely in such a way that anode of the fifth diode (47) is connected to the cathode of the first diode (29), that the anode of the sixth diode (48) is connected to the cathode of the fifth diode (47) and that the cathode of the sixth diode (48) is connected to a first output contact (13).







411.3



7,14



# **EUROPEAN SEARCH REPORT**

Application Number EP 10 00 4949

| Category                       |  | ndication, where appropriate,                                | Relevant   | CLASSIFICATION OF THE                        |
|--------------------------------|--|--|--|--|
|                                | of relevant pass   |  | to claim   | APPLICATION (IPC)                            |
| X                              | US 2005/218838 A1 (6 October 2005 (200 * paragraphs [0133] [0171] - [0174], [8,13,15,20A *   |  | 1-14   | INV.<br>H01F7/18<br>F23N5/24<br>H01H47/00    |
| A                              | 16 May 1989 (1989-6<br>* column 10, lines  | LFUSS ROBERT C [US]) 15-16) 25-37 * 16 - column 14, line 3 * | 8-14   |  |
| A                              | US 6 256 185 B1 (MA<br>3 July 2001 (2001-6<br>* column 1, lines 5<br>* column 5, lines 3   | 5-10 *   | 8-13   |  |
| A                              | US 3 943 386 A (SIM<br>ALEXANDRE) 9 March<br>* column 1, lines 5<br>* column 2, line 24<br>figure 1 *  | 1976 (1976-03-09)  | 8-11   | TECHNICAL FIELDS<br>SEARCHED (IPC)           |
| A                              | EP 1 868 214 A1 (DE 19 December 2007 (2 * paragraphs [0001] [0046]; figure 9 *   |  | 1  | H01F<br>F23N<br>H01H<br>H02H<br>F16K<br>H02M |
|                                |  |  |  |  |
|                                | The present search report has  | ·  |  |  |
|                                | Place of search  | Date of completion of the search                             | _  | Examiner                                     |
|                                | The Hague  | 19 October 2010  | les  | ske, Ekkehard                                |
| X : parti<br>Y : parti<br>docu | ATEGORY OF CITED DOCUMENTS cularly relevant if taken alone cularly relevant if combined with anot ment of the same category nological background | L : document cited fo  | ument, but publi<br>e<br>i the application<br>ir other reasons |  |

### ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 10 00 4949

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-10-2010

|    | Patent document<br>ed in search report |        | Publication date |                                  | Patent family<br>member(s)                                     |                    | Publication date   |
|----|--|--------|------------------|----------------------------------|--|--------------------|--|
| US | 2005218838                             | A1     | 06-10-2005       | NONE                             |  |                    |  |
| US | 4831313                                | Α      | 16-05-1989       | NONE                             |  |                    |  |
| US | 6256185                                | B1     | 03-07-2001       | NONE                             |  |                    |  |
| US | 3943386                                | A      | 09-03-1976       | DE<br>ES<br>FR<br>GB<br>IT<br>JP | 2430328<br>427784<br>2238393<br>1466091<br>1015629<br>50049740 | A1<br>A5<br>A<br>B | 13-02-197<br>01-08-197<br>14-02-197<br>02-03-197<br>20-05-197<br>02-05-197 |
| EP | 1868214                                | <br>A1 | 19-12-2007       | US                               | 2007285195   | A1                 | 13-12-200  |
|    |  |        |                  |                                  |  |                    |  |
|    |  |        |                  |                                  |  |                    |  |

© For more details about this annex : see Official Journal of the European Patent Office, No. 12/82