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(54) **Methods for operating a semiconductor device**

(57) A capacitorless memory device based on a multi-gate MOSFET and requiring relatively low bias voltages. By providing a sufficient body factor and inducing a V_T -feedback loop, using an accumulation layer to link threshold voltage with gate-to-body voltage, a hysteresis window (H) can be induced allowing the MOSFET to store '1' or '0' values (54, 51), and to read (within a program window PW) and hold (50) the stored values. The device operates with relatively low operating voltages such as 1.5V, high reliability e.g. 10^{16} operations, and long retention time such as ~5sec.

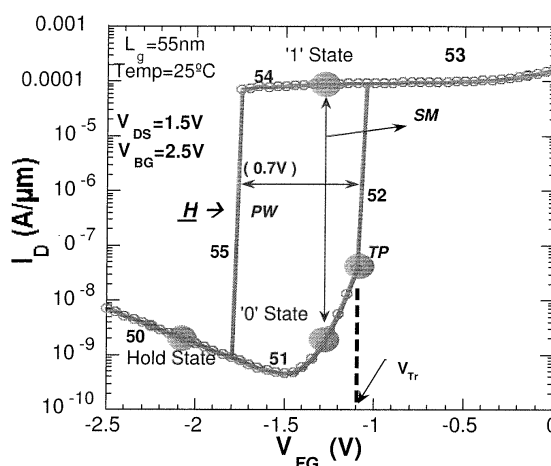


FIGURE 5A