(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 405 482 A9**

(12) **CORRECTED EUROPEAN PATENT APPLICATION**

(15) Correction information:
Corrected version no 1 (W1 A2)
Corrections, see
Claims
Description

(48) Corrigendum issued on:
25.04.2012 Bulletin 2012/17

(43) Date of publication:
11.01.2012 Bulletin 2012/02

(21) Application number: **11008150.2**

(22) Date of filing: **12.01.2006**

(51) Int Cl.:
H01L 29/861 *(2006.01)* ***H01L 29/06*** *(2006.01)*
H01L 27/06 *(2006.01)*

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

(30) Priority: **20.01.2005 US 40180**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
06718439.0 / 1 846 953

(71) Applicants:
- **Diodes, Inc.**
  Westlake Village, CA 91362 (US)
- **DII Taiwan Corporation Ltd.**
  Hsin Tien City
  T'ai pei Hsien (TW)

(72) Inventors:
- **Chang, Paul**
  Saratoga
  CA 95070 (US)
- **Chern, Geeng-chuan**
  Cupertino
  CA 95014 (US)
- **Ghosh, Prognyan**
  Oakland
  CA 94611 (US)
- **Hsueh, Wayne Y.W.**
  San Jose
  CA 95113 (US)
- **Rodov, Vladimir**
  Seattle
  Washington 98149 (US)

(74) Representative: **Beresford, Keith Denis Lewis**
Beresford & Co.
16 High Holborn
London
WC1V 6BX (GB)

Remarks:
This application was filed on 07-10-2011 as a divisional application to the application mentioned under INID code 62.

(54) **Integrated circuit including power diode**

(57) A method of fabricating a semiconductor integrated circuit including a power diode includes providing a semiconductor substrate (10) of first conductivity type, fabricating a integrated circuit such as a CMOS transistor circuit in a first region (12) of the substrate, and fabricating a power diode in a second region in the semiconductor substrate. Dielectric material is formed between the first region and the second regions thereby providing electrical isolation between the integrated circuit in the first region and the power diode in the second region. The power diode can comprise a plurality of MOS source/drain elements and associated gate elements all connected together by one electrode of the diode, and a semiconductor layer in the second region can function as another source/drain of the power diode.

EP 2 405 482 A9

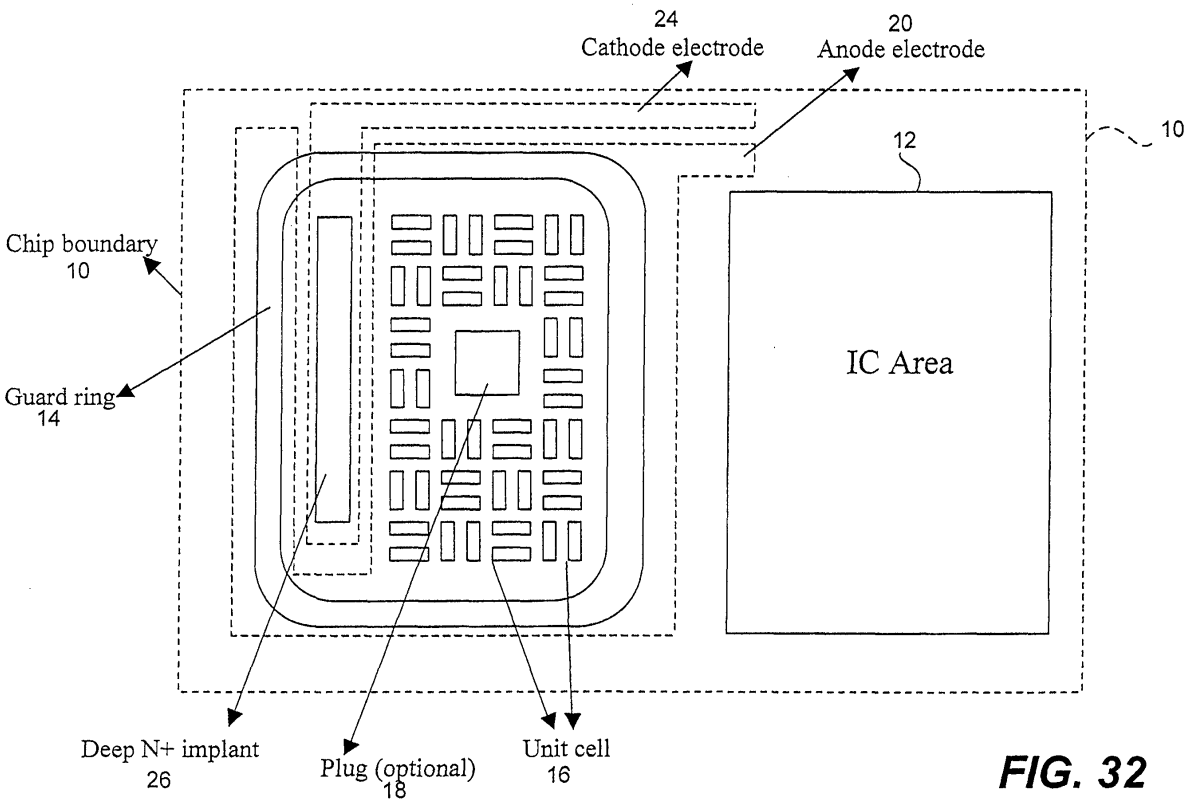
24
Cathode electrode
20
Anode electrode
10
12
Chip boundary
10
Guard ring
14
IC Area
Deep N+ implant
26
Plug (optional)
18
Unit cell
16

FIG. 32

Description

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to power semiconductor devices including power diode rectifiers, and more particularly the invention relates to a power diode fabricated in a semiconductor integrated circuit and the method of fabricating the same.

[0002] The above referenced patents and pending patent application disclose semiconductor power diodes and rectifiers including one or more MOSFET structures in which a common electrode contacts gates and source/drain regions in one surface of a semiconductor body. The diodes have low on resistance, fast recovery time, and a very low forward voltage drop. The diodes can function as a discrete device and in an integrated circuit, hi one embodiment, one contact to the diode is the common electrode contacting the gates and source/drain regions in or on one surface of the semiconductor structure. Another contact can be placed on an opposing of the semiconductor structure or otherwise electrically contacting second source/drain regions in the semiconductor structure.

[0003] When fabricated as a component in an integrated circuit, the diode structure must be electrically isolated from the integrated circuit structure with power buses connecting electrodes of the diode to power contacts of the integrated circuit. The diode can the be effectively operated as a power source for the integrated circuit without adversely effecting circuit operation.

[0004] The present invention is directed to a process and resulting structure in which a power diode comprises an integral part of an integrated circuit.

SUMMARY OF THE INVENTION

[0005] In accordance with the invention, one or more diode regions are formed in a semiconductor substrate with the diode regions having a dopant conductivity opposite to the dopant conductivity of the substrate in which an integrated circuit is to be formed. For example, N-/N+ dopant can be implanted in a substrate having P-/P+ dopant. Alternatively, a trench can be formed in the semiconductor substrate and then refilled epitaxially with doped N-/N+ semiconductor material.

[0006] A diode region is electrically isolated from the integrated circuit region by shallow trench oxide isolation or by dielectric spacers on sidewalls of an etched trench in the substrate which is subsequently refilled by epitaxial semiconductor growth of conductivity opposite to the substrate.

[0007] A plurality of source/drain and gate regions are formed in a surface of the device region using the technology disclosed in the above commonly assigned patents and application. An internal source/drain region, which is connected to the surface source/drain region by gate controlled channels, is contacted from the surface of the semiconductor substrate through an implanted contact channel which is electrically isolated from the plurality of source/drain regions on the surface by shallow trench isolation, for example.

[0008] The resulting diode in the integrated circuit has the feature and performance of diodes described in the commonly owned patents, supra, with improved electrical isolation and electrical access from the substrate surface.

[0009] The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

Figs. 1-24 are section views illustrating steps in fabricating an integrated circuit including a power diode in accordance with embodiments of the invention.

Figs. 25-26 are section views illustrating the fabrication of an isolated diode region in accordance with one embodiment of the invention.

Figs . 27-31 are section views illustrating alternative power diode structures.

Figs 32-34 are top views illustrating integrated circuits including power diodes in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF ILLUSTRATED EMBODIMENTS

[0011] Power sources for integrated circuits require diode rectifiers which can be separate from the integrated circuit but which advantageously are incorporated in the integrated circuit. Figs. 32-34 are top views illustrating integrated circuits including power diodes in accordance with embodiments of the present invention. Typically the integrated circuits are fabricated in a silicon substrate 10 with the integrated circuit fabricated in a first portion 12 of substrate 10 and a power diode fabricated within a guard ring 14 in a second portion of substrate 10. Guard ring 14 and the diode structures fabricated therein are electrically isolated from integrated circuit 12 as will be described further herein.

[0012] The diode within guard ring 14 comprises a plurality of unit cells 16, each of which includes a gate electrode and one or more surface oriented source/drain regions which are connected to an internal source/drain region though a gate controlled channel. An optional doped plug (P) 18 can be provided in the diode region as a bypass diode in parallel with unit cells 16. Anode 20 comprises common metallization to the gates and surface oriented source/drain regions of the unit cells 16, and a cathode electrode 24 contacts an internal source/drain region common to all unit cells through a deep N+ implant 26. rn accordance with the invention, implant 26

is electrically isolated from the gates and surface source/drain regions of the unit cells, and the diode structure within guard ring 14 is dielectrically isolated from integrated circuit area 12.

[0013] As described in the referenced patents, the unit cells can take many forms including short rectangular structures as shown in Fig. 32, hexagonal structures as shown in Fig. 33, and elongated stripes as shown in Fig. 34.

[0014] Consider now Figs. 1-24 which are section views illustrating steps in fabricating an integrated circuit including a power diode in accordance with embodiments of the invention. The starting material is a silicon substrate including a P+ doped layer 30 and a P- doped layer 32 which can be epitaxially grown on layer 30. A silicon oxide layer 34 is grown on a surface of layer 32, and then a photoresist pattern 36 is formed on the surface of oxide 34 to define the power diode area. If more than one power diode is to be fabricated, multiple photoresist openings would be defined. In Fig. 2 a conventional anisotropic etch is performed to form a trench in silicon layer 32. Thereafter, as shown in Fig. 3, the photoresist is removed and silicon oxide or silicon nitride spacers 38 are formed on sidewalls of the silicon trench by vapor deposition followed by anisotropic etch to remove material from the bottom of the trench. After surface treatment to facilitate epitaxial growth, selective epitaxial deposition is employed to form N+ layer 40 and N- layer 42 which fill the trench. The oxide layer 34 functions as a mask for the selective epitaxial deposition.

[0015] In Fig. 4 oxide 34 is removed by etching, and then a plurality of trenches are formed in the surface by anisotropic etch and then the trench surfaces are oxidized to form conventional shallow trench isolation (STI) 44. The surface of the structure is then patterned with photoresist 46 as shown in Fig. 5 to define a deep N+ implant 48 between two oxide isolation areas 44. Either phosphorus or arsenic can be used as the implanted N+ dopant.

[0016] In Fig. 6 photoresist 46 is stripped and a photoresist pattern 50 is formed over the surface to define a P guard ring and optionally a P plug (not shown) with boron and BF2 implant forming guard ring 14.

[0017] Following formation of guard ring 14, photoresist 50 is removed and the surface is again selectively masked for ion implantation in forming P wells 52 and N wells 54 for CMOS transistors in the integrated circuit, as shown in Fig. 7. Thereafter, gate oxide 56 is grown on the surface of the structure as shown in Fig. 8. If the gate oxide thickness of the power diode is different from that of the integrated circuit transistors in P well 52 and N well 54, then the gate oxide growth requires two different time periods with suitable masking to limit growth of the oxide over the integrated circuit wells. In Fig. 9 a first layer of polysilicon (30-250 nm) is deposited. If the polysilicon layer over the diode is different from that over the integrated circuit, photoresist masking as shown in Fig. 9 is employed to remove the polysilicon from over the diode by polysilicon etch as shown in Fig. 10, and then a second layer 58' of polysilicon (30-150 nm) is the deposited on the surface of the diode region and over the first polysilicon layer 58 over the integrated circuit region. (Fig. 11) Again, if the polysilicon thickness over the super diode is the same as the polysilicon thickness over the integrated circuit transistors, the photoresist masking, etching and second polysilicon deposition steps are not necessary.

[0018] Thereafter, a photoresist pattern is formed to cover the integrated circuit area as shown in Fig. 12, and then arsenic is implanted (30-150 nm) into the surface of the diode region. This arsenic implant facilitates the later ohmic contact of a surface electrode to the surface of the diode. In Fig. 13, the photoresist of Fig. 12 is removed and a layer 60 of CVD silicon oxide is deposited with thickness on the order of 100-400 nm. A photoresist pattern 62 is then employed to define the MOS transistor unit cells for the power diode and to cover the integrated circuit area. It will be appreciated that mask 62 is used in forming a plurality of unit cells.

[0019] Isotropic etch is then applied as shown in Fig. 14 to variably etch oxide 60 under photoresist mask 62 and remove oxide 60 elsewhere over the diode region. It will be appreciated that the oxide etch stops at polysilicon layer 58. Thereafter, using the same mask, polysilicon layer 58 is anisotropically etched and removed from silicon layer 56 over the diode region. A first boron implant (dose = 1.5~5.5E12/cm2, energy 40-80KeV) forms P doped regions 64 aligned with gate oxide 58 in the diode structure. This boron implant can also be performed before the anisotropic polysilicon etch.

[0020] Thereafter, oxide 56 is removed from the surface of the diode region except for the gate structure as shown in Fig. 15. Arsenic is then implanted (1.0~5.0E13, energy 40-60KeV) followed by rapid thermal annealing for subsequently forming N doped source/drain regions 66 in P doped regions 64. The rapid thermal annealing drives the implanted arsenic under gate oxide 56.

[0021] The exposed silicon surface of the device region is then anisotropically etched to remove 50-200 nm of silicon, as shown in Fig. 16, and thereafter a BF2 implant (dose = 1.0~5. OEI 5; energy 10-60KeV) is implanted and annealed to activate the BF2 and increase the P type doping (e.g. boron) in the P doped surface regions. As shown in Fig. 17, photoresist is then removed and a second boron implant (dose = 1.0~2.5E12/cm2, energy 20-60KeV) is employed to created lateral graded P-type pockets 68 for the channels of the power diode cells as further described in U.S. Patent No. 6,624,030, supra.

[0022] The integrated circuit is then fabricated as shown in Figs. 18-21. A photoresist pattern is first formed to cover the diode area and expose only the integrated circuit area as shown in Fig. 18, and then oxide layer 60 is removed in the integrated circuit area. In Fig. 19, another photoresist pattern is formed to cover the super diode area and define the MOS transistor gate areas for the integrated circuit. Exposed polysilicon layer is re-

moved by anisotropic polysilicon etch which forms the gate structures of transistors in P well 52 and N well 54. The photoresist is then removed as shown in Fig. 20 and another photoresist pattern is used to cover the super diode area and the P channel MOS transistor (e.g. N well) areas, and then phosphorus or arsenic is implanted to form N channel source and drain and to dope the N channel transistor polysilicon gate as shown in Fig. 20.

[0023] The photoresist is then removed as shown in Fig. 21 and another photoresist pattern covers the power diode area and the N channel MOS transistor (e.g. P well) areas. Boron and/or BF2 is then implanted to form P channel source and drain regions and to dope the P channel transistor polysilicon gate as shown in Fig. 21. The photoresist is then stripped as shown in Fig. 22, and a layer 70 of inter-dielectric such as CVD silicon oxide, PSG or BPSB is deposited on the surface of the structure. Oxide layer 70 is then photoresist masked to define contact areas followed by etch of the exposed oxide layer to open contact areas for the power diode and the integrated circuit, hi Fig. 24 the device is completed by removing the photoresist and forming metal inter-connects by depositing a layer of metal and using conventional photo masking and etching to form a metal anode contact 72, metal cathode contact 74, a metal anode contact 76 to surface source/drain 66 and gate 58, and source and drain contacts 78 to the CMOS transistors in P well 52 and N well 54.

[0024] hi the final product illustrated in Fig. 24, the oxide or nitride spacers 38 are employed to electrically isolate the power diode from the integrated circuit. Fig. 25-26 are section views illustrating the fabrication of the isolated diode region in accordance with another embodiment of the invention. As shown in Fig. 25 the starting P-/P+ substrate has shallow trench isolation regions 80 formed to provide isolation areas without the forming of a trench as shown in Fig. 2, above. As noted in the description of Fig. 4, conventional local oxidation can be used rather than the conventional shallow trench isolation method. Thereafter as shown in Fig. 26, a photoresist pattern is employed to define the super diode areas with phosphorus and/or arsenic multiple implants with different energies and doses to form the N-/N+ well for the power diode. Again, if more than one power diode is to be fabricated, multiple photoresist openings would be defined.

[0025] The final product using shallow trench isolation is shown in Fig. 27 which is similar to the final structure shown in Fig. 24 except for the oxide or nitride spacers 38 in Fig. 24 being replaced by the STI oxide 80. Note that all process steps as shown in Figs. 5-24 are employed in forming the final product of Fig. 27.

[0026] Fig. 28 illustrates a section view of another structure in accordance with the invention which is similar to the device of Fig. 24 except for the provision of a super junction region 84 between N+ layer 40 and N- layer 42 of the power diode. Provision of the super junction is described in U.S. Patent No. 6,743,703, supra.

[0027] In another embodiment of the invention, reduced reverse bias leakage current in the power diode can be provided by a shallow boron implant under the gate of the metal anode as shown at 86 in Fig. 29. The use of a lightly doped boron implant under all of the gate structure for reducing reverse bias leakage current is described in co-pending application serial number 10/159,558, supra.

[0028] Enhanced pinch off for current limiting can be provided in the power diode by providing a P doping profile 88 in the body so tailored with ion implantation that a depletion region pinches off to limit current, as described in U.S. Patent No. 6,515,330, supra. This is shown in Fig. 30.

[0029] In another embodiment of the invention, the channel regions need not be tapered as shown at 68 in Fig. 24, but can have an essentially constant thickness as shown at 68' in the finished product in Fig. 31. This structure and the method of fabrication is described in U.S. Patent No. 6,420,225, supra.

[0030] There have been described several embodiments of an integrated circuit including one or more super power diodes in accordance with the invention. However, while the invention has been described with reference to specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

[0031] The content of the following clauses is included as part of the present disclosure:

1. A semiconductor integrated circuit comprising:

   a) a semiconductor substrate having material of a first conductivity type,

   b) a first region in said substrate in which an integrated circuit is fabricated,

   c) a second region in said substrate having material of a second conductivity type in which a power diode is fabricated, and

   d) dielectric material between the first region and the second region providing electrical isolation between the first region and the second region.

2. The integrated circuit of clause 1 where the dielectric material comprises silicon oxide formed in a surface of the semiconductor substrate, and the second region includes implanted dopant of a second conductivity type.

3. The integrated circuit of clause 2 wherein the dielectric material comprises silicon oxide.

4. The integrated circuit as defined by clause 1 wherein the second region includes epitaxial semiconductor material grown in a trench in one surface

of the substrate, and the dielectric material comprises spacers formed on sidewalls of the trench.

5. The integrated circuit as defined by clause 1 wherein the power diode includes a conductive layer on a surface of the substrate functioning as a first electrode, and a conductive via extending from the surface into the substrate and contacting semiconductor material of the second conductivity type which functions as a second electrode.

6. The integrated circuit as defined by clause 5 wherein the power diode comprises a plurality of MOS source/drain elements and associated gate elements all connected together by the first electrode, a semiconductor layer of a second conductivity type in the second region and in which the plurality of MOS source/drain elements are fabricated, the semiconductor layer being contacted by the second electrode.

7. The integrated circuit as defined by clause 6 wherein each MOS source/drain element is electrically connectable to the semiconductor layer through a channel controlled by a gate element.

8. The integrated circuit as defined by clause 7 wherein each channel is laterally graded under a gate element with a sloped P-N junction separating the channel region from the semiconductor layer.

9. The integrated circuit as defined by clause 8 wherein the P-N junction underlies all of the gate element to provide reduced reverse bias leakage current.

10. The integrated circuit as defined by clause 5 wherein the dielectric material comprises silicon oxide formed in a surface of the semiconductor substrate, and the second region includes implanted dopant of a second conductivity type.

11. The integrated circuit as defined by clause 10 wherein the dielectric material comprises silicon oxide.

12. The integrated circuit as defined by clause 5 wherein the second region includes epitaxial semiconductor material grown in a trench in surface of the substrate, and the dielectric material comprises spacers formed on side walls of the trench.

13. A method of fabricating an integrated circuit including a power diode in a semiconductor body comprising the steps of:

a) providing a semiconductor substrate including a surface layer of first conductivity type.

b) forming a dielectric material in a surface of the semiconductor substrate around a first region in which a power diode is to be fabricated and separated from a second region in which an integrated circuit is to be fabricated,

c) forming semiconductor material of a second conductivity type in the first region,

d) fabricating an integrated circuit in the second region,

e) fabricating a plurality of MOS source/drain elements and associated gate elements in a surface of the device region and in the semiconductor material of second conductivity type,

f) forming a first diode electrode contacting the plurality of MOS source/drain elements and associated gate elements,

g) forming a conductive via from the surface of the device region to the semiconductor material of second conductivity type as a second diode electrode.

14. The method of clause 13 wherein step b) includes forming a trench in the first region, and forming dielectric side wall spacers on the trench, and step c) includes epitaxially growing semiconductor material of second conductivity type in the trench.

15. The method of clause 13 wherein step b) includes forming dielectric material in a surface of the semiconductor substrate, and step c) includes implanting dopant of second conductivity type into the first region.

16. The method as defined by clause 13 and further including the step of:

h) forming a doped guard ring of first conductivity type in the first region abutting the dielectric material.

17. The method as defined by clause 16 and further including the step of:

i) forming a plug of first conductivity type in the first region extending into the semiconductor material of second type.

18. The method as defined by clause 13 wherein step g) includes forming dielectric spacers between the conductive via and the plurality of MOS source/drain elements.

19. The method as defined by clause 13 wherein step d) includes forming a plurality of P wells and a plurality of N wells for CMOS transistors.

Claims

1. A method of fabricating an integrated circuit integrating a power diode in a semiconductor body comprising the steps of:

forming a device region in a surface layer of a semiconductor substrate, wherein the device re-

gion is defined by walls of silicon and a substrate layer adjacent to the semiconductor substrate, the substrate layer being of a conductivity different from a conductivity type of the surface layer;
forming a dielectric material around the device region;
forming an integrated circuit (IC) region that is insulated from the device region;
fabricating an IC in the IC region, wherein the IC includes a transistor;
fabricating a plurality of MOS source/drain elements and associated gate elements in the device region;
forming a first diode electrode in the device region contacting the plurality of MOS source/drain elements and associated gate elements; and
forming a conductive via from the surface of the device region to semiconductor material of the same type as the substrate layer as a second diode electrode.

2. The method of claim 1, further comprising;
forming a trench in the device region, and forming dielectric side wall spacers on side walls of the trench;
epitaxially growing semiconductor material in the trench that is the same conductivity type as the substrate layer.

3. The method of claim 1, further comprising implanting dopant into the device region, wherein the dopant is the same conductivity type as the substrate layer.

4. The method of claim 1, further comprising forming a doped guard ring in the device region that is the same conductivity type as the surface layer, wherein the guard ring further forms protection for devices in the device region, the device region abuts the dielectric material and wherein the device region is isolated by the dielectric material.

5. The method of claim 4 further comprising:

forming a plug in the device region;
forming dielectric spacers between the conductive via and the plurality of MOS source/drain elements; and
forming a plurality of P wells and a plurality of N wells for CMOS transistors.

6. A semiconductor integrated circuit comprising:

a semiconductor substrate having a device region having semiconductor material of a conductivity type different from a conductivity type of the semiconductor substrate, a power diode being fabricated in the device region, wherein the device region is defined by vertical walls of silicon, and a substrate layer adjacent to the semiconductor substrate;
the semiconductor region further having an integrated circuit (IC) region separated from the device region;
dielectric material between the device region and the IC region providing electrical isolation between the device region and the IC region, wherein the device region includes epitaxial semiconductor material grown in a trench in one surface of the substrate, and the dielectric material comprises spacers formed on sidewalls of the trench; and
wherein the power diode includes a conductive layer on a surface of the substrate functioning as a first electrode, and a conductive via extending from the surface into the substrate and contacting semiconductor material of type different from the conductivity type of the semiconductor substrate which functions as a second electrode.

7. The integrated circuit of claim 6 wherein the dielectric material comprises silicon oxide formed in a surface of the semiconductor substrate, and the device region includes implanted dopant.

8. The integrated circuit of claim 8 wherein the dielectric material comprises silicon nitride formed in a surface of the semiconductor substrate.

9. The integrated circuit of claim 6 wherein the power diode comprises a plurality of MOS source/drain elements and associated gate elements all coupled by the first electrode, a semiconductor layer of the type different from the conductivity type of the semiconductor substrate in the second region and in which the plurality of MOS source/drain elements are fabricated, the semiconductor layer being contacted by the second electrode.

10. The integrated circuit of claim 9 wherein each MOS source/drain element is electrically coupleable to the semiconductor layer through a channel controlled by a gate element.

11. The integrated circuit of claim 10 wherein each channel is laterally graded under a gate element with a P-N junction separating the channel region from the semiconductor layer.

12. The integrated circuit of claim 11 wherein the P-N junction underlies all of the gate elements to provide reduced reverse bias leakage current.

13. The integrated circuit of claim 6 wherein the device region includes epitaxial semiconductor material

grown in a trench in a surface of the substrate, and the dielectric material comprises spacers formed on side walls of the trench.

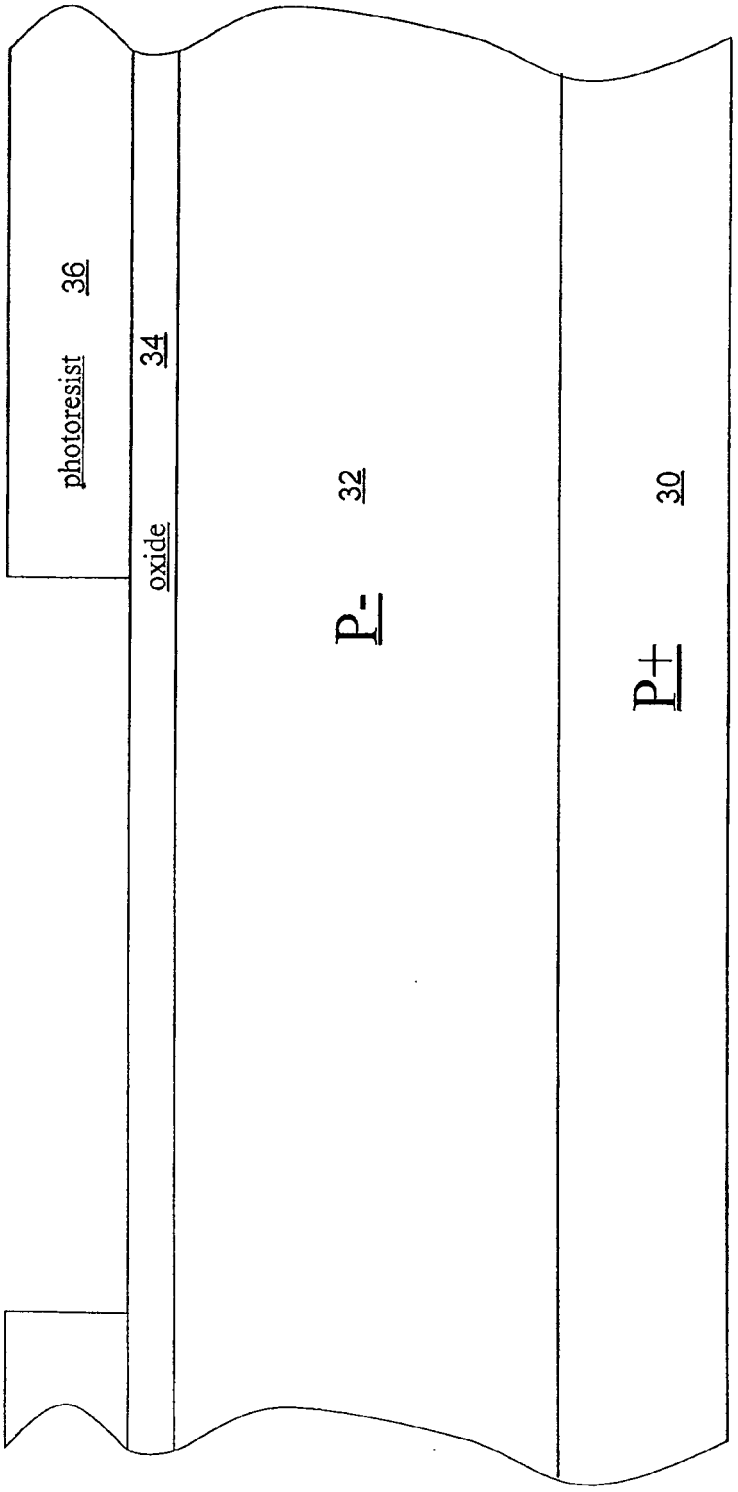

FIG. 1

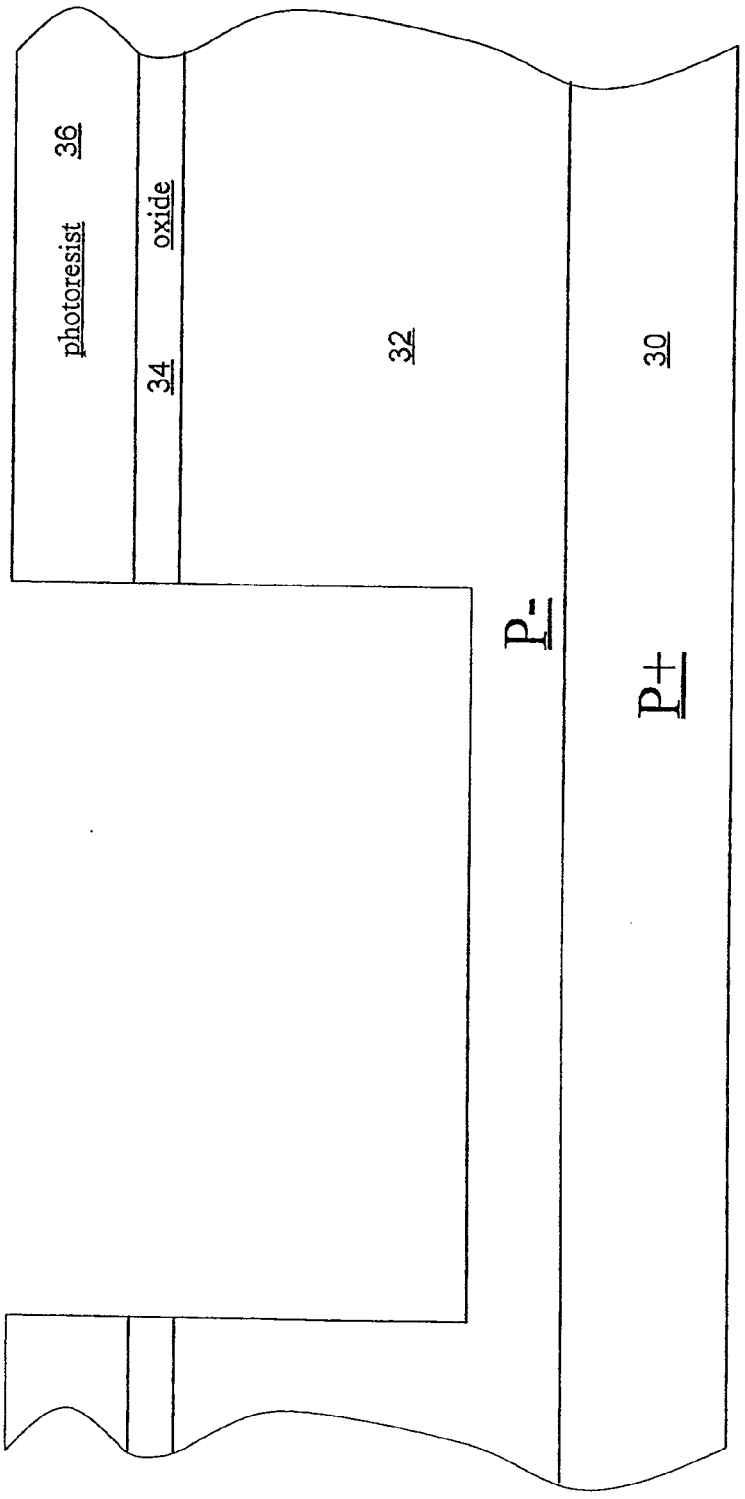

FIG. 2

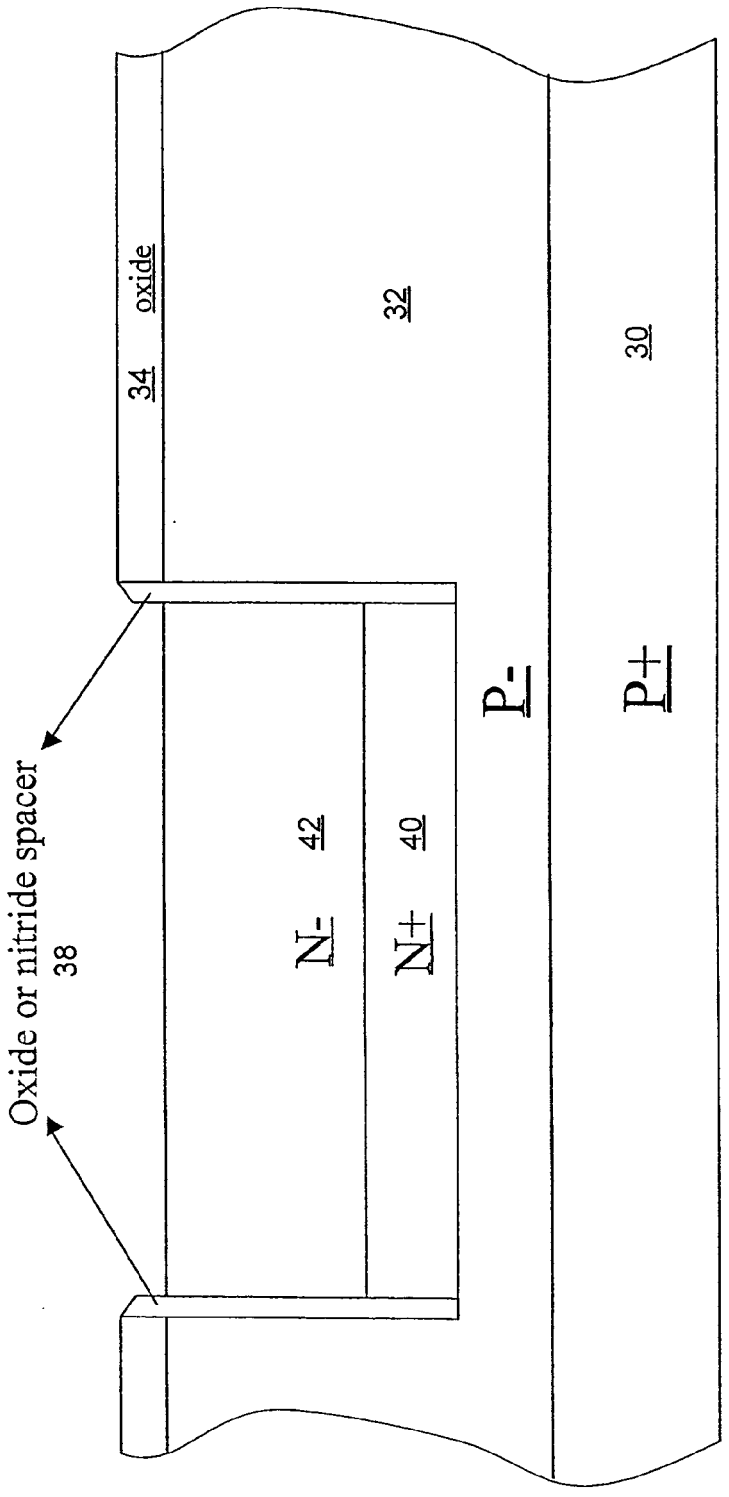

FIG. 3

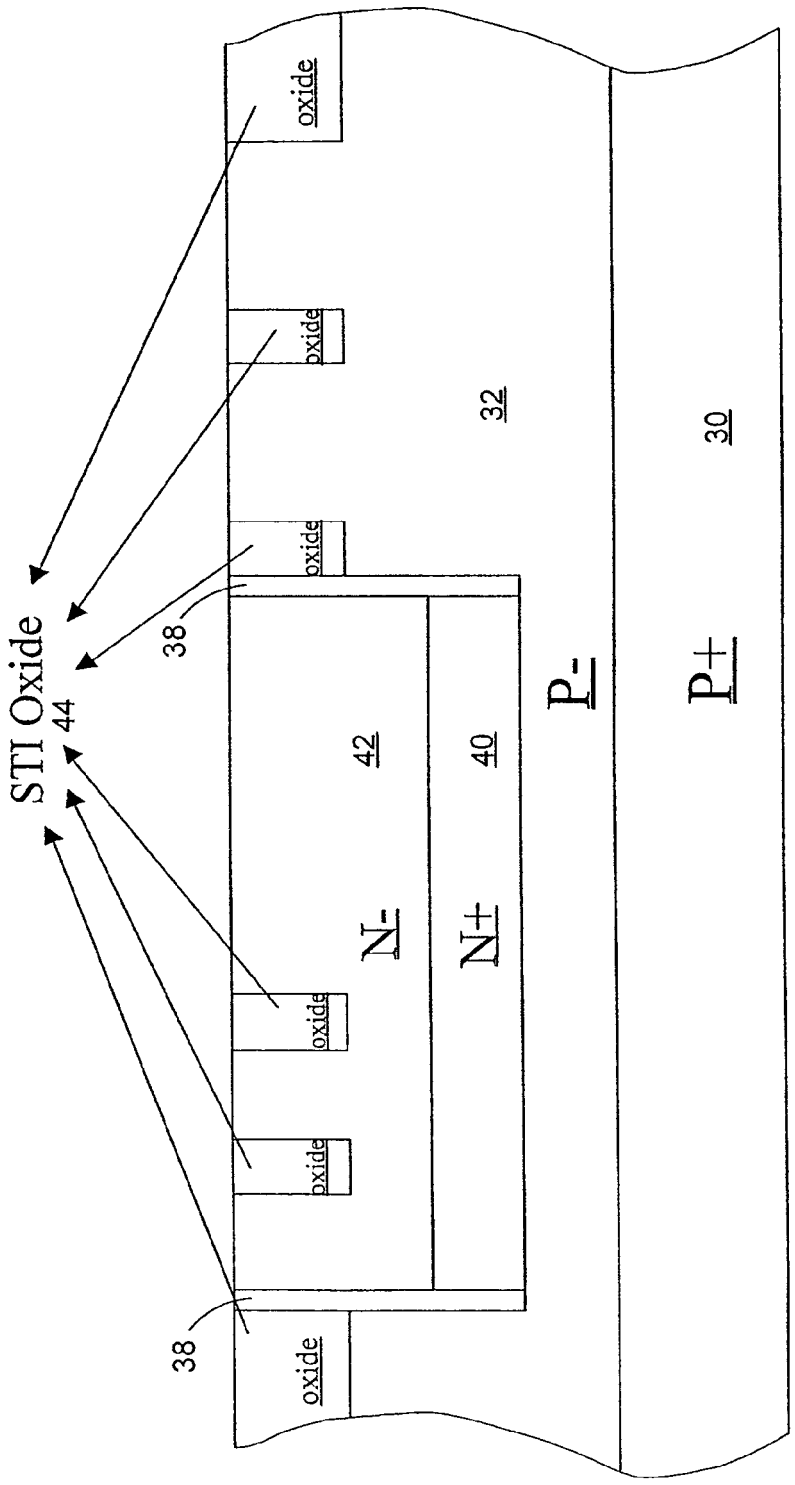
STI Oxide
44
oxide
oxide
oxide
oxide
oxide
oxide
38
38
32
30
42
40
N-
N+
P-
P+

FIG. 4

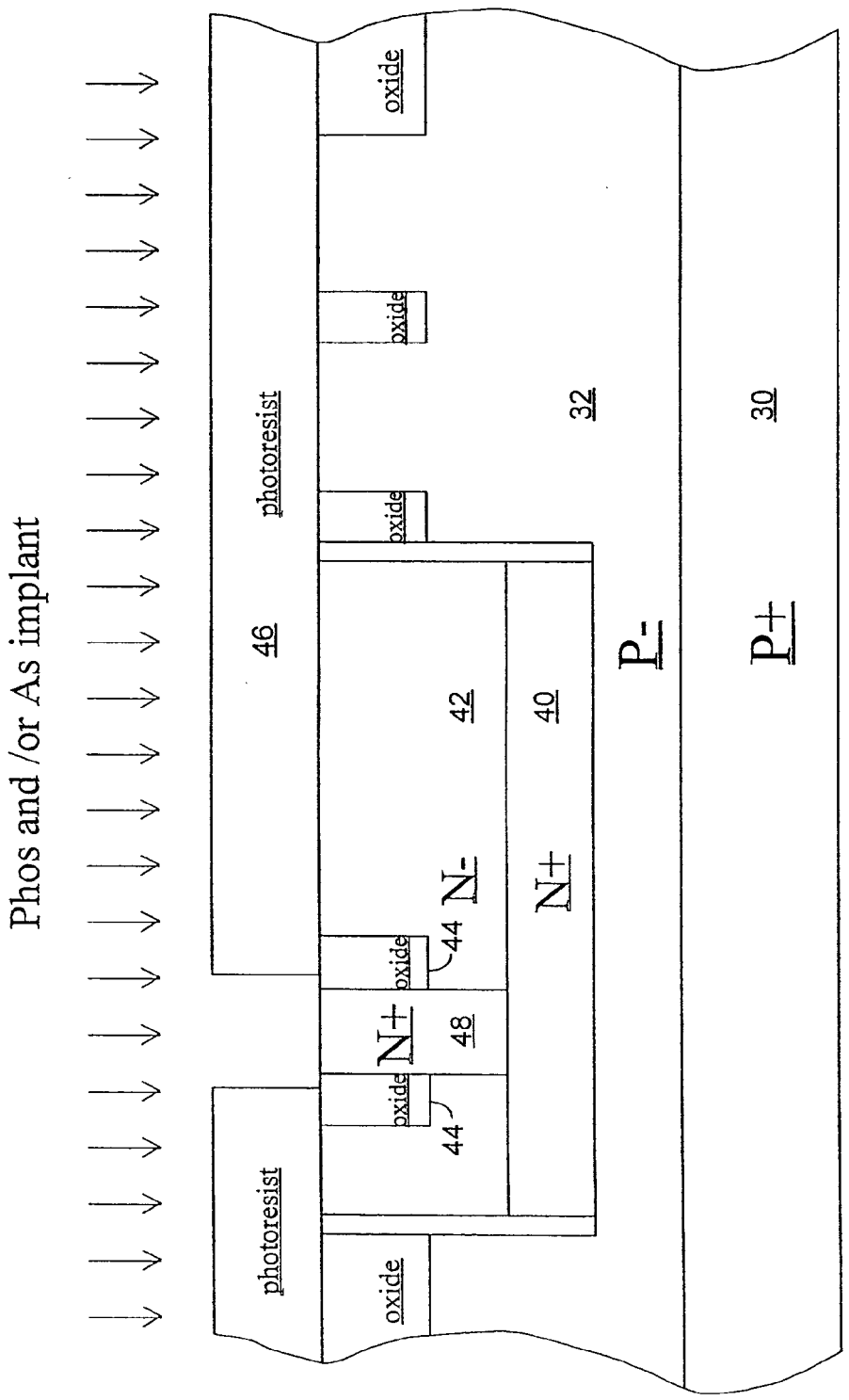
Phos and /or As implant
photoresist
oxide
oxide
oxide
oxide
oxide
photoresist
46
32
30
P-
P+
42
40
N-
N+
44
48
N+
44

FIG. 5

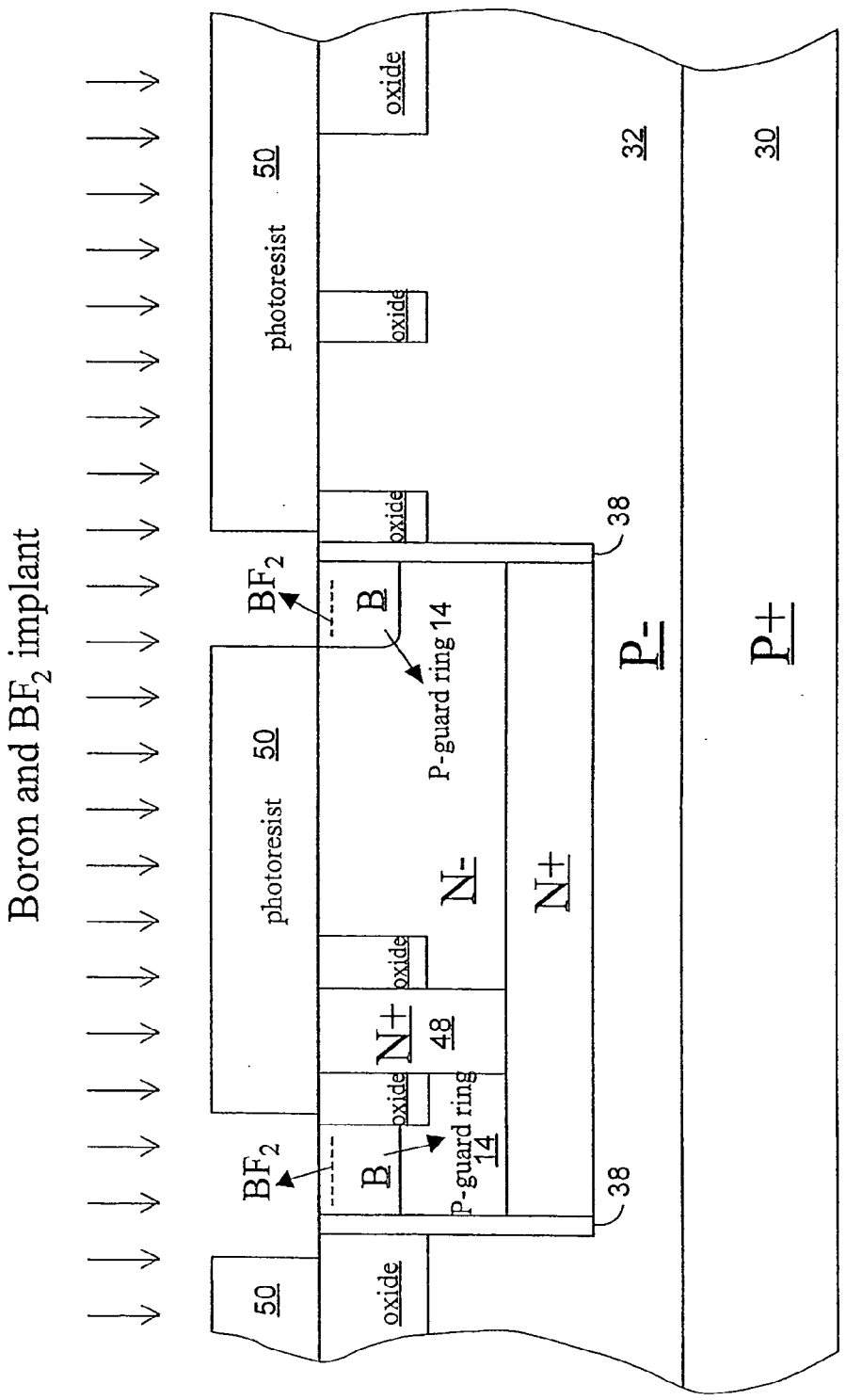
Boron and BF_2 implant
50
oxide
photoresist
50
oxide
oxide
oxide
32
30
38
BF_2
B
P-guard ring 14
P-
P+
photoresist
50
N-
N+
oxide
N+
48
oxide
BF_2
B
P-guard ring
14
38
50
oxide

FIG. 6

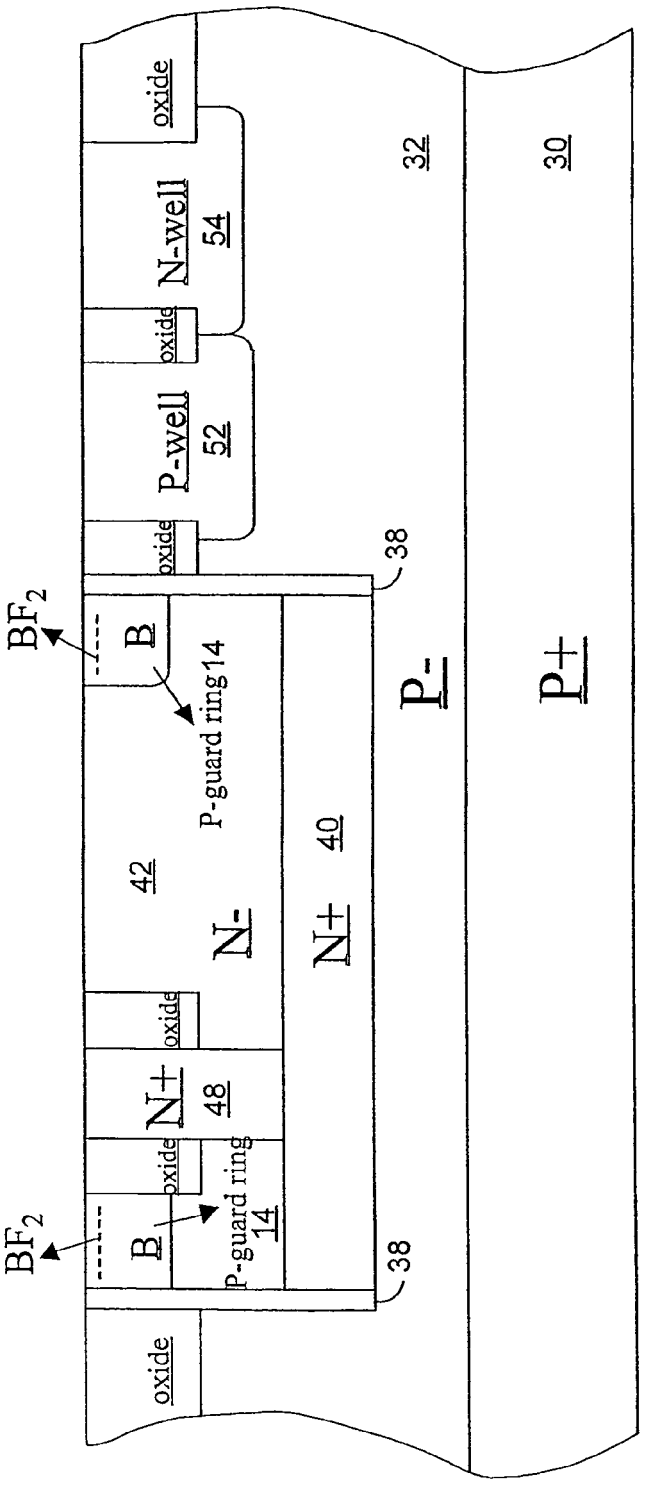
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
BF2
B
P-guard ring14
42
N-
N+
40
P-
P+
oxide
N+
48
oxide
BF2
B
P-guard ring
14
38
oxide

FIG. 7

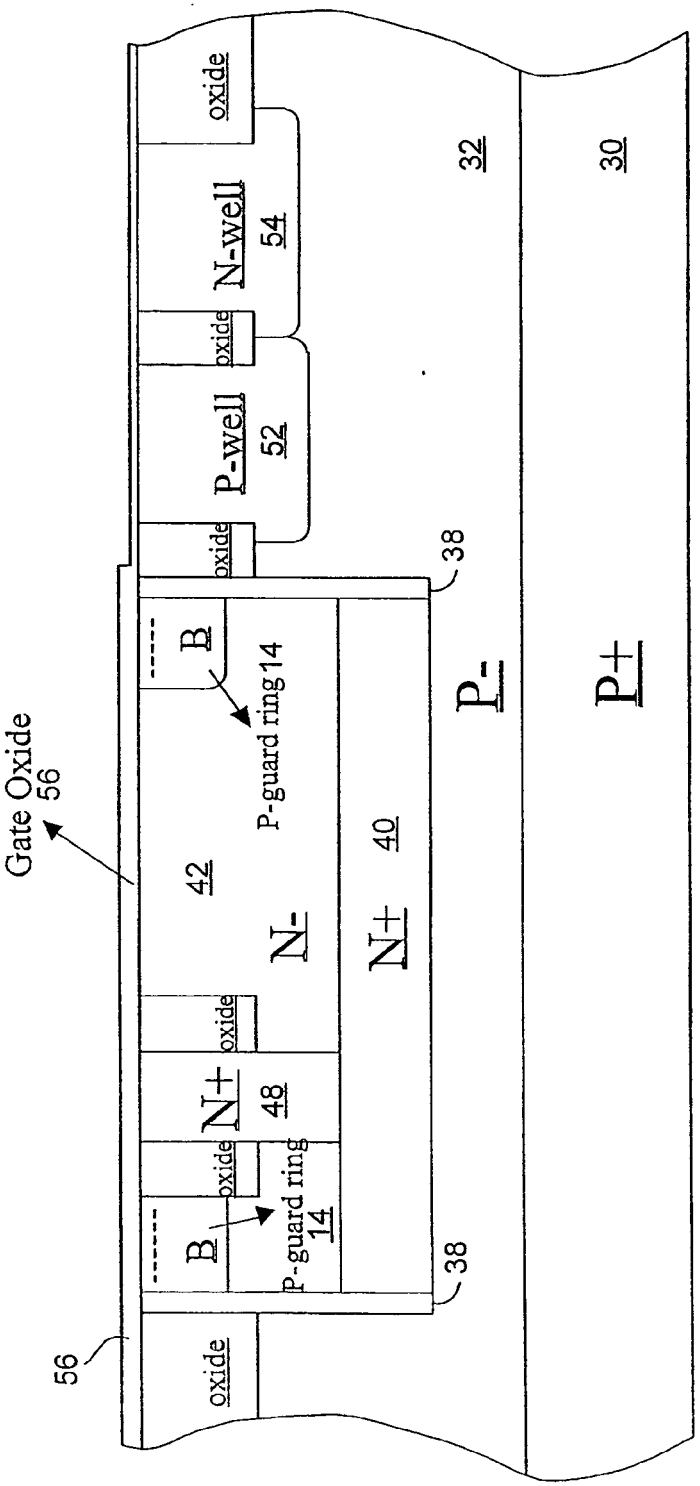
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
B
P-guard ring 14
Gate Oxide
56
42
N-
40
N+
P-
P+
oxide
N+
48
oxide
B
P-guard ring
14
38
56
oxide

FIG. 8

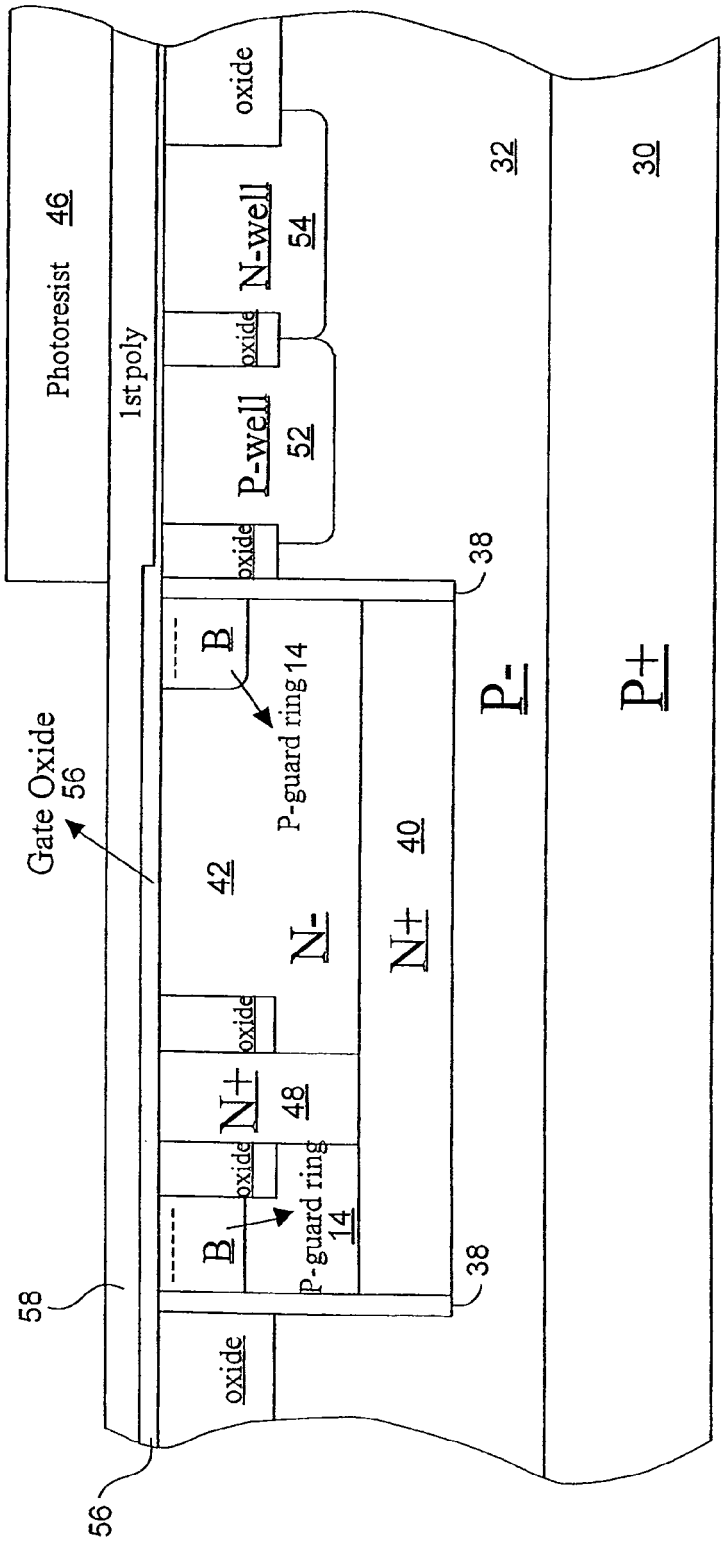
Photoresist 46
1st poly
oxide
N-well 54
oxide
P-well 52
oxide
32
30
38
B
P-guard ring 14
Gate Oxide 56
42
N-
N+ 40
P-
P+
oxide
N+ 48
oxide
B
P-guard ring 14
38
58
oxide
56

FIG. 9

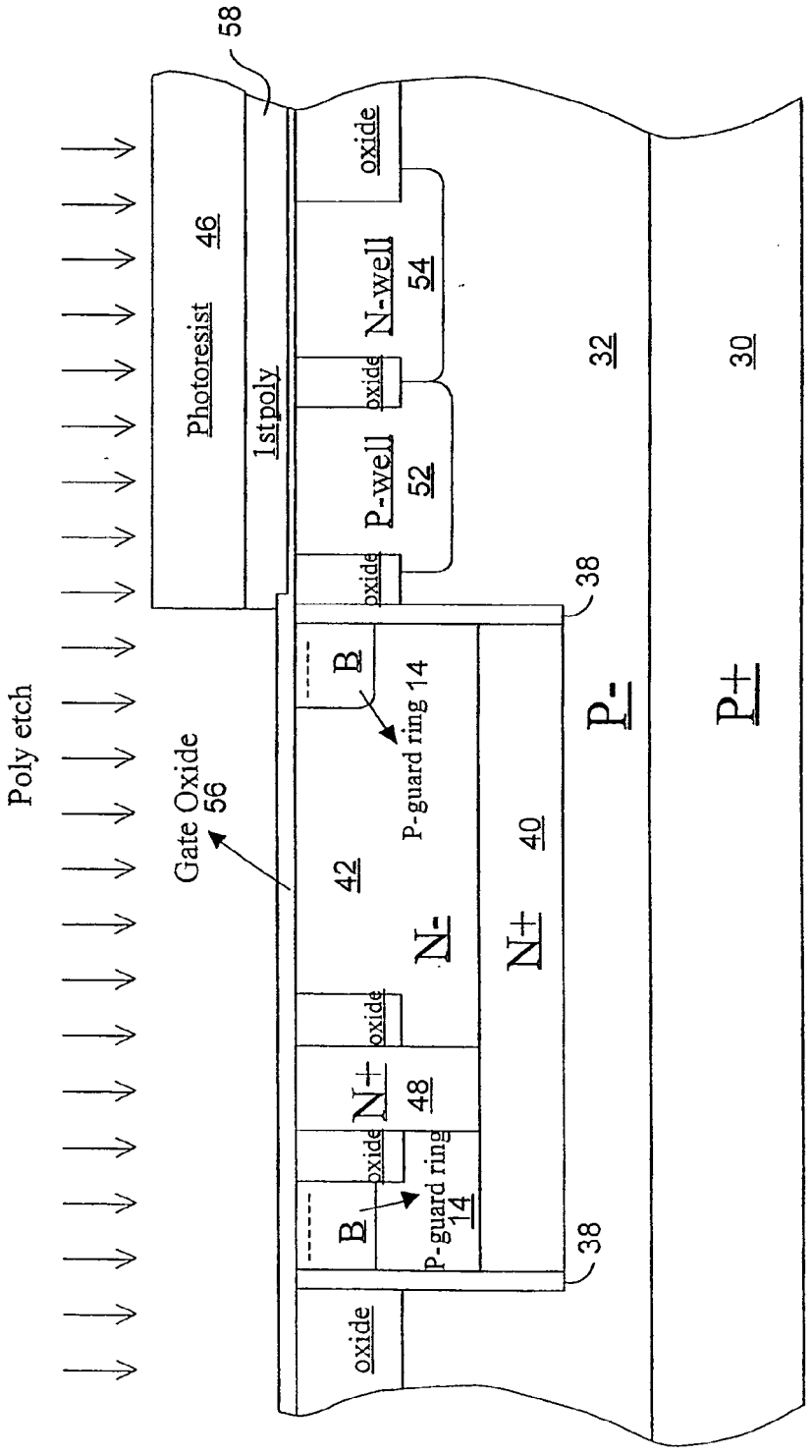
Poly etch
Gate Oxide
56
58
Photoresist
46
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
38
B
P-guard ring 14
42
N-
40
N+
P-
32
P+
30
oxide
N+
48
oxide
B
P-guard ring
14
38
oxide

FIG. 10

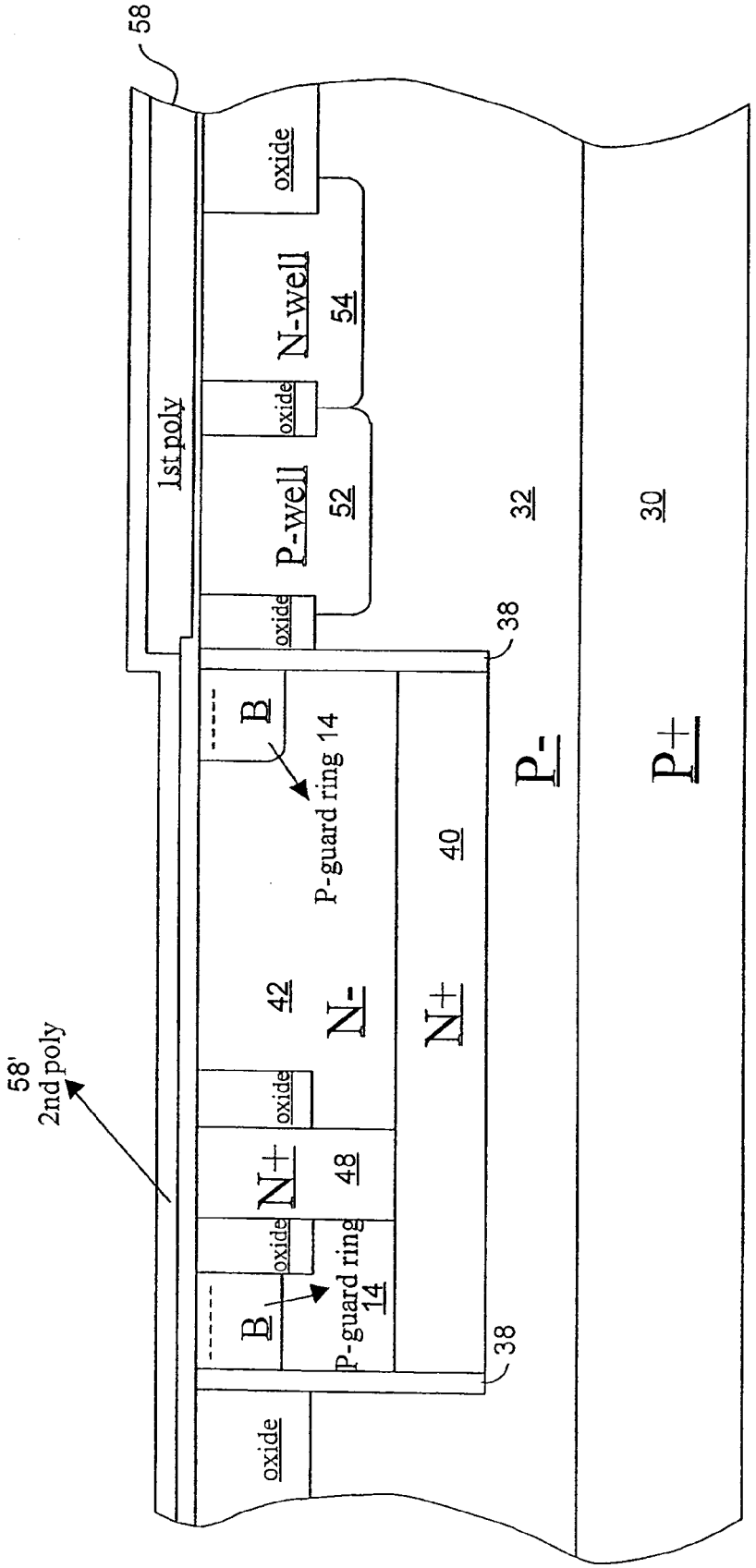
58
oxide
N-well
54
1st poly
oxide
P-well
52
oxide
38
B
P-guard ring 14
P-
32
30
P+
40
42
N-
N+
58'
2nd poly
oxide
N+
48
oxide
B
P-guard ring
14
38
oxide

FIG. 11

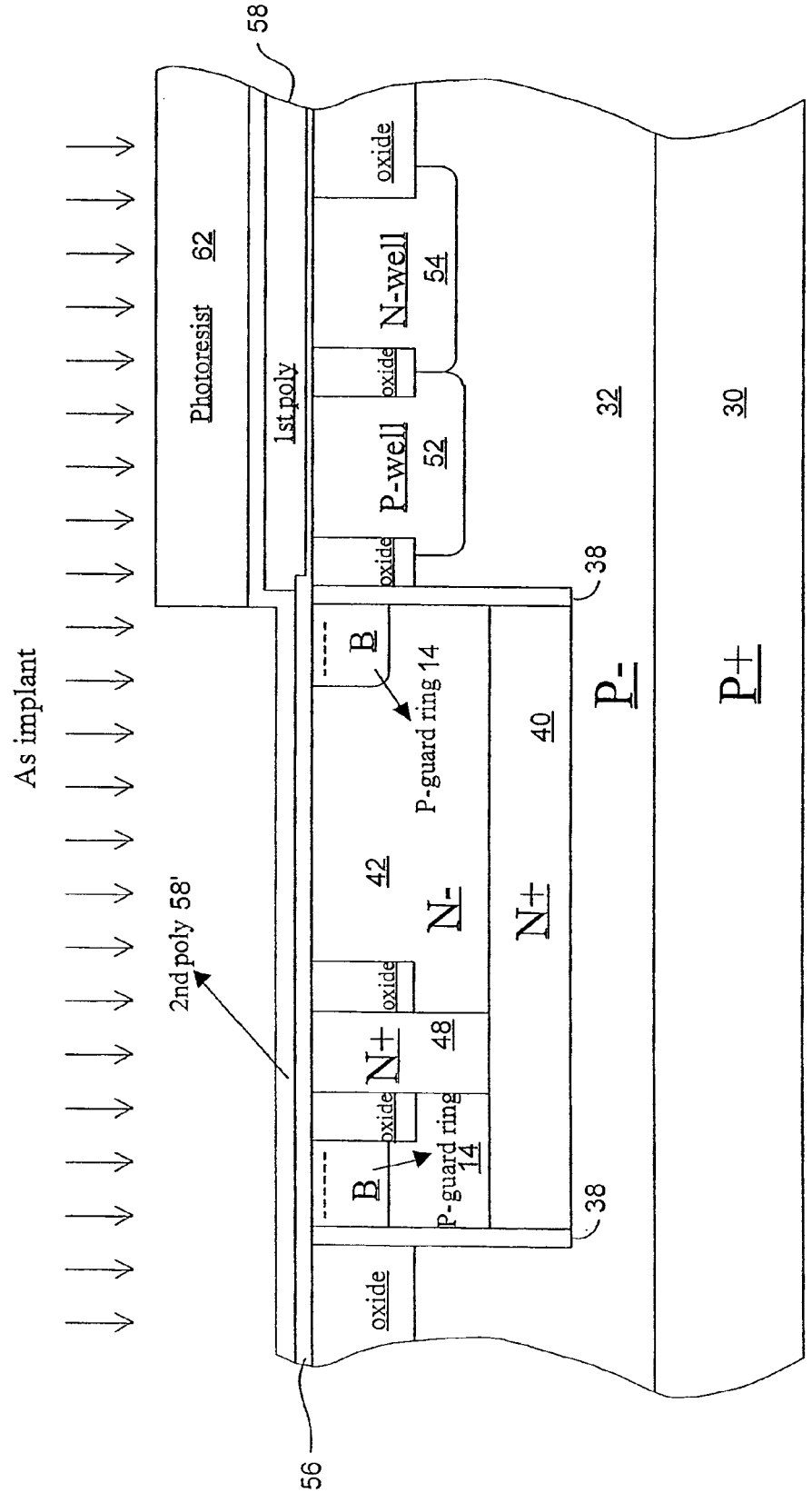
As implant
Photoresist 62
58
1st poly
oxide
N-well 54
oxide
P-well 52
oxide
38
B
P-guard ring 14
42
N-
40
N+
P-
32
P+
30
2nd poly 58'
oxide
N+ 48
oxide
B
P-guard ring 14
38
oxide
56

FIG. 12

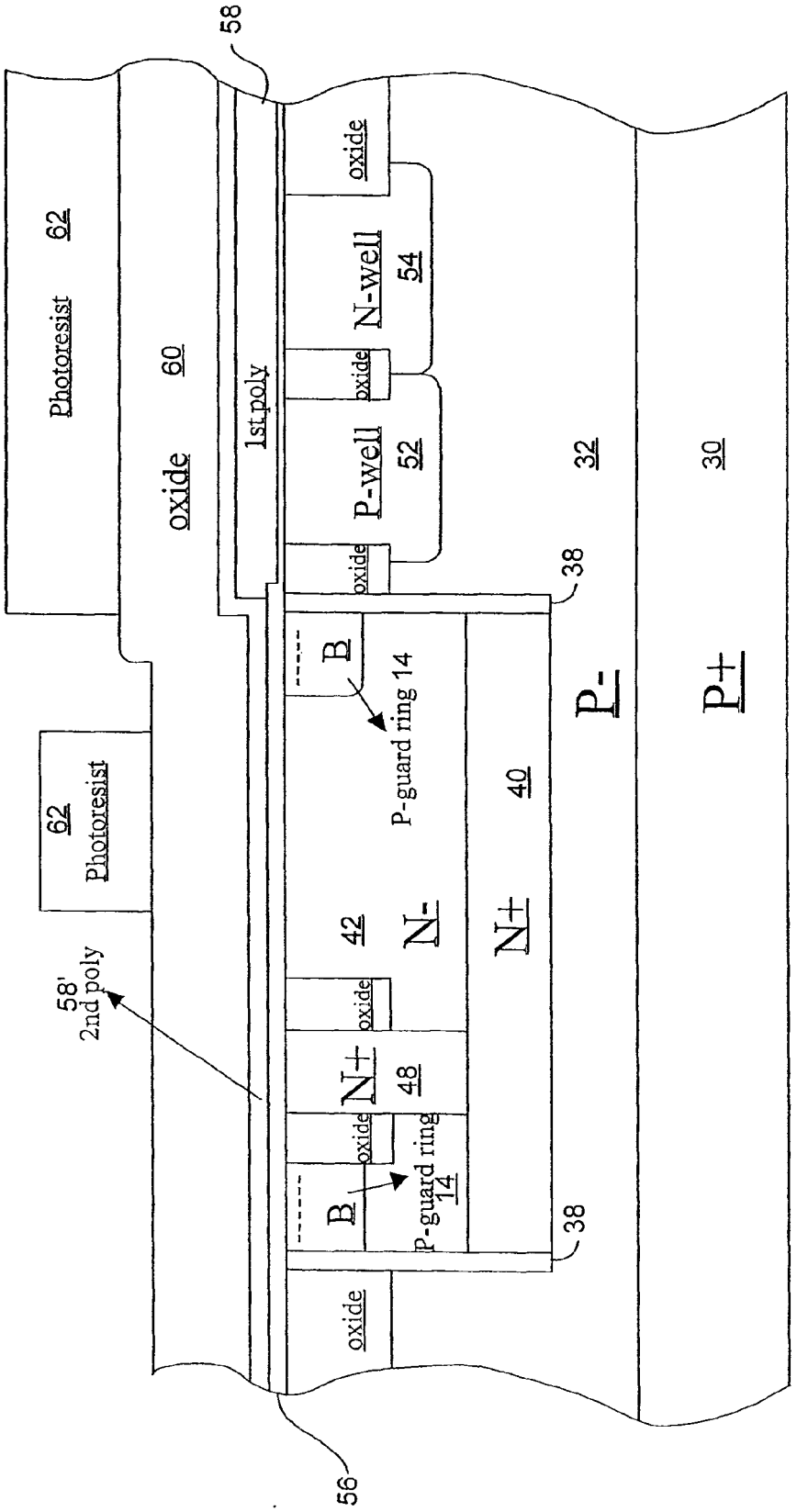
58
Photoresist 62
oxide 60
1st poly
oxide
N-well 54
oxide
P-well 52
oxide
38
B
P-guard ring 14
P- 32
P+ 30
62 Photoresist
58' 2nd poly
42
N-
N+ 40
oxide
N+ 48
oxide
B
P-guard ring 14
38
oxide
56

FIG. 13

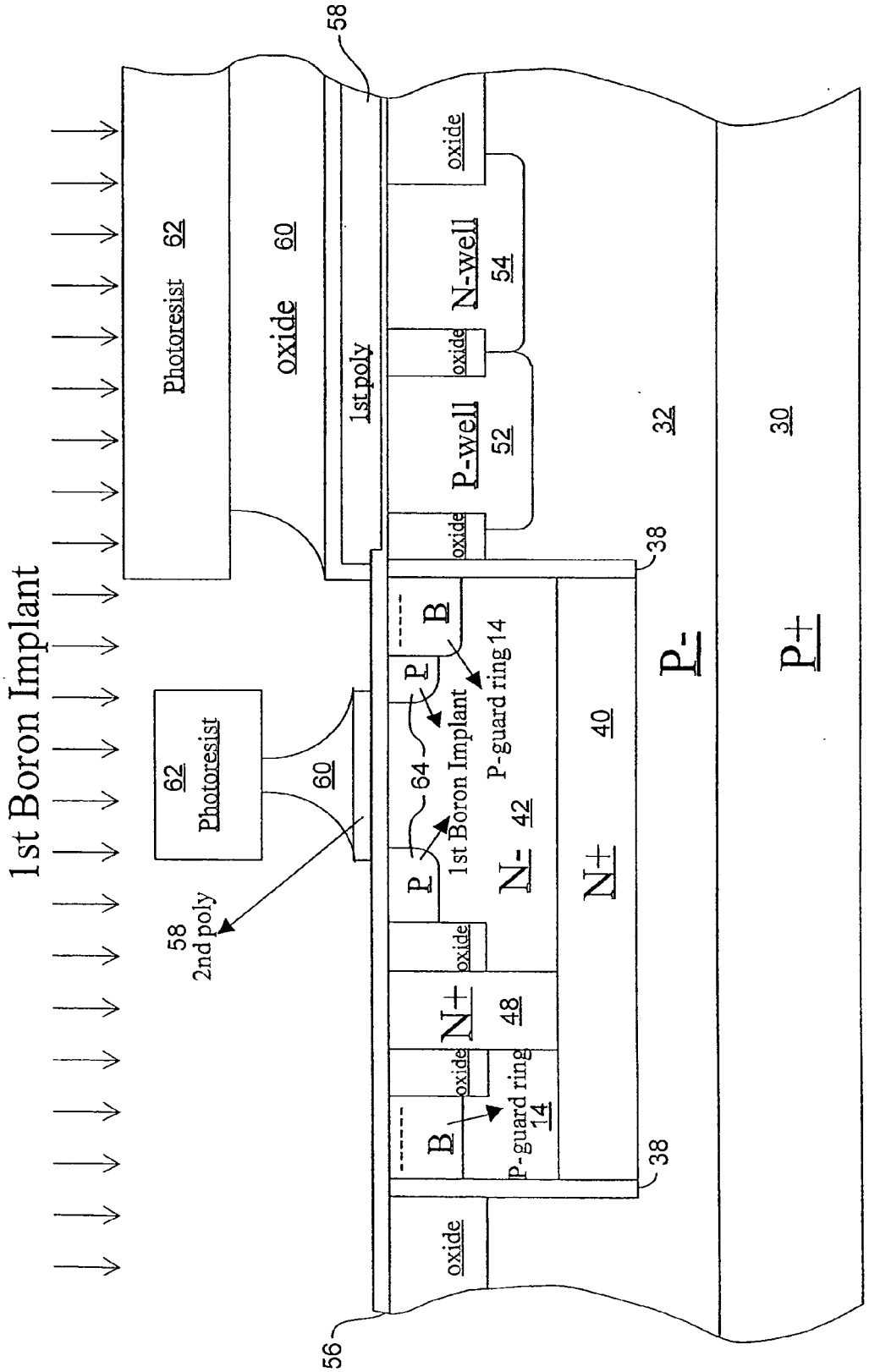
1st Boron Implant
62
Photoresist
60
oxide
58
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
38
B
P
64
1st Boron Implant
P-guard ring 14
N- 42
N+
40
P-
32
P+
30
62
Photoresist
60
58
2nd poly
oxide
N+
48
oxide
B
P-guard ring
14
38
oxide
56

FIG. 14

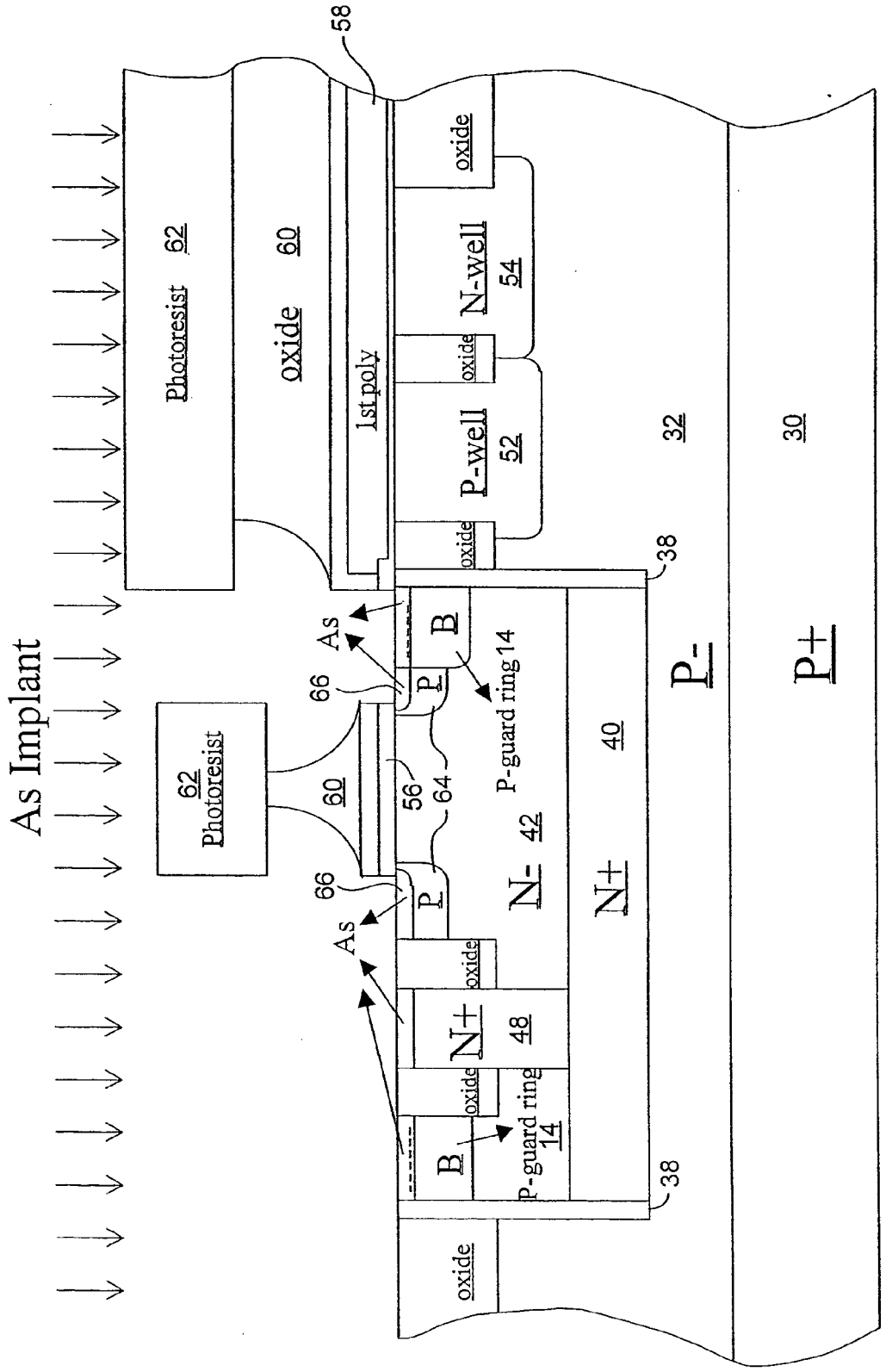
As Implant
62
Photoresist
60
oxide
Photoresist
62
58
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
As
66
B
P
P-guard ring 14
56
64
60
P-
P+
40
N-
42
N+
66
As
P
oxide
N+
48
oxide
B
P-guard ring
14
38
oxide

FIG. 15

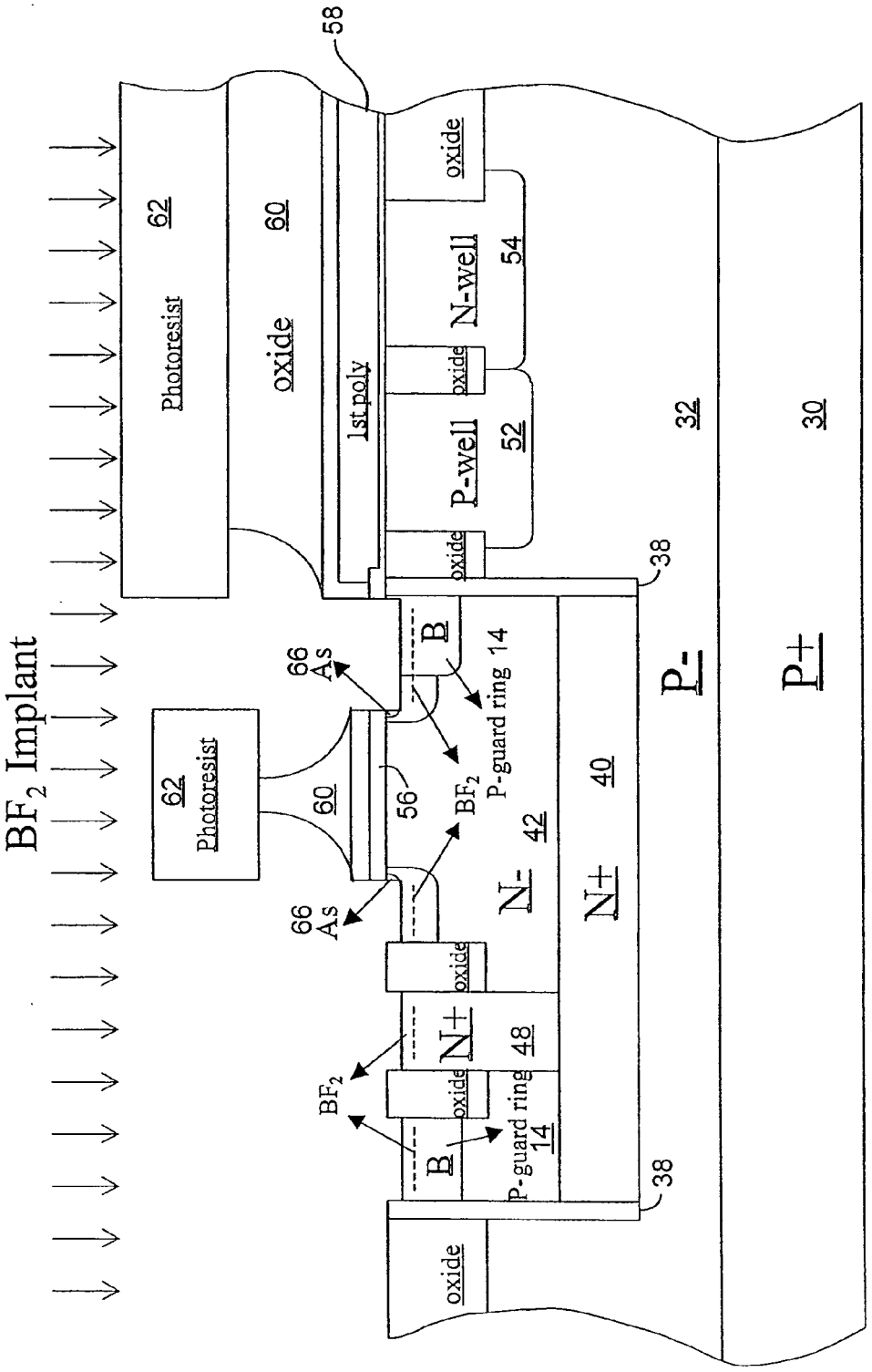
BF2 Implant
62
Photoresist
60
oxide
58
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
B
66
As
P-guard ring 14
62
Photoresist
60
56
BF2
P-
P+
N-
42
40
N+
66
As
oxide
N+
48
BF2
oxide
B
P-guard ring
14
38
oxide

FIG. 16

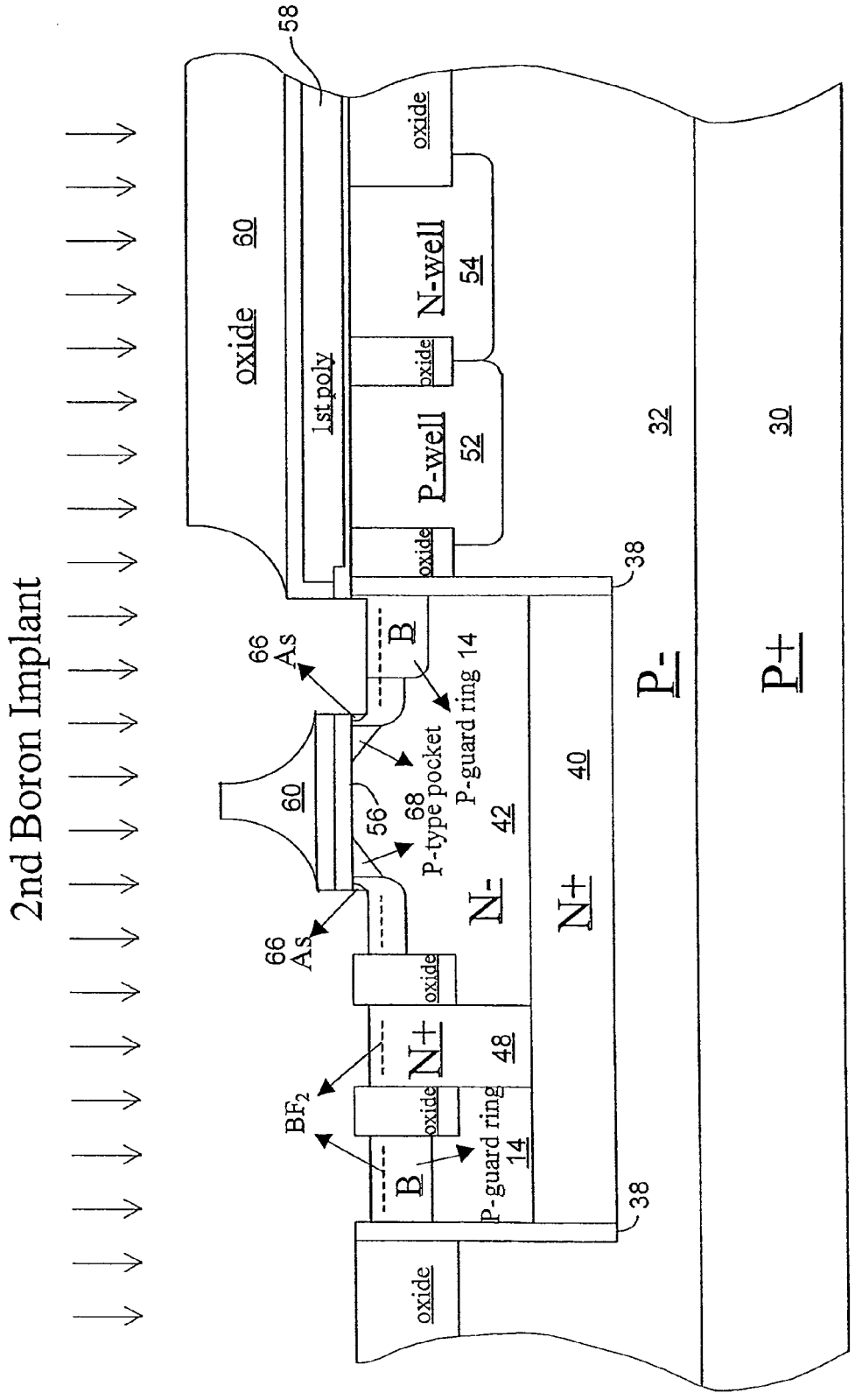
2nd Boron Implant
58
oxide
60
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
66
As
B
P-guard ring 14
60
56
68
P-type pocket
42
N-
40
N+
P-
P+
66
As
oxide
N+
48
BF2
oxide
B
P-guard ring
14
38
oxide

FIG. 17

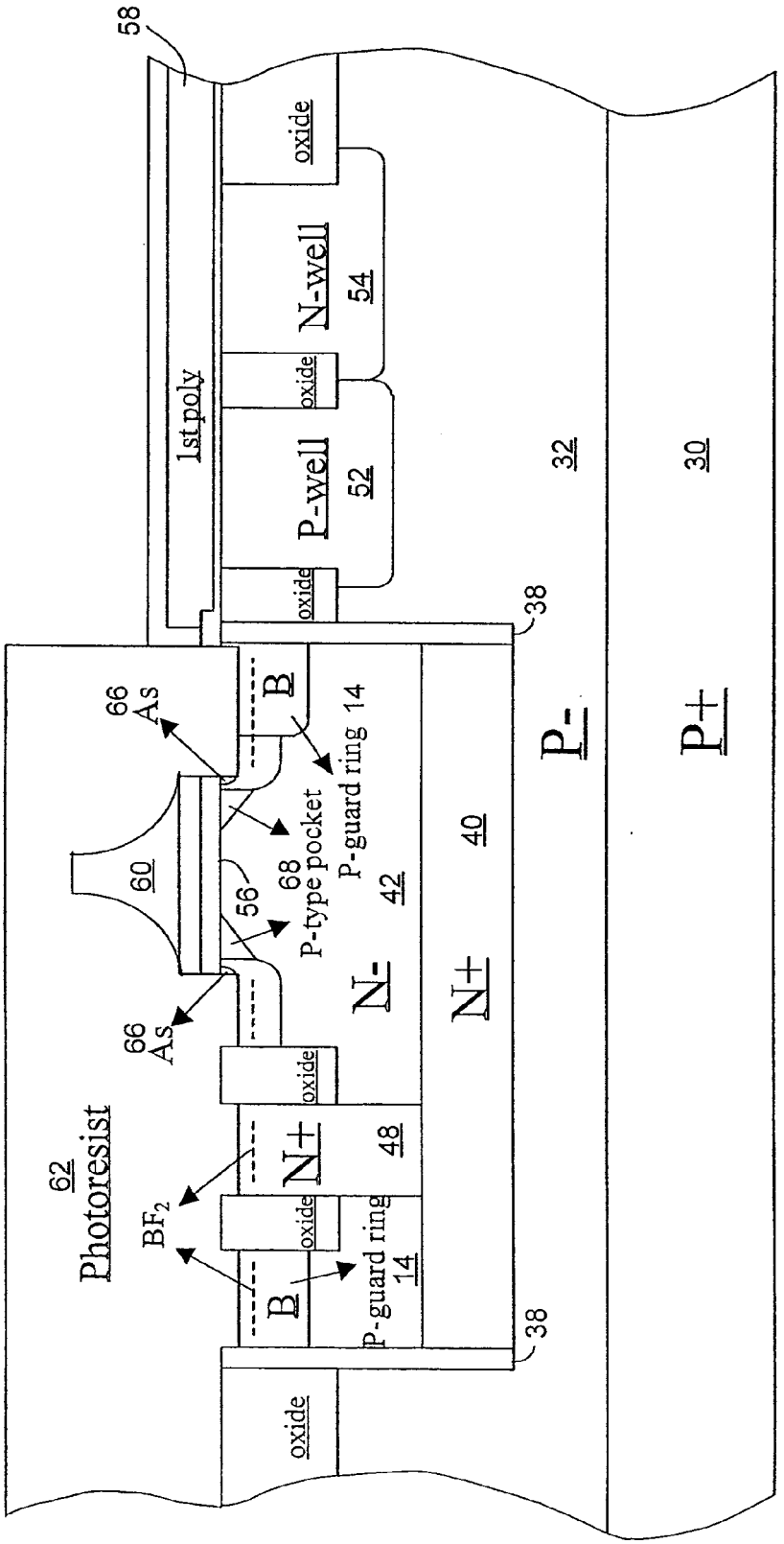
58
1st poly
oxide
N-well
54
oxide
P-well
52
oxide
32
30
38
66
As
B
P-guard ring 14
60
68
P-type pocket
56
42
P-
P+
66
As
N-
40
N+
oxide
62
Photoresist
N+
48
BF_2
oxide
B
P-guard ring
14
38
oxide

FIG. 18

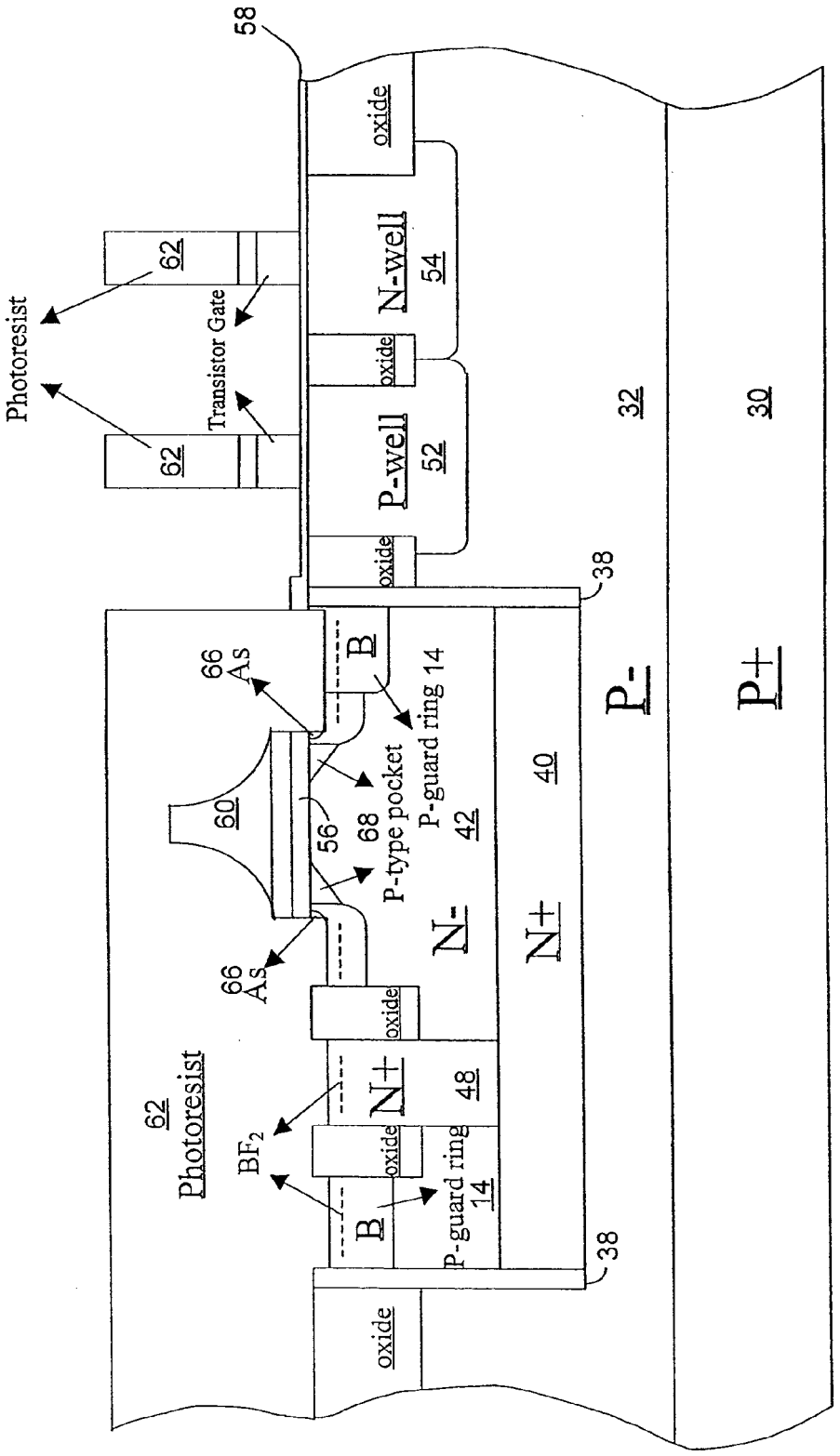
58
oxide
N-well
54
62
Photoresist
Transistor Gate
62
oxide
P-well
52
oxide
32
30
38
66
As
B
P-guard ring 14
P-type pocket
60
56
68
42
40
P-
P+
66
As
N-
N+
oxide
62
Photoresist
48
N+
BF2
oxide
B
P-guard ring
14
38
oxide

FIG. 19

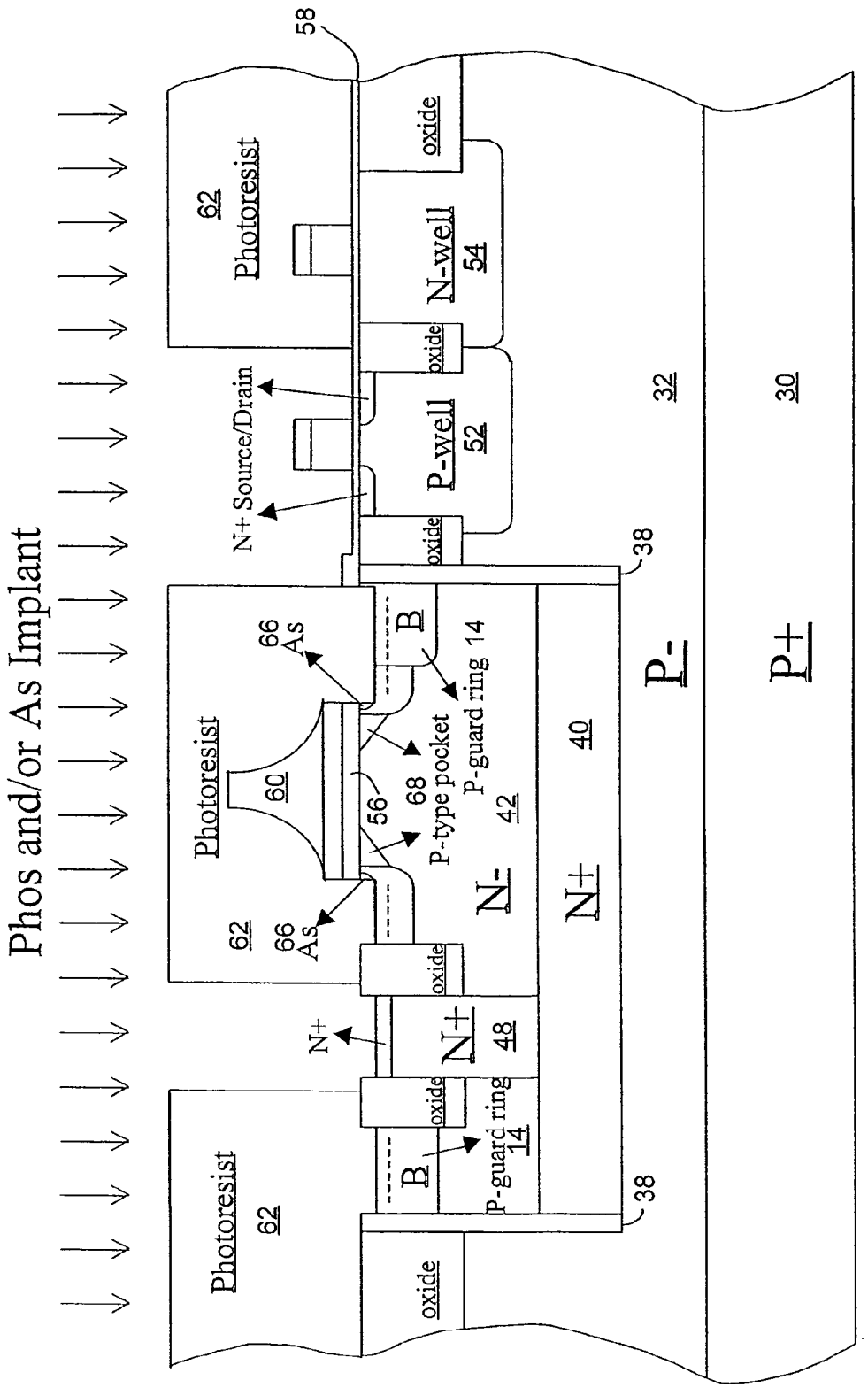
Phos and/or As Implant
58
62
Photoresist
oxide
N-well
54
oxide
P-well
52
oxide
N+ Source/Drain
32
30
38
66
As
B
P-guard ring 14
Photoresist
60
56
68
P-type pocket
42
62
66
As
N-
40
P-
P+
oxide
N+
48
N+
oxide
B
P-guard ring
14
Photoresist
62
oxide
38

FIG. 20

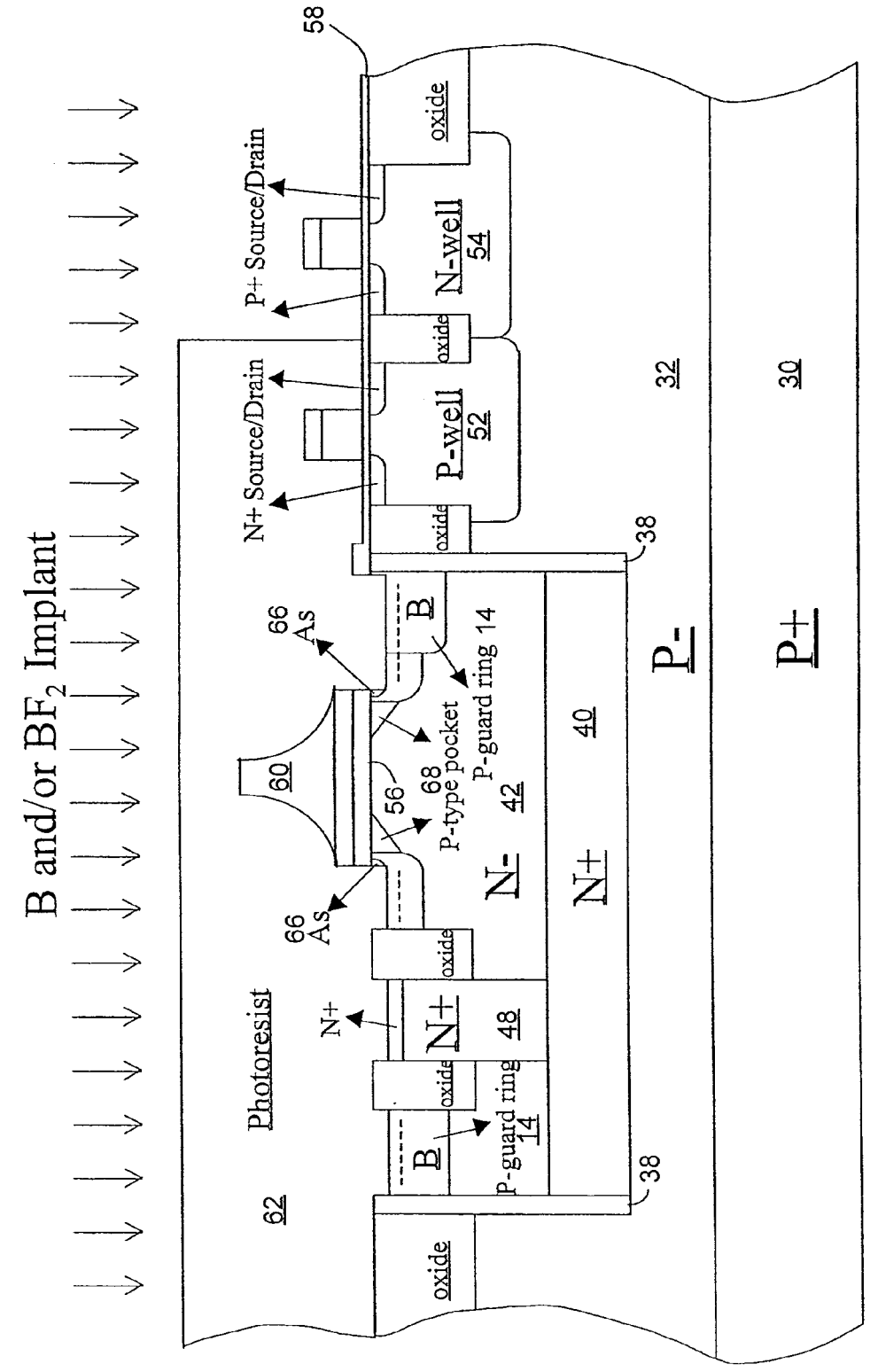
B and/or BF_2 Implant
58
P+ Source/Drain
N+ Source/Drain
oxide
N-well 54
P-well 52
32
30
38
66 As
B
P-guard ring 14
60
56
68
P-type pocket
42
40
P-
P+
N-
N+
66 As
Photoresist
62
N+
48
P-guard ring 14
38

FIG. 21

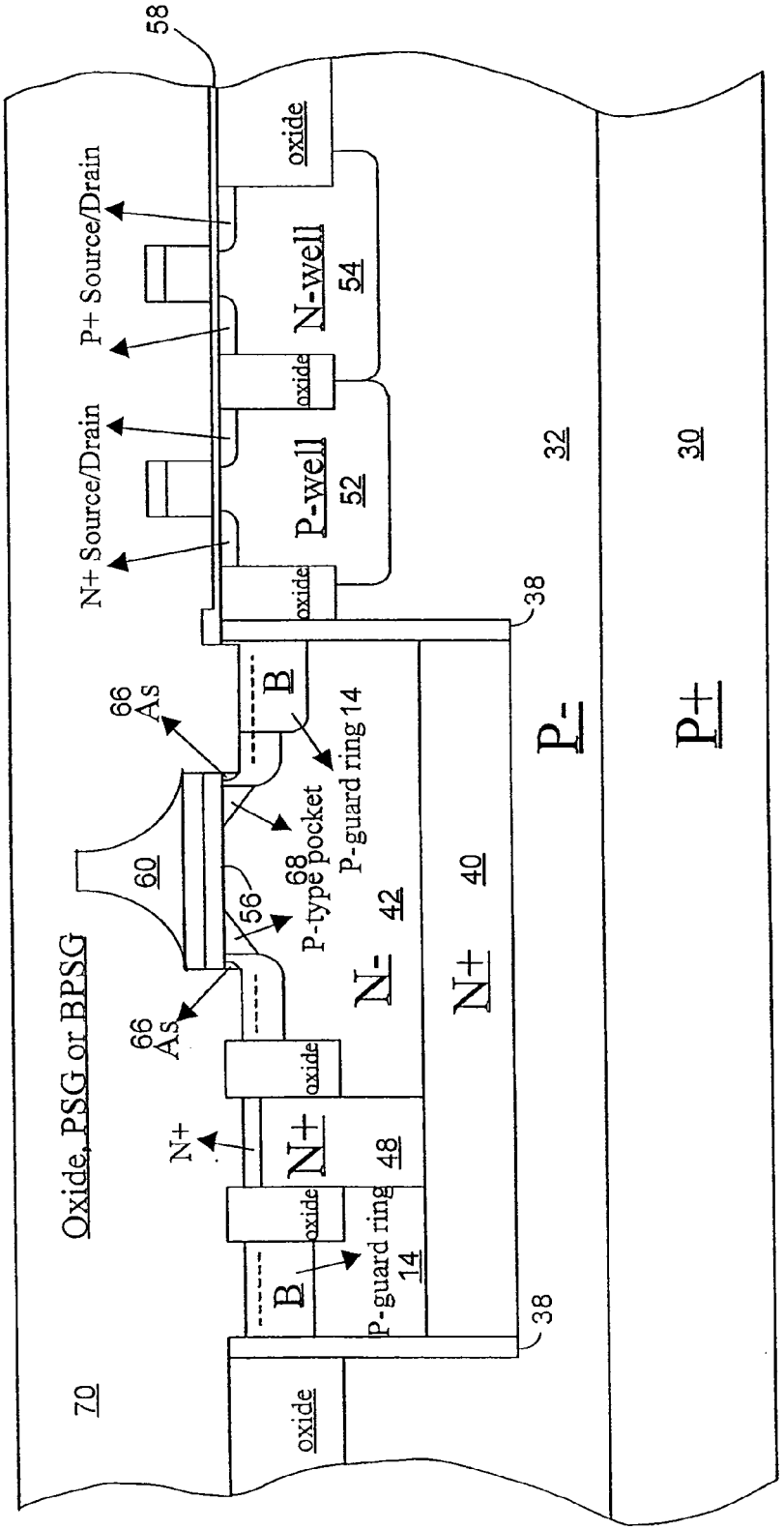
58
oxide
P+ Source/Drain
N-well
54
oxide
N+ Source/Drain
P-well
52
oxide
32
30
38
66
As
B
P-guard ring 14
60
68
P-type pocket
56
66
As
N-
42
N+
40
P-
P+
oxide
N+
N+
48
oxide
B
P-guard ring
14
38
Oxide, PSG or BPSG
70
oxide

FIG. 22

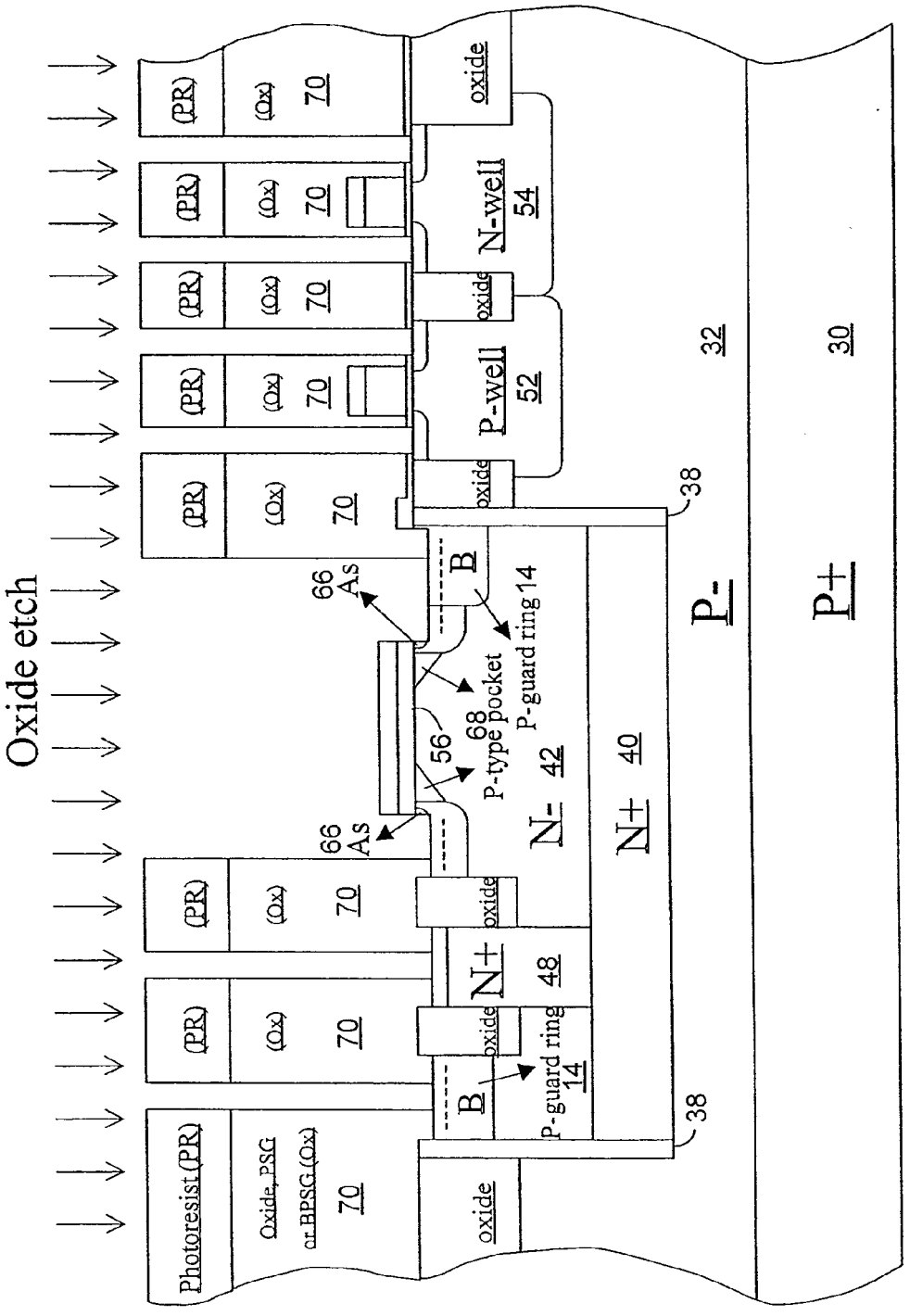
Oxide etch
Photoresist (PR)
Oxide, PSG or BPSG (Ox)
70
(PR)
(Ox)
oxide
N-well 54
P-well 52
32
30
P-
P+
38
B
66 As
P-guard ring 14
68
P-type pocket
56
N- 42
N+ 40
N+ 48

FIG. 23

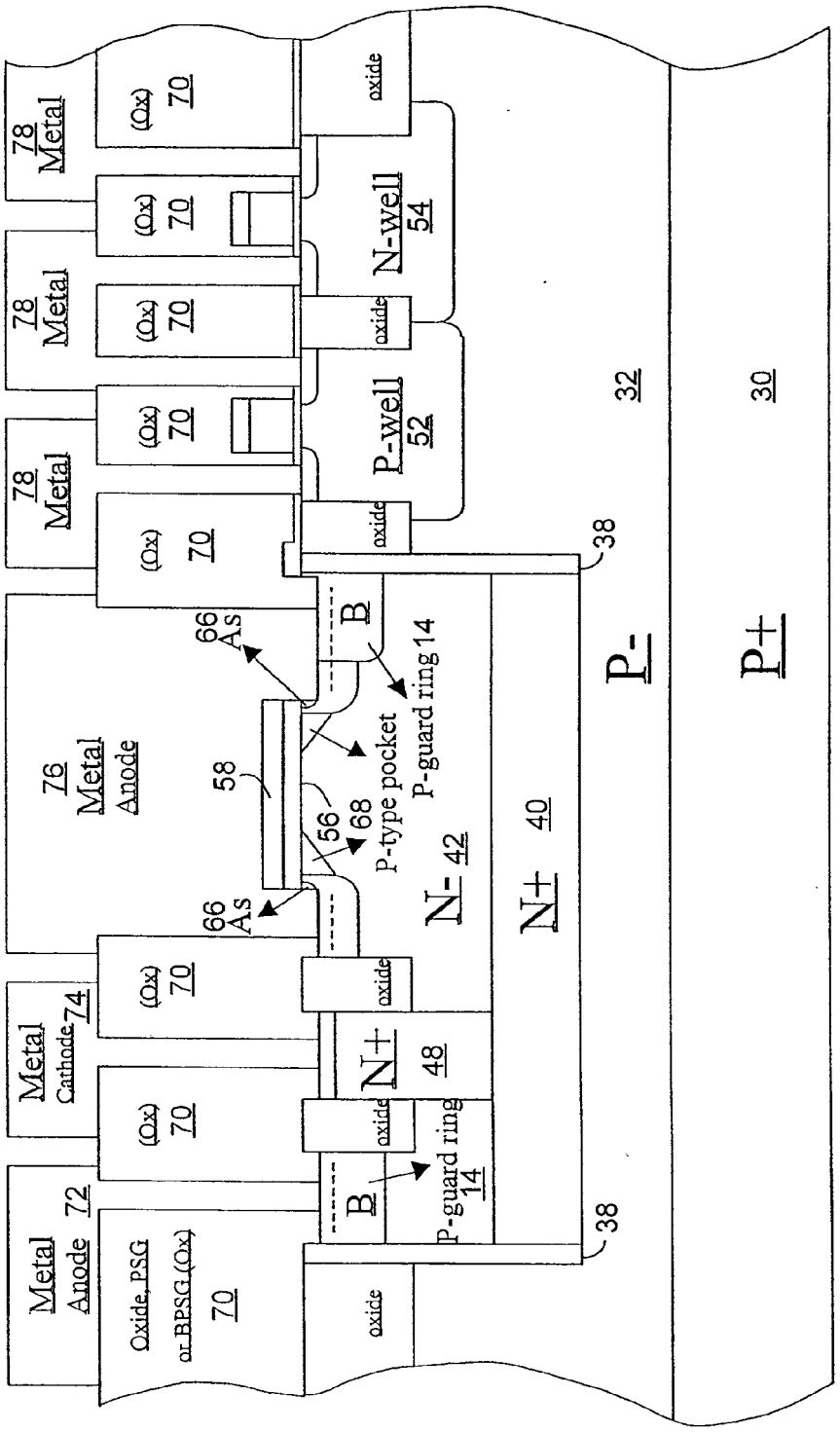
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
32
30
38
66 As
B
P-guard ring 14
P-type pocket
76 Metal Anode
58
56
68
66 As
N- 42
N+ 40
P-
P+
Metal Cathode 74
N+ 48
Metal Anode 72
Oxide, PSG or BPSG (Ox) 70
B
P-guard ring 14
38
oxide

FIG. 24

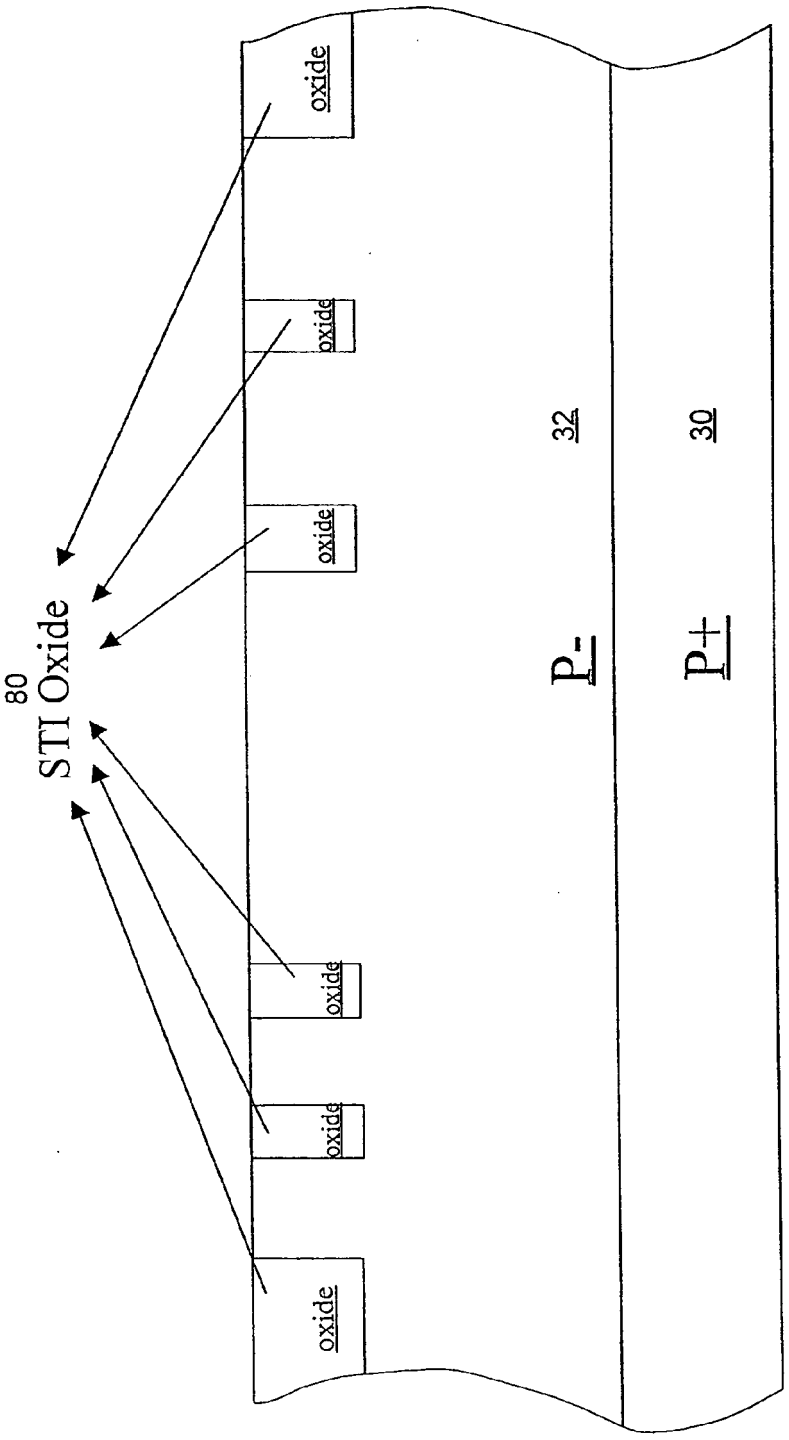

FIG. 25

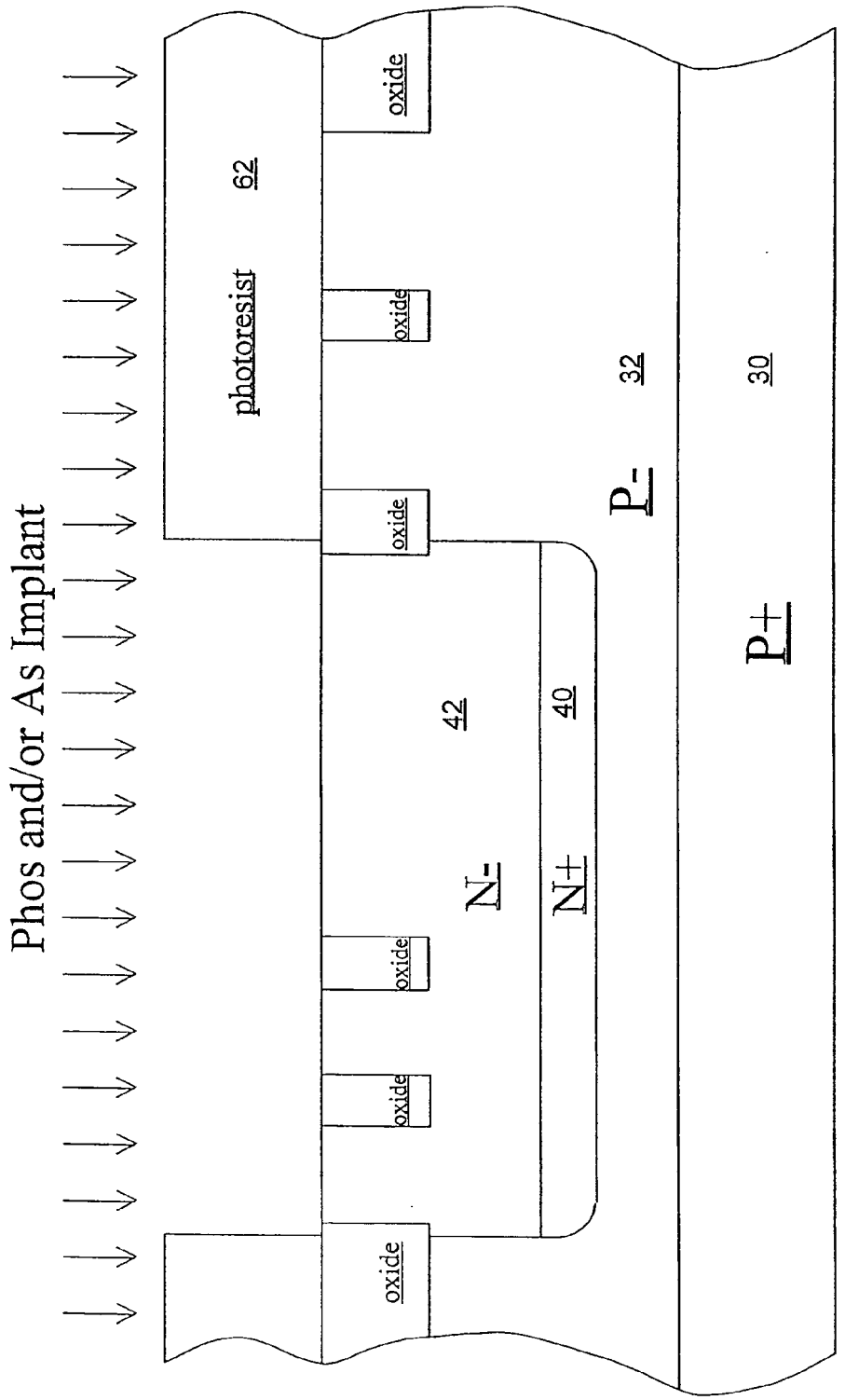
Phos and/or As Implant
photoresist
62
oxide
oxide
oxide
oxide
oxide
oxide
42
40
N-
N+
P-
32
30
P+

FIG. 26

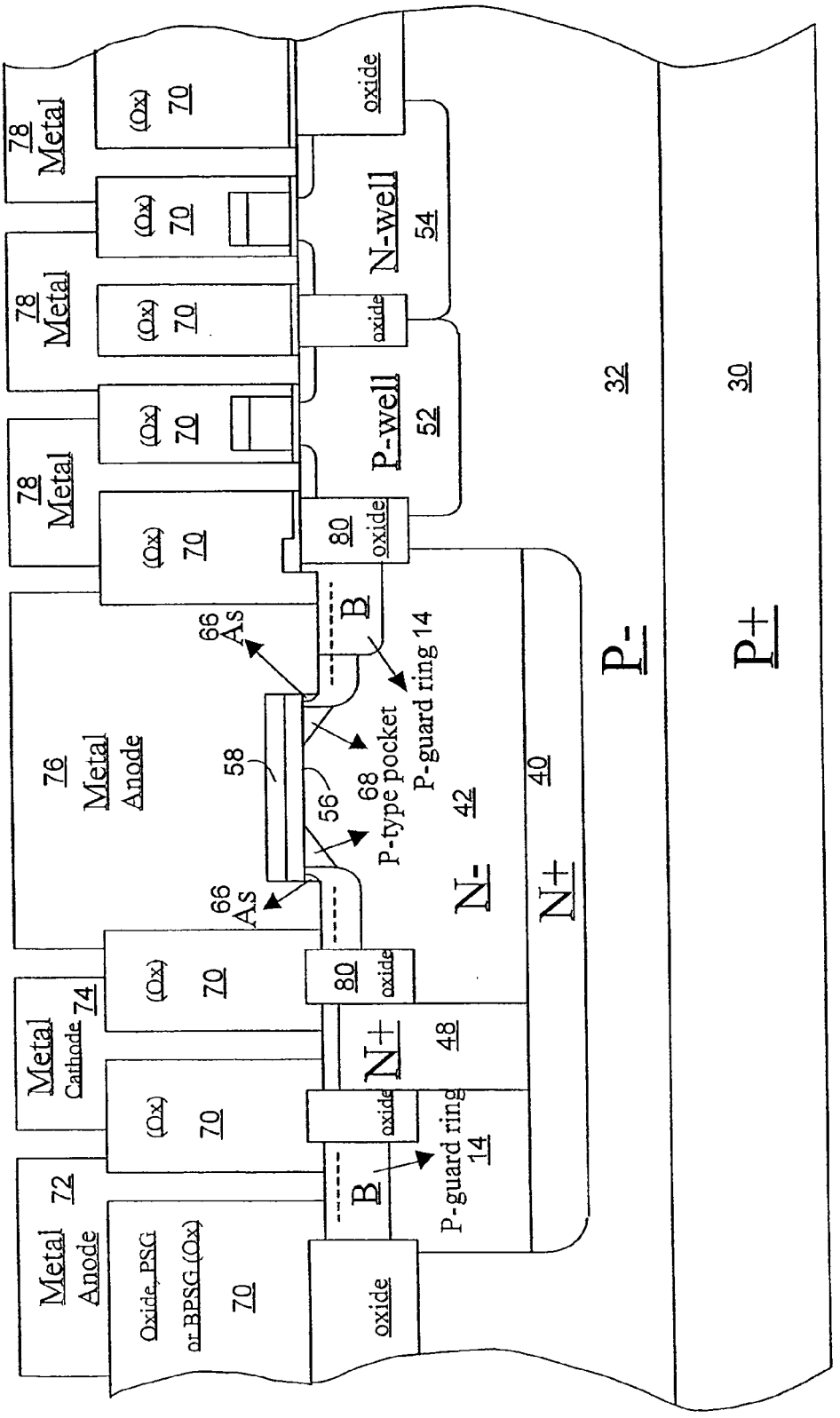
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
32
30
80 oxide
B
66 As
58
56
68 P-type pocket
P-guard ring 14
76 Metal Anode
42
40
P-
P+
N-
N+
48
74 Metal Cathode
72 Metal Anode
Oxide, PSG or BPSG (Ox) 70

FIG. 27

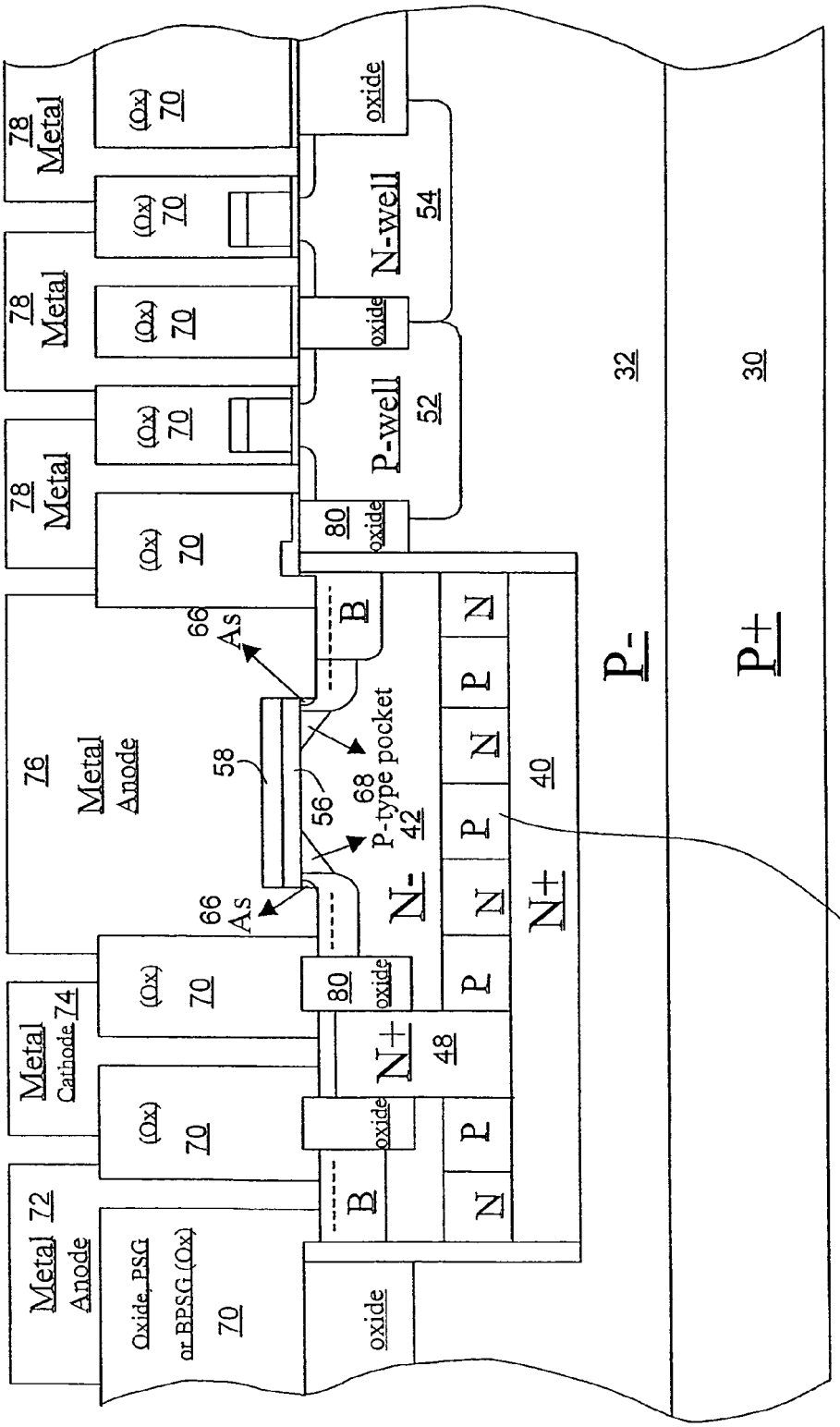
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
32
30
80 oxide
B
N
P
N+
48
P-
P+
66 As
58
56
68 P-type pocket
42
N-
40
76 Metal Anode
74 Metal Cathode
72 Metal Anode
Oxide, PSG or BPSG (Ox) 70
84

FIG. 28

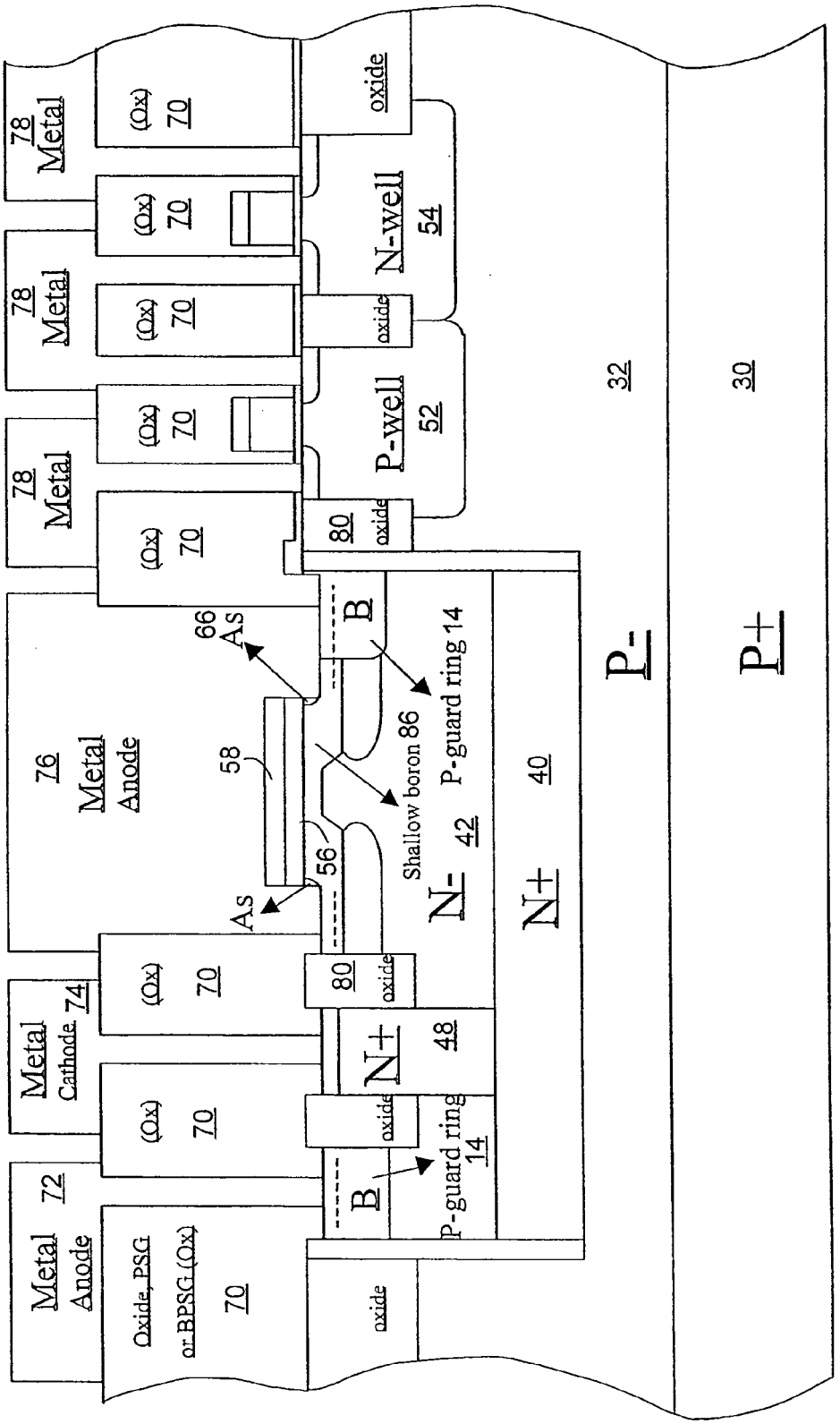
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
80 oxide
B
66 As
76 Metal Anode
58
56
As
Shallow boron 86
P-guard ring 14
N- 42
N+ 48
40
P- 32
P+ 30
74 Metal Cathode
72 Metal Anode
Oxide, PSG or BPSG (Ox) 70
P-guard ring 14

FIG. 29

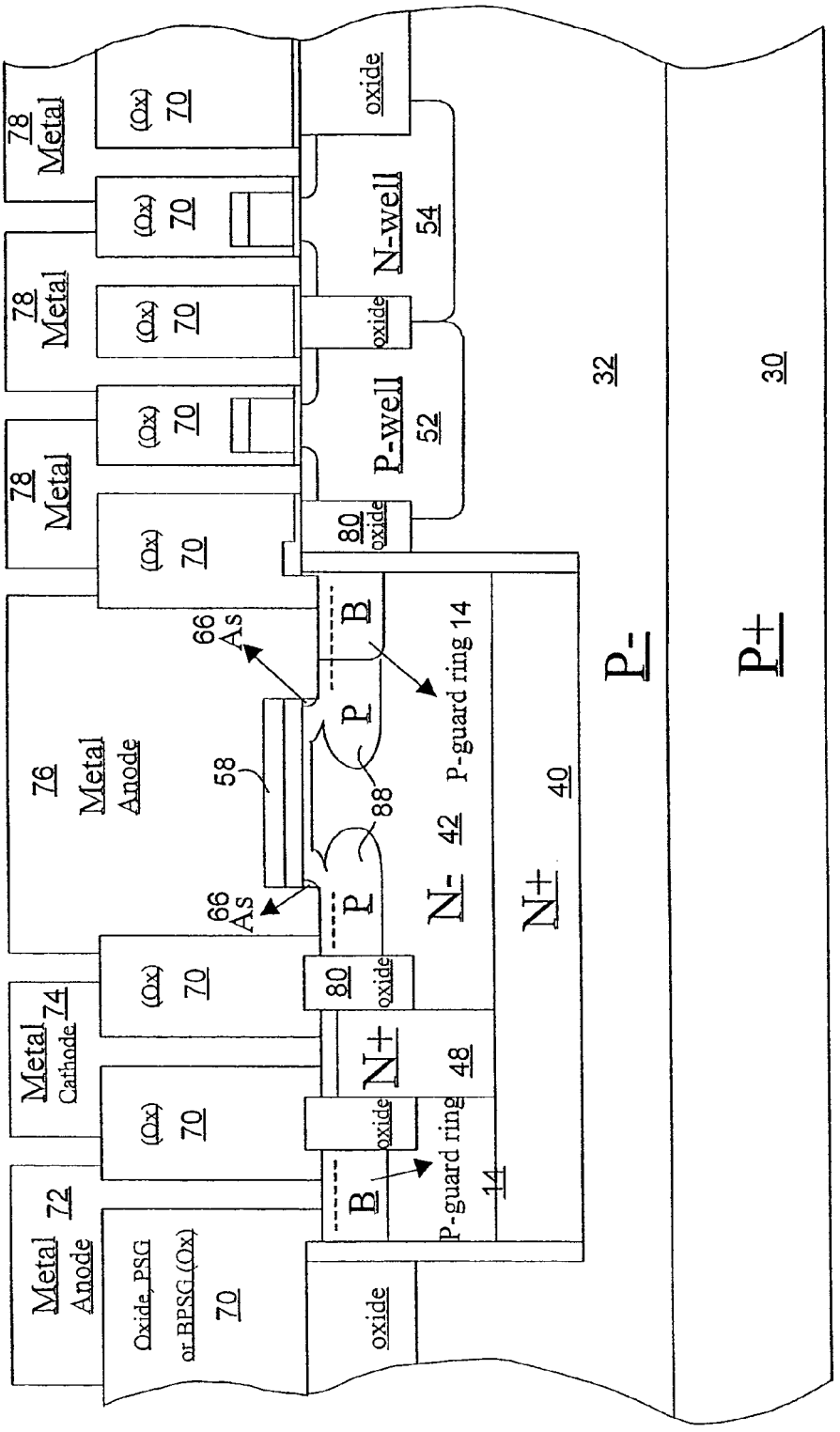
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
80 oxide
32
30
66 As
B
P
P-guard ring 14
76 Metal Anode
58
88
P-
P+
42
N-
40
N+
74 Metal Cathode
48
72 Metal Anode
Oxide, PSG or BPSG (Ox) 70
P-guard ring

FIG. 30

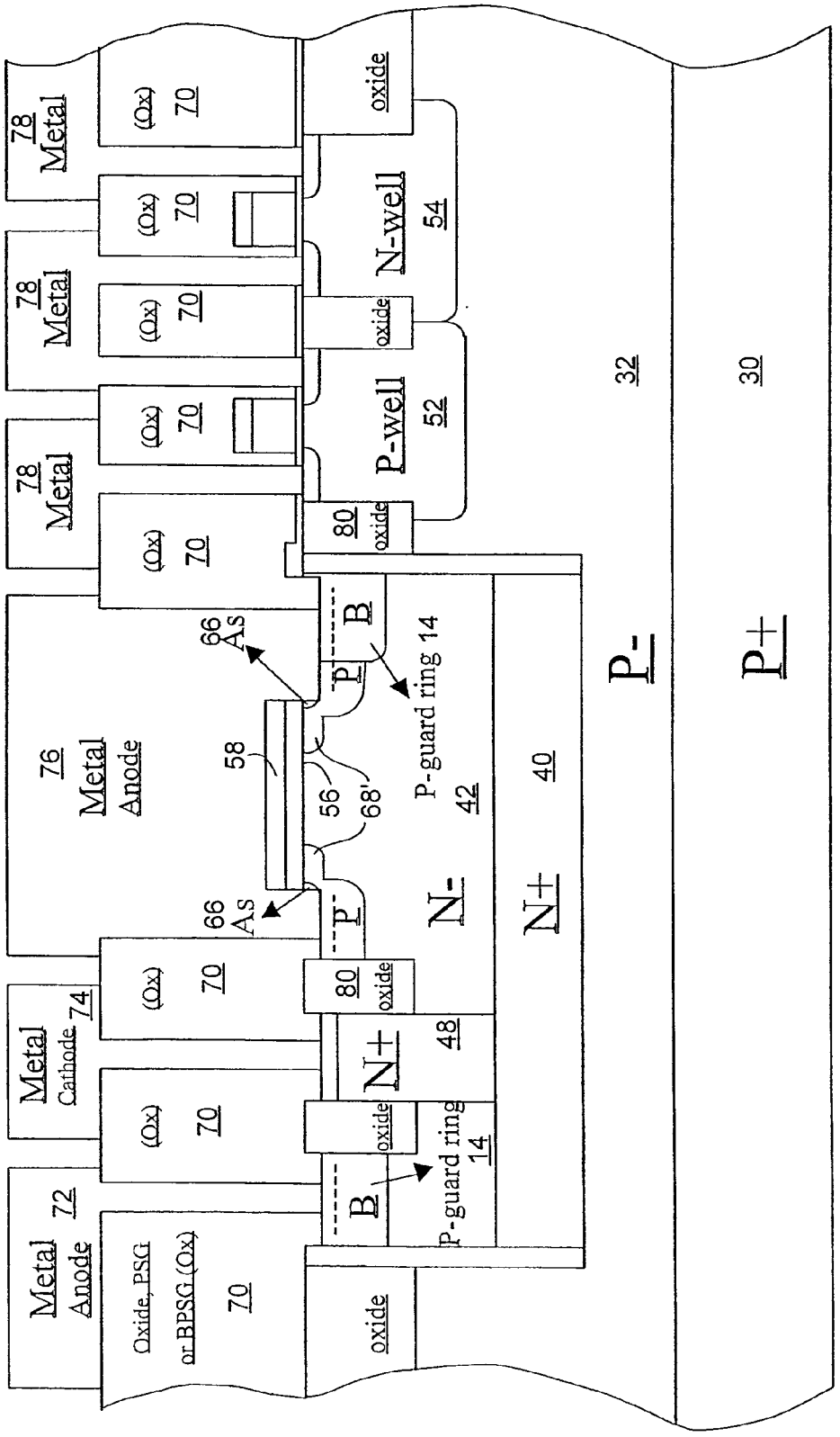
78 Metal
(Ox) 70
oxide
N-well 54
P-well 52
32
30
80 oxide
B
P
66 As
58
56
68'
P-guard ring 14
42
76 Metal Anode
40
P-
P+
N-
N+
48
74 Metal Cathode
72 Metal Anode
Oxide, PSG or BPSG (Ox) 70
P-guard ring 14

FIG. 31

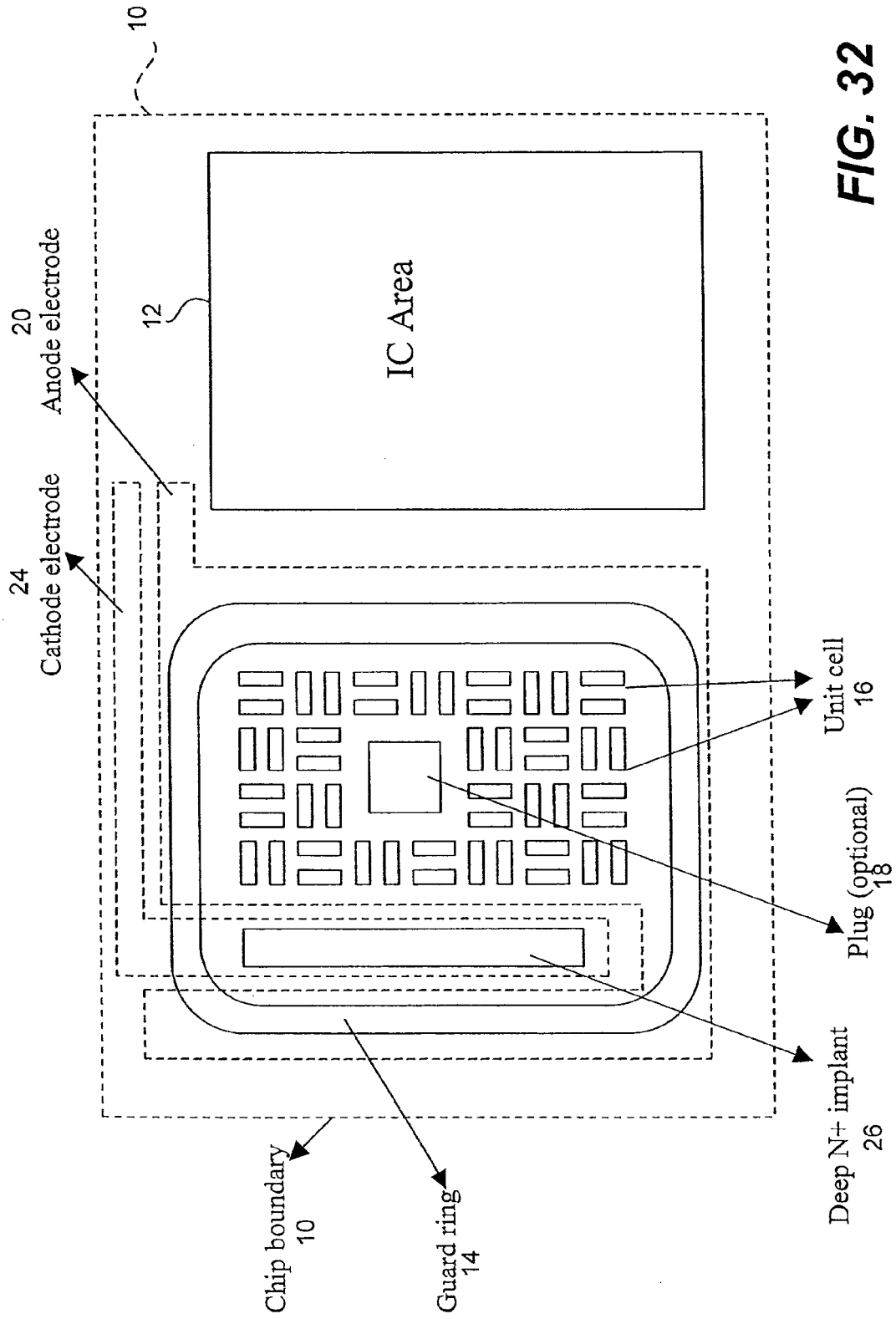
10
IC Area
12
20
Anode electrode
24
Cathode electrode
Unit cell
16
Plug (optional)
18
Deep N+ implant
26
Chip boundary
10
Guard ring
14

FIG. 32

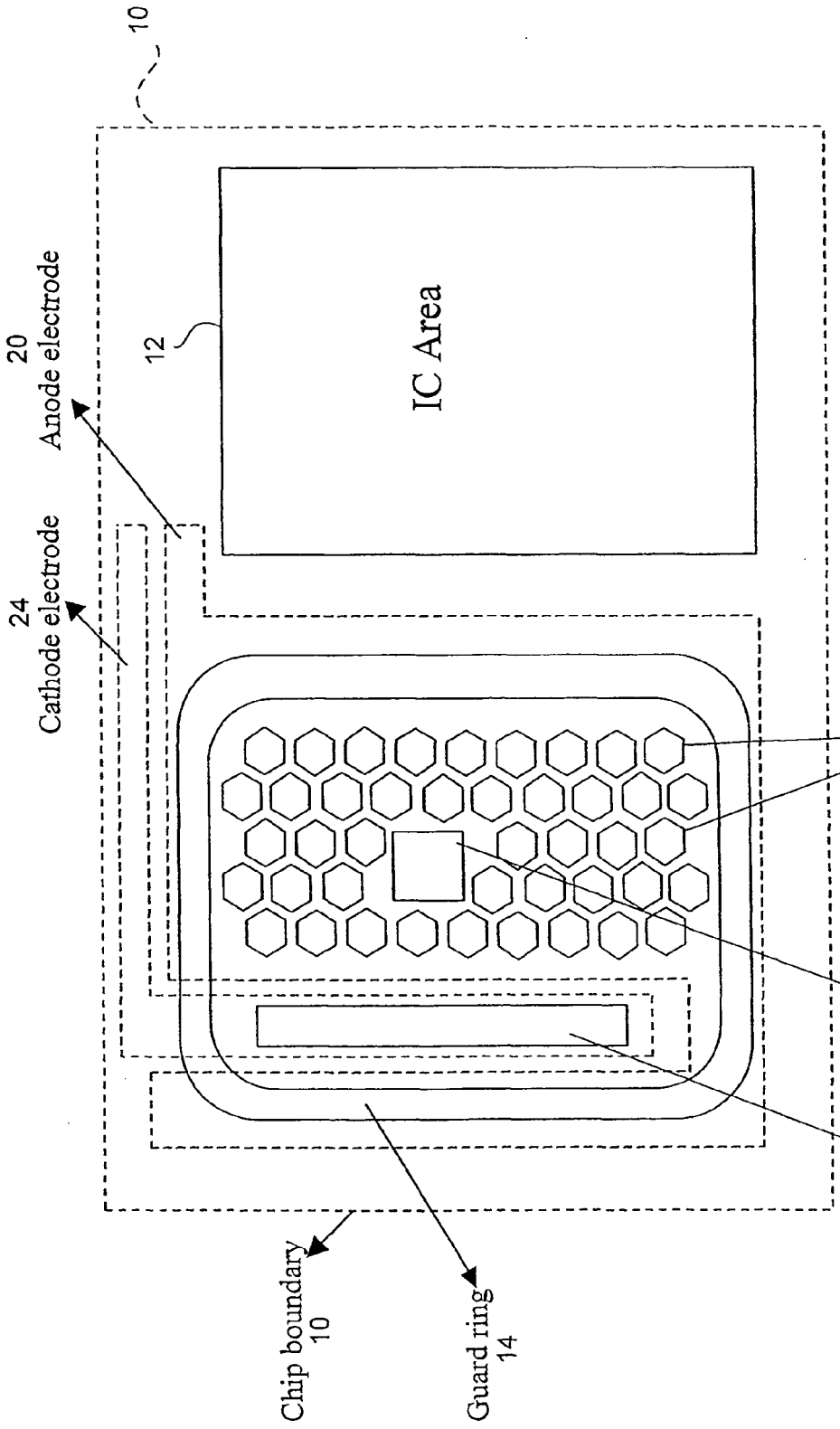
10
IC Area
12
20
Anode electrode
24
Cathode electrode
Unit cell
16
Plug (optional)
18
Deep N+ implant
26
Chip boundary
10
Guard ring
14

FIG. 33

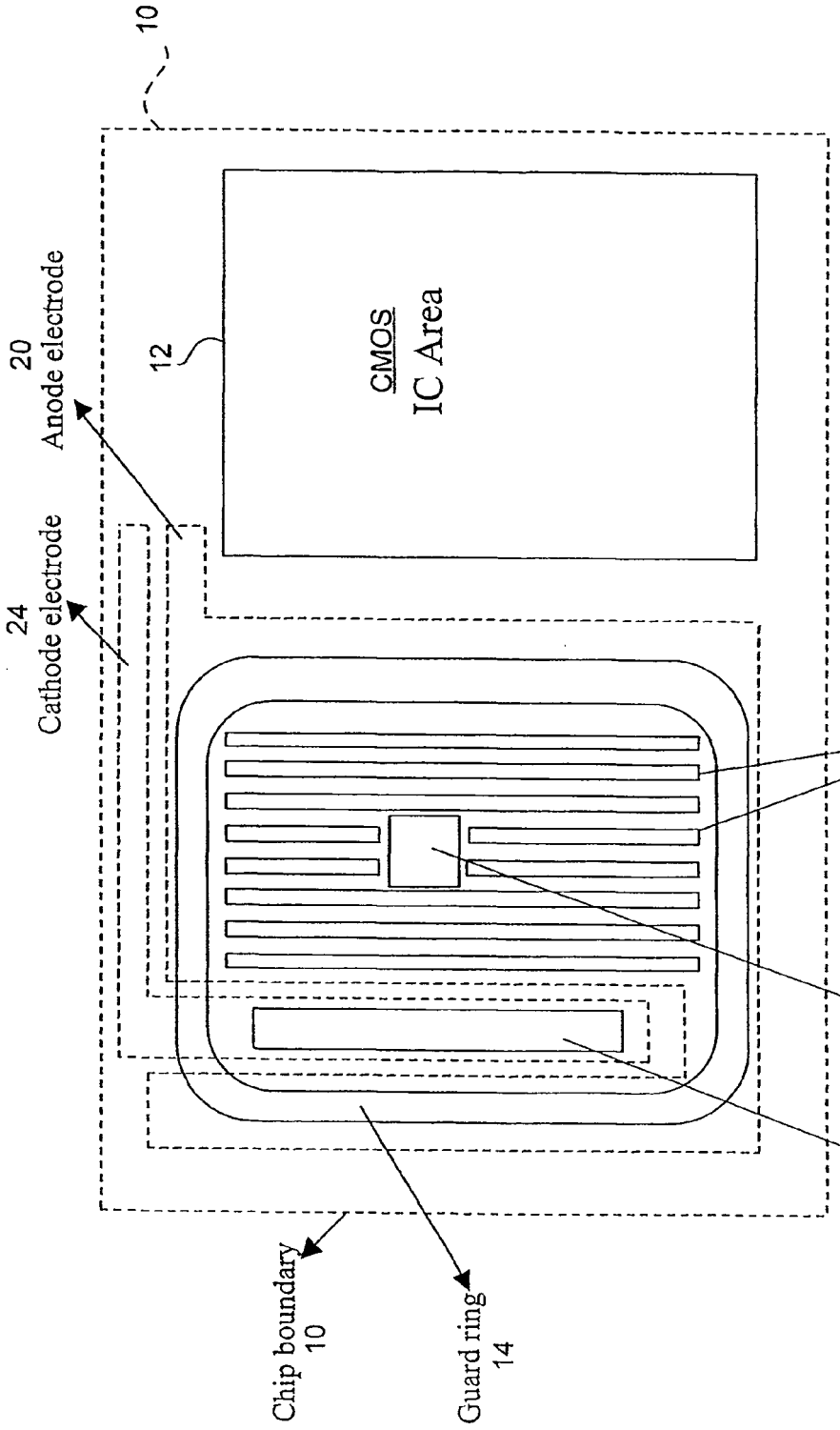
10
12
CMOS
IC Area
20
Anode electrode
24
Cathode electrode
Unit cell
16
Plug (optional)
18
Deep N+ implant
26
Chip boundary
10
Guard ring
14

FIG. 34

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 6624030 B **[0021]**
- US 6743703 B **[0026]**
- US 10159558 B **[0027]**
- US 6515330 B **[0028]**
- US 6420225 B **[0029]**