(19) **Europäisches Patentamt**
European Patent Office
Office européen des brevets

(11) **EP 2 425 329 B8**

(12) **CORRECTED EUROPEAN PATENT SPECIFICATION**

(15) Correction information:
Corrected version no 1 (W1 B1)
Corrections, see
Bibliography INID code(s) 84

(48) Corrigendum issued on:
07.02.2018 Bulletin 2018/06

(45) Date of publication and mention
of the grant of the patent:
27.12.2017 Bulletin 2017/52

(21) Application number: **10717728.9**

(22) Date of filing: **27.04.2010**

(51) Int Cl.:
G06F 9/38 (2018.01)

(86) International application number:
PCT/GB2010/000832

(87) International publication number:
WO 2010/125336 (04.11.2010 Gazette 2010/44)

(54) **METHOD AND APPARATUS FOR SCHEDULING THE ISSUE OF INSTRUCTIONS IN A MULTITHREADED MICROPROCESSOR**

VERFAHREN UND GERÄT ZUM PLANEN DER AUSGABE VON BEFEHLEN IN EINEM MULTITHREADED PROZESSOR

MÉTHODE ET APPAREIL POUR PLANIFIER L'EMISSION D'INSTRUCTIONS DANS UN PROCESSEUR MULTIFILIÈRE

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

(30) Priority: **28.04.2009 GB 0907286**

(43) Date of publication of application:
07.03.2012 Bulletin 2012/10

(73) Proprietor: **Imagination Technologies Limited**
Kings Langley
Hertfordshire WD4 8LZ (GB)

(72) Inventor: **WEBBER, Andrew, David**
Tring
Hertfordshire HP23 5E (GB)

(74) Representative: **Slingsby Partners LLP**
1 Kingsway
London WC2B 6AN (GB)

(56) References cited:
US-A1- 2006 101 241   US-A1- 2006 136 915

• **IL PARK ET AL: "Implicitly-multithreaded processors" PROCEEDINGS OF THE 30TH. INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE. ISCA 2003. SAN DIEGO, CA, JUNE 9 - 11, 2003; [INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE.(ISCA)], LOS ALAMITOS, CA : IEEE COMP. SOC, US, 9 June 2003 (2003-06-09), pages 39-50, XP010796919 ISBN: 978-0-7695-1945-6**

EP 2 425 329 B8