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(54) A method for precisely controlled masked anodization

(57) The present invention is related to a method for masked anodization of an anodizable layer on a substrate, for example an aluminium layer present on a sacrificial layer, wherein the sacrificial layer needs to be removed from a cavity comprising a Micro or Nano Electromechanical System (MEMS or NEMS). Anodization of an Al layer leads to the formation of elongate pores, through which the sacrificial layer can be removed. According to the method of the invention, the anodization of the Al layer is done with the help of a first mask which defines the area to be anodized, and a second mask which defines a second area to be anodized, said second area surrounding the first area. Anodization of the areas defined by the first and second mask leads to the formation of an anodized structure in the form of a closed ring around the first area, which forms a barrier against unwanted lateral anodization in the first area.

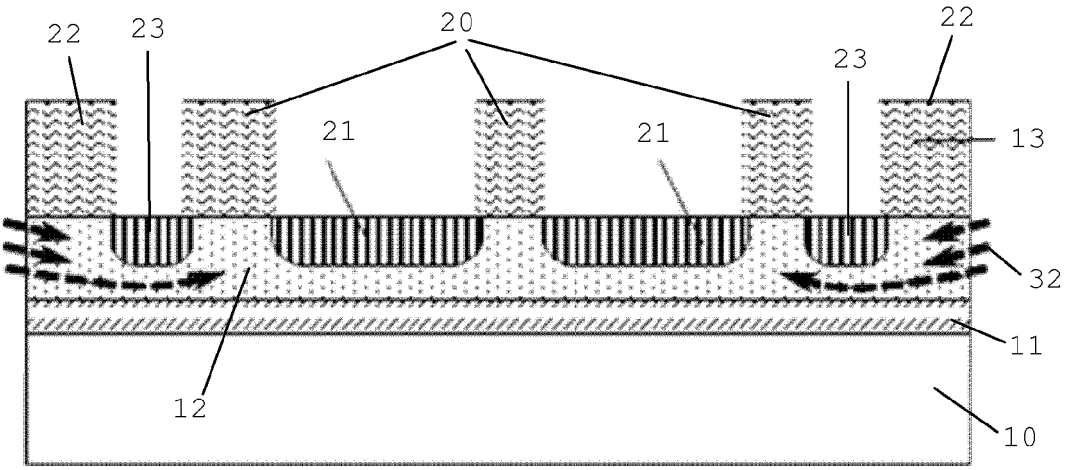

FIG. 3a

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Description

Field of the Invention

[0001] The present invention is related to methods for precisely controlling a masked anodization process.

[0002] The present invention is further related to manufacturing semiconductor devices, especially to methods of encapsulation and to such devices. More specifically it may relate to zero-Level or wafer level packaging of semiconductor devices.

[0003] More particularly, the present invention relates to Nano- and/or Micro-Electro-Mechanical Systems (NEMS and /or MEMS) and to processes of encapsulating (or packaging) said systems.

State of the art.

[0004] Creating patterns of a dielectric or porous material within a conductive thin film by means of masked anodization (wet electrochemical oxidation and/or etching) has several advantages over conventional thin film deposition and etching techniques, such as the simplicity of the fabrication process and the relatively planar (and aligned) structures that result from such process. Masking the anodization process is normally achieved by applying a masking structure on top of the layer to be anodized. The masking structure can be applied by means of conventional photolithography (photoresist mask) or by means of deposition and patterning of another material that is resistant to the anodization process (hard mask). A photoresist mask is simpler to implement than a hard mask but photoresists are normally attacked during the anodization process resulting in poor control over the lateral extent of the anodized patterns.

[0005] Finding a simple technique for high-precision masked anodization is necessary to fabricate planar patterns of a dielectric or porous material within a conductive thin film. Such patterns are for example useful to create interconnecting metal lines (patterns) which are isolated from each other by a porous dielectric material of low dielectric constant which provides the advantage of reduced capacitance between the interconnecting lines. Because of this, the speed of signals that can be transmitted through these interconnects can be increased and the cross-coupling between the different interconnects can be reduced, resulting in better performance for integrated circuits.

[0006] Another application requiring a high-precision masked anodization is the packaging (encapsulation) of Nano- and/or Micro-Electro-Mechanical Systems (NEMS/MEMS). Said NEMS/MEMS systems cannot be directly packaged in a plastic or ceramic package, the so-called first level package, since NEMS/MEMS are often composed of fragile and/or mobile free-standing parts that can easily be damaged during dicing and assembly. To avoid such damage, NEMS/MEMS devices have to be protected at the wafer level, before dicing. This is possible by the so-called zero-level packaging or wafer-level packaging techniques. Most NEMS/MEMS systems therefore require an encapsulation under vacuum or under a controlled atmosphere and pressure in order to ensure either a good performance or an acceptable lifetime of operation. The encapsulation has to be performed without the direct deposition of sealing material on the NEMS/MEMS device, as such deposition can cause damage to the device. Therefore there is a need to deposit first an encapsulation made of a layer having holes (pores) through which a vacuum and/or controlled atmosphere can be realized and thereafter deposit a sealing layer. A simple and cheap process led to the idea of encapsulating NEMS/MEMS devices with a porous membrane. This facilitates the manufacturing of the device as it avoids the need to shape access holes in the membrane using photolithography since the device can be released through the pores of the membrane.

[0007] Porous alumina (AlOx) membranes are recently being investigated for use as porous membranes in said thin film vacuum packaging of NEMS/MEMS devices as shown in figure 1, which shows a schematic image of a substrate 1 (e.g. Si), carrying on its surface a MEMS device 2, encapsulated by a porous membrane 3. The membrane 3 is covered by a sealing layer 4. The porous membrane 3 is obtained by anodization of an aluminum thin film (deposited on top of a dielectric thin film) in a low-pH electrolyte, and using a patterned photoresist layer as the mask. The anodization process may be performed on masked Al layers using a photoresist mask (Hellin Rico et al., J. Electrochem. Soc. Vol. 154, No. 9 (2007)). The pores 5 (not drawn to scale), are elongate openings through the membrane's thickness, through which pores the release of the MEMS device 2 takes place, which is the etching away of a sacrificial layer deposited onto the MEMS device prior to the deposition of the membrane layer 3. This masked anodization process using photoresist has the drawback that the openings in the photoresist do not appropriately limit the anodization process to the desired area, as shown in figure 2. This figure shows the substrate 1, with a dielectric thin film 11 on the surface of the substrate, and a membrane layer 12 on the thin film 11. A photoresist mask 13 covers the membrane film except for a portion 14 which defines the area of the membrane which is to be anodized. As described in more detail further, anodization generally takes place by submerging the substrate into an anodization bath. When the substrate is left too long in the anodization bath, anodization continues until an anodized region 15 is formed which is too wide (see borders 16), i.e. unwanted continuous growth of the anodized region occurs.

[0008] Especially when applying the anodization voltage to a full wafer or large area substrate comprising the layer to be anodized and leaving the substrate (wafer) in the anodization bath results in said unwanted continuous growth of the anodized region beyond the limits defined by the photoresist mask. The problem of performing the masked anodization process on a full wafer scale is the

fact that areas defined by the masks being present in the central areas (middle) of the substrate (wafer) surface are not yet completely anodized while the areas defined by the masks being present around the substrate (wafer) edges are already completely anodized and will become over-anodized. The problem of unwanted continuous growth is caused by edge peeling (resulting in "undercut") of the photoresist mask due to:

(1) Attack by the high-acidity level electrolyte,
(2) Expansion of the AlOx thin film, and
(3) Gas formations occurring during the anodization process.

[0009] Hence there still exists a problem in state of the art techniques to provide a reliable and controllable method for providing precisely-defined anodized patterns within a conductive layer using a photoresist mask, and the application of such anodized patterns to provide for example a thin film vacuum packaging for NEMS/MEMS.

Summary of the invention

[0010] It is an object of the invention to provide an improved method for creating precise patterns of anodized material within an anodizable layer by means of masked anodization. More specifically it is an object to create precise patterns of a dielectric or porous material within a conductive thin film using masked anodization. It is thereby in particular an object to provide an improved and cost-efficient masked anodization process for application in manufacturing of semiconductor devices on (full) wafer scale to make the anodization process applicable in large scale production of semiconductor devices.

[0011] It is further an object of embodiments of the present invention to provide a reliable and controllable method for performing wet anodization processes which locally transform an anodizable layer e.g. a conductive (metal) layer into an anodized layer e.g. a dielectric or porous layer. It is the goal of the invention to perform said anodization uniformly on a (full) wafer scale.

[0012] A further object is to provide a microelectronic process technology for Nano- and Micro Electro Mechanical Systems (NEMS/MEMS) in order to achieve a controllable and uniform (full) wafer scale encapsulation or packaging process for said NEMS/MEMS devices.

[0013] The above objectives are accomplished by a method and device according to the present invention. The present invention solves the problem of achieving a uniform and controllable anodization by surrounding a group (plurality) of mask structures with an additional surrounding mask structure. In other words the problem is solved by using an additional surrounding photoresist or other mask structure with high precision which defines small areas on the surface to be exposed selectively to the anodization process without causing over-anodization leading towards delamination or undercut of the mask layer during the anodization. The presence of said additional surrounding mask structure results in self-limitation of the anodization process as the anodized border becomes anodized (oxidized) simultaneously with the anodized areas within said border, so that said border prevents further anodization current from reaching the anodized region of the mask structures to avoid unwanted further anodization. Since the electrical current needed for the anodization process is supplied at the edge (perimeter) of the substrate, surrounding every group of structures on the anodization mask with an additional surrounding mask structure (defining a borderline of anodized material) results in self-limitation of the anodization process as the anodized border becomes simultaneously anodized (oxidized) and prevents further anodization current from reaching the anodized region. The additional surrounding mask structure (defining the borderline or protection ring) may be applied at different scales during the mask design for the anodization process (i.e. the borderline can surround a small group or a large group of structures, or possibly surround the whole substrate (wafer). The width of the additional surrounding mask structure and the surrounded area can be chosen (or adjusted) to guarantee a full vertical anodization of the enclosed structures, and at the same time protect these structures from large lateral extensions of the anodization process.

[0014] By applying the masked anodization process according to the invention in a packaging process for NEMS/MEMS devices, an additional surrounding mask structure is surrounding a group of individual NEMS/MEMS devices and will result in self-limitation of the anodization process as the anodized border becomes simultaneously anodized (oxidized) and prevents further anodization current from reaching the anodized region of the mask structures to avoid unwanted further anodization.

[0015] It is an advantage of embodiments according to the present invention that providing the additional surrounding mask structure does not need extra processing steps as said additional mask structure may be provided simultaneously with the provision of the first mask structure(s).

[0016] The invention is thus related to a method as disclosed in the appended claims. Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

[0017] As such, the invention is related to a method for masked anodization, said method comprising the steps of

- providing a substrate,
- providing an anodizable layer on said substrate,
- providing on said anodizable layer at least one first mask defining one or more first structures to be an-

odized and an additional second mask defining a second structure to be anodized, said second structure surrounding said one or more first structures,
- anodizing said anodizable layer in the regions defined by the first and second mask in order to create anodized structures,
- removing the first and second mask.

The expression 'anodizing said anodizable layer in the regions defined by the first and second mask' means that the anodization continues until the layer is anodized over the totality of its thickness in said regions.
With 'surrounding' is meant that the second structure forms a closed ring structure around the first structure(s).

[0018] According to the preferred embodiment, the step of anodizing said anodizable layer is performed by inserting the substrate in an electrolyte and applying a voltage (or electrical current) on said substrate.

[0019] The step of anodizing said anodizable layer may also be performed using a two-step anodization process comprising a first anodizing step to form a first anodized layer, followed by a second anodizing step after etching away the first anodized layer.

[0020] According to a preferred embodiment, the step (s) of anodizing is(are) performed by inserting the substrate in an electrolyte selected from the group consisting of sulphuric acid, phosphoric acid, oxalic acid, hydrofluoric acid, ethanol, isopropyl alcohol, and mixtures of these chemicals.

[0021] According to the preferred embodiment, said anodizing step(s) produce(s) elongate pores in said anodized structure(s), said pores extending from the front surface to the back surface of said anodizable layer.

[0022] According to an embodiment, the anodizable layer is an Al layer and the step(s) of anodizing is(are) performed by inserting the substrate in a sulphuric-acid based electrolyte at temperatures in the range of 20-40°C and applying a voltage of around 20V.

[0023] According to an embodiment, the anodizable layer is a metal layer which is to be anodized to form a metal oxide layer, and said anodization bath comprises an etchant suitable for etching said oxide, and wherein said anodization step comprises a first time period during which said voltage is applied, said voltage being removed at the end of said first time interval, and a second time period following said first time period, during which second period the substrate is left in said bath, to thereby remove a barrier layer at the bottom of said pores.
In the latter embodiment, said metal may be aluminium and said etchant phosphoric acid.

[0024] According to an embodiment :

- said step of providing a substrate comprises depositing a sacrificial layer onto a base substrate,
- said anodizable layer is provided onto said sacrificial layer,
- said first mask defines a structure to be a anodized,
- said anodizing step(s) produce(s) elongate pores in said anodized structure, said pores extending from the front surface to the back surface of said anodizable layer,
- at least a portion of the sacrificial layer is removed through said pores, so as to form a cavity, and
- a sealing layer is applied onto said anodized structures in order to seal off said cavity.

[0025] In the latter embodiment, the sacrificial layer can be made of a material selected from the group consisting of polycrystalline SiGe, oxide-based or nitride-based films, polymer, single crystal or polycrystalline Si. In the latter embodiment, said substrate may comprise a NEMS/MEMS device, which is(are) encapsulated in said cavity.

[0026] In the latter case, the step of removing at least some of the sacrificial material is performed using a selective wet or dry etching that does not damage the enclosed NEMS/MEMS device.

[0027] In the latter embodiment, the sacrificial layer may be silicon-oxide and the selective etching may be performed using a vapor-phase hydrofluoric (HF) acid mixed with other gases such as nitrogen and ethanol or water vapor in a reduced-pressure chamber.

[0028] In the latter embodiment, the sacrificial layer may be a polymer-based material and the selective etching may be performed using a dry plasma etching in a low-pressure chamber in the presence of oxygen ions.

[0029] In the latter embodiment, the sealing layer may be :

- a conductive layer such as Al, Cu, Ni, polycrystalline Si or SiGe, or
- a dielectric material such as oxide- or nitride-based silicon compounds, or
- a polymer, or
- a combination or a stack of two or more materials, Said sealing layer may be deposited using an evaporation technique or a chemical (CVD) or physical vapour deposition (PVD) technique in a low-pressure chamber..

[0030] In the method of the invention, the anodizable layer may be a metal layer or semiconducting layer. Said anodizable layer may be selected from the group consisting of Al, Ta, Ti, Cu, Ni, polycrystalline Si, polycrystalline SiGe.

[0031] In the method of the invention, the mask structures may be formed by photolithographic patterning of a photosensitive layer.

Brief description of the figures

[0032] Figure 1 illustrates the concept of thin film MEMS packaging using a porous membrane as known in the prior art.

[0033] Figure 2 illustrates the large lateral extension of the Al anodization process using a photoresist mask

(problem to be solved by the invention).

[0034] Figure 3a illustrates an intermediate stage during the anodization process of the invention whereby the anodization current may still reach the anodization region before the vertical anodization is complete.

[0035] Figure 3b is a top view of a wafer comprising several masks and provided with a ring electrode arranged along the circumference of the wafer.

[0036] Figure 3c illustrates the final stage of the anodization process of the invention (when the vertical anodization is complete) whereby the borderline is completely anodized (oxidized) forming a dielectric isolation ring around the anodization region which blocks further supply of the electric charges needed for anodization.

[0037] Figure 4a-4d illustrate different steps in a suitable process flow to use the masked anodization process for thin film packaging of a NEMS/MEMS device according to embodiments of the invention.

[0038] Figure 4a illustrates the step of depositing a metal layer on top of the sacrificial layer covering the NEMS/MEMS structure and interconnects.

[0039] Figure 4b illustrates the step of masked anodization and thin barrier oxide layer removal.

[0040] Figure 4c illustrates the step of removing the sacrificial layer and depositing a sealing layer.

[0041] Figure 4d illustrates the step of removing the layers covering the metal pads for electrical access and illustrates the final NEMS/MEMS device encapsulation.

[0042] Figure 5 illustrates the form the pores formed by anodization of an Aluminium layer, and the oxide barrier layer formed at the bottom of the pores.

[0043] Figure 6 illustrates an example of a mask design defining a ring structure in accordance with the invention.

[0044] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. Any reference signs in the claims shall not be construed as limiting the scope. In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of the invention

[0045] According to an aspect of the invention a method is provided for uniform and controllable masked anodization, said method comprising at least the steps of (with reference to figure 3) :

- providing (i.e. supplying or producing) a substrate (10,11), and then
- providing an anodizable layer (12) on said substrate, and then
- providing on said anodizable layer (12) at least one first mask (20) defining the dimensions of one or more first structures (21) to be anodized and an additional second mask (22) defining a second structure (23) to be anodized, said second structure surrounding said first structure(s), and then
- anodizing said anodizable layer (12) in the regions defined by the first (20) and second (22) mask in order to create anodized structures (21,23), and then
- removing the mask structures (20,22).

[0046] Figure 3a shows again a substrate 10. In this embodiment (but not limiting to the scope of the invention), a dielectric layer 11 is deposited on the substrate, which may for example be a sacrificial layer. Layer 12 is a membrane layer and layer 13 is a mask layer, preferably a patterned photoresist layer. According to the invention, the mask layer comprises at least one first mask 20, which defines the areas 21 which are to be anodized. The mask layer further comprises a second mask 22 which defines an area 23 which surrounds said one or more first areas 21 to be anodized, forming a closed ring structure (not necessarily a circular-shaped ring) around said areas 21. Figure 3b shows a top view of a semiconductor wafer 30 carrying on its surface the mask layer 13 which comprises a plurality of masks 20 which define areas 21 to be anodized. Around each mask 20 (and thus around each group of areas 21), the mask layer defines a ring structure 23 to be anodized which encircles the masks 20. The 'second mask structure' 22 thus corresponds to the totality of the mask layer 13 minus the mask structures 20.

[0047] Along the edge of the wafer 30, an electrode 31 is placed, which is in electrical contact with the layer 12 to be anodized (preferably a metal layer, see further). The electrode 31 will play the role of the anode during the anodization. This assembly is submerged in an anodization bath, filled with an electrolyte. The second electrode (the cathode) is part of the anodization bath (preferably a metal plate immersed in the anodization bath, facing the front side of the wafer, i.e. the side carrying the masks 20/22). When anodization starts, the charge flows in the direction shown by the arrows 32 in figures 3a and 3b, i.e. starting from the outer edge of the wafer 30, and from the outer edge of each mask 20 towards the centre.

[0048] The drawing in figure 3a illustrates an intermediate stage during the anodization process of the invention whereby the anodization current (charge flow) may still reach the anodization regions 21 before the vertical anodization is complete. Figure 3c illustrates the final stage of the anodization process of the invention (when the vertical anodization is complete) whereby the ring structure 23 is completely anodized (oxidized), thereby acting as borderline and hence forming a dielectric isolation ring around the anodization regions 21, which blocks further supply of the electric charges needed for anodization.

[0049] According to embodiments, the material for use as anodizable layer 12 may be a metal or semiconducting layer which is selected from Al, Ta, Ti, Cu, Ni, polycrystalline Si, polycrystalline SiGe, etc... For example Aluminum layers may be used of around 0.5-10μm thick which may be deposited e.g. by using a sputtering process per-

formed at low temperature. Prior to anodizing, the Al layers may be cleaned by placing them in an ultrasonic bath of deionized water.

[0050] According to embodiments, the first and second mask structures 20,22 may be formed by state of the art photolithographic patterning of a photosensitive layer (resist). The advantage of using a photoresist (photosensitive layer) is the simplicity of forming the mask structures compared to other techniques involving deposition and patterning (by chemical or physical etching) of another mask material.

[0051] According to embodiments, the step of anodizing said anodizable layer 12 may lead to the formation of a porous (metal) layer. The pores (holes) in said porous layer may have a length greater than ten times their width, and a width in the range 5-200 nm, e.g. 20 nm or between 20nm and 200 nm, or between 5 and 20 nm.

[0052] According to embodiments, the step of anodizing said anodizable (metal) layer 12 may be performed by means of a one-step anodization process. As already mentioned, said one step-anodization process may be performed by inserting the substrate in an electrolyte and applying a voltage (or electrical current) on said substrate. Said electrolyte may be sulphuric acid, phosphoric acid, oxalic acid, hydrofluoric acid, ethanol, isopropyl alcohol, or a mixture of these or other chemicals. By applying a voltage in the range of 5-200V, pores are formed on the surface of the anodizable (metal) layer which are distributed randomly or in a hexagonal order. To achieve better hexagonal order of the pores, optimized process conditions (anodization voltage, electrolyte, and temperature) should be chosen to reach the best volume expansion factor for the porous layer.

[0053] According to embodiments, the step of anodizing said anodizable (metal) layer 12 may be performed by means of a two-step anodization process. Said two step-anodization process may be performed by first applying a short anodizing step which patterns the surface of the anodizable (metal) layer 12. Later, this patterned surface acts as self-assembled marks for the second anodizing step [Mei et al., "Formation mechanism of alumina nanotubes and nanowires from highly ordered porous anodic alumina template," Journal of Applied Physics, Vol. 97, 034305 (2005)]. An extended second anodizing step, after etching away the first anodized layer not only improves the regularity of the cell arrangement but also reduces the number of defects and dislocations. A third anodizing step does not significantly improve the ordering of the pores and the size of the well-ordered domains.

[0054] According to embodiments, the voltage (current) applied to achieve anodization of the anodizable (metal) layer is applied between the anodizable (metal) layer on the substrate and the electrolyte or a reference electrode therein. The voltage applied for anodizing lies in the range between a few volts and a few hundreds of volts. A voltage of 20V can be used for example when performing anodization in a sulphuric-acid based electrolyte at temperatures in the range of 20-40°C.

[0055] According to embodiments, when the anodization of the additional structure 23 (vertical anodization) is complete, said additional structure forms a protective structure 23 acting as a dielectric isolation ring which blocks further supply of the electric charges needed for anodization and thereby avoids unwanted extension of the anodized structures 21 surrounded by the additional structure 23.

[0056] According to embodiments, the anodizable (metal) layer may be an Aluminum layer and the anodization process conditions may be optimized for a given electrolyte, such as anodizing voltage and temperature, and acid concentration. Synthesis of porous aluminium oxide (AlO_x) membranes can start from a sputter-deposited or evaporated Al film. The main anodizing parameters to be selected are dependent on the type of the electrolyte since this affects the diameter of the pores and the inter-pore distance, voltage and temperature, and the sequence of anodizing steps. The anodization may occur within a glass- or Teflon-based chamber in which a conductive reference electrode is inserted. The substrate 30 carrying the metal layer 12 to be anodized may be inserted into the anodization chamber by means of a Teflon- or polymer-based holder which protects the edges and backside of the substrate from contacting the anodization electrolyte. The anodization process may be performed by applying the anodization voltage (or current) between the reference electrode and the anodizable (metal) layer 12 on the substrate. Once the vertical anodization is complete and the dielectric isolation rings 23 (borderlines) are formed within the additional mask structure 22, the anodization process is automatically stopped because of the impossibility of electric charges to travel through the isolation rings 23.

[0057] According to a further aspect of the invention a method is provided for (hermetically) sealing a cavity in a semiconductor device thereby using the uniform and controllable masked anodization process described in previous embodiments, said method comprising at least the steps of (with reference to figure 4) :

- providing a sacrificial layer (40) on a substrate wherein a micro cavity is to be located in said sacrificial layer (40), and wherein said substrate comprises a base substrate 10, a dielectric layer 11 and a MEMS or NEMS device 50, provided with electrical connections structures 51 to said device 50, and then
- providing a metal membrane layer (41) having a thickness greater than 0.5 micron on top of the sacrificial layer (40), and then
- providing on said metal layer (41) a first mask (42) defining the dimensions of a first structure 43 to be anodized, said dimensions corresponding to the dimensions of the cavity and an additional second mask defining a structure (not shown) to be anodized surrounding said first structure (43), and then
- anodizing said metal layer (41) to form a porous metal oxide layer (43) having pores (holes) extending

from the front surface of said porous metal oxide layer (43) towards the back surface of said porous metal oxide layer (43),

- removing the mask structures and at least some of the sacrificial layer (40) through the porous metal oxide layer (43), to form the micro cavity (44), and
- sealing (closing) with a sealing layer 45 the pores of said porous layer (43) in order to form a (hermetically) sealed cavity (44).

[0058] Figure 4a-4d illustrate different steps in a suitable process flow to use the masked anodization process for thin film packaging of a NEMS/MEMS device.

[0059] According to embodiments, the substrate (10,11,50,51) and the sacrificial layer (40) may be any substrate and layer used and compatible with semiconductor processing, more particular NEMS/MEMS processing. Examples of substrates, which may be used are, for example, single crystal or polycrystalline Si, single crystal or polycrystalline Ge, glass, quartz, polymer, etc.

[0060] As shown, fragile devices 50 may be located in the cavity, said fragile device may be any NEMS/MEMS device requiring a vacuum or controlled atmosphere and pressure encapsulation.

[0061] According to embodiments, the sacrificial layer 40 may be made of a material selected from polycrystalline SiGe, oxide-based or nitride-based films, polymer, single crystal or polycrystalline Si, etc. Said sacrificial material may be a material which can be removed using a wet or dry etching technique that does not extensively damage the enclosed NEMS/MEMS device (selective etching). For example a silicon oxide sacrificial layer 40 can be removed by vapor-phase hydrofluoric (HF) acid mixed with other gases (such as nitrogen and ethanol or water vapor) in a reduced-pressure chamber. Such diluted vapor-phase HF mixture can remove the sacrificial silicon oxide layer without reacting with the NEMS/MEMS device or the porous layer surrounding the cavity.

[0062] According to embodiments, the sacrificial material 40 is filling a cavity 44 which is present under said membrane layer 41. The cavity can further comprise a NEMS/MEMS device 50, the functioning and structure of which is inert to said sacrificial material etchant. It can comprise a fragile object, on which substantially no material may be deposited during the closure process to guarantee the proper working and lifetime of the device. In certain embodiments the cavity 44 is closed except for said pores and optionally a vent hole (not shown). A vent hole is an additional hole which connects the cavity with the outside.

[0063] According to embodiments, the material for use as metal layer 41 may be a metal or semiconducting layer which is selected from Al, Ta, Ti, Cu, Ni, polycrystalline Si, polycrystalline SiGe, etc... For example Aluminum layers of around 0.5-10μm thick may be deposited by a sputtering process performed at low temperature. Prior to anodizing, the Al layers may be cleaned by placing them in an ultrasonic bath of deionized water.

[0064] According to embodiments, the step of anodizing said metal layer in order to form a porous metal oxide layer is such that a layer with pores (holes) is achieved, also referred to as porous membrane. Said porous membrane has a front main surface and a back main surface and the pores (holes) in said membrane (holes can be a set of sub-surface interconnected pores) extend from the front main surface towards the back main surface.

[0065] According to embodiments the pores (holes) in said porous layer may have a length greater than ten times their width, and a width in the range 5-200 nm, e.g. 20 nm or between 20nm and 200 nm, or between 5 and 20 nm.

[0066] According to the invention, when the anodization of the additional structure (vertical anodization) is complete, a protective structure is formed acting as a dielectric isolation ring surrounding the NEMS/MEMS devices which blocks further supply of the electric charges needed for anodization and thereby avoids unwanted extension of the anodized structures surrounded by the additional structure.

[0067] According to embodiments, a thin oxide barrier layer may be present after anodization at the bottom of the pores (holes) of the porous oxide layer 43 and may be removed by leaving the wafer for longer time in the anodization electrolyte after the completion of the vertical anodization process (after the end of the anodization current) and by further adding a small amount of an etching chemical to the anodization electrolyte. This allows for chemical etching of a very small portion of the porous layer because the anodization electrolyte (mixture) and temperature can be chosen to provide slow etching of the porous oxide layer (for example by adding a small amount of phosphoric acid which is an etchant of aluminium oxide). The advantage of performing the barrier oxide layer removal in the anodization electrolyte is that the inner surface of the pores (holes) is already wet upon completion of the anodization process which facilitates the access of the etching chemicals to the bottom of the pores. The oxide barrier layer may alternatively be removed by a separate wet or dry chemical etching step after the anodization step, although difficulties are expected when attempting to use wet etching techniques because porous aluminium oxide may have hydrophobic properties that prevent the etching chemicals from penetrating the narrow pores to reach the barrier oxide layer.

[0068] Figure 5a illustrates the above described barrier layer. The figure illustrates the elongate shape of the pores 60 in the anodized region 21 shown in figure 3c. The barrier layer is formed by the small amount 61 of oxide at the bottom of the pores 60. By leaving the substrate in the anodization bath for a given time after the anodization current has been stopped, the additional etchant in the bath ensures the removal of the barrier layer (see figure 5b).

[0069] According to embodiments, the step of removing the sacrificial material 40 under the porous Al layer

(membrane) may be performed using an etchant until said sacrificial material is at least partially removed (etched away) through the pores 60 (holes) in said porous layer 43. The sacrificial material may be an oxide-based compound (such as SiO_2) and the removal of this material may be performed in a reduced-pressure chamber containing a mixture of gases including an etchant of the sacrificial material (such as hydrofluoric acid) in a vapor form in addition to other gases such as ethanol vapor, nitrogen, or water vapor. Alternatively the sacrificial layer 40 may be a polymer-based material such as photoresist, which can be removed through the pores of said porous 43 layer by dry plasma etching in a low-pressure chamber in the presence of oxygen ions. The removal of the sacrificial material results in a cavity 44 that may be used to host a NEMS/MEMS structure.

[0070] According to embodiments, the sealing layer 45 may be deposited by an evaporation technique or a chemical (CVD) or physical vapour deposition (PVD) technique in a low-pressure chamber. Said sealing layer 45 may be a conductive layer such as Al, Cu, Ni, polycrystalline Si or SiGe. Alternatively, the sealing layer 45 may be a dielectric material such as oxide- or nitride-based silicon compounds, or a polymer. Alternatively, the sealing layer may be a combination or a stack of two or more materials. The very high aspect ratio of the pores 60 of the porous membrane 43 prevents the deposition of the sealing layer 45 onto the NEMS/MEMS structure 50 and thus prevents damage or alteration of the NEMS/MEMS structure. Deposition of the sealing layer results in a sealed cavity 44 that may host a NEMS/MEMS device.

[0071] According to embodiments, the cavity 44 may be sealed under controlled atmosphere and pressure by controlling the gases and pressure present in a chamber used to deposit the sealing layer which in turn closes the pores (holes) 60 leading to the formation of a sealed cavity 44 with controlled atmosphere and pressure.

DEFINITIONS

[0072] Where reference is made in embodiments of the present invention to the term 'a controlled atmosphere', a controlled constitution of ambient gas is meant. The notion of 'horizontal' is defined as substantially orthogonal to the direction of a gravitational field, for example the earth's gravitational field.

[0073] For the purpose of this disclosure, the notion of 'essentially no material passing through the openings' should be understood as 'no or only a limited amount of material passing in and/or through the openings'. In the context of sealing of a cavity that comprises a fragile device, it should be such that the proper working of the device is not affected by the limited amount of material that may pass.

[0074] For the purpose of this disclosure, the term Nano- and Micro-Electro-Mechanical Systems (NEMS/MEMS) refers to miniature systems with both electrical and non-electrical (e.g. mechanical) functionalities. Examples of NEMS/MEMS devices are inkjet printer heads, miniature mechanical switches, and sensors for applications that include accelerometers (e.g. for air bags in cars) and gyroscopes (e.g. for roll-over detection in cars).

[0075] For the purpose of this disclosure, the term "zero-level packaging" refers to the encapsulation of NEMS/MEMS structures at the wafer level before dicing the individual NEMS/MEMS devices. Because the NEMS/MEMS structures themselves are often freestanding and fragile they must be encapsulated at the wafer level to avoid damage during wafer dicing and in use. Additionally a porous thin film (membrane) may be part of said encapsulation. The membrane is preferably provided directly above the NEMS/MEMS device. After removing the sacrificial layer (surrounding the NEMS/MEMS structure) through the membrane, the membrane is sealed in order to provide the desired zero level encapsulation and to enclose the required atmosphere at a desired pressure in the cavity. One advantage of this approach is that it reduces the thickness and area of the packaged device compared to the traditional approach.

EXAMPLES

[0076] By way of illustration, embodiments of the present invention not being limited thereto, a number of further particular examples are discussed below, illustrating features and advantages of embodiments according to the present invention.

[0077] In a first particular example, anodization of a 1μm-thick Al layer (deposited by sputtering on top of a silicon oxide layer on 200mm Si wafer) has been performed using a photoresist mask not including the border line structure resulting in a large unwanted extension of the anodization region width from 160μm up to 800μm as shown in figure 2. The anodization process is performed in a Teflon-based chamber housing a sulfuric-acid-based electrolyte. The anodization temperature and voltage used here are within the range of 20-30°C and 10-20V respectively. By performing the same anodization process of an Al layer using a photoresist mask defining a border line 23 (ring) surrounding a plurality of other structures 21 as shown in figure 6, the anodization region width has been well controlled by the photoresist mask resulting in only approximately 6μm lateral extension of the edges of the anodized regions 21. This means that in the areas 25, substantially no undercut of the photoresist occurs. The latter is illustrative for the good control of the anodization process using a simple photoresist mask comprising a borderline (ring) which surrounds the anodized region and illustrates advantages of embodiments according to the present invention.

[0078] In a second particular example, a thin film vacuum package has been constructed according to embodiments of the invention and the process flow of Figures 4a-4d by following the subsequent steps :

1. Deposition and patterning of a 3μm-thick silicon oxide layer 40 on top of a 200mm Si wafer 10+11.
2. Sputter-deposition of a 1.5μm-thick Al layer 41 on top of the sacrificial layer 40 as shown in Figure 4a.
3. Masked anodization of the Al layer using a photoresist mask 42 in a sulphuric-acid-based electrolyte at 30°C by applying a constant voltage of 20V as shown in Figure 4b.
4. Upon completion of the vertical anodization process and termination of the anodization current, the resulting porous AlOx structures 43 are left in the anodization electrolyte for a period of 20-30 minutes to allow for wet chemical etching of a small portion of the AlOx layer to (at least partially) remove the barrier AlOx layer 61 present at the bottom of the pores (holes) - see figure 5.
5. The wafer is placed in a low-pressure chamber and exposed to a mixture of HF vapor, ethanol vapor and nitrogen to remove the sacrificial layer 40 below the porous AlOx structures 43 resulting in cavities 44 as shown in Figure 4c.
6. The cavities 44 are sealed by deposition of a 4μm-thick silicon nitride layer 45 in a vacuum chamber using a PECVD technique as shown in Figure 4c, resulting in thin film vacuum packages as shown in Figure 4d.

[0079] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. The invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

[0080] The foregoing description details certain embodiments of the invention. It will be appreciated, however, that no matter how detailed the foregoing appears in text, the invention may be practiced in many ways, and is therefore not limited to the embodiments disclosed. It should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to include any specific characteristics of the features or aspects of the invention with which that terminology is associated.

Claims

1. A method for masked anodization, said method comprising the steps of

   - providing a substrate (10,11),
   - providing an anodizable layer (12) on said substrate,
   - providing on said anodizable layer at least one first mask (20) defining one or more first structures (21) to be anodized and an additional second mask (22) defining a second structure (23) to be anodized, said second structure surrounding said one or more first structures (21),
   - anodizing said anodizable layer (12) in the regions defined by the first and second mask (20,22) in order to create anodized structures (21,23),
   - removing the first and second mask (20,22).

2. Method according to claim 1, wherein the step of anodizing said anodizable layer (12) is performed by inserting the substrate in an electrolyte and applying a voltage (or electrical current) on said substrate.

3. Method according to claim 1 or 2, wherein the step of anodizing said anodizable layer is performed using a two-step anodization process comprising a first anodizing step to form a first anodized layer, followed by a second anodizing step after etching away the first anodized layer.

4. Method according to any one of claims 1 to 3, wherein the step(s) of anodizing is(are) performed by inserting the substrate in an electrolyte selected from the group consisting of sulphuric acid, phosphoric acid, oxalic acid, hydrofluoric acid, ethanol, isopropyl alcohol, and mixtures of these chemicals.

5. Method according to any one of clams 1 to 4, wherein said anodizing step(s) produce(s) elongate pores (60) in said anodized structure(s) (21), said pores extending from the front surface to the back surface of said anodizable layer (12).

6. Method according to claim 5, wherein the anodizable layer (12) is an Al layer and wherein the step(s) of anodizing is(are) performed by inserting the substrate in a sulphuric-acid based electrolyte at temperatures in the range of 20-40°C and applying a voltage of around 20V.

7. Method according to claim 5, wherein the anodizable layer (12) is a metal layer which is to be anodized to form a metal oxide layer, and wherein said anodization bath comprises an etchant suitable for etching said oxide, and wherein said anodization step comprises a first time period during which said voltage

is applied, said voltage being removed at the end of said first time period, and a second time period following said first time period, during which second period the substrate is left in said bath, to thereby remove a barrier layer (61) at the bottom of said pores (60).

8. Method according to claim 7, wherein said metal is aluminium and said etchant is phosphoric acid.

9. Method according to any one of claims 2 to 8, wherein :

- said step of providing a substrate comprises depositing a sacrificial layer (40) onto a base substrate (10, 11, 50, 51) ,
- said anodizable layer (41) is provided onto said sacrificial layer (40),
- said first mask (42) defines a structure (43) to be a anodized,
- said anodizing step(s) produce(s) elongate pores (60) in said anodized structure, said pores extending from the front surface to the back surface of said anodizable layer,
- at least a portion of the sacrificial layer (40) is removed through said pores, so as to form a cavity (44), and
- a sealing layer (45) is applied onto said anodized structure (43) in order to seal off said cavity (44).

10. Method according to claim 9 wherein the sacrificial layer (40) is made of a material selected from the group consisting of polycrystalline SiGe, oxide-based or nitride-based films, polymer, single crystal or polycrystalline Si.

11. Method according to claim 9 or 10, wherein said substrate comprises a NEMS/MEMS device (50), which is (are) encapsulated in said cavity (44).

12. Method according to claim 11, wherein the step of removing at least some of the sacrificial material (40) is performed using a selective wet or dry etching that does not damage the enclosed NEMS/MEMS device (50).

13. Method according to any one of claim 9 to 12 wherein the sacrificial layer (40) is silicon-oxide and the selective etching is performed using a vapor-phase hydrofluoric (HF) acid mixed with other gases such as nitrogen and ethanol or water vapor in a reduced-pressure chamber.

14. Method according to any one of claim 9 to 12 wherein the sacrificial layer (40) is a polymer-based material and the selective etching is performed using a dry plasma etching in a low-pressure chamber in the presence of oxygen ions.

15. Method according to any one of claim 9 to 14 wherein the sealing layer (45) is

- a conductive layer such as Al, Cu, Ni, polycrystalline Si or SiGe, or
- a dielectric material such as oxide- or nitride-based silicon compounds, or
- a polymer or
- a combination or a stack of two or more materials,

and wherein said sealing layer is deposited using an evaporation technique or a chemical (CVD) or physical vapour deposition (PVD) technique in a low-pressure chamber.

16. Method according to any one of claims 1 to 15, wherein the anodizable layer is a metal layer or semiconducting layer.

17. Method according to claim 16, wherein the anodizable layer is selected from the group consisting of Al, Ta, Ti, Cu, Ni, polycrystalline Si, polycrystalline SiGe.

18. Method according to any one of the preceding claims, wherein the mask structures are formed by photolithographic patterning of a photosensitive layer.

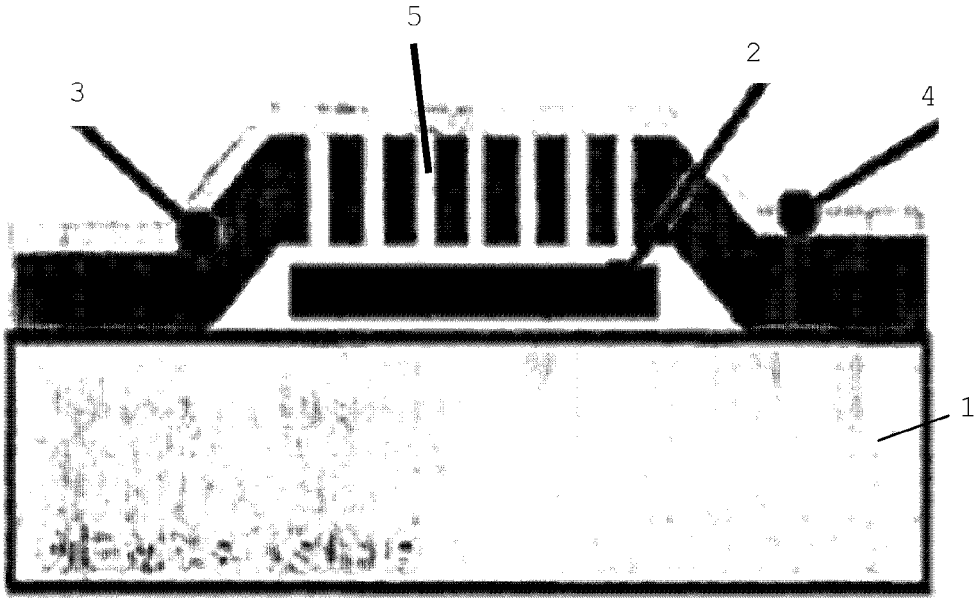

FIG. 1

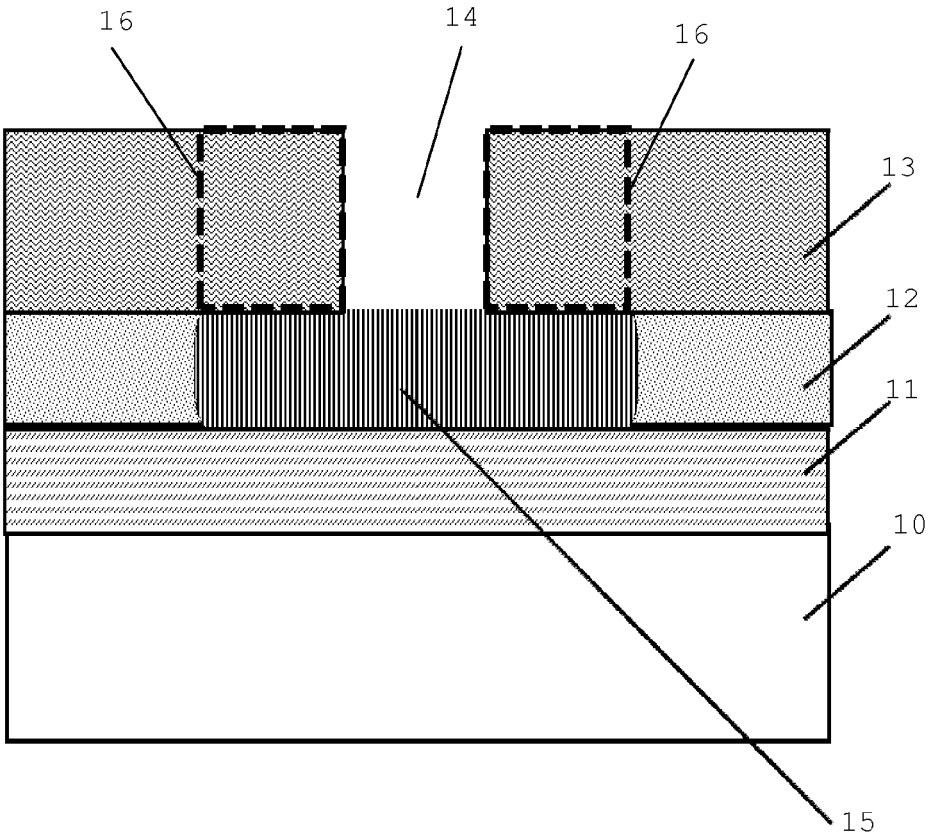

FIG. 2

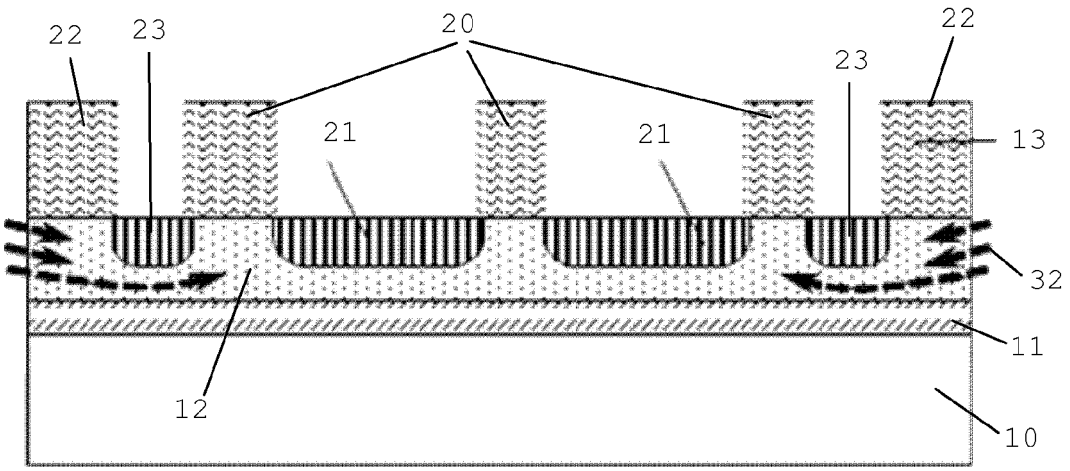

FIG. 3a

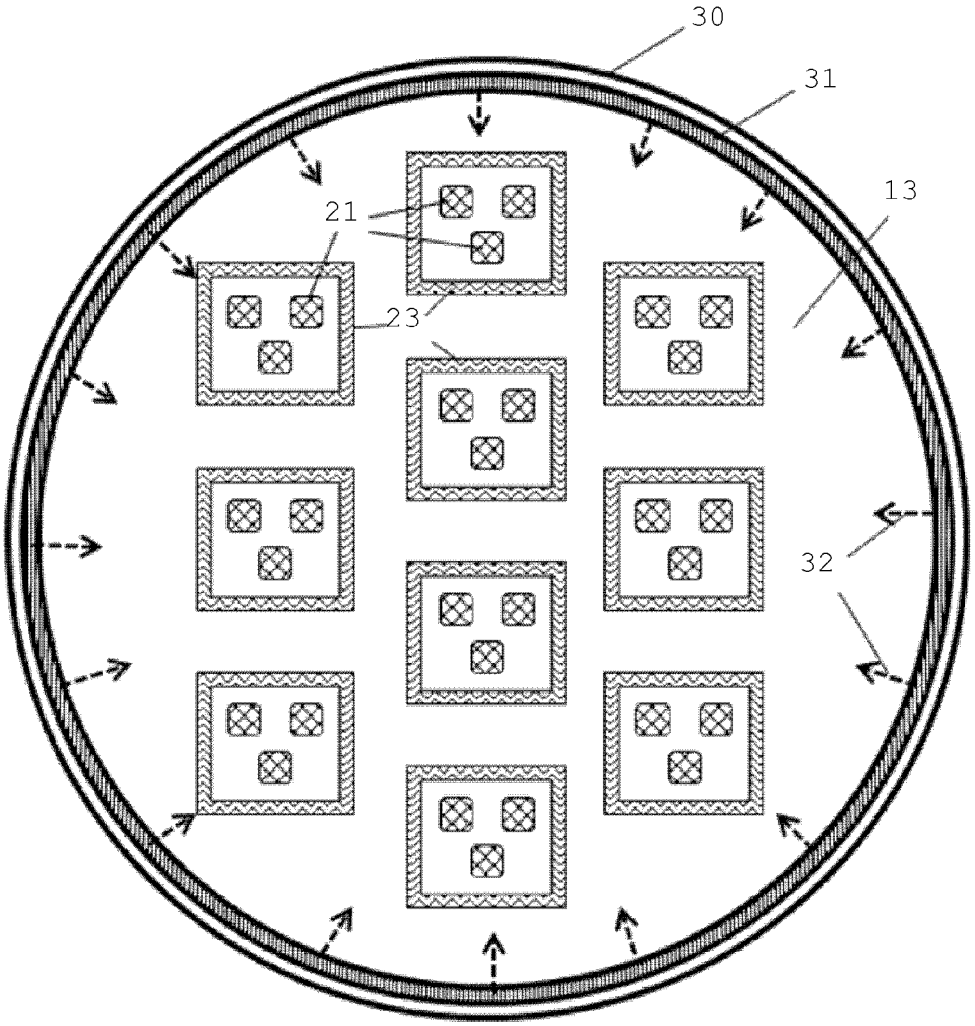

FIG. 3b

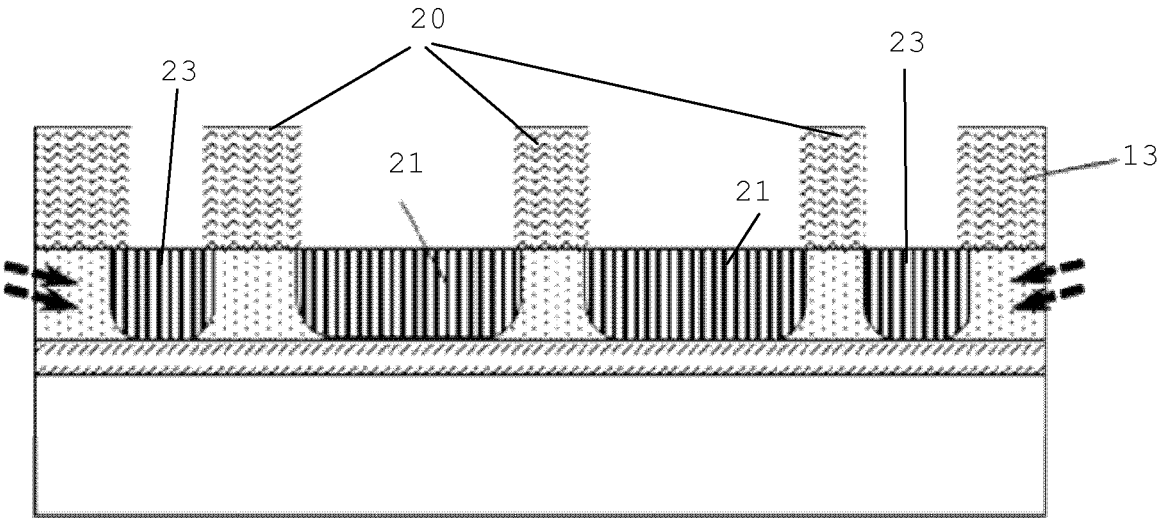

FIG. 3c

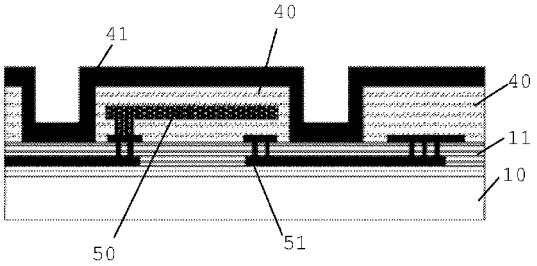

FIG. 4a

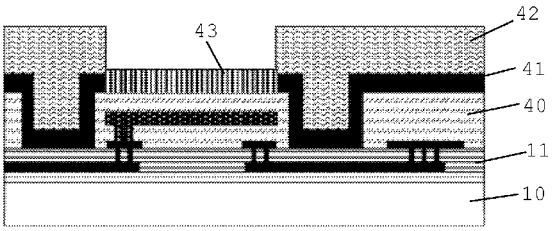

FIG. 4b

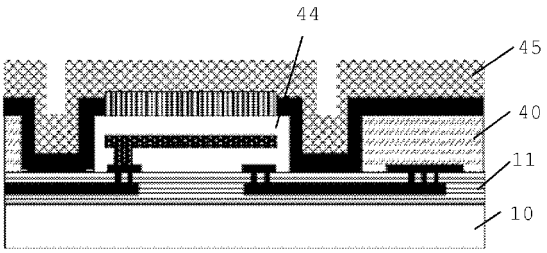

FIG. 4c

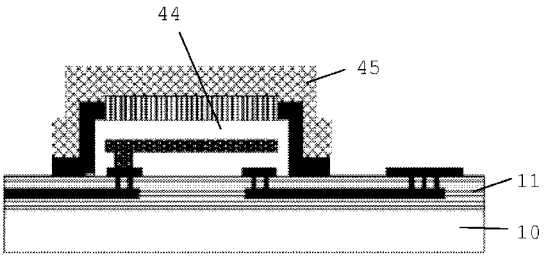

FIG. 4d

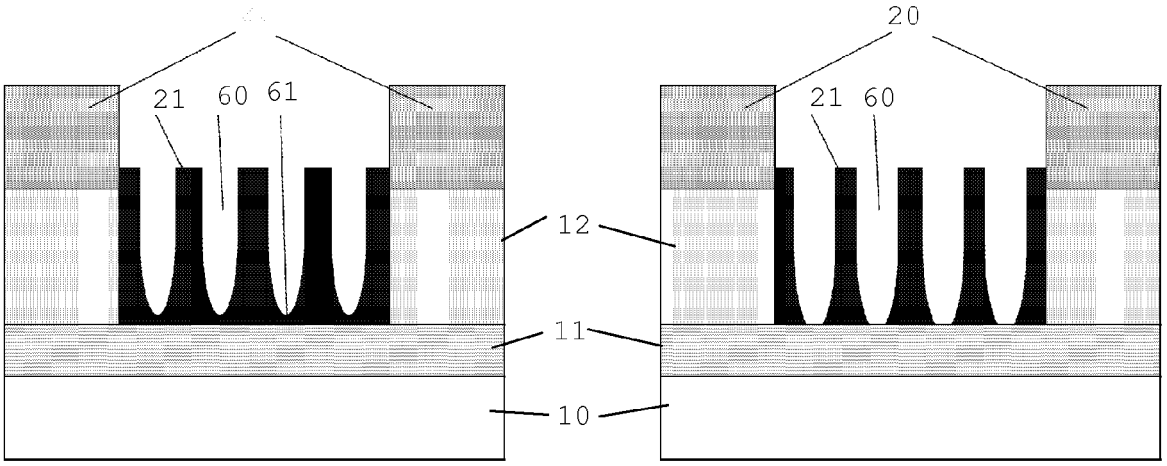

FIG. 5a

FIG. 5b

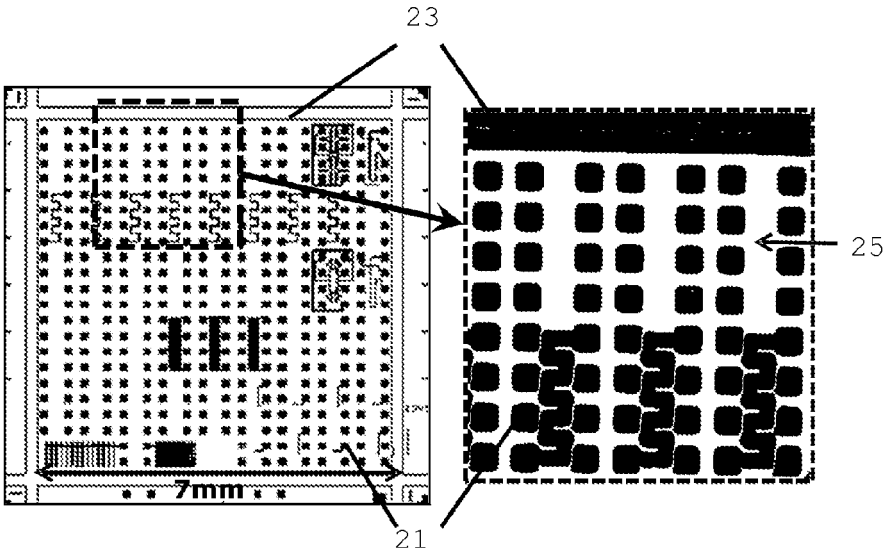

FIG. 6

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EUROPEAN SEARCH REPORT

Application Number
EP 11 16 2495

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C25D

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The Hague	30 November 2011	Suárez Ramón, C

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