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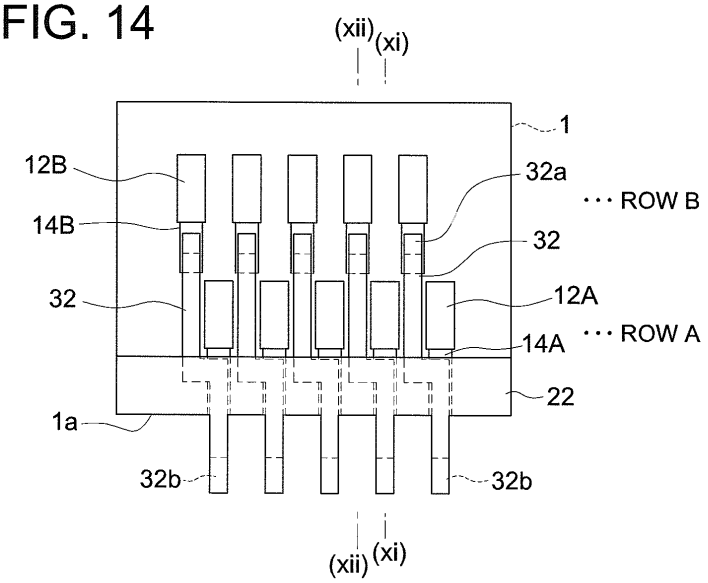
(54) **METHOD FOR MANUFACTURING INKJET HEAD**

(57) Provided is a method for manufacturing an inkjet head, wherein a plurality of first electrodes for applying electrical signals to pressure-generating elements are formed in a plurality of rows on one surface of a head chip, and second electrodes for connecting to a drive circuit are formed in such a way that each of the second electrodes electrically connects to each of the first electrodes of the head chip. An insulating layer is placed between a second electrode corresponding to one row of first electrodes and a second electrode corresponding to another adjacent first electrode in said first electrode row. The second electrodes are stacked in layers in the thickness direction of the insulating layers at each second electrode corresponding to a row of first electrodes, and the second electrodes are successively formed on the first electrode forming surface side of the head chip, one end of the second electrodes and of the insulating layers being formed to protrude at the same end side of the head chip.

FIG. 14



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Description

TECHNICAL FIELD

[0001] The present inventions relates to a method of manufacturing an inkjet head, and in particular, to a method of manufacturing an inkjet head which facilitates electric connections between drive circuits and electrodes formed on one end surface of a head chip in which a plurality of pressure chambers are disposed.

PRIOR ART

[0002] In the inkjet head, there are tendencies that liquid droplets are minimized and the nozzles are disposed densely so as to enable high resolution and high speed recording. Thus in the inkjet heads the dense nozzles are achieved by arraying a plurality of pressure chambers and a plurality of pressure generating elements to create pressure change in the plurality of the pressure chambers, in a plurality of rows in the head chip. In such head chip, on one end surface of the head chip, a plurality of electrodes to apply electric signals onto each of the pressure generating elements are formed in a plurality of rows. Therefore, electric connection with the drive circuit uses the aforesaid end surface.

[0003] In the past, as an inkjet head having the above head chip, there has been known an inkjet head that a shear mode type head chip is used as a so-called harmonica structured head chip wherein opening sections of the channels are disposed at a front end surface and a rear end surface of the head chip oppositely, in the share mode type head chip, the channels to be the pressure chambers are formed by cutting a piezoelectric substrate and driving electrodes are formed on dividing walls dividing the channels and by applying voltage on the drive electrode the dividing wall deforms thus ink in the channel is ejected from the nozzle. In the above head chip of the harmonica structure, the electrodes electrically connected with the driving electrodes disposed in pressure chambers are arrayed at the rear end surface of the head chip.

[0004] As a method to electrically connect the electrode disposed at the rear end surface of the head chip of the harmonica structure and the drive circuit, there is know a connection method that by connecting an external wiring substrate made of a hard material such as glass and ceramic, on which wiring electrodes are formed in the same pitch as that of the head chip, with the rear end surface of the head chip in a way that the end section of the substrate protrudes at a side direction of the head chip, the electrode connected with each drive electrode is lead to an end section of the external wiring substrate protruding in the side direction of the head chip, then a FPC (flexible print circuit) is connected with an end section of the external wiring substrate, whereby each driving electrode and the drive circuit is electrically connected via the wiring electrode of the external wiring substrate and the FPC (Patent Document 1 : Unexamined Japanese Patent Application Publication No. 2006-82396).

[0005] In the above method, even if the head chip has two channel rows, by forming the external wiring substrate in the way that the external wiring substrate protrudes from the end sections of the head chip opposed to each other, connection with each FPC is possible with use of both end sections of the external wiring substrate.

[0006] However, in case a head chip in which three or more channel rows are formed to make nozzles dense, each driving electrode of a channel row inside sandwiched by the channel rows at both end sections is difficult to be connected with the FPC.

[0007] In Fig. 9 of Patent Document 1, there is shown an embodiment where a through hole is formed on the external wiring substrate and is filled with a conductive material inside to form a through electrode, so that each driving electrode of the channel row inside sandwiched by the channel rows at both end sections is connected with the FPC, thus via the through electrode, each driving electrode of the channel row inside is lead to a surface of the external wiring substrate opposite to a jointing surface with the head chip. In the above method there is a problem that the through electrode has to be formed in advance on the external wiring substrate thus manufacturing of the external wiring substrate is complicated.

[0008] Also, in the above method the FPCs have to be connected to both surfaces of the end section of the external wiring substrate. Thus, it is necessary that the head chip to which the FPC is connected is turned over after connecting the FPC with one surface of the end section of the external wiring substrate, then another FPC is connected to another surface of the end section of the external wiring substrate. Therefore there is also a problem that the connection work of the FPC is cumbersome.

[0009] As one method to solve the above problems, there is known a method to lead the electrodes corresponding to the channel row inside among the plurality of the channel rows to the end section of the head chip by passing between each channel of the outside channel row adjacent to the electrode and each electrode corresponding to the channel (Patent Document 2: Unexamined Japanese Patent Application Publication No.2002-283560).

[0010] However, in the above method, since all the electrodes corresponding to all the channel rows are formed directly on the rear end surface of the head chip, as the nozzles become dense, namely as the number of the channel rows increases, areas in which forming of further electrodes is possible between the electrodes becomes narrow. As a result a width of the electrode has to be narrow, thus there is a problem that dangerousness of short circuit increases and number of the channel rows applicable is limited.

[0011] Also, in case the FPC is connected only at one end section side of the head chip so that the leading out direction from the head chip to the FPC is the same one direction, since the electrodes are led out from the head chip to the FPC in the same direction, the maximum

number of the applicable channel rows is two and it cannot be applied to a head chip having three or more than three channel rows.

[0012] Incidentally, a method to form wiring densely on a substrate is suggested in Patent Document 3: Unexamined Japanese Patent Application Publication No.2006-103117. In the above method, wiring on the substrate surface is extended in a thickness direction of the substrate passing through a through hole. Then by laminating a number of such substrates, a multilayer substrate is formed, wherein wiring of each substrate surface is led out to one surface. Therefore it is considered that instead of the aforesaid external wiring substrate, with use of the multilayer substrate each electrode formed in the array on the rear end surface of the head chip can be connected with the FPC.

[0013] However the method to extend the wiring in the thickness direction of the substrate passing through the through hole requires forming of a land at a periphery of the through hole whose diameter is larger than width of the wiring. Thus because of land having the large diameter, there is a limit of narrowing a wiring pitch for one substrate. Also, the wiring of the multilayer substrate means multilayer wiring via a through hole which is difficult to manufacture and expensive. In addition, when each electrode of the multilayer substrate is connected with each electrode formed in the plurality of the rows on the end surface of the head chip, the electrodes displace each other due to contraction and extension of the substrate material due to heat, whereby there is problem that it is difficult to connect all the electrodes with excellent reliability. Since the above problem is noticeable in high density multiple row nozzle, it is extremely difficult in the practice to connect each electrode formed in the multiple rows on the end surface of the head chip by substituting the multilayer substrate for the aforesaid external wiring substrate.

PRIOR ART DOCUMENT

PATENT DOCUMENT

[0014]

Patent Document 1: Unexamined Japanese Patent Application Publication No. 2006-82396
Patent Document 2: Unexamined Japanese Patent Application Publication No. 2002-283560
Patent Document 3: Unexamined Japanese Patent Application Publication No. 2006-103117

DISCLOSURE OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0015] An object of the present invention is to provide a method to manufacture an inkjet head which facilitates connection of an external electrode to be connected with a drive circuit with respect to each electrode in a plurality of rows arrayed on an end surface of the head chip and enables all the aforesaid external electrodes to be led out to the same end side of the head chip without creating dangerousness of disconnection and short circuit even if the number of the rows of the electrodes array on the end surface of the head chip increases.

MEANS TO SOLVE THE PROBLEM

[0016] The above problem is solved by the following.

Item 1. A method of manufacturing an inkjet head having a head chip provided with a plurality of pressure chambers to which ink is supplied and a plurality of pressure-generating elements to generate pressure change in each of the pressure chambers, wherein a plurality of first electrodes for applying electrical signals to the pressure-genecating elements are formed in a plurality of rows on one surface of the head chip, and a plurality of second electrodes are formed to electrically connect a drive circuit with each of the first electrodes, the method comprising steps of: forming the second electrodes sequentially on a first electrode forming surface side of the head chip by laminating in a thickness direction of an insulation layer, wherein the insulation layer intervenes between the second electrodes corresponding to the first electrodes in a row and the second electrodes corresponding to the first electrodes in another row adjacent to the row, in a way that an end of each of the second electrodes and the insulation layer protrude at a same end section side of the head chip.

Item 2. The method of manufacturing the inkjet head of item 1, wherein each of the second electrodes corresponding to the first electrodes in another row adjacent to the row are formed so as to overlap each other in the thickness direction of the insulation layer at a position protruding to the same end section side of the head chip.

Item 3. The method of manufacturing the inkjet head of item 1 or 2, wherein by forming the second electrode corresponding to each of the first electrodes in the row of the first electrodes in advance on a surface to be contact with a first electrode forming surface of the insulation layer formed at first with respect to the first electrode forming surface side of the head chip, each of the first electrodes in the row of the first electrodes is electrically connected with the second electrode formed in advance by jointing the insulation layer and the head chip.

Item 4. The method of manufacturing the inkjet head of any one of items 1 to 3, wherein the second electrodes formed on a surface of the insulation layer on opposite side to the first electrode forming surface side of the head chip are electrically connected with the corresponding first electrodes via the surface on

which the second electrodes are formed and an end surface adjacent to the surface thereof

Item 5. The method of manufacturing the inkjet head of any one of items 1 to 3, wherein the second electrodes formed on a surface of the insulation layer on opposite side to the first electrode forming surface side of the head chip are electrically connected with the corresponding first electrodes via through holes formed on the insulation layer

Item 6. The method of manufacturing the inkjet head of any one of items 1 to 5 further comprising steps of: removing an unnecessary portion of the insulation layer on which the second electrodes are formed

Item 7. The method of manufacturing the inkjet head of item 6, wherein the isolation layer is configured with an organic film and in the removing step, the unnecessary portion of the insulation layer is removing by etching or by laser.

Item 8. The method of manufacturing the inkjet head of item 7, wherein a thickness of the insulation layer is not more than 20μm.

Item 9. The method of manufacturing the inkjet head of any one of items 1 to 8, wherein the pressure-generating element is a piezoelectric element, the head chip has a plurality of the rows which are configured by alternately arranging a plurality of pressure chambers, each formed in a channel shape, and a plurality of dividing walls between adjacent channels configured with the piezoelectric elements, each of the pressure chambers opens to a front end surface and a rear end surface of the head chip, nozzles are disposed on the front end surface, drive electrodes are formed on the dividing walls facing inside the pressure chambers, ink is ejected from the nozzles, by applying electric signals onto the drive electrodes, and the first electrodes are formed in a plurality of rows on the rear end surface of the head chip.

EFFECT OF THE INVENTION

[0017] According to the present invention, provided is a method to manufacture an inkjet head which facilitates connection of an external electrode to be connected with a drive circuit with respect to each electrode in a plurality of rows arrayed on an end surface of the head chip and enables all the aforesaid external electrodes to be led out to the same end side of the head chip without creating dangerousness of disconnection and short circuit even if the number of the rows of the electrodes array on the end surface of the head chip increases.

[0018] According to the present invention, in the head chip, the external electrode can be readily connected without causing displacement with respect to each electrode formed in three or more than three rows on the end surface of the head chip and all the external electrodes can be led to the same end section side of the head chip, thus the high resolution and high speed inkjet head can be manufactured readily.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

Fig. 1a to 1e are diagrams describing an exemplary method of manufacturing a head chip.

Fig. 2 is a diagram describing a method of forming a first electrode on a head chip.

Fig. 3 is a diagram as viewed from a rear end surfaces side of a head chip in which a first electrode is formed.

Fig. 4 is a diagram to stack a first insulation layer on a rear end surface of a head chip.

Fig. 5a is a cross-sectional view along a line (i) to (i) in Fig. 4.

Fig. 5b is a cross-sectional view along a line (ii) to (ii) in Fig. 4.

Fig. 6 is a diagram describing a method of forming a second electrode on a rear end surface of a head chip.

Fig. 7a is a cross-sectional view along a line (iii) to (iii) in Fig. 6.

Fig. 7b is a cross-sectional view along a line (iv) to (iv) in Fig. 6.

Fig. 8 is a diagram as viewed from a rear end surface side of a head chip in which a second electrode is formed.

Fig. 9a is a cross-sectional view along a line (v) to (v) in Fig. 8.

Fig. 9b is a cross-sectional view along a line (vi) to (vi) in Fig. 8.

Fig. 10 is a diagram of a head chip as viewed from a rear end surface side wherein an unnecessary area of a first insulation layer is removed.

Fig.11a is a cross-sectional view along a line (vii) to (vii) in Fig.10.

Fig.11b is a cross-sectional view along a line (viii) to (viii) in Fig. 10.

Fig.12 is a diagram describing a method to stack a second insulation layer on a rear surface of a head chip.

Fig. 13a is a cross-sectional view along a line (ix) to (ix) in Fig.12.

Fig. 13b is a cross-sectional view along a line (x) to (x) in Fig.12.

Fig. 14 is a diagram of a head chip wherein an unnecessary area of a second insulation layer is removed, as viewed from a rear end surface side

Fig.15a is a cross-sectional view along a line (xi) to (xi) in Fig. 14.

Fig.15b is a cross-sectional view along a line (xii) to (xii) in Fig. 14.

Fig.16 is a perspective exploded view of an inkjet head.

Fig.17 is a diagram related to a second embodiment describing a method to stack a second insulation layer on a rear end surface of ahead chip having three channel rows.

Fig.18a is a cross-sectional view along a line (xiii) to (xiii) in Fig.17.
Fig.18b is a cross-sectional view along a line (xiv) to (xiv) in Fig. 17.
Fig.18c is a cross-sectional view along a line (xv) to (xv) in Fig. 17.
Fig.19 is a diagram describing a method of forming a second electrode on a second insulation layer on a rear surface of the head chip.
Fig. 20a is a cross-sectional view along a line (xvi) to (xvi) in Fig.19.
Fig. 20b is a cross-sectional view along a line (xvii) to (xvii) in Fig.19.
Fig. 20c is a cross-sectional view along a line (xviii) to (xviii) in Fig.19.
Fig. 21 is a diagram as viewed from a rear end surface side of a head chip wherein an unnecessary area of a second insulation layer is removed.
Fig. 22a is a cross-sectional view along a line (xix) to (xix) in Fig. 21.
Fig. 22b is a cross-sectional view along a line (xx) to (xx) in Fig. 21.
Fig. 22c is a cross-sectional view along a line (xxiv) to (xxiv) in Fig. 21.
Fig. 23 is a diagram describing a method to stack a third insulation layer on a rear surface of a head chip.
Fig. 24a is a cross-sectional view along a line (xxii) to (xxii) in Fig. 23.
Fig. 24b is a cross-sectional view along a line (xxiii) to (xxiii) in Fig. 23.
Fig. 24c is a cross-sectional view along a line (xxiv) to (xxiv) in Fig. 23.
Fig. 25 is a diagram of a head chip as viewed from a rear end surface side wherein an unnecessary area of a third insulation layer is removed.
Fig. 26a is a cross-sectional view along a line (xxii) to (xxii) in Fig. 25.
Fig. 26b is a cross-sectional view along a line (xxiii) to (xxiii) in Fig. 25.
Fig. 26c is a cross-sectional view along a line (xxiv) to (xxiv) in Fig. 25.
Fig. 27 is a diagram of a head chip as viewed from a rear end surface side, having three channel rows related to another channel array form, wherein an unnecessary area of a second insulation layer is removed.
Fig. 28 shows an embodiment wherein a through hole is formed in an insulation layer related to a fourth embodiment.
Fig. 29 shows an inkjet head related to a fifth embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] In the present invention, the inkjet head is provided with a head chip having a plurality of pressure chambers to which ink is supplied, and a plurality of pressure generation elements to generate pressure change in each of the pressure chambers. On one end surface of the head chip, a plurality of first electrodes to apply electric signals with respect to respective pressure generation elements are arrayed in a plurality of rows. Second electrodes are sequentially formed with respect to each row of the first electrodes on the end surface of the head chip so as to electrically connect the second electrodes representing external electrodes which enables connection with drive circuits, thus all the second electrodes are lead out to the same end section side of the head chip.

[0021] Namely, in the present invention the second electrodes sequentially formed on a first electrode forming surface side of the head chip by laminating the second electrode in a thickness direction of an insulation layer having the insulation layer between second electrodes corresponding to the first electrodes in one row and second electrodes corresponding to the first electrodes in another row adjacent to the row, in a way that one end of each of the second electrodes and the insulation layer penetrate at a same end section side of the head chip. Whereby, on the first electrode forming surface of the head chip, a laminated structure of the second electrode and the insulation layer are formed corresponding to number of the rows of the first electrodes. The end section of the head chip herein is an end section of the first electrode in an array direction when the head chip is viewed from the first electrode forming surface side.

[0022] In the present invention, on the end surface of the head chip in which the first electrodes are arrayed in the plurality of rows, the second electrodes (to correspond with one row of the first electrodes) are formed for wiring with respect to each row of the first electrode preferably from a row of the first electrode at either end section of the head chip to adjacent to the rows of the first electrodes sequentially. Therefore, compare to a conventional method that a separate substrate on which the electrodes are formed in the plurality of rows in advance such as an external wiring substrate is electrically connected while adjusting position with respect to the electrodes in the plurality of the rows of the head chip, complication of connection work can be reduced.

[0023] Further, since all the second electrodes are formed to protrude at one end section side of the head chip, in case the external substrate such as the FPC is connected to the second electrode, only a work at one side with respect to one end section side of the head chip has to be done. Whereby, there is an effect that the connection work can be simplified.

[0024] The method to from the second electrode on the insulation layer is not limited. In general, the metal material to be the electrode is applied on the insulation layer via a vapor-deposition method or a spattering method to form a metal film and a pattern is formed on the metal film via exposing and developing with use of a mask. With use of the above technology the second electrode is formed in a pattern.

[0025] Also, according to the present invention, among the first electrodes in the plurality of the rows in the head chip, the second electrodes electrically connected to one row of the first electrode and the second electrodes electrically connected to another row of the first electrode are laminated on one surface (upper surface) and another surface (lower surface) of the insulation layer, therefore a pitch between the second electrodes cannot be narrow even if number of rows of the first electrodes increases. Thus, it is not necessary to narrow the width of the second electrode neither as the number of the first electrodes increases, there is no dangerousness that breaking or circuit occurs.

[0026] In the present invention, the head chip configured by forming three or more than three rows of the first electrode is particularly preferred. Even for a head chip having three or more than three rows of the first electrode, the present invention facilitates connection of the second electrodes with the row of the first electrode sandwiched between rows of the first electrodes at both end sections without having dangerousness of displacing, breaking and short circuit

[0027] In the present invention it is preferred that second electrodes respectively corresponding to the row of the first electrodes and the adjacent row of the first electrodes are formed on one surface and another surface of the insulation layer to overlap each other in the thickness direction of the insulation layer at a section protruding to the same end section side of the head chip. Since all the second electrodes protruding from the same end section side of the head chip can be arrayed in the same pitch, in case the external substrate such as the FPC is connected to the protruding section, connection work can be done readily.

[0028] Also, in the present invention, on the insulation layer surface in contact with a first electrode forming surface wherein the insulation layer is formed at first with respect to the first electrode forming surface of the head chip, the second electrode corresponding to each first electrode in the row of the first electrode arrayed either end section of the head chip is formed in advance, then by jointing the insulation layer with the head chip, each of first electrodes in the row of the first electrodes and the second electrodes formed in advance can be electrically connected.

[0029] According to the above method, in addition to the aforesaid effect, the surface of the second electrode can be exposed towards an opposite surface side to the first electrode forming surface in the head chip thus when the external substrate such as FPC is connected to the second electrode while placing the head chip on a work bench, connection work can be conducted from one direction with respect to all the second electrodes in a stable condition wherein the first electrode forming surface side of the head chip is facing down which is further superior in workability.

[0030] Incidentally, when jointing of the first insulation layer on which the second electrodes are formed in advance, each of the second electrodes in one row has only to be positioned with respect to each of the first electrodes in one raw arrayed on either end section of the head chip, therefore complication such that each of the first electrodes in a plurality of the rows and each of the second electrodes in a plurality of the rows are positioned is not required.

[0031] Incidentally, in case the second electrode formed on an insulation surface on an opposite side to the first electrode forming surface side of the head chip and the first electrodes on the head chip end surface are connected electrically, the second electrode has to be laid also in the thickness direction of the insulation layer perpendicular to the surface on which the second electrode is formed. Therefore, it is preferred that the second electrodes on the insulation layer surface on the opposite side to the first electrode forming surface side of the head chip, are formed to be electrically connected with the corresponding the first electrodes from the surface of the insulation layer on which the second electrode is formed via an end surface adjacent the surface thereof

[0032] According to the above method, the second electrode on the insulation layer extends from the surface of the insulation layer (forming surface of the second electrode) and via the edge of the insulation layer, the second electrode is bent in the thickness direction of the insulation layer towards the head chip side then through an end surface extending in the thickness direction of the insulation layer adjacent to a surface of the insulation layer thereof, the second electrode is electrically connected with the first electrode. Thus the land in case the through hole is used is not necessary and widening of the wiring pitch of the second electrode per one insulation layer is prevented. Therefore, even in case the pitch between the first electrodes in one row is narrow, the second electrodes corresponding to the first electrodes thereof can be formed readily.

[0033] Also, in the present invention, in order to lay the second electrode also in the thickness direction of the insulation layer, the second electrode formed on a surface on an opposite side to the first electrode forming surface side of the head chip on the insulation layer can be connected with the corresponding first electrode via a through hole formed in the insulation layer.

[0034] The through hole can be formed on the insulation layer jointed on the edge surface of the chip head by etching or by laser work at a portion of the insulation layer which overlaps with the first electrode. A metal material fills inside of the through hole at the same time when the metal material is applied onto the insulation layer to form the second electrode, whereby by laying the second electrode in the thickness direction of the insulation layer on the surface thereof the second electrode is conducted with the corresponding first electrode. Thus different form the through hole which requires the land having larger diameter than the with of the electrode, the second electrode can be laid in the thickness direction of the insulation layer within the width of the second electrode.

[0035] Therefore, in the above method, in the same manner as the aforesaid method, even in case the pitch between the first electrodes in one row is narrow, the second electrodes corresponding thereto can be formed readily. In addition to the above effect, when the insulation layer is laminated on the head chip, the end surface of the insulation layer is not used, the end section of the insulation layer where the edge surface of the insulation layer locates is not necessary to be positioned accurately with respect to the first electrode, thus there is an effect that forming work of the second electrode is even easier.

[0036] It is preferred that the present invention includes a removing process to remove unnecessary portions of the insulation layer on which the second electrode is formed. The removing process can be performed every time when forming the laminated structure wherein the second electrodes are formed on the insulation layer on the end surface of the head chip. The unnecessary portions means portions of the insulation layer unnecessary for serving a reinforcement function for the second electrode and a prevention function for short circuit between the second electrodes laminated in a thickness direction of the insulation layer and a portion of the insulation layer covering an electrical connection portion to be connected with the external substrate in case the external substrate such as the FPC is connected with the second electrode. Removing method is appropriately determined in accordance with the material used in the insulation layer.

[0037] In the present invention, it is preferred that the insulation layer is configured with an organic film. The insulation layer formed with the organic film is easy to produce and to laminate, also in the removing process, the unnecessary area of the insulation layer can be removed readily by etching or by laser thus the insulation layer can be removed accurately and easily.

[0038] As the organic film, for example, various kinds of resin films such as polyimide, liquid crystal polymer, aramid, polyethylene terephthalate and so forth. Among them the polyimide film having an excellent etching characteristic is preferred Also, to make dry etching easy, use of a thinnest possible film is preferred. In this case use of the aramid film which can maintain strength even if it is thin is preferred. As the insulation layer a silicon substrate capable of dry etching can be used. However the dry etching of silicon requires special gas such as DF_4 and SF_5 and special equipment thus generally it causes cost increase.

[0039] The thickness of the insulation layer is preferred to be not more than 20μm considering swelling by being contacted with ink and easiness of the removing work in the removing process. A lower limit value is preferred to be not less than 3μm from a view point of maintaining the strength.

[0040] In the head chip of the present invention is a harmonica structure chip that there are a plurality of rows configured by disposing a number of the pressure cambers formed in a shape of a channel and dividing walls configured with piezoelectric elements arranged between adjacent pressure chambers in a plurality of rows alternately in parallel, wherein the pressure chambers are opened at a front end surface and a rear end surface of the head chip, nozzles are arranged at the front end surface, driving electrodes are formed on the surface of the dividing walls facing the pressure camber side, and by applying electric signals onto the driving electrodes the dividing walls deform and ink in the pressure chamber is ejected from the ejection ports. It is preferred that a first electrode is formed on the rear surface of the head chip.

[0041] In general, in such harmonic structure head chip it is difficult to connect each driving electrode facing the pressure chamber with the driving circuit electrically. However according to the present invention, with respect to each first electrode formed on the rear end surface of the head chip, the second electrode representing the external electrode to enable connection with the driving circuit can be connected easily without causing displacing. Also, even if the number of the rows of the first electrodes increases due to increase of the number of the rows of the pressure chamber, there is no dangerousness of braking and short circuit of the second electrode, further all the second electrodes can be easily led out to the same end section side of the head chip.

[0042] The piezoelectric element of the present invention is not limited as far as one which generates pressure change to eject ink in the pressure chamber. For example, besides a PZT representing an electro-mechanical conversion element, it can be heater to eject ink by rupturing bubble of the ink.

[0043] A method of manufacturing an inkjet head related to the present invention will be described with reference to the drawings as follow.

<First Embodiment>

(Manufacturing Method of Head Chip)

[0044] An exemplary method of manufacturing the head chip will be described with reference to Fig. 1. Here, a head chip of a harmonica structure in which two channel rows are formed are shown.

[0045] First of all, a piezoelectric element substrate 101 configured with a polarized PZT (a direction of polarization is shown by an arrow in the figure) is jointed on a substrate 100 configured with a ceramic and so forth with an epoxy family adhesive and so forth then a dry film 102 is further adhered on a surface of the piezoelectric element substrate 101 (Fig. 1a).

[0046] Then, a plurality of parallel channels 103 are formed with use of a cutting device such as a dicing saw and so forth from a dry film 102 side. Each channel 103 is cut from one end of the piezoelectric element substrate 101 to another end with a consistent depth to reach the substrate 100 whereby straight channels having consistent size and shape across the length direction is formed (Fig. 1b).

[0047] Next, a metal material such as Ni, Au, Cu or Al for forming the electrode is applied from a cutting side of the channel 103 via spattering method or vapor deposition method and a metal film 104 is formed on an upper surface of the dry film remaining at cutting and on an inner surface of each channel 103 (Fig. 1c).

[0048] After that by removing the dry film 102 along with the metal film 104 formed on the surface thereof, the substrate 105 wherein the metal film 104 are formed only on the inner surface of each channel 103 is obtained. Then by preparing two substrates 105 formed in the same manner, each substrate 105 is positioned so that channels 103 correspond each other, then by jointing the substrates 105 with use of the epoxy family adhesive or so forth, a chip substrate having one channel row is formed (Fig. 1d).

[0049] Next by preparing two chip substrates 106 formed in the above manner, the two chip substrates are positioned in a way that the channels 103 of each chip substrate are displaced by a half pitch each other and are stacked and bonded in a direction perpendicular to a lineup direction of the channels, thereafter by cutting it in a direction perpendicular to the length direction of the channel, a plurality of the head chips having two channel rows in which two chips are stacked can be manufactured at one time. Each channel 103 configures a channel 12 representing the pressure chamber of the head chip of the harmonica structure, and the metal film 104 inside each channel 13 becomes a drive electrode 13 and then a dividing wall 11 configured with the piezoelectric element is formed between the adjacent channels. Intervals between cutting lines C, by which the head chips are formed, determine a drive length (L length) of the channels 12 (Fig.1e).

[0050] In the above head chip 1, by applying a predetermined voltage onto each drive electrode 13 on both dividing walls 11 of the channel 12 from the drive circuit, the dividing walls are subject to share deformation in a shape of a dogleg by voltage sliding effect then pressure change occurs in the channel 12 and then an energy for ejection is given to ink supplied in the channel 12. On one end surface of the head chip 1 a nozzle plate to be described is jointed. Ink in the channel 12 is ejected from a nozzle formed on the nozzle plate as a fine ink droplet.

[0051] The head chip 1 obtained in the above manner, two channel rows, configured by disposing the dividing walls 11 and the channels 12 representing the pressure chambers alternately in parallel, are arrayed one above the other in the figure. While the number of the channels in each channel row is not limited, the number of the channels in each channel row is preferred to be two or more.

[0052] Incidentally, since the head chip is a hexahedron, a mane of each end surface is defined here. In the present invention, in the head chip 1 a surface from which ink is ejected is called a "front end surface", a surface opposite to the front end surface is called a "rear end surface", Also, outside end surfaces located in a laminating direction of the chip substrates 106 sandwiching the rows of each channel 12 arranged in parallel in the head chip 1, namely the arraying direction of the channel rows (vertical direction in the figure) are called an "upper end surface" and a "lower end surface" respectively.

[0053] In the following description, a row of the channels 12A locating at a lower side in figure is called a row A and a row of the channels 12B locating at an upper side is called a row B.

(Forming Process of First Electrode)

[0054] Next, a method to form the first electrode on the rear surface of the head chip 1 will be described with reference to Figs. 2 and 3. Figs. 2 and 3 are views of the head chip 1 as viewed from the rear end surface side.

[0055] First, a dry film 200 is adhered on the rear end surface of the head chip 1, then openings corresponding to an entire surface of channels 12A ad 12B, openings 201A to form the first electrodes 14A in the row A and openings 201B to form the first electrodes 14B in the row B, are formed so as to correspond to each of channels 12A and 12B via exposing and developing (Fig. 2).

[0056] Next, from the dry film 200 side, by applying, for example Al as a metal for forming the electrode via vacuum vapor deposition, Al films are selectively formed in each of openings 201A and 201B. With the Al film, each of the first electrodes 14A in the row A and the first electrodes 14B in the row B corresponding to each of channels 12A and 12B are formed on the rear end surface of the head chip 1.

[0057] In order to ensure electrical connection between each of the first electrodes 14A and 14B with the driving electrodes 13 in each of the channels 12A and 12B, it is preferred that vapor deposition is carried out two time in different directions. In practice, it is preferred that the vapor deposition is conducted at angles of 30° upward and downward with respect to a vertical direction to the surface shown in the figure. Further, to ensure electrical connection between the metal films 104 separated one above the other, vapor deposition at an angle of 30° from left or right direction is preferred.

[0058] As a forming method of the A1 film, common technologies to form thin films can be utilized without being limited to the vapor deposition method. Also, as a forming method of the Al film, a method to coat a conductive paste via inkjet can be utilized. Also spattering method is preferable since the metal film can be formed inside the channels without changing direction because flying directions of the metal particles are random. After forming the A1 film, Al film formed on the dry film 200 is removed by resolving and removing the dry film 200 with a solvent. Whereby, on the rear end surface of the head chip 1, only the first electrodes 14A in the row A and the first electrodes 14B in the row B remain, thus a plurality of rows of the first electrodes 14A and a plurality of rows of the first electrodes 14 B are arrayed in parallel one above the other on the rear end surface of the head chip 1.

[0059] Incidentally, considering workability of a developing process and a water washing process of the dry film 200, it is preferred that the dry film 200 has openings at all the end surfaces of the channels 12 A and 12B. Owing to the openings at all the end surfaces of the channels 12A and 12B, developing liquid and washing water in the channels 12A and 12B can be removed easily.

(Lamination Process of the Isolation Layer - First Layer)

[0060] Next, an insulation layer is laminated on the rear end surface of the head chip 1. The method will be described with reference to Fig. 4 and Fig. 5. Fig. 4 is a view of the head chip as viewed from a rear end surface side, Fig. 5a is a cross-sectional view along a line (i) to (i) in Fig. 4, and Fig. 5b is a cross-sectional view along a line (ii) to (ii) in Fig. 4. Incidentally, in Fig. 5a and 5b, descriptions of the drive electrodes 13 formed on an upper surface of the channels 12 A and 12B are omitted.

[0061] The insulation layer 12 is adhered on the rear end surface of the head chip 1 where each of the first electrodes 14 A and the first electrodes 14B have been formed on the read end surface thereof

[0062] The insulation layer 21 is configured with an organic film, wherein a length of the insulation layer 21 in a horizontal direction in the figure along an array direction of each of the channels 12A or channels 12B is longer than a length of the head chip in an array direction of each of channels 12A or channels 12B. The insulation layer 21 has a length in a vertical direction in the figure along an array direction of the rows A and B of each channel, which is set to prevent the insulation layer 21 from overlapping with each channel 12B in the row B. Also the length is set in a way that the insulation layer 21 is extended from an overlapping position with the head chip 1 where each first electrode 14B in the row B and a portion of each first electrode 14B are exposed and protrudes to a large extent from an end section 1a on the row A side at rear end surface of the head chip 1 beyond each first electrode 14A in the row A. In the above state, a portion of each first electrode 14B on the channel 12A side in the row A, each channel 12A in the row A and each first electrode 14A are covered by the insulation layer 21.

[0063] Here, on the insulation layer 21 patterns of the second electrodes 31 is formed in a way that the patterns has the same pitch as that of the first electrodes 14A corresponding to each first electrode 14A in the row A arrayed at a lowermost end section of the head chip 1 (forming of the second electrode at a first layer). When an end section 21 a of the insulation layer 21 is positioned in a state shown by the figure that the end section 21 a overlaps with each first electrode 14B in the row B, an end section 31 a of each second electrode 31 is at a position to overlap with each electrode 14A on the row A, and another end section 3 1b of each second electrode 31 is extended just until another end section 21 b of the insulation layer 21, protruding from the head chip 1. Between the end section 31b of each second electrode 31 and the end section 21b of the insulation layer 21 an electrode non-forming section having no second electrode 31 is formed. Therefore, when the insulation layer 21 is positioned and jointed with the rear end surface of the head chip 1, the end section 31b of the second electrode 31 protrudes to a large extent outside from the enc section 1a on the row A side of the head chip 1 and is exposed, also the end section 21b of the insulation layer 21 is protruded and exposed outside further from the end section 31b of the second electrode 31.

[0064] Whereby, each first electrode 14A in the row A of the head chip 1 is led out to an outside of the head chip 1 via the second electrode 31 representing an external electrode.

[0065] In the above forming method of the second electrode 31, the second electrode 31 can be formed in advance on one surface of the insulation layer 21 in the same manner as the method to form the patters of the first electrodes 14A and 14B. While a fine positioning between each first electrode 14A and each second electrode 31 is necessary for electrical connection, positioning of one row of the electrodes versus one row of the electrodes is only required, complication that a plurality of the rows are position at one time is not required.

[0066] To joint such insulation layer 21 with respect to the rear end surface of the head chip 1, a surface on which the second electrodes 31 are formed is faced to the rear end surface of the head chip 1 and the positioning is conducted so as to connect each first electrode 14 A in the row A with each second electrode 31 electrically, then the insulation layer 21 and the rear end surface of the head chip 1 are bonded each other with an adhesive. Here, as the adhesive an epoxy family adhesive (Epoxy Technology Inc. Epotech 323ND) was used under curing conditions that a pressure of 10kg/cm2 is applied for 30 min under a temperature of 100°C.

[0067] Conduction between the first electrode 14A in the row A and the second electrode 31 when bonding the insulation layer is realized by a NCP method (Non Conductive Paste Method) wherein the metal films are electrically connected by pressure bonding with use of an adhesive. In the above case the epoxy family adhesive serves a function as an adhesive to joint the insulation layer 21 as well as a function as NCP. In case of NCP method, connection may be difficult if a surface of the metal film oxidizes, thus surfaces of the first electrode 14A and the second electrode 31 are preferred to be metals diffcult to oxidize, such as Au, Pt or so forth. It can be achieved by making the metal film multilayered.

[0068] ACP method (Anisotropic Conductive Paste Method) with use of an adhesive in which metal particles are dispersed in an adhesive can be utilized. In this case, since the metal particles break an oxide film an the surface of the metal film to be conducted, reliable electrical connection can be easily realized even if the first electrode 14A and the second electrode 31 is formed with a metal such as AI and so forth whose surface easily oxi-

dize.

(Forming Process of Second Electrode - Second Layer)

[0069] Next, the second electrode is formed on the insulation layer 21 laminated on the rear end surface of the head chip 1 so as to correspond to each first electrode 14B in the row B adjacent to the row A of the first electrode 14A. The above method is described with reference to Figs. 6 to 9. Incidentally, in Fig. 7 and Fig. 9 the drive electrodes 13 formed on the upper surfaces of the channels 12A and 12B are omitted to be shown in the figure.

[0070] First, a dry film 4 is laminated on all the surfaces including a surface of the insulation layer 21 laminated at first on the rear surface of the head chip 1 and on an exposed surface of the rear end surface of the head chip 1 not covered by the insulation layer 21. On the dry film 4, openings 41 to be forming areas for the second electrodes to correspond to the each of the first electrodes 14B in the row B are formed (Fig. 6 and Fig. 7).

[0071] Each opening 41 is formed from a gap between each channel 12B in the row B and one end section 21a of the insulation layer 21 overlapping with each first electrode 14B in the row B to the other end section 21b of the insulation layer 21 protruding from an end 1 a of the head chip 1 to a large extent. Here since each channel 12A in the row A and each channel 12B in the row B are displaced by a half pitch each other, each opening 41 is formed in a shape of a crank (hook) in a way that the opening 41 is extended from the overlapping position with each first electrode 14B in the row B towards the row A side and passes through a side of each channel 12A in the row A or between each channel 12A then after bends in a lateral direction so as to overlap with each first electrode 14A in the row A, each opening 41 is again extended straight towards the other end section 21b of the insulation layer 21.

[0072] Next, the metal material is applied to the surface of the dray film 4 where the openings 41 are formed in the same forming method as that of the first electrodes14A and 14B. After forming a metal film in each opening 41, the dry film 4 is removed (lift off) and the second electrode 32 is formed on the insulation layer 21 (Fig. 8 and Figs. 9a and 9b).

[0073] Since an end of the opening 41 on the row B side of the dry film 4 is located between each channel 12 in the row B and one end section 21 a of the insulation layer 21, a boundary section between each first electrode 14B in row B and one end section 21 a of the insulation layer 21 is exposed in the opening 41. Therefore, the end section 32a of the second electrode 32 on the row B side formed by applying the metal material onto the opening 41 is extended from the surface of the insulation layer 21 in the thickness direction of the insulation layer 21 via an end surface 21c of the insulation layer 21 adjacent to the surface of the insulation layer 21, and laminated on the surface of the first electrode 14B in the row B so as to be electrically connected with each first electrode 14B (Fig. 9b). As viewed from the rear end surface side of the head chip 1, the second electrode 32 on the second layer and the second electrode 31 formed in advance on the first layer are overlapped each other from the top of the first electrode 14A in the row A to a section protruding to the end section 1a side of the head chip 1 in the thickness direction of the insulation layer 21. However, since the insulation layer intervenes between the both electrodes, short circuit does not occur.

(Removing Process of Insulation Layer-First Time)

[0074] Next, an unnecessary area of the insulation layer 21 is removed. The method of removing will be described with reference to Fig. 10, Fig. 11a and Fig. 11b. Incidentally, in Figs. 11a and 11b, the drive electrodes 13 formed on upper surfaces of the channels 12A and 12B are omitted to be shown in the figures.

[0075] In the state where only the second electrode 32 is formed by removing the dry film 4 (Fig. 8, Fig. 9a and Fig. 9b), each channel 12A in the row A which opens on the rear end surface of the head chip 1 is closed by the insulation layer 21 and ink cannot be supplied to each channel 12A in the row A as it is. Thus, after this, the unnecessary area ofthe insulation layer 21 including the opening area of each channel 12A in the row A is removed.

[0076] Here, since an organic film capable of etching is used as the insulation layer 21, dry etching is carried out from the rear end surface side of the head chip 1 so as to remove unnecessary portion of the insulation layer 21 exposing at an area other than the area in which the second electrode 32 is formed.

[0077] Specific methods of dry etching can be appropriately selected in accordance with the resin used for the insulation layer 21. For example, in case a polyimide film is used, dry etching using oxygen plasma is possible. During the etching since the second electrode 32 is not resolved by the oxygen plasma, as Fig. 10, Fig. 11a and Fig. 11b show, the second electrode 32 masks and maintains the insulation layer 21 underneath and the other portion of the insulation layer 21 is removed.

(Lamination Process of Insulation Layer - Second Layer)

[0078] Next, a second insulation layer 22 is laminated on a surface of the second electrode 32 from the rear end surface side of the head chip 1. The method of laminating will be described with reference to Fig. 12, Fig. 13a and Fig. 13b. Incidentally, in Figs.13a and 13b, the drive electrodes 13 formed on upper surfaces of the channels 12A and 12B are omitted to be shown by the figures.

[0079] The same material is used in the insulation layer 22 as that of insulation layer 21. The material has a size to cover all the second electrode 32 arrayed on the end section 1a side of the head chip 1 with respect to the channel 12A in the row A. An end section 22a of the material on a side adjacent to the channel 12 A in the

row A is positioned so as not to cover the channel 12A in the row A, and another end section 22b on an opposite side thereto is extended to the same position as the end section 21b protruding an outermost side in the first insulation layer 21 laminated in advance (Fig. 12 and Figs. 13a and 13b). The insulation layer 22 serves a function of a reinforcing layer to reinforce the end section 21b side of the second electrode 32 afterward.

(Removing Process of Insulation Layer-Second Time)

[0080] Next, an unnecessary area of the insulation layer 22 is removed. A method of removing will be described with reference to Fig. 14, Fig. 15a and Fig. 15b. Incidentally, in Figs. 15a and 15b, the drive electrodes 13 formed on the upper surfaces of the channels 12A and 12B are omitted to be shown by the figures.

[0081] After laminating the insulation layer 22, etching is carried out from a front end surface side (left side in Fig. 15a and 15b) of the head chip 1 so as to remove a portion (a portion shown by broken lines) of the insulation layers 21 and 22 exposing at the front end surface side (Fig. 14, Fig. 15a and Fig. 15b).

[0082] By the above etching, a portion, not masked by the second electrode 31 and the second electrode 32, of the insulation layers 21 and 22 protruding from the end section 1a of the head chip1 is removed, whereby the end section 32 b of each second electrode 32 protrudes further than the second electrode 31 and the insulation layer 21, and is exposed towards the front end surface side of the head chip 1 in the same manner as the second electrode 31. Then on an opposite surface of each second electrode 32 with respect to the insulation layer 21, the insulation layer 22 not removed by the etching remains and serves a function as the reinforcing layer and an end section 32b further protruding outside is reinforced.

(Jointing Process of External Substrate, Nozzle Plate and Ink Manifold)

[0083] From the head chip 1 manufactured as above having two channel rows i.e. the row A and the row B, the second electrodes 31 and 32 representing the external electrodes electrically connected with the first electrodes 14A and 14B in the both channel rows are collectively lead out to one end section side, namely a lower end section of the rear end surface of the head chip 1 in figure. Therefore, connection with each of the external substrates (FPC) 5A and 5B corresponding to the row A and the row B to enable connection with the drive circuit is possible only at the above end section side (Fig. 15a, Fig. 15b and Fig. 16).

[0084] Further, in the present embodiment, since the both second electrodes 31 and 32 are exposed toward the front end surface side of the head chip1, connection with the external substrates 5A and 5B is possible in one direction on the front end surface side of the head chip 1, thus connection work can be simplified. Since an reverse surface sides of each of the second electrodes 31 and 32 is reinforced by the insulation layers 21 and 22, there is no dangerousness that each of electrodes 31 and 32 is damaged or deformed.

[0085] On the front end surface of the head chip 1, a nozzle plate 6 on which a nozzle 61 corresponding to each channel 12 is formed is jointed. On the rear end surface side, an ink manifold 7 forming a common ink chamber to supply ink to each of channels 12A and 12B is jointed via the insulation layer 22. Whereby, an inkjet head H is completed (Fig. 16).

<Second Embodiment>

[0086] The above embodiments are exemplary manufacturing methods of the inkjet heads having the head chip where two channel rows i.e. the row A and the row B are formed. In the present invention by sequentially repeating the laminating process of the insulation layer, the forming process of the second electrode and the removing process of the insulation layer for every channel row (for every row of the first electrode), all the second electrodes can be lead out to one end section side of the head chip, even an inkjet head having a head chip in which three or more than three channel rows (rows of the first electrode) are formed.

[0087] Figs 17 to Figs. 26a, 26b, 26c and 26d show examples to form the second electrode on the rear surface side of the head chip 10 having three channel rows (row A to row C) in the same manner as the first embodiment. Incidentally, each channel row is arrayed to displaced by a 1/3 pitch each other. In Figs. 18a, 18b, 18c, 20a, 20b 20c, 22a, 22b, 22c, 24a, 24b, 24c, 26a, 26b and 26c drive electrodes 13 formed on the upper surfaces of the channels 12A, 12B and 12C are omitted to be shown by the figure.

[0088] The forming methods of the head chip 10 and each first electrode corresponding to each channel row are the same as that of the firs embodiment up to the process of removing the unnecessary area of the insulation layer 21 (the removing process of the insulation layer - first time), after forming the second electrodes 31 and 32 corresponding to each of first electrodes 14A and 14B in the row A and the row B, since one channel row (row C) is added by further laminating one more chip substrate 106 with respect to two chip substrates 106 configuring the head chip 1 having the two channel rows in the first embodiment so as to only add first electrodes 14C corresponding the row C. Therefore, the methods thereof are omitted to be described and description will be started from a method to form the second electrodes 3 3 with respect to the first electrode 14C in the row C corresponding to each channel 12C in the row C.

(Lamination Process of Insulation Layer - Second Time)

[0089] With respect to each of the first electrodes 14A

and 14B in the row A and the row B, each of the second electrodes 31 and 32 are formed and after removing the unnecessary area of the isolation layer 21, the second insulation layer is laminated on the rear end surface of the head chip 10. The method will be described with reference to Figs. 17 and 18a, 18b and 18c.

[0090] An insulation layer 22 configured with an organic film is laminated on the rear end surface of the head chip 10 where each of the second electrodes 32 corresponding to each of the first electrodes 14B in the row B.

[0091] A length of the insulation layer 22 in a horizontal direction in the figure along an array direction of the channel 12A to 12C is longer than a length of the head chip 10 in a array direction of the channels 12A, 12B or 12C. Also a length of the insulation layer in the vertical direction in the figure along an array direction of each of channel rows A to C is set so that the insulation layer 22 does not cover each channel C in the row C, extends from a position where the insulation layer 22 is overlapping in a way that each first electrode 14C in the row C and a portion of the first electrode 14C are exposed, and protrudes to a large extent from the end section 32b of each second electrode 32 electrically connected with each first electrode 14B in the row B, beyond the end section 10a on the row A side on the rear end surface of the head chip 10. Therefore, there is formed an electrode nonforming section 32c having no second electrodes 22 ofthe second layer between the end section 32b of each second electrode 32 and the end section 22b of the insulation layer 22 protruding to a large extent.

[0092] In the above state, the insulation layer 22 covers all the area from a row B side of each first electrode 14C in the row C to the second electrode 32 in the row B via each of channels 12B and 12A in the row B and the row A, and each of the first electrodes 14B and 14A in the row B and the row A.

(Forming Process of First Electrode - Third Layer)

[0093] Next, the second electrodes of the third layer are formed on the insulation layer 22 laminated on the rear end surface of the head chip 10. The method thereof will be described with reference to Figs. 19 to 24c.

[0094] The second electrode of the third layer can be formed by patterning in the same manner as the first embodiment. Namely, a dry film (not illustrated) is laminated on the surface of the insulation layer 22 laminated on the surface of the insulation layer 22 laminated on the rear end surface of the head chip 10 and the entire exposed surface not covered by the insulation layer 22 on the rear end surface of the head chip 10, then by applying a metal material in the same manner as forming the second electrode 32 corresponding to the first electrode 14B in the row B, the second electrode 33 electrically connected with each first electrode 14C in the row C on the insulation layer 22 is formed (Fig. 19 and Fig. 20).

[0095] The end section 33a of the second electrode 33 on the channel row C side is laminated on the surface of the first electrode 14C in the row C via the end surface 22c on the channel 12C side in the row C on the insulation layer 22 from the surface of the insulation layer 22 in the same manner as the second electrode 32 on the second layer, and connected with each first electrode 14C electrically (Fig. 20c).

[0096] Also, each second electrode 33 passes through a side of or between each of the channels 12B in the row B from each first electrode 14C in the row C and bends in the same lateral direction between the row B and row A of the channels, thereafter passes through a side of or between each of channels 12A in the row A, then bends in the same lateral direction again, whereby, each second electrode 33 is formed in a shape of a crank (aduncate shape) having two bending portions so as to overlap with the second electrode 32 on the second layer formed in advance.

[0097] In the above embodiment, as view from the rear end surface side of the head chip 10, all of the second electrodes 31 to 33 are overlapped each other in the thickness direction of the insulation layers 21 and 22, however since the insulation layers 21 and 22 intervene between them, short circuit does not occur.

[0098] Further, while two second electrodes 32 and 33 are wired so as to pass between each channel 12A in the row A, since the second electrodes 32 and 33 are laminated in the thickness direction ofthe insulation layers 21 and 22 via the insulation layers 21 and 22, a width for one second electrode is sufficient as the width necessary for wiring between the channels 12A and even if the number of wiring increases, narrowing down of the width of the second electrode is not necessary.

(Removing Process of Insulation Layer - Second Time)

[0099] Next an unnecessary area of the insulation layer 22 is removed.

[0100] Since the insulation layer 22 is also the organic film capable of etching, by carrying out etching from the rear end surface side of the head chip 10, the unnecessary area of the insulation layer 22 being exposed in an area other than an area where the second electrode 33 is formed is removed using the second electrode 33 as a mask. Whereby, as Figs. 21, 22a, 22b and 22c show, the insulation layer 22 beneath the second electrode 33 remains without being etched and other insulation layer 22 is removed.

(Lamination Process of Insulation Layer-Third Layer)

[0101] Next The third insulation layer 23 is laminated on the surface of the second electrode 33 on the rear end surface of the head chip 10. The method thereof will be described with reference to Fig. 23 and Figs. 24a, 24b and 24c.

[0102] Third insulation layer 23 is provided so as to serve a function of the reinforcing layer in the same manner as the second insulation layer 22 provided in the first

embodiment.

[0103] In the above embodiment, the isolation layer 23 has a size to cover a portion the second electrode 33 arranged on the end section side 10a of the head chip 10 with respect to the channel 12A in the row A. The end section 23 a on a side adjacent to the channel 12A in the row A is position so as not to cover the channel 12A in the row A and the end section 23 b on the other end side is extended to the same position as the end section 33b protruding to an outermost side of the second electrode 33.

(Removing Process of Insulation Layer- Third Time))

[0104] After that, by etching from a front end surface side of the head chip 10, portions (a portion of broken lines in the figure) of insulation layers 21, 22 and 23 exposing towards the front end surface side are removed (Fig. 25 and Fig. 26).

[0105] Through the above etching, the portions of the insulation layers 21,22 and 23, protruding from the end section 10a of the head chip 10, not masked by the second electrodes 31, 32 and 33 including the no electrode forming sections 31c and 32c are removed, and all the second electrodes 31 to 33 are exposed towards the front end surface side of the head chip 10. Then, on a surface of each second electrode 33 opposite to the insulation layer 22, the remaining insulation layer 23 without being etched serves a function in a reinforcing layer and the protruding end section 33b side is reinforced.

[0106] Incidentally, in the etching from the front end surface side, since the second electrode of each layer can serve a function of the mask, after forming all the second electrodes and the insulation layers, only one time of the etching is necessary through the entire manufacturing process of the inkjet head.

[0107] The head chip 10 having three channel rows manufactured in the above manner facilitates connection with the external substrates (FPC) 5A to 5C, which enables connection with the drive circuit, from the front end surface side of the head chip 10 at one end section side of the lower end section side of the front end surface side of the head chip 10 (Fig. 26).

[0108] In the above case also, since each of the electrodes 31 to 33 is reinforced by the insulation layers 21,22 and 23 from the back surface side, there is no dangerousness of damaging or deforming each of the second electrodes 31 to 33.

[0109] Incidentally, in the above description, while each of the channel rows of the head chip 10 is arranged to be displaced by a 1/3 pitch each other, as Fig. 27 shows, it can be formed that the channels in the channel rows adjacent each other are displaced by a half pitch in an arrayed direction of each channel row (vertical direction in the figure) the and the channels in every other channel rows (i.e. channel row A and channel row C) can be located at the same positions in the arrayed direction of each channel row. In such head chip 10, in case some nozzle is disabled to eject, instead of the channel corresponding to the disabled nozzle, a channel in other channel row in the same pitch position as that of the channel corresponding to the disable nozzle can be used so as to address the disabled nozzle.

<Third Embodiment>

[0110] In each of the aforesaid embodiments, the forming methods of the second electrodes 32 and 33 were described in a way that the second electrodes 32 and 33 are electrically connected with the corresponding first electrodes 14B and 14C via the end surfaces 21c and 22c of the insulation layers 21 and 22. Next, a method to form through holes on the insulation layer and to electrically connect the second electrodes and the corresponding first electrodes via the through holes will be described.

[0111] Fig. 28 is a cross-sectional view showing electrical connection portion between the first electrode 14B in the row B and the second electrode 32 of the head chip 1 shown in the first embodiment Incidentally, in Fig. 28, the drive electrode 13 formed on the upper surface of the channel 12B is omitted to be shown by the figure.

[0112] In the above case, the through hole 21B is formed at an overlapping area with the first electrode 14B on the insulation layer 21 by etching or by laser. While the through hole 21B can be formed at a corresponding position before jointing the insulation layer 21 with the head chip 1, forming after jointing the insulation layer 21 with the head chip 1 is preferred, because it is not necessary to consider displacement in position due to extension when jointing the insulation layer 21, and the through hole 21B can be formed while verifying the positional relation with the corresponding first electrode 14B without being displaced.

[0113] After forming the through hole 21 B, the second electrode 32 can be formed by vapor deposition or by spattering using the dry film as the foregoing. The metal material applied on the insulation layer 21 via vapor deposition or spattering fills the inside of the through hole 21B to be a wiring extending in the thickness direction of the insulation layer 21 and configures a through electrode section 32B of the second electrode 32 to electrically connect the second electrode 32 formed on the surface of the insulation layer 21 with the first electrode 14B.

[0114] The above through hole 21B and through electrode section 32B does not required to form a land, of which diameter is larger than the diameter of the hole, at a periphery of the hole such as an ordinary through hole. For the above reason, even if the channels 12 are densely arrayed, there is no dangerousness of short circuit and the second electrode can be wired densely.

[0115] In addition to the method via the end surface of the insulation layer, the method to electrically connect the first electrode and the second electrode via the above through hole and the through electrode section therein can be also applied to a case that the first electrode in

any position in the head chip is electrically connected with and the corresponding second electrode.

<Fourth Embodiment>

[0116] Fig. 29a shows an inkjet head H wherein an elongated laminated member 8, elongated by further extending the laminated structure configured with the insulation layer protruding at one end section side of the head chip1,10, is electrically connected with a drive circuit 9. The elongated laminated member 8 can serve a function to enable flexible wiring such as the FPC by using an organic film having flexibility as the insulation layer. By providing a connecter 81 at a front end of the elongated laminated member 8, an embodiment in which the drive circuit 9 is connected through the connecter 81 is realized.

[0117] Also, as Fig. 29b shows, the inkjet head H having the elongated laminated member 8 can be an embodiment in which an driver IC 91 for driving is directly connected with the elongated laminated member 8.

<Others>

[0118] In the present invention, each channel in the plurality of the channel rows arrayed in the head chip can be formed in a way that the pitches between each channel coincide among the channel rows.

[0119] Also, the head chip ofthe present invention is not limited to the shear mode type inkjet head which causes shear deformation of the dividing wall to eject ink inside the channel.

[0120] Further, the present invention is not limited to forming all the second electrodes to be exposed towards the front end surface side of the head chip, and in the present invention it is obvious that all the second electrodes can be formed towards the rear end surface side of the head chip.

DESCRIPTION OF THE SYMBOLS

[0121]

1,10 Head chip
11 Dividing wall
12A to 12C Channel
13 Drive electrode
14A to 14 C First electrode
21 to 23 Insulation Layer
31 to 33 Second electrode
4 Dry film
5 External substrate (FPC)
6 Nozzle plate
61 Nozzle hole
7 Ink manifold
8 Elongated laminated member
81 Connecter
9 Drive circuit
91 Driver IC

Claims

1. A method of manufacturing an inkjet head having a head chip provided with a plurality ofpressure chambers to which ink is supplied and a plurality of pressure-generating elements to generate pressure change in each of the pressure chambers, wherein a plurality of first electrodes for applying electrical signals to the pressure-generating elements are formed in a plurality of rows on one surface of the head chip, and a plurality of second electrodes are formed to electrically connect a drive circuit with each of the first electrodes, the method comprising steps of:

   forming the second electrodes sequentially on a first electrode forming surface side of the head chip by laminating in a thickness direction of an insulation layer, wherein the insulation layer intervenes between the second electrodes corresponding to the first electrodes in a row and the second electrodes corresponding to the first electrodes in another row adjacent to the row, in a way that an end of each of the second electrodes and the insulation layer protrude at a same end section side of the head chip.

2. The method of manufacturing the inkjet head of claim 1, wherein each of the second electrodes corresponding to the first electrodes in another row adjacent to the row are formed so as to overlap each other in the thickness direction of the insulation layer at a position protruding to the same end section side of the head chip.

3. The method of manufacturing the inkjet head of claim 1 or 2, wherein by forming the second electrode corresponding to each of the first electrodes in the row of the first electrodes in advance on a surface to be contact with a first electrode forming surface of the insulation layer formed at first with respect to the first electrode forming surface side of the head chip, each of the first electrodes in the row of the first electrodes is electrically connected with the second electrode formed in advance by jointing the insulation layer and the head chip.

4. The method of manufacturing the inkjet head of any one of claims 1 to 3, wherein the second electrodes formed on a surface of the insulation layer on opposite side to the first electrode forming surface side of the head chip are electrically connected with the corresponding first electrodes via the surface on which the second electrodes are formed and an end surface adjacent to the surface thereof.

5. The method of manufacturing the inkjet head of any one of claims 1 to 3, wherein the second electrodes formed on a surface of the insulation layer on opposite side to the first electrode forming surface side of the head chip are electrically connected with the corresponding first electrodes via through holes formed on the insulation layer.

6. The method of manufacturing the inkjet head of any one of claims 1 to 5 further comprising steps of:

removing an unnecessary portion of the insulation layer on which the second electrodes are formed.

7. The method of manufacturing the inkjet head of claim 6, wherein the isolation layer is configured with an organic film and in the removing step, the unnecessary portion of the insulation layer is removing by etching or by laser.

8. The method of manufacturing the inkjet head of claim 7, wherein a thickness of the insulation layer is not more than 20μm.

9. The method of manufacturing the inkjet head of any one of claims 1 to 8, wherein
the pressure-generating element is a piezoelectric element,
the head chip has a plurality of the rows which are configured by alternately arranging a plurality of pressure chambers, each formed in a channel shape, and a plurality of dividing walls between adjacent channels configured with the piezoelectric elements,
each of the pressure chambers opens to a front end surface and a rear end surface of the head chip, nozzles are disposed on the front end surface,
drive electrodes are formed on the dividing walls facing inside the pressure chambers,
ink is ejected from the nozzles, by applying electric signals onto the drive electrodes,
and the first electrodes are formed in a plurality of rows on the rear end surface of the head chip.

FIG. 1a

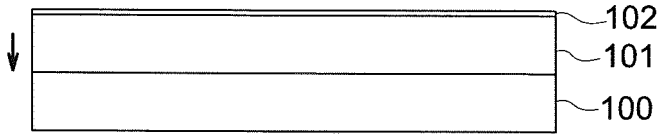


FIG. 1b

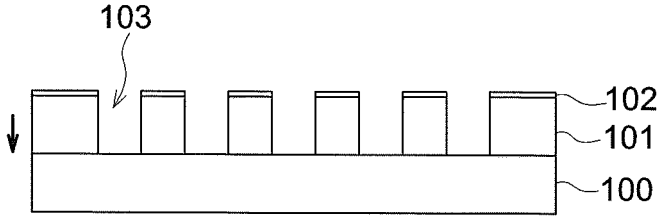


FIG. 1c

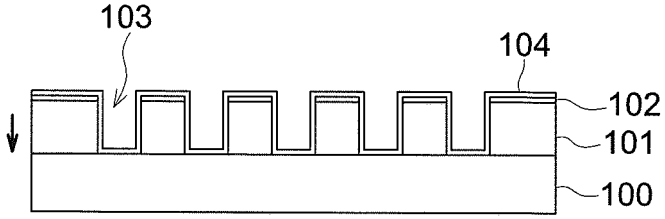


FIG. 1d

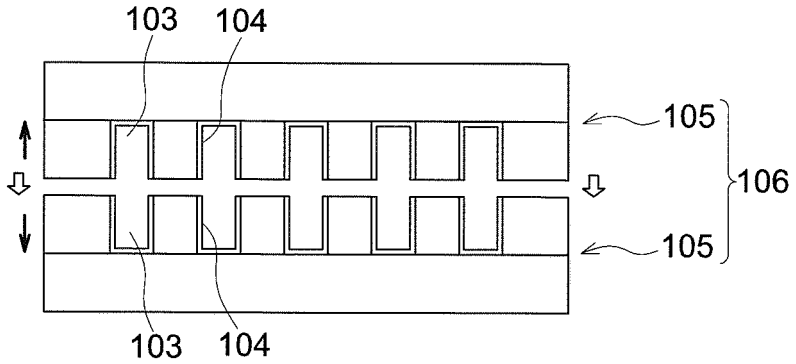


FIG. 1e

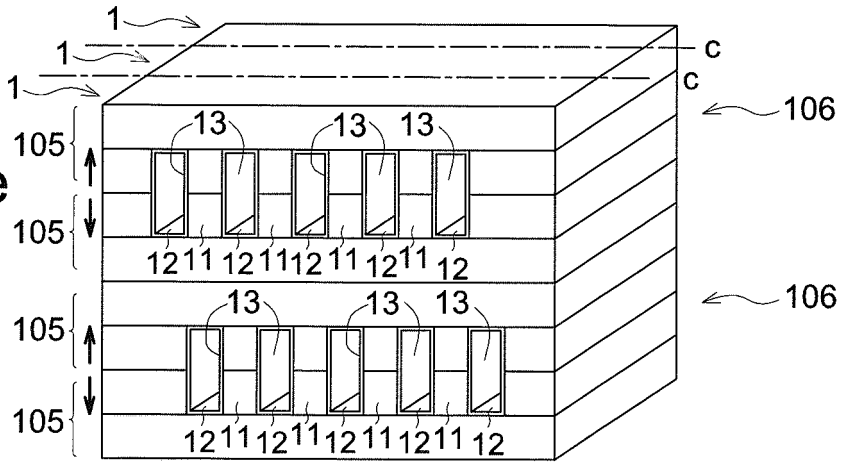


FIG. 2

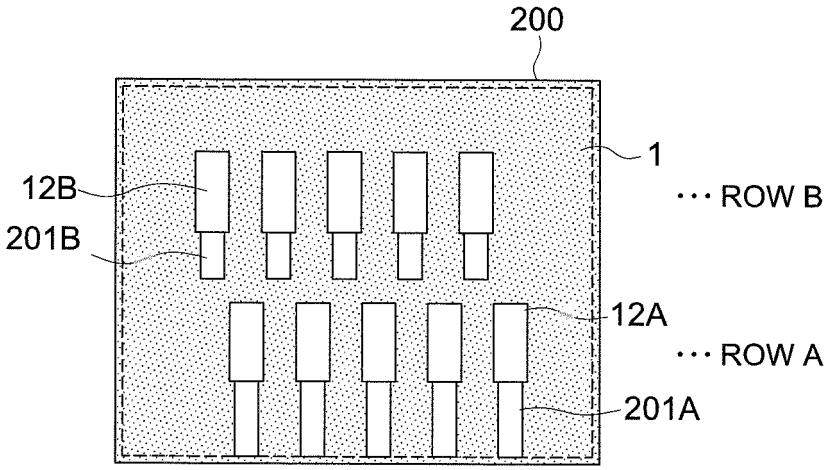


FIG. 3

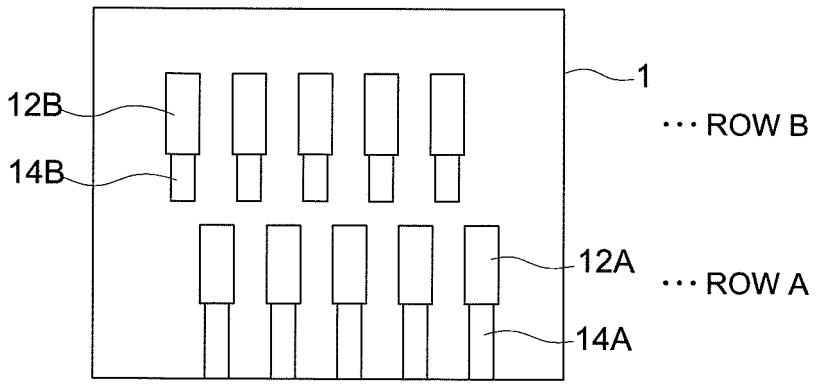


FIG. 4

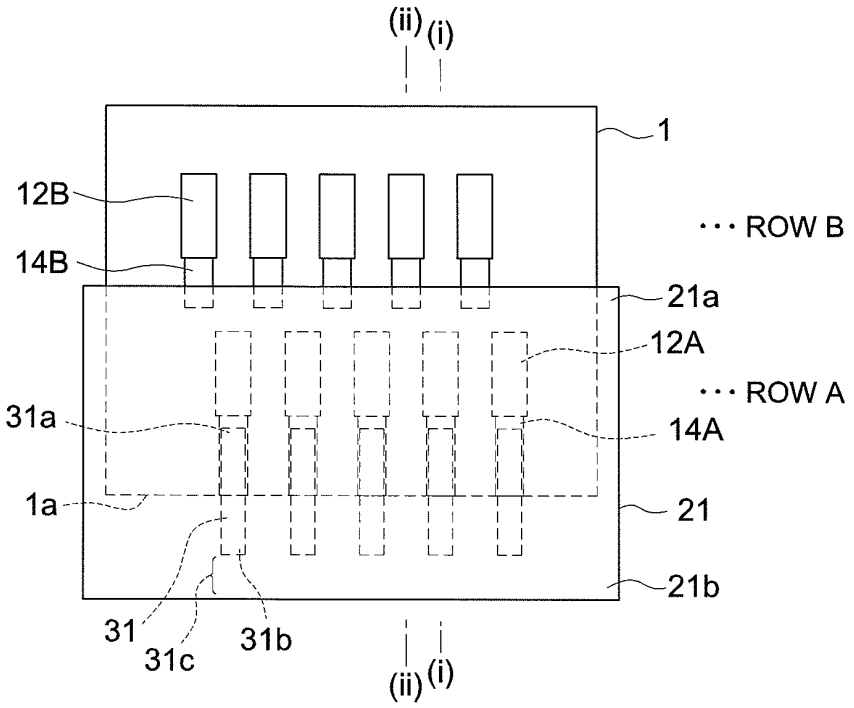


FIG. 5a

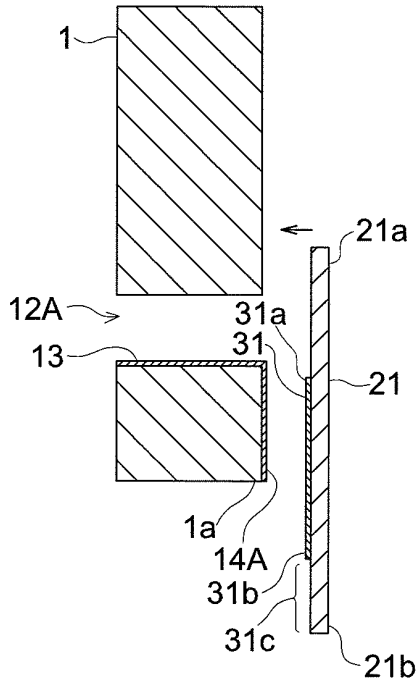


FIG. 5b

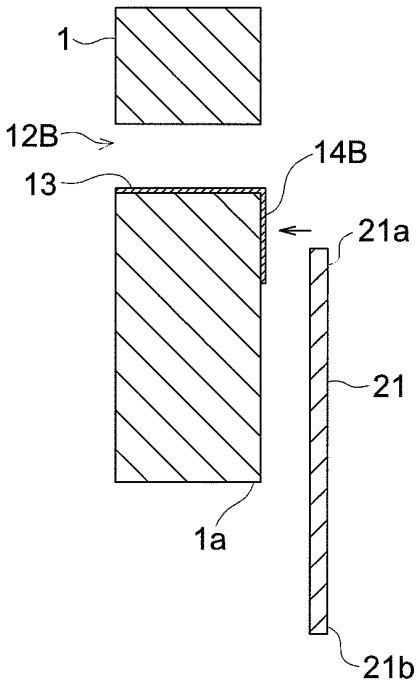


FIG. 6

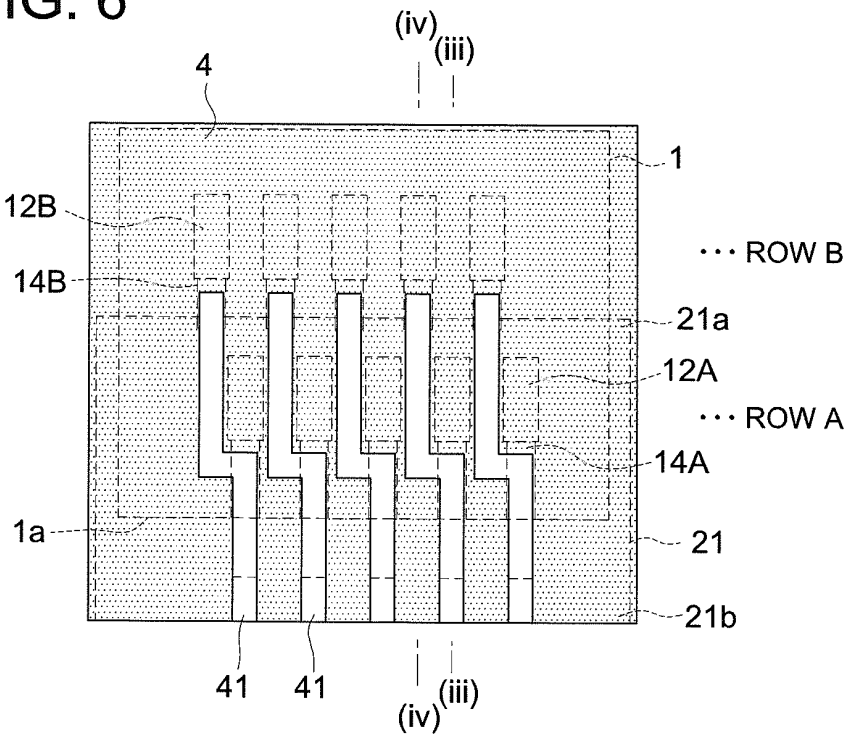


FIG. 7a

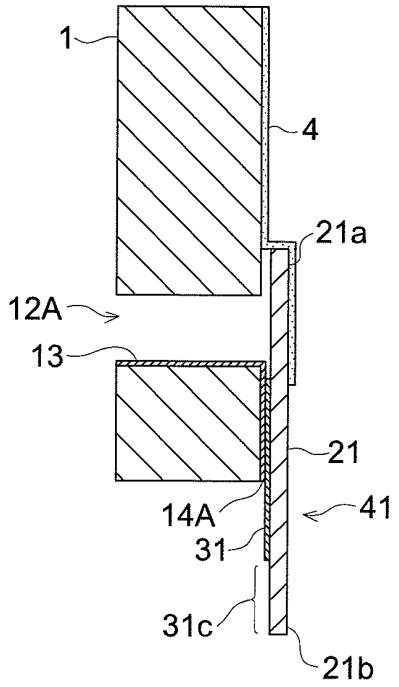


FIG. 7b

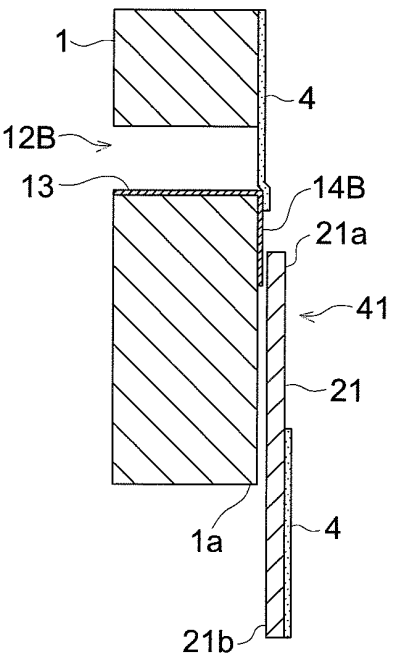


FIG. 8

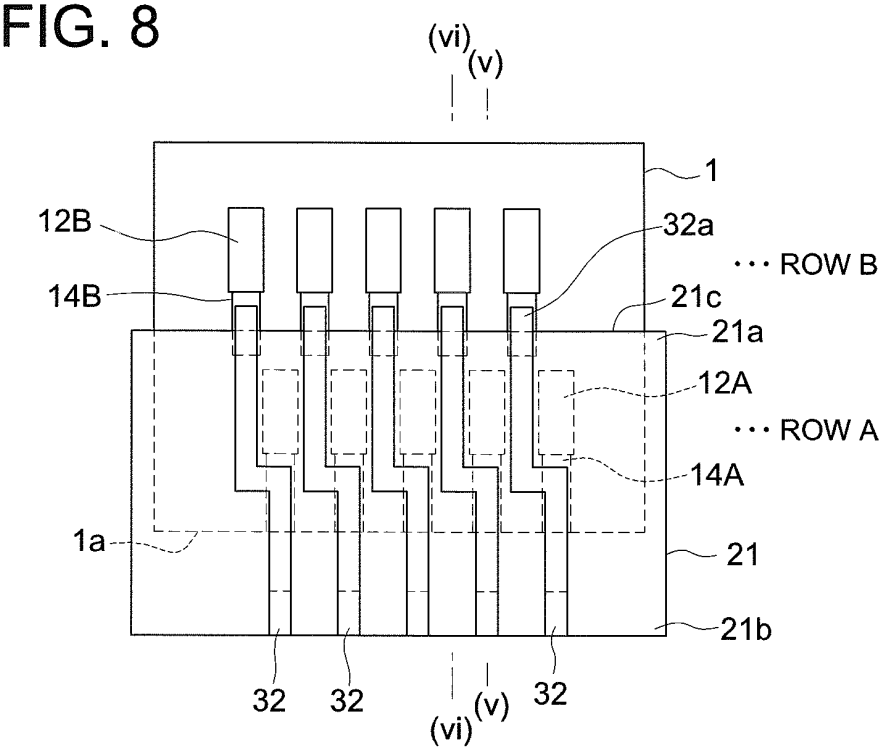


FIG. 9a

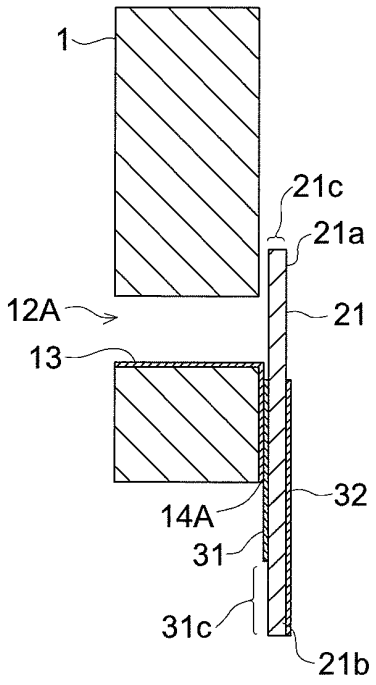


FIG. 9b

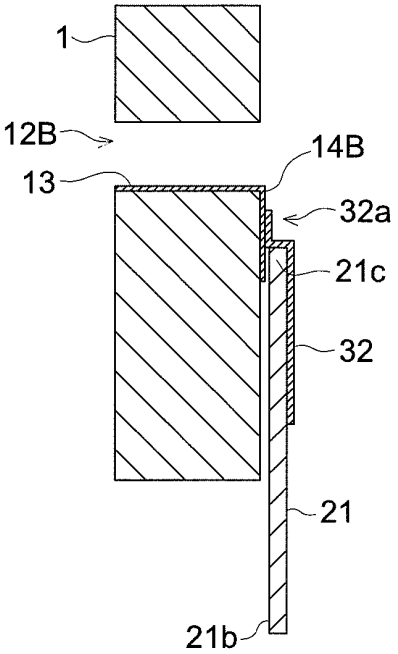


FIG. 10

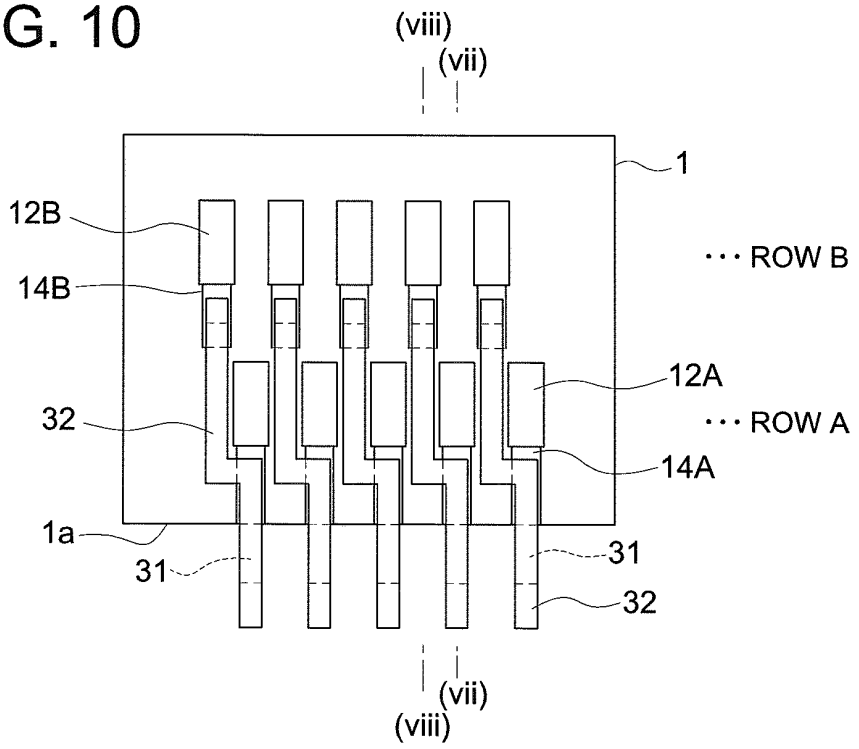


FIG. 11a

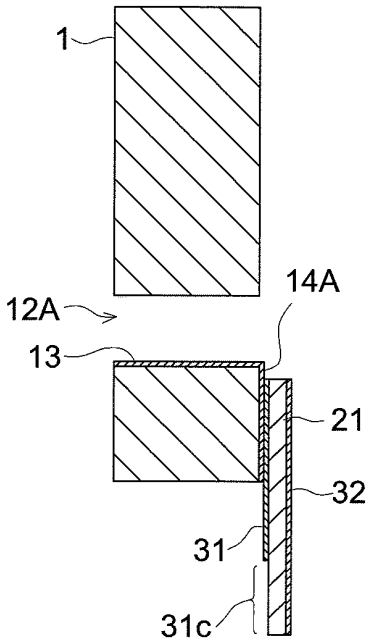


FIG. 11b

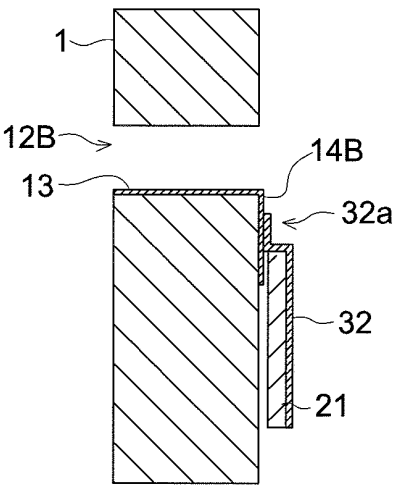


FIG. 12

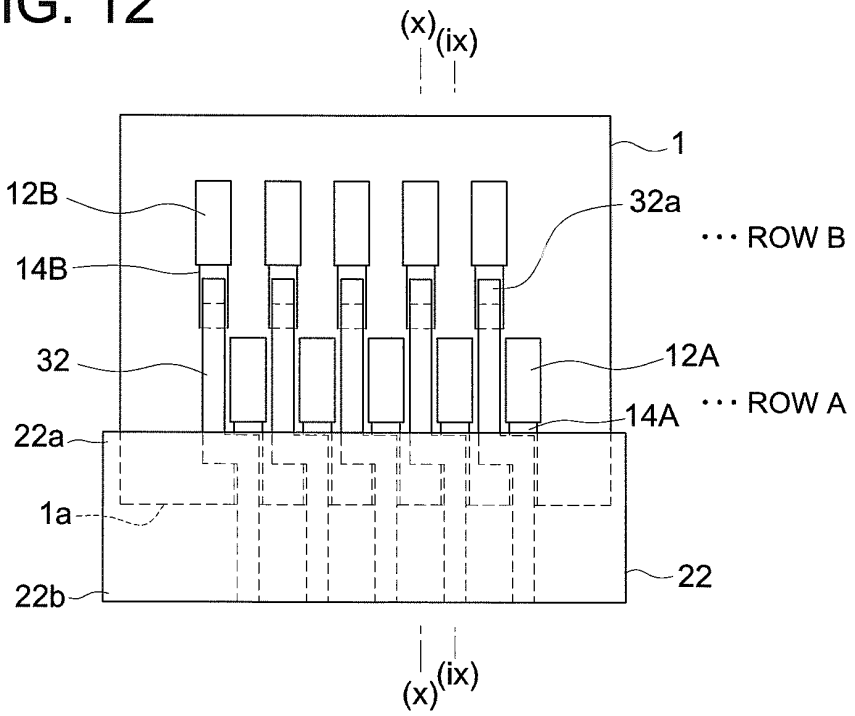


FIG. 13a

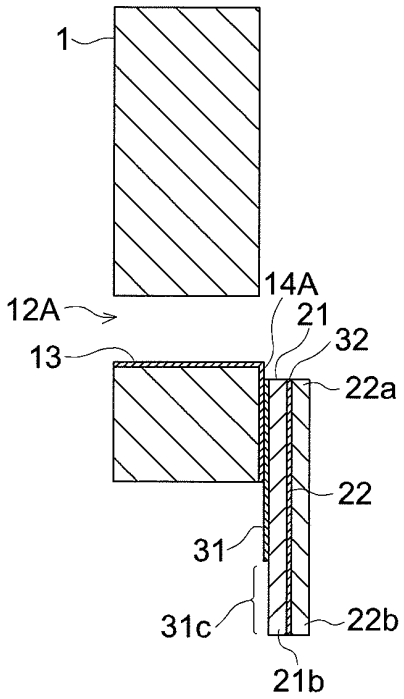


FIG. 13b

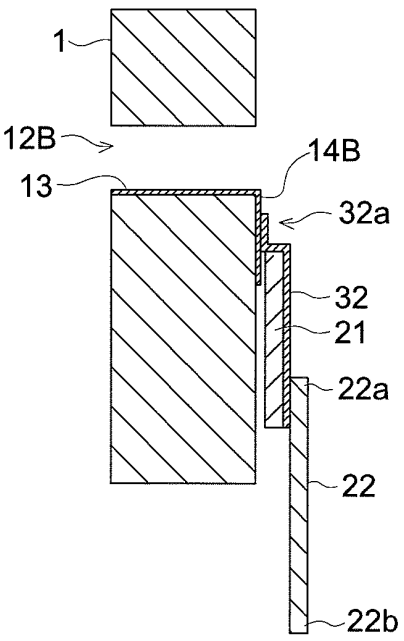


FIG. 14

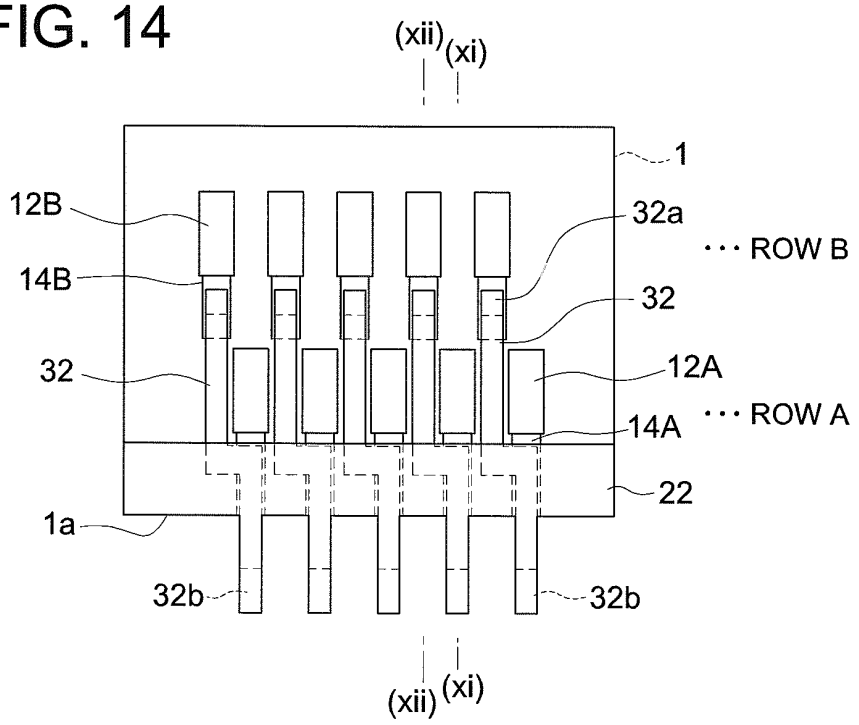


FIG. 15a

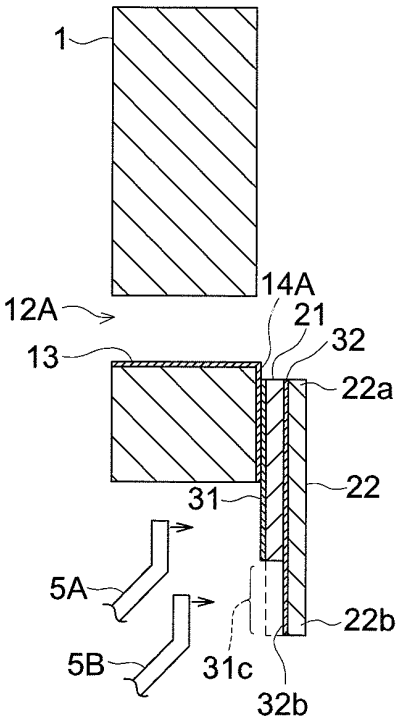


FIG. 15b

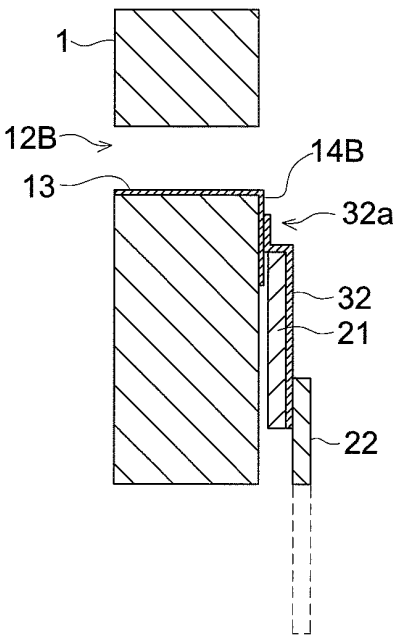


FIG. 16

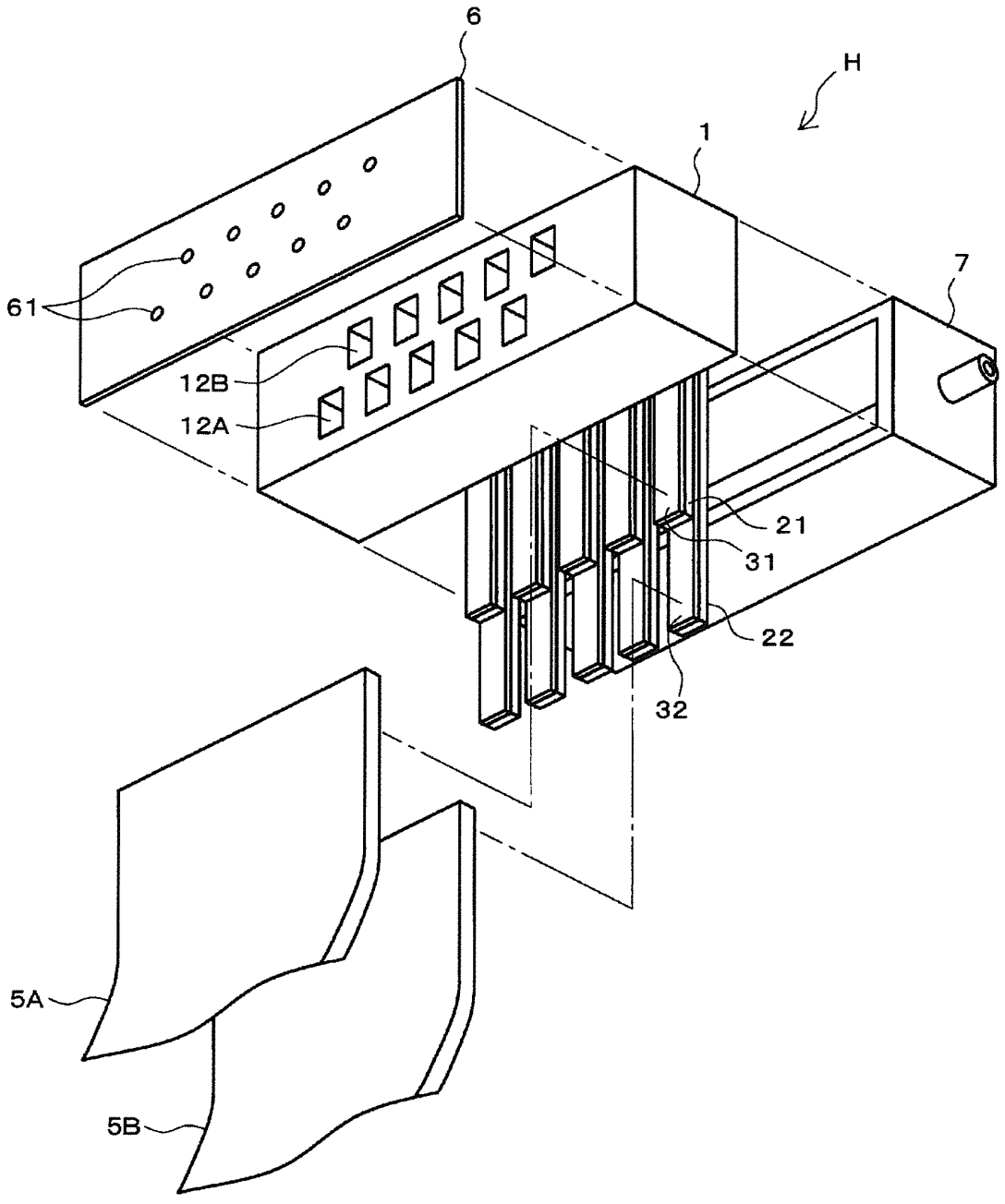


FIG. 17

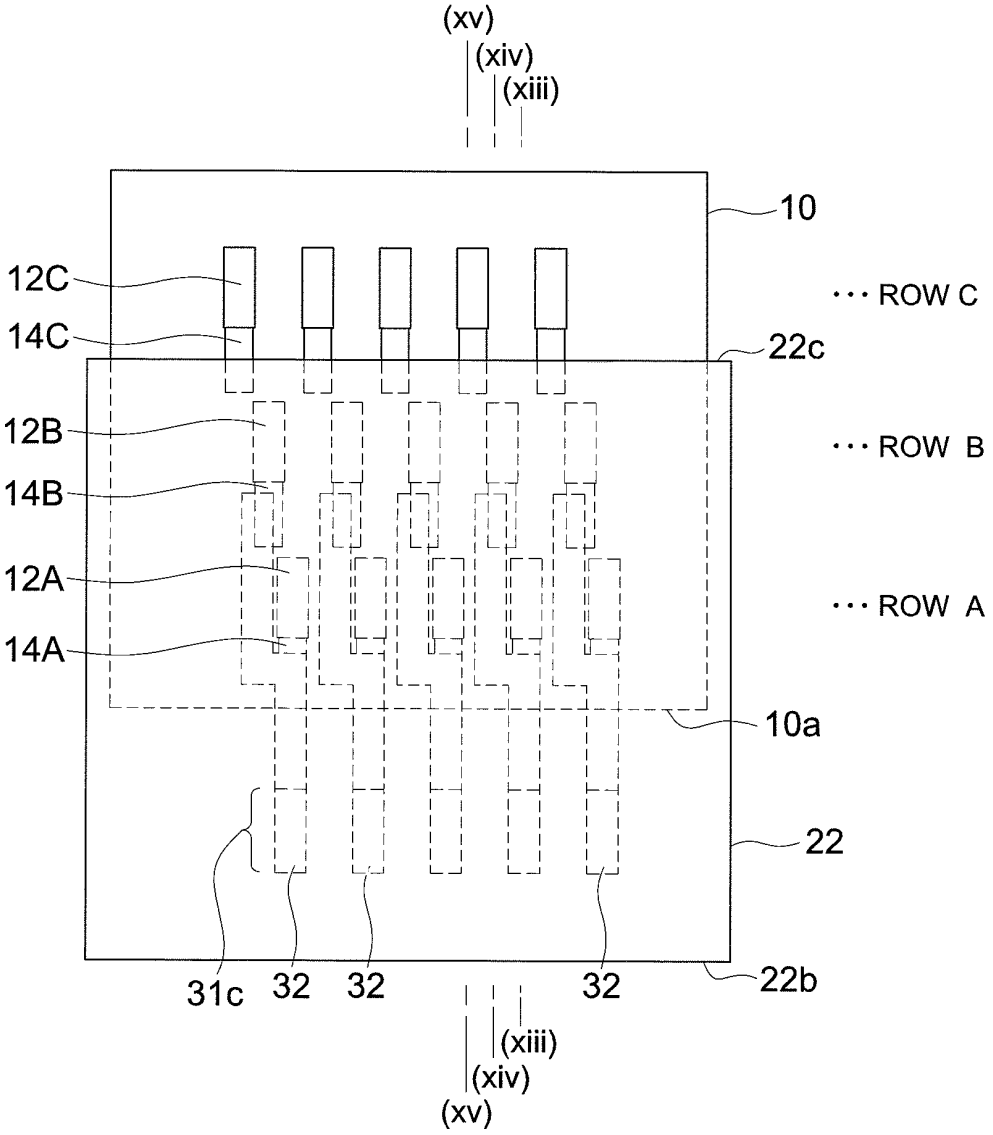

(xv)
(xiv)
(xiii)
10
12C
14C
··· ROW C
22c
12B
14B
··· ROW B
12A
14A
··· ROW A
10a
22
31c
32
32
32
22b
(xiii)
(xiv)
(xv)

FIG. 18c

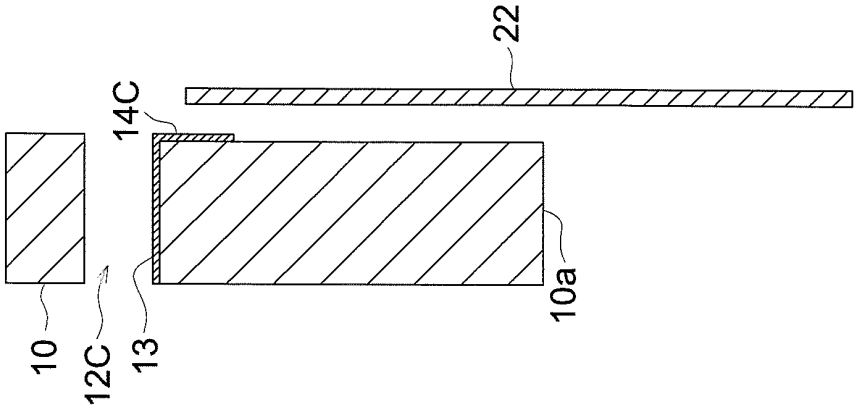


FIG. 18b

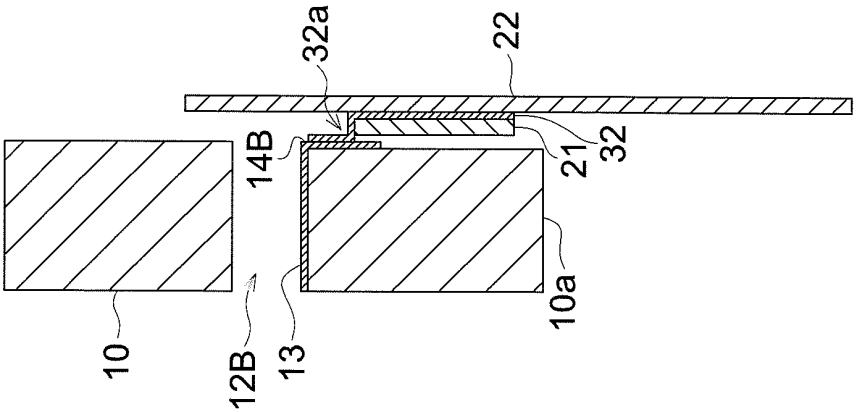


FIG. 18a

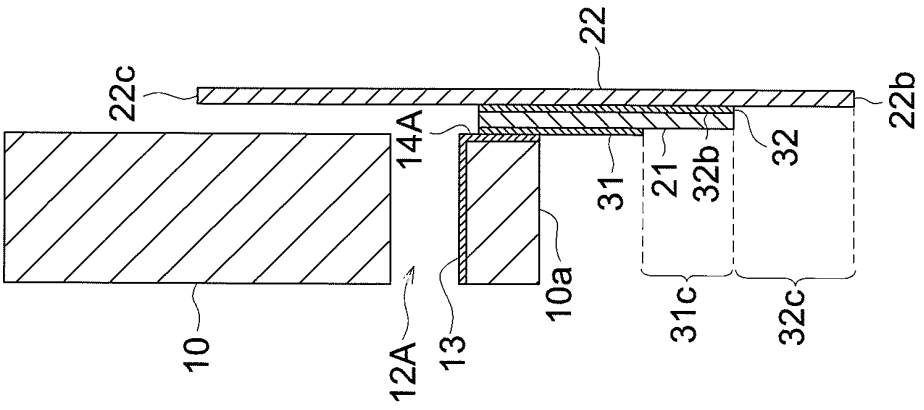


FIG. 19

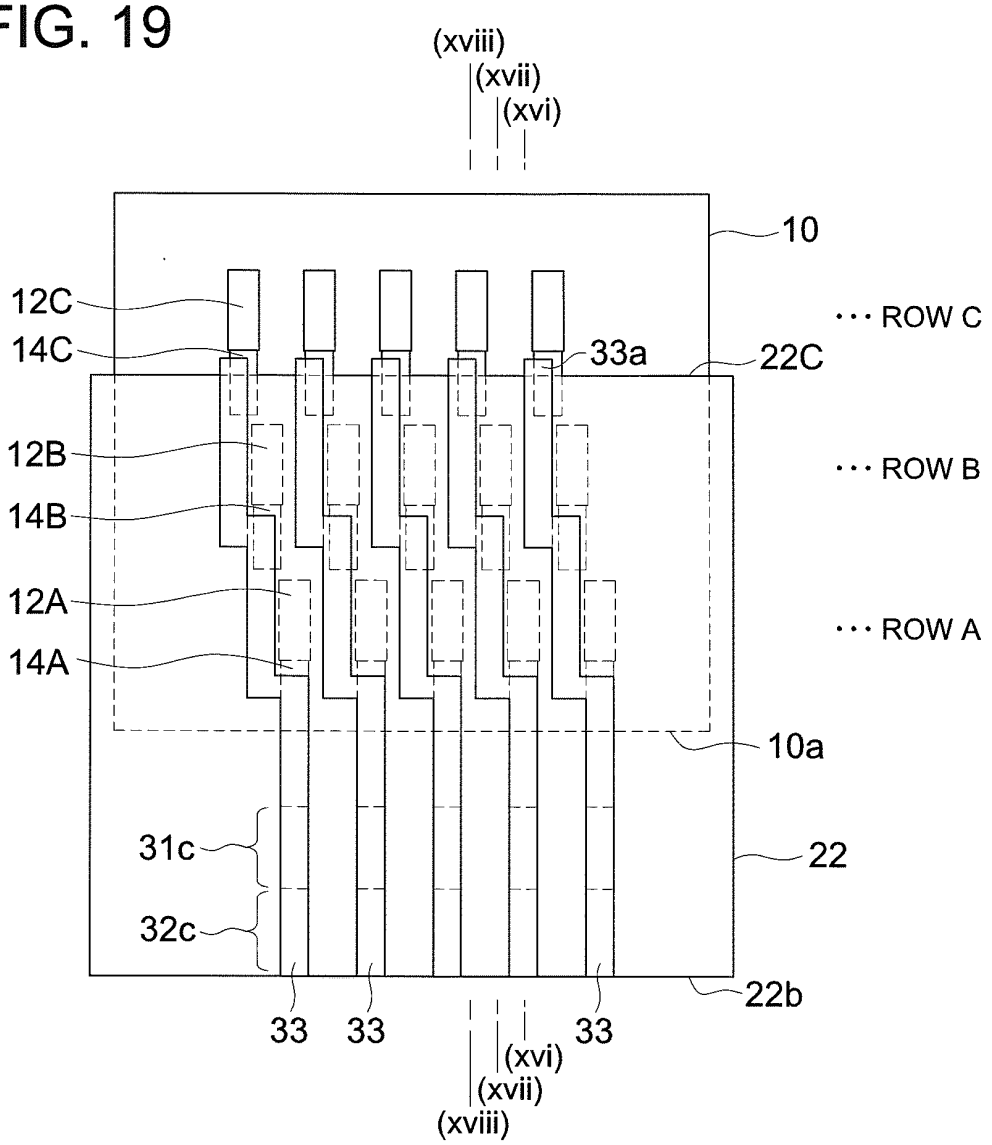

(xviii)
(xvii)
(xvi)
10
12C
14C
33a
22C
··· ROW C
12B
14B
··· ROW B
12A
14A
··· ROW A
10a
31c
32c
22
22b
33
33
33
(xvi)
(xvii)
(xviii)

FIG. 20c

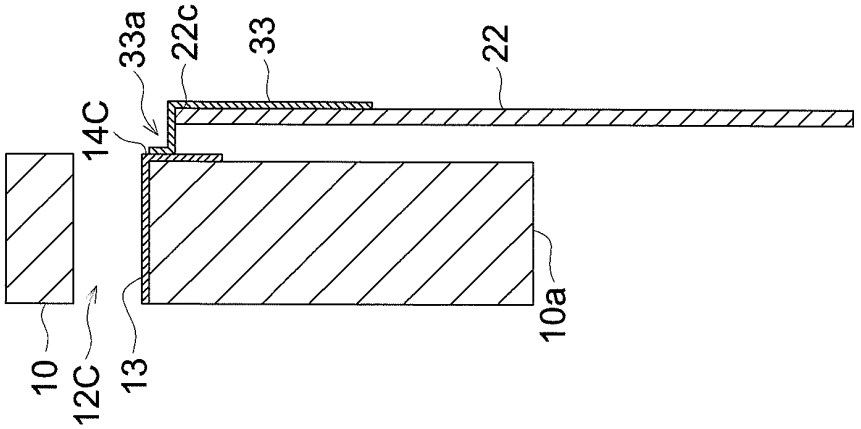


FIG. 20b

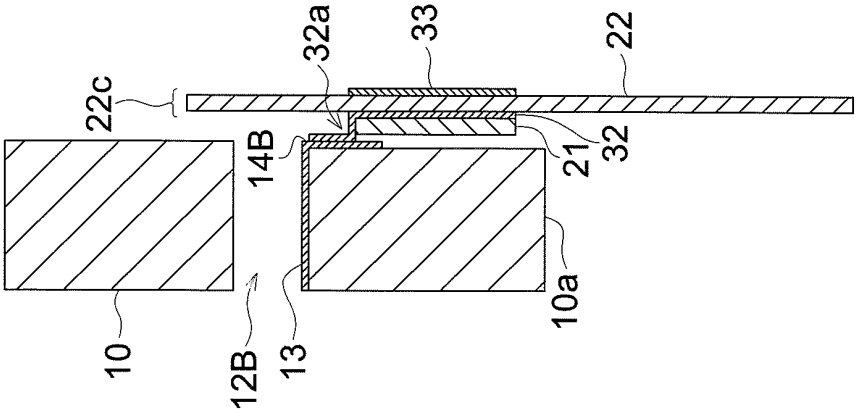


FIG. 20a

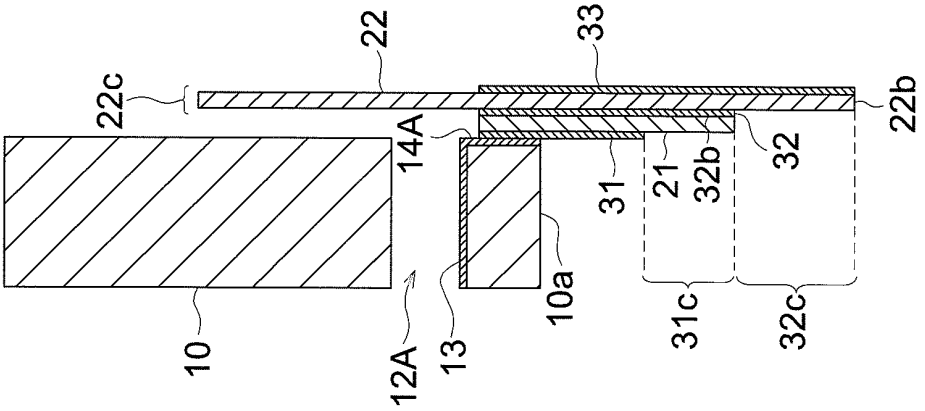


FIG. 21

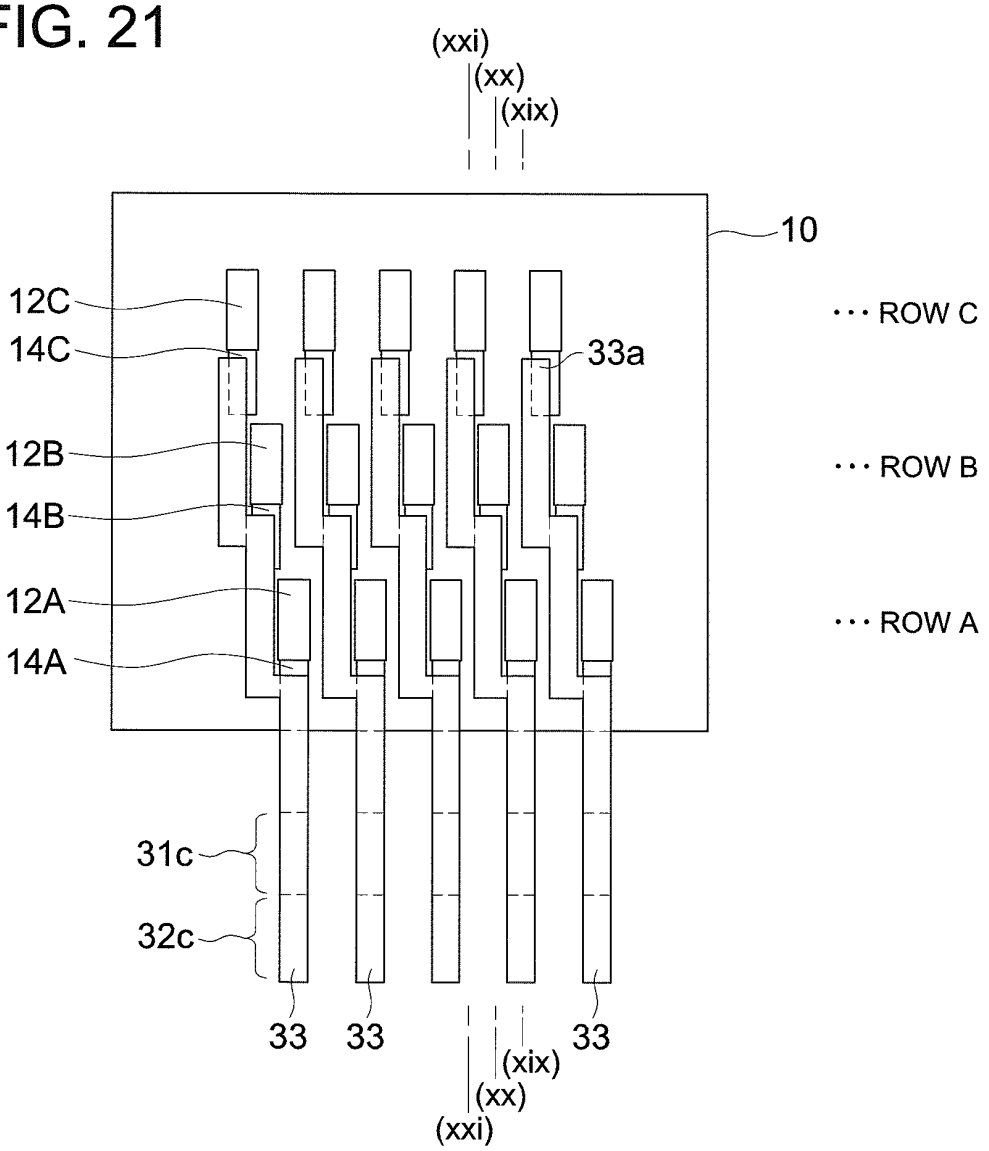

(xxi)
(xx)
(xix)
10
12C
14C
33a
12B
14B
12A
14A
··· ROW C
··· ROW B
··· ROW A
31c
32c
33
33
33
(xix)
(xx)
(xxi)

FIG. 22c

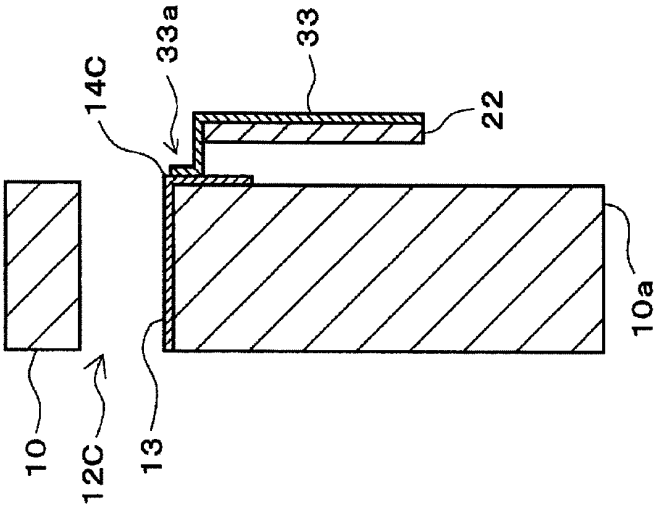


FIG. 22b

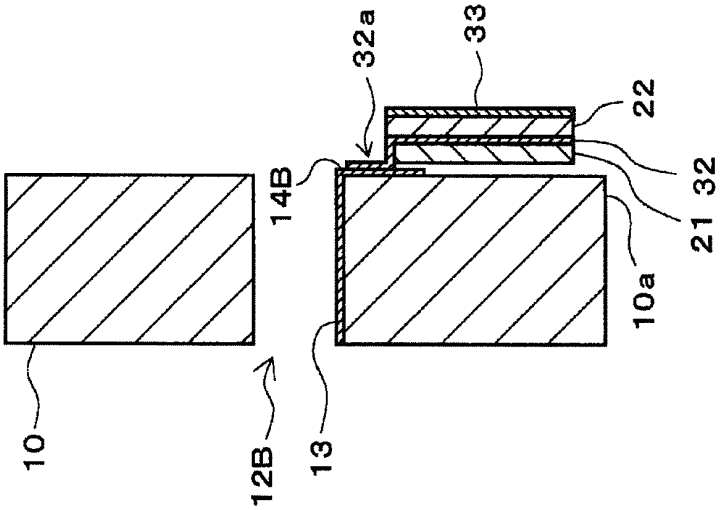


FIG. 22a

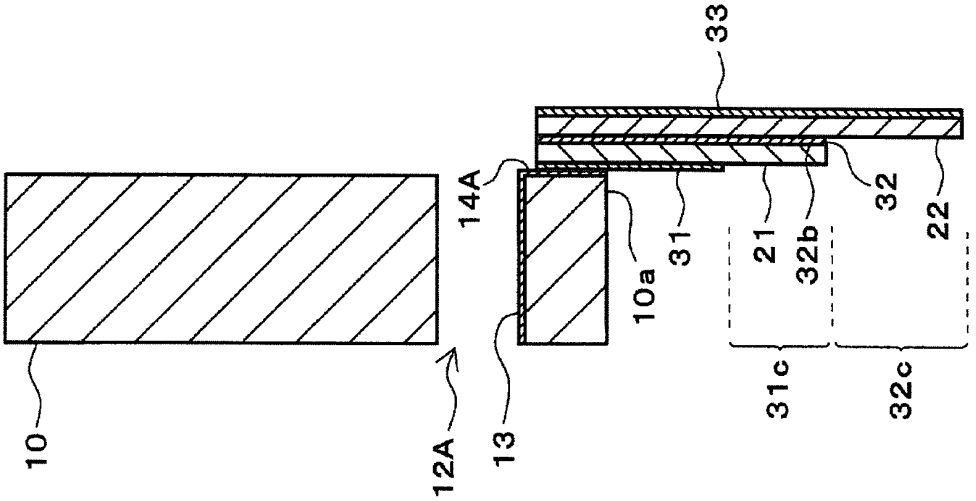


FIG. 23

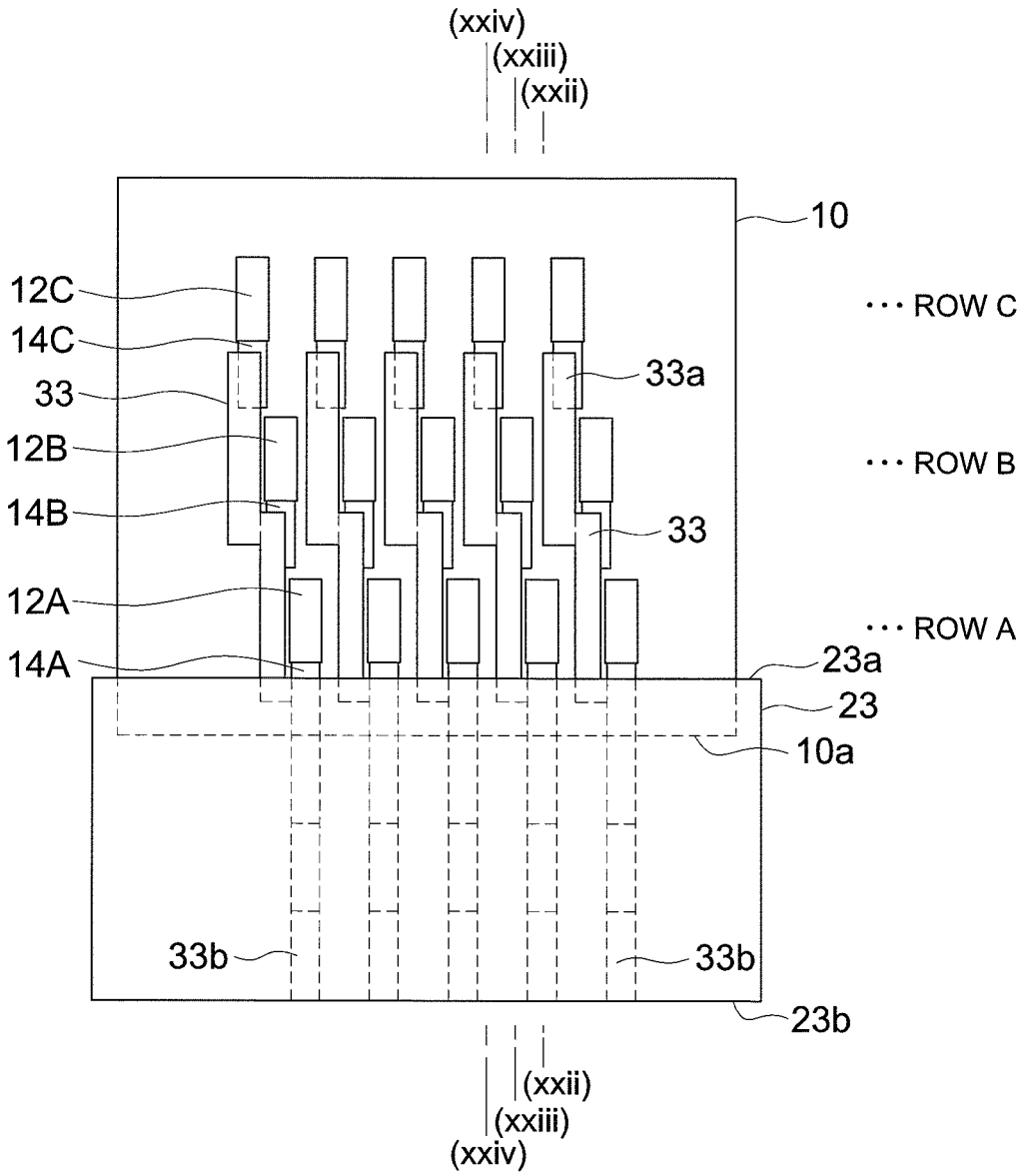

(xxiv)
(xxiii)
(xxii)
10
12C
14C
33
12B
14B
12A
14A
33a
33
23a
23
10a
33b
33b
23b
··· ROW C
··· ROW B
··· ROW A
(xxii)
(xxiii)
(xxiv)

FIG. 24a

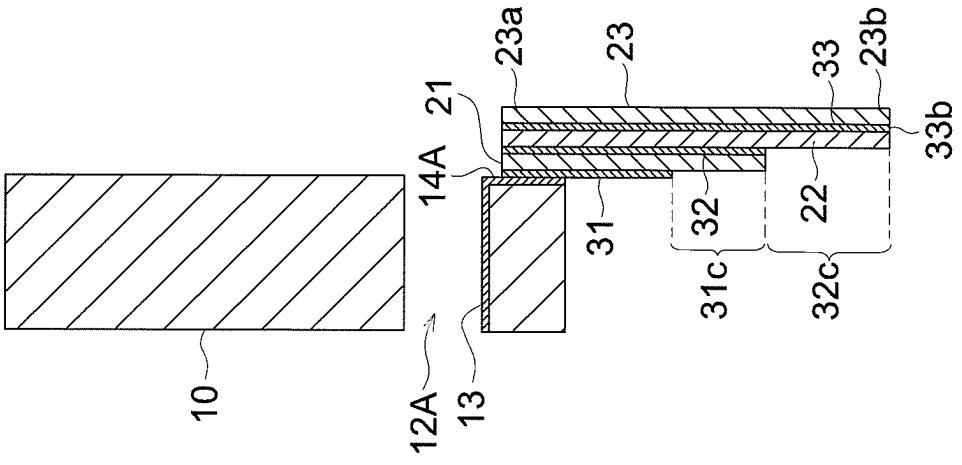


FIG. 24b

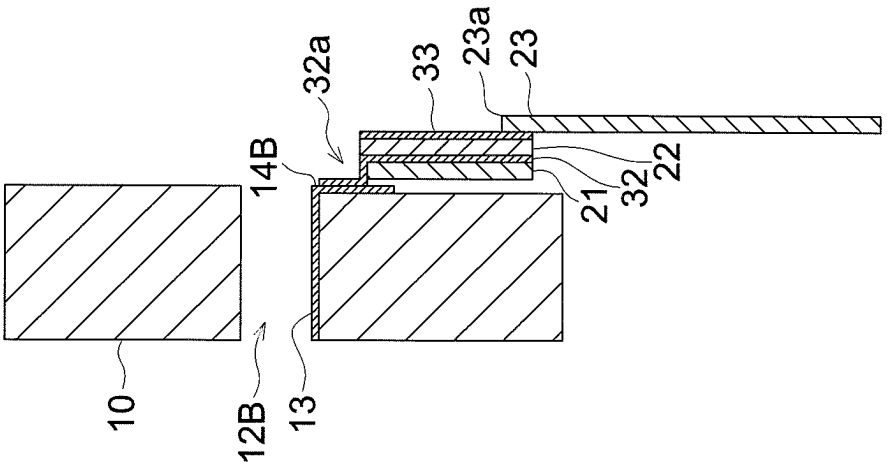


FIG. 24c

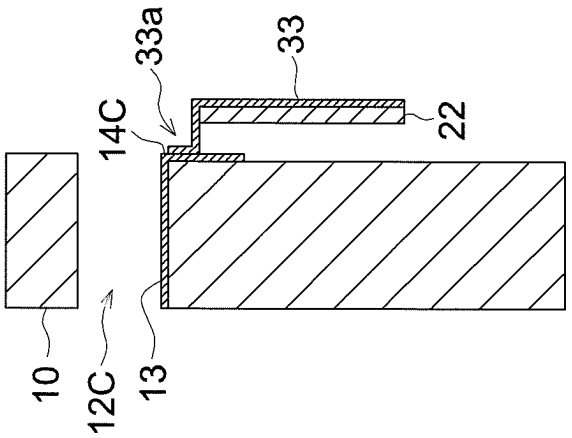


FIG. 25

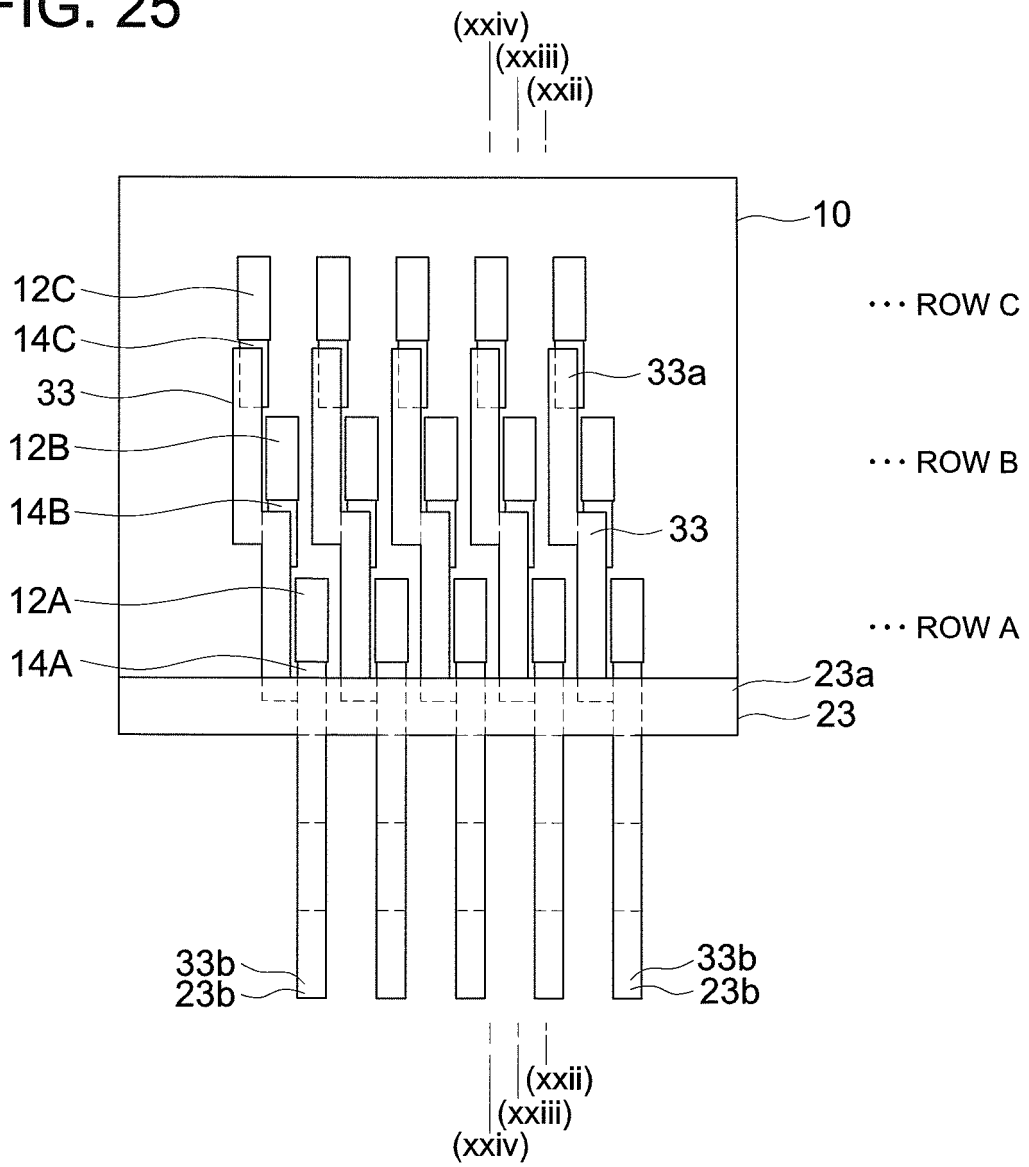

(xxiv)
(xxiii)
(xxii)
10
12C
14C
33
12B
14B
12A
14A
33a
33
23a
23
··· ROW C
··· ROW B
··· ROW A
33b
23b
33b
23b
(xxii)
(xxiii)
(xxiv)

FIG. 26c

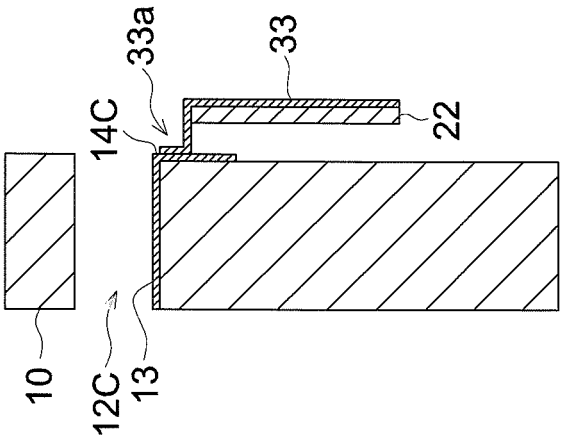


FIG. 26b

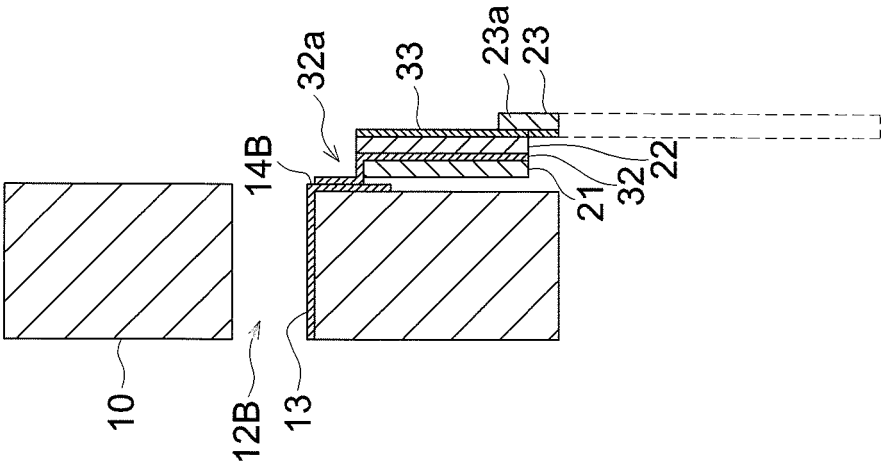


FIG. 26a

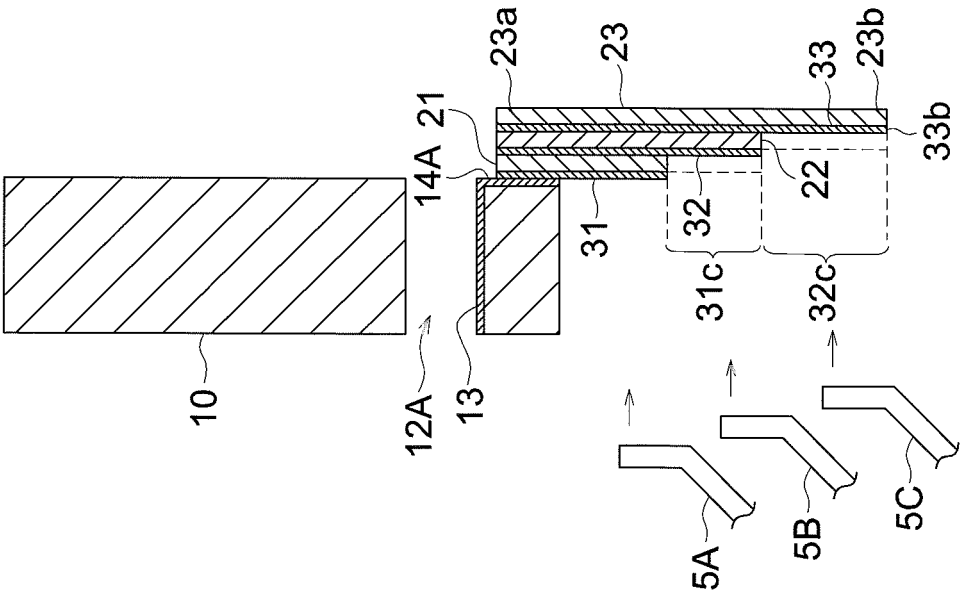


FIG. 27

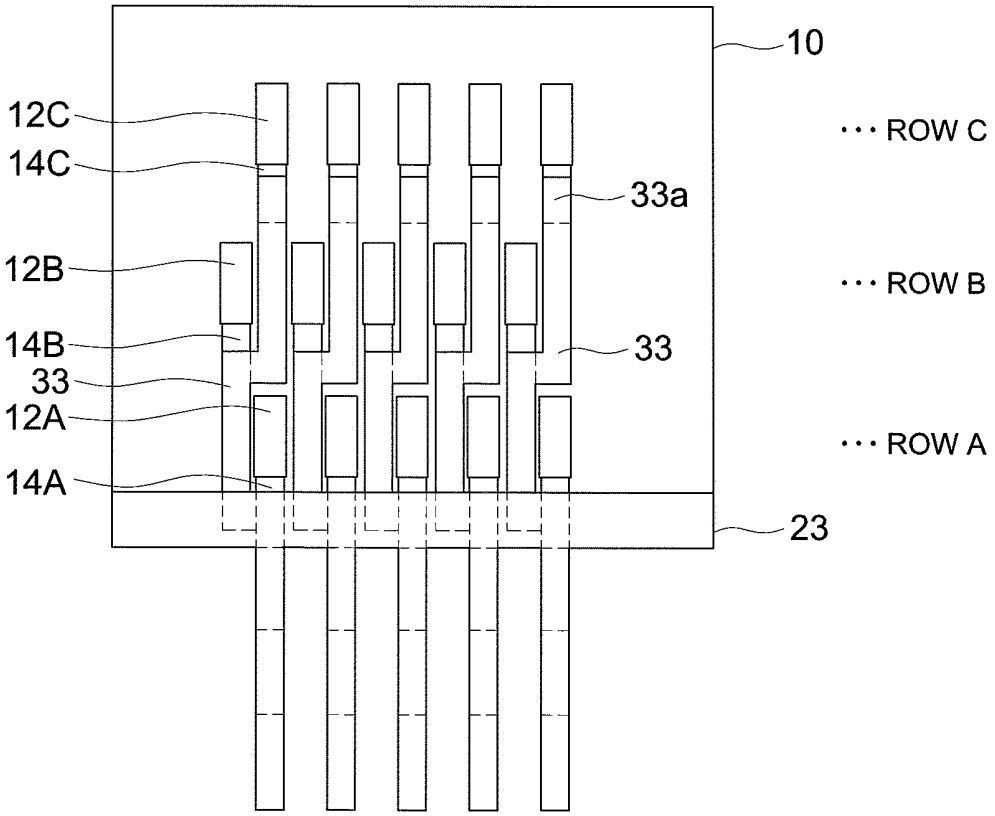

10
12C
14C
33a
··· ROW C
12B
··· ROW B
14B
33
33
12A
··· ROW A
14A
23

FIG. 28

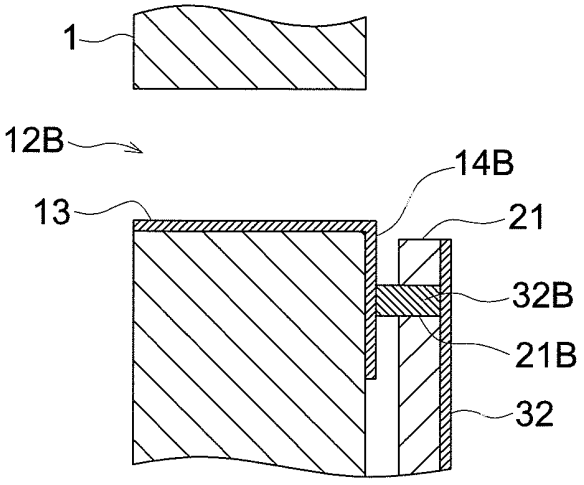

1
12B
14B
13
21
32B
21B
32

FIG. 29a

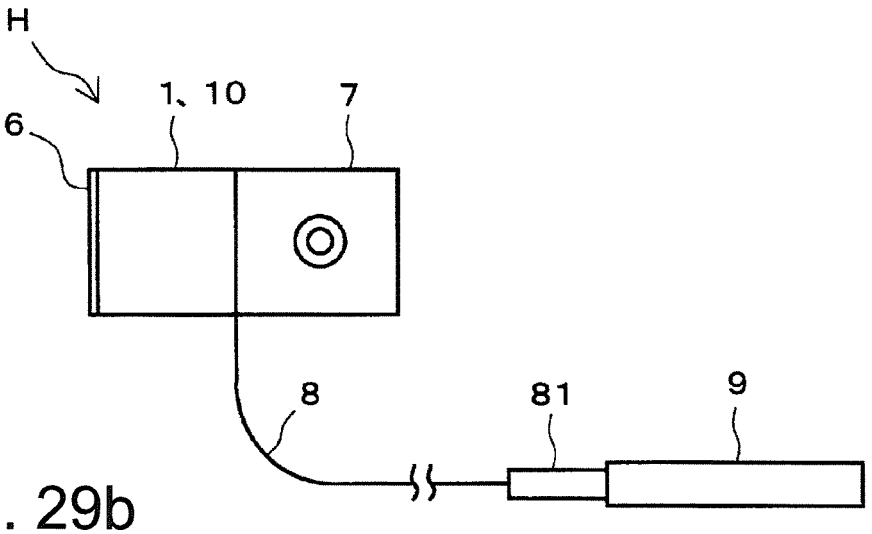
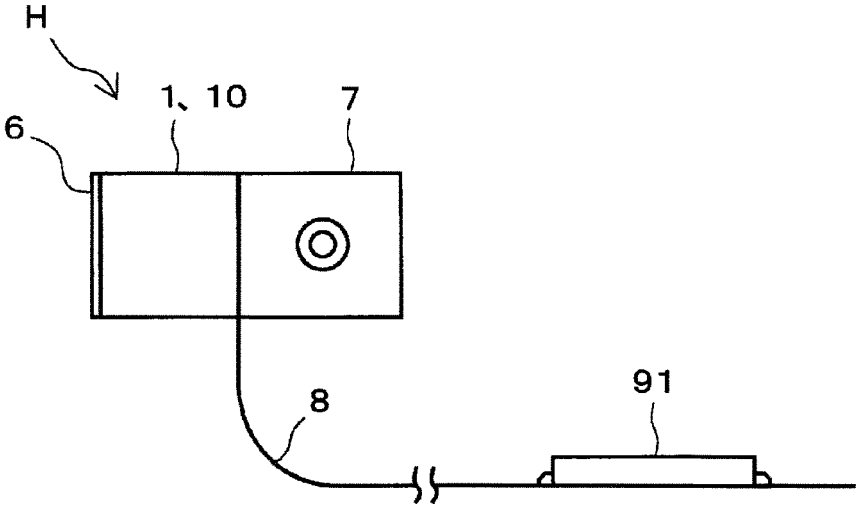


FIG. 29b



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/069573

A. CLASSIFICATION OF SUBJECT MATTER
B41J2/16(2006.01)i, *B41J2/045*(2006.01)i, *B41J2/055*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B41J2/16, B41J2/01, B41J2/045, B41J2/055, B41J2/335, B41J2/345, H01R12/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Kokai Jitsuyo Shinan Koho	1971-2010	Toroku Jitsuyo Shinan Koho	1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2009-226677 A (Konica Minolta IJ Technologies, Inc.), 08 October 2009 (08.10.2009), paragraphs [0023] to [0061]; fig. 1 to 10 (Family: none)	1-9
A	JP 2006-88676 A (Fuji Xerox Co., Ltd.), 06 April 2006 (06.04.2006), paragraphs [0059] to [0154]; fig. 1 to 20 (Family: none)	1-9

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search 07 December, 2010 (07.12.10)	Date of mailing of the international search report 21 December, 2010 (21.12.10)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/069573

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Microfilm of the specification and drawings annexed to the request of Japanese Utility Model Application No. 36587/1985(Laid-open No. 153278/1986) (Rohm Co., Ltd.), 22 September 1986 (22.09.1986), page 4, line 1 to page 6, line 12; fig. 1 to 4 (Family: none)	1-9
A	JP 2006-297669 A (Canon Inc.), 02 November 2006 (02.11.2006), paragraphs [0022] to [0044]; fig. 1 to 11 & US 2006/0232633 A1	1-9

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2006082396 A **[0004] [0014]**
- JP 2002283560 A **[0009] [0014]**
- JP 2006103117 A **[0012] [0014]**