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(54) **Low-power and area-efficient scan cell for integrated circuit testing**

Niederstrom- und bereichswirksame-Scanzelle für eine integrierte Schaltungsprüfung

Cellule de balayage à rendement surfacique élevé et faible consommation pour test de circuit intégré

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Description

Priority Claim

[0001] The present application claims priority to U.S. Provisional Patent Application Serial No. 61/467,411, filed March 25, 2011 and entitled "Low Power Flip-Flop Design.

Field of the Invention

[0002] The present invention relates generally to integrated circuit testing, and more particularly to integrated circuit testing using scan test circuitry.

Background of the Invention

[0003] Integrated circuits are often designed to incorporate scan test circuitry that facilitates testing for various internal fault conditions. Such scan test circuitrytypically comprises scan chains, which are chains of flip-flops that are used to form serial shift registers for applying test patterns at inputs to combinational logic of the integrated circuit and for reading out the corresponding results. A given one of the flip-flops of the scan chain may be viewed as an example of what is more generally referred to herein as a "scan cell."

[0004] In one exemplary arrangement, an integrated circuit with scan test circuitry may have a scan shift mode of operation and a functional mode of operation. A flag may be used to indicate whether the integrated circuit is in scan shift mode or functional mode. In the scan shift mode, the flip-flops of the scan chain are configured as a serial shift register. A test pattern is then shifted into the serial shift register formed by the flip-flops of the scan chain.Once the desired test pattern has been shifted in, the scan shift mode is disabled and the integrated circuit is placed in its functional mode. Internal combinational logic results occurring during this functional mode of operation are then captured by the chain of scan flip-flops. The integrated circuit is then once again placed in its scan shift mode of operation, in order to allow the captured combinational logic results to be shifted out of the serial shift register formed by the scan flip-flops, as a new test pattern is being scanned in.This process is repeated until all desired test patterns have been applied to the integrated circuit.

[0005] As integrated circuits have become increasingly complex, scan compression techniques have been developed which reduce the number of test patterns that need to be applied when testing a given integrated circuit, and therefore also reduce the required test time. Additional details regarding compressed scan testing are disclosed in U.S.Patent No. 7,831,876, entitled "Testing a Circuit with Compressed Scan Subsets," which is commonlyassigned herewith.

[0006] U.S. Patent Application Publication No. 2008/0250283 discloses a scannable flip-flop having a normal operating mode during which normal data output is enabled and scan data output is disabled and a scan-shift mode during which normal data output is disabled and scan data output is enabled. U.S. Patent Application Publication No. 2009/0172819 discloses methods and apparatus for implementing integrated circuit security features to selectively disable testability features on an integrated circuit chip. U.S. Patent Application Publication No. 2006/0095802 discloses conserving energy during a functional mode of a processor by disabling a scan chain.

[0007] Nonetheless, a need remains for further improvements in scan test circuitry. For example, significant reductions in the power and area requirements associated with implementation of scan chains would be highly desirable.

Summary of the Invention

[0008] The invention provides an apparatus according to claim 1. The invention further provides a method according to claim 8.

[0009] Illustrativeembodiments of the invention provide improved circuitry and techniques for scantesting of integrated circuits.For example, in one or more such embodiments, scan test circuitryof an integrated circuit is configured to include at least one scan chain that comprises low-power and area-efficient scan cells. The scan cells are advantageously configured to provide reduced power consumption for an integrated circuit in both scan shift and functional modes of operation, by eliminating unnecessary logic transitions that would otherwise occur in these modes in portions of the integrated circuit that are driven by corresponding scan and functional data outputs of the scan cells. This may be achieved in one or more of the illustrative embodiments without any substantial increase in the power consumption or area requirements of the scan cells themselves, so as to provide an overall reductionin the power consumption and area requirements of the integrated circuit.

[0010] In one arrangement, an integrated circuit comprises scan test circuitry and additional circuitry subject to testing utilizing the scan test circuitry. The scan test circuitry comprises at least one scanchain having a plurality of scan cells, with the scan chain being configured to operate as a serial shift register in a scan shift mode of operation and to capture functional data from at least a portion of the additional circuitry in a functional mode of operation. At least a given one of the scan cells of the scan chain comprises output control circuitry which is configured to disable a functional data output of the scan cell in the scan shift mode of operation and to disable a scan output of the scan cell in the functional mode of operation.

[0011] In another arrangement, a scan cell is configurable with a plurality of other scan cells into a scan chain having a scan shift mode of operation and a functional mode of operation. The scan cell comprises output con-

trol circuitry which is configured to disable a functional data output of the scan cell in the scan shift mode of operation and to disable a scan output of the scan cell in the functional mode of operation.

[0012] A given scan cell in one or more of the illustrative embodiments may comprise, in addition to its functional data output and its scan output, a functional data input, a scan input, a scan enable input, a multiplexer, and a flip-flop. The multiplexer has a first input coupled to the functional data input, a second input coupled to the scan input, and a select line coupled to the scan enable input, and the flip-flop has an input coupled to an output of the multiplexer.The output control circuitry iscoupled between an output of the flip-flop and the functionaldata and scan outputs of the scan cell.

[0013] Suchascan cell configuration eliminates unnecessary logic transitions that would otherwise occur in those portions of an integrated circuit that are driven by a scan output of the scan cell in the functional mode of operation or by a functional data outputof the scan cell in the scan shift mode of operation. As mentioned above, this advantage is achieved without significantly increasing the power or area requirements of the scan cell itself. For example, the scan cell does not require additional flip-flops or signal ports, nor does it exhibit significant additional timing dependencies.

Brief Description of the Drawings

[0014]

FIG. 1 is a block diagram showing an integrated circuit testing system comprising a tester and an integrated circuit under test in an illustrative embodiment.

FIG. 2 illustrates one example of the manner in which scan chains may be arranged between combinational logic in the integrated circuit of FIG. 1.

FIG.3 is a schematic diagram showing one possible implementation of a given one of the scan cells of FIG. 2.

FIG. 4 is a schematic diagram showing another possible implementation of a given one of the scan cells of FIG. 2.

FIG. 5 shows a substantially equivalent circuit of the FIG. 4 scan cell using a NAND gate.

FIG. 6 shows one possible implementation of the testing system of FIG. 1.

FIG. 7 is a block diagram of a processing system for generating an integrated circuit design comprising one or more scan chains each having one or more scan cells of the type shown in FIGS. 3-5.

Detailed Description of the Invention

[0015] The invention will be illustrated herein in conjunction with exemplary testing systems and corresponding integrated circuits comprising scan test circuitry for supporting scan testing of other internal circuitry of those integrated circuits. It should be understood, however, that the invention is more generally applicable to any testing system or associated integrated circuit in which it is desirable to provide improved performance in terms of reduced power consumption and area requirements for scan testing.

[0016] FIG. 1 shows a testing system 100 comprising a tester 102 and an integrated circuit under test 104. The integrated circuit 104 comprises scan test circuitry 106 that is coupled to additional internal circuitry 108 that is subject to testing utilizing the scan test circuitry 106. The tester 102 stores scan data 110 associated with scan testing of the integrated circuit. Such scan data may correspond to test patterns provided by a test pattern generator 112. In other embodiments, at least a portion of the tester 102, such as the test pattern generator 112, may be incorporated into the integrated circuit 104.

[0017] The particular configuration of testing system 100 as shown in FIG. 1 is exemplary only, and the testing system 100 in other embodiments may include other elements in addition to or in place of those specifically shown, including one or more elements of a type commonly found in a conventional implementation of such a system. For example, various elements of the system 100 may be implemented, by way of example and without limitation, utilizing a microprocessor, central processing unit (CPU), digital signal processor (DSP), application-specific integrated circuit (ASIC), field-programmable gate array (FPGA), or other type of data processing device, as well as portions or combinations of these and other devices.

[0018] Embodiments of the present invention may be configured to utilize compressed or noncompressed scan testing, and the invention is not limited in this regard. However, certain embodiments such as that shown in FIG. 2 will be described primarily in the context of compressed scan testing.

[0019] Referring now to FIG. 2, portions of one potential configuration of the integrated circuit 104 are shown in greater detail. In this compressed scan testing arrangement, the scan test circuitry 106 comprises a decompressor 200, a compressor 202, and a plurality of scan chains 204-k, where $k = 1, 2, \ldots K$. Each of the scan chains 204 comprises a plurality of scan cells 206, and is configurable to operate as a serial shift register in a scan shift mode of operation of the integrated circuit 104 and to capture functional data from circuitry under test 207 in a functional mode of operation of the integrated circuit 104. The first scan chain 204-1 is of length n_1 and therefore comprises n_1 scan cells denoted 206-1 through 206-n_1. More generally, scan chain 204-k is of length n_k and therefore comprises a total of n_k scan cells. Circuitry under test 207 in this embodiment comprises a plurality of combinational logic blocks, of which exemplary blocks 208, 210 and 212 are shown. The combinational logic blocks are illustratively arranged between primary inputs 214 and primary outputs 216 and separated from one

another by the scan chains 204.

[0020] Combinational logic blocks such as 208, 210 and 212 may be viewed as examples of what are more generally referred to herein as "additional circuitry" that is subject to testing utilizing scan test circuitry in embodiments of the present invention. By way of example, such blocks may represent portions of different integrated circuit cores, such as respective read channel and additional cores of a system-on-chip (SOC) integrated circuit in a hard disk drive (HDD) controller application.

[0021] The decompressor 200 receives compressed scan data from the tester 102 and decompresses that scan data to generate scan test input data that is shifted into the scan chains 204 when such chains are configured as respective serial shift registers in a scan shift mode of operation. The compressor 202 receives scan test output data shifted out of the scan chains 204, also when such chains are configured as respective serial shift registers in the scan shift mode of operation, and compresses that scan test output data for delivery back to the tester 102. Additional details regarding the operation of scan compression elements such as decompressor 200 and compressor 202 may be found in the above-cited U.S. Patent No. 7,831,876. Again, scan compression elements such as decompressor 200 and compressor 202 may be eliminated in other embodiments.

[0022] The scan cells 206 in the illustrative embodiment of FIG. 2 are advantageously configured as low-power and area-efficient scan cells that can controllably disable their functional data outputs in the scan shift mode of operation and controllably disable their scan outputs in the functional mode of operation. Such an arrangement provides reduced power consumption for the integrated circuit 104 in both scan shift and functional modes of operation, by eliminating unnecessary logic transitions that would otherwise occur in these modes in portions of the integrated circuit 104 that are driven by corresponding scan and functional data outputs of the scan cells. As will become apparent, this desirable functionality is achieved without significantly increasing the power or area requirements of the scan cell itself. For example, the scan cells 206 do not require additional flip-flops or signal ports to implement the controllable output disabling functionality, nor do they exhibit significant additional timing dependencies as a result of such functionality.

[0023] FIG. 3 shows a given one of the scan cells 206-*i* in an illustrative embodiment. The scan cell in this embodiment comprises a multiplexer 300, a flip-flop 302, first and second tri-state buffers 304-1 and 304-2, and an inverter 305. The scan cell 206-*i* has a functional data input (D), a scan input (SI), a scan enable input (SE), a functional data output (Q), a scan output (SO), a reset input (RST) and a clock input (CLK). The reset and clock inputs of the scan cell are coupled to corresponding inputs of the flip-flop 302. The flip-flop 302 also has a data input denoted D and a data output denoted Q, although these should be distinguished from the corresponding functional data input D and functional data output Q of the scan cell itself.

[0024] The multiplexer 300 has a first input 310 coupled to the functional data input D of the scan cell, a second input 312 coupled to the scan input SI of the scan cell, and a select line 314 coupled to the scan enable input SE of the scan cell. The flip-flop 302 is illustratively a resettable D-type flip-flop in the present embodiment, although other types of flip-flops can be used in other embodiments. The data input D of the flip-flop 302 is coupled to an output 315 of the multiplexer 300. The data output Q of the flip-flop 302 is coupled to inputs of the respective tri-state buffers 304-1 and 304-2.

[0025] The first and second tri-state buffers 304-1 and 304-1 and the inverter 305 may be collectively viewed as an example of what is more generally referred to herein as "output control circuitry" of the scan cell. Such output control circuitry is generally configured to disable the functional data output Q of the scan cell 206-*i* in the scan shift mode of operation and to disable the scan output SO of the scan cell 206-*i* in the functional mode of operation. The term "disable" in this context is intended to be broadly construed, and will generally cover arrangements in which logic level transitions which would otherwise occur in the corresponding output are instead prevented under certain conditions.

[0026] It will be assumed in this embodiment that a scan enable signal applied to the scan enable input SE of the scan cell is at a logic "1" level when the integrated circuit 104 is in a scan shift mode of operation and at a logic "0" level when the integrated circuit 104 is in the functional mode of operation. Other types and combinations of operating modes and scan enable signaling may be used in other embodiments.

[0027] The output control circuitry in this embodiment is coupled between the data output Q of the flip-flop 302 and the functional data and scan outputs Q and SO of the scan cell, and is operative responsive to the scan enable signal applied to the scan enable input SE of the scan cell. More particularly, the output control circuitry is operative to disable the functional data output Q of the scan cell and enable the scan output SO of the scan cell responsive to the scan enable signal being at a first binary logic level, in this embodiment a logic "1" level, and to disable the scan output SO of the scan cell and enable the functional data output Q of the scan cell responsive to the scan enable signal being at a second binary logic level, in this embodiment a logic "0" level.

[0028] In order to achieve this functionality, the scan enable signal is applied to a control input of the second tri-state buffer 304-2 and a complemented version of the scan enable signal, generated from the scan enable signal by the inverter 305, is applied to the control input of the first tri-state buffer 304-1. As a result, in the functional mode the scan output SO of the scan cell is tri-stated, thereby preventing functional transitions from propagating into portions of the integrated circuit that are driven by the scan output SO. Similarly, in the scan shift mode

of operation, the functional data output Q of the scan cell is tri-stated, thereby preventing scan transitions from propagating into portions of the integrated circuit that are driven by the functional data output.

[0029] Although only a single scan cell 206-*i* is shown in FIG. 3, it may be assumed that the other scan cells 206 of the scan chains 204 in the scan test circuitry of FIG. 2 are each configured in substantially the same manner. Alternatively, different types of scan cells may be used in different ones of the scan chains, or within the same scan chain.

[0030] As indicated above, an advantage of the scan cell 206-*i* configured as shown in FIG. 3 is that it eliminates unnecessary logic transitions that would otherwise occur in both the scan shift and functional modes of operation in portions of the circuitry under test 207 that are driven by the corresponding scan and functional data outputs of the scan cells. Such transitions can occur in portions of the integrated circuit driven by the Q output of the scan cell in the scan shift mode of operation and in portions of the integrated circuit driven by the SO output of the scan cell in the functional mode of operation. Thus, this scan cell configuration reduces power consumption in the integrated circuit 104 in both the scan shift and functional modes of operation, without unduly increasing the circuit area required to implement the scan cells or the timing complexity of the scan test circuitry.

[0031] A scan cell of the type shown in FIG. 3 may be generated by modifying a standard scan cell from an integrated circuit design library to incorporate the output control circuitry in the form of a wrapper around the standard cell. This can be achieved without requiring the modification of any internal signaling or timing features of the standard cell, and without adding ports, extra flip-flops or other internal circuitry to the standard cell. The additional circuit area needed to accommodate the output control circuitry is minimal.

[0032] It should be noted that other types of scan cells and output control circuitry may be used in other embodiments. FIG. 4 shows an example of a scan cell 206-*i* configured in accordance with another illustrative embodiment of the invention. In this embodiment, the scan cell includes the multiplexer 300 and flip-flop 302, and has the same inputs and outputs as in the FIG. 3 embodiment. However, in this embodiment the output control circuitry comprises a first pair of MOS gates 400 and a second pair of MOS gates 402.

[0033] The first pair of MOS gates 400 more particularly comprises a first PMOS transistor P1 having its gate coupled to the scan enable input SE of the scan cell, its source coupled to the data output Q of the flip-flop 302, and its drain coupled to the functional data output Q of the scan cell, and a first NMOS transistor N1 having its gate coupled to the scan enable input SE of the scan cell, its drain coupled to an upper supply potential V_{DD} and its source coupled to the functional data output Q of the scan cell.

[0034] The second pair of MOS gates 402 more particularly comprises a second PMOS transistor P2 having its gate coupled to the scan enable input SE of the scan cell, its source coupled to the scan output SO of the scan cell, and its drain coupled to a lower supply potential, illustratively ground potential in this embodiment, and a second NMOS transistor N2 having its gate coupled to the scan enable input SE of the scan cell, its source coupled to the scan output SO of the scan cell, and its drain coupled to the data output Q of the flip-flop.

[0035] In this embodiment, when a scan enable signal applied to the scan enable input SE of the scan cell 206-*i* is at a logic "1" level, the first and second PMOS transistors P1 and P2 are turned off and the first and second NMOS transistors N1 and N2 are turned on, such that the functional data output Q of the scan cell is disabled by being disconnected from the flip-flop output Q via the first PMOS transistor P1 and the scan output SO of the scan cell is enabled by being connected to the flip-flop output Q via the second NMOS transistor N2. When the scan enable signal applied to the scan enable input SE of the scan cell is at a logic "0" level, the first and second PMOS transistors P1 and P2 are turned on and the first and second NMOS transistors N1 and N2 are turned off, such that the functional data output Q of the scan cell is enabled by being connected to the flip-flop output Q via the first PMOS transistor P1 and the scan output SO of the scan cell is disabled by being disconnected from the flip-flop output Q via the second NMOS transistor N2.

[0036] It should also be noted that the particular arrangement of MOS gates used in the FIG. 4 embodiment is presented by way of example only, and other embodiments may use different circuitry arrangements to achieve the desired functionality. For example, analogous arrangements may be configured in which the NMOS gates are replaced with PMOS gates and vice-versa, with appropriate adjustment of signaling polarities.

[0037] FIG. 5 shows a substantially equivalent implementation of the FIG. 4 embodiment. In this implementation, the output control circuitry comprises a logic gate 500 having a first input coupled to the Q output of the flip-flop 302, a second input coupled to the scan enable input SE of the scan cell, a first output coupled to the functional data output Q of the scan cell and a second output coupled to the scan output SO of the scan cell. The logic gate 500 is illustratively a NAND gate in the present embodiment, although other types and arrangements of logic gates can be used in other embodiments.

[0038] As mentioned above, low-power and area-efficient scan cells such as those illustrated in FIGS. 3 through 5 can significantly reduce the power consumption of an integrated circuit in both scan shift and functional modes of operation, without adversely impacting signaling and timing of the scan test circuitry. Existing scan flip-flops or other types of scan cells can be easily replaced with the low-power and area-efficient scan cells without any change in scan test functionality.

[0039] The tester 102 in the testing system 100 of FIG. 1 need not take any particular form. One possible exam-

ple is shown in FIG. 6, in which a tester 602 comprises a load board 604 in which an integrated circuit 605 to be subject to scan testing using the techniques disclosed herein is installed in a central portion 606 of the load board 604. The tester 602 may also comprise processor and memory elements for executing stored computer code, although such elements are not explicitly shown in the figure. Numerous alternative testers may be used to perform scan testing of an integrated circuit as disclosed herein.

[0040] The insertion of scan cells to form scan chains in scan test circuitry of an integrated circuit design may be performed in a processing system 700 of the type shown in FIG. 7. Such a processing system is configured for use in designing integrated circuits such as integrated circuit 104 to include scan test circuitry 106. The processing system 700 comprises a processor 702 coupled to a memory 704. Also coupled to the processor 702 is a network interface 706 for permitting the processing system to communicate with other systems and devices over one or more networks. The network interface 706 may therefore comprise one or more transceivers. The processor 702 implements a scan module 710 for supplementing core designs 712 with scan cells 714 in the manner disclosed herein, in conjunction with utilization of integrated circuit design software 716.

[0041] Elements such as 710, 712, 714 and 716 are implemented at least in part in the form of software stored in memory 704 and processed by processor 702. For example, the memory 704 may store program code that is executed by the processor 702 to implement particular scan cell insertion functionality of module 710 within an overall integrated circuit design process. The memory 704 is an example of what is more generally referred to herein as a computer-readable medium or other type of computer program product having computer program code embodied therein, and may comprise, for example, electronic memory such as RAM or ROM, magnetic memory, optical memory, or other types of storage devices in any combination. The processor 702 may comprise a microprocessor, CPU, ASIC, FPGA or other type of processing device, as well as portions or combinations of such devices.

[0042] As indicated above, embodiments of the present invention may be implemented in the form of integrated circuits. In a given such integrated circuit implementation, identical die are typically formed in a repeated pattern on a surface of a semiconductor wafer. Each die includes scan test circuitry as described herein, and may include other structures or circuits. The individual die are cut or diced from the wafer, then packaged as an integrated circuit. One skilled in the art would know how to dice wafers and package die to produce integrated circuits. Integrated circuits so manufactured are considered part of this invention.

[0043] Again, it should be emphasized that the embodiments of the invention as described herein are intended to be illustrative only. For example, the invention can be implemented using a wide variety of other types of scan test circuitry, with different types and arrangements of scan cells, gates and other circuit elements, than those previously described in conjunction with the illustrative embodiments. These and numerous other alternative embodiments within the scope of the following claims will be readily apparent to those skilled in the art.

Claims

1. An apparatus for use in scan testing an integrated circuit (104), the apparatus comprising:

a scan cell (206) configured to be arranged with a plurality of other scan cells into a scan chain (204) having a scan shift mode of operation and a functional mode of operation;
wherein the scan cell comprises output control circuitry (304-1, 304-2, 305; 400, 402; 500) which is configured to disable a functional data output of the scan cell in the scan shift mode of operation and to disable a scan output of the scan cell in the functional mode of operation;

wherein the scan cell further comprises:

a functional data input;
a scan input;
a scan enable input;
a multiplexer (300) having a first input coupled to the functional data input, a second input coupled to the scan input, and a select line coupled to the scan enable input; and
a flip-flop (302) having an input coupled to an output of the multiplexer;
the output control circuitry being coupled between an output of the flip-flop and the functional data and scan outputs of the scan cell; and

CHARACTERIZED IN THAT the output control circuitry comprises one of:

i) a first tri-state buffer (304-1) coupled between the output of the flip-flop and the functional data output of the scan cell; and
a second tri-state buffer (304-2) coupled between the output of the flip-flop and the scan output of the scan cell;
wherein a scan enable signal is applied to a control input of one of the first and second tri-state buffers and a complemented version of the scan enable signal is applied to the control input of the other one of the first and second tri-state buffers;
ii) a first pair of devices comprising a first transistor and a second transistor; and
a second pair of devices comprising a third tran-

sistor and a fourth transistor;
wherein the first pair of devices is configured to disable the functional data output of the scan cell responsive to a scan enable signal being at a first binary logic level and to enable the functional data output of the scan cell responsive to a scan enable signal being at a second binary logic level;
wherein the second pair of devices is configured to disable the scan output of the scan cell responsive to the scan enable signal being at a second binary logic level and to enable the scan output of the scan cell responsive to the scan enable signal being at a first binary logic level; and
wherein the first transistor and the third transistor are one of NMOS transistors and PMOS transistors and the second and fourth transistors are the other one of NMOS transistors and PMOS transistors; and
iii) a logic gate (500) having a first input coupled to the output of the flip-flop, a second input coupled to the scan enable input of the scan cell, a first output coupled to the functional data output of the scan cell and a second output coupled to the scan output of the scan cell.

2. The apparatus of claim 1 wherein the output control circuitry is operative to disable the functional data output of the scan cell and enable the scan output of the scan cell responsive to a scan enable signal being at a first binary logic level and to disable the scan output of the scan cell and enable the functional data output of the scan cell responsive to the scan enable signal being at a second binary logic level.

3. The apparatus of claim 1 wherein:

the first transistor comprises a first PMOS transistor having its gate coupled to the scan enable input, its source coupled to the output of the flip-flop, and its drain coupled to the functional data output of the scan cell;
the second transistor comprises a first NMOS transistor having its gate coupled to the scan enable input, its drain coupled to an upper supply potential and its source coupled to the functional data output of the scan cell;
the third transistor comprises a second PMOS transistor having its gate coupled to the scan enable input, its source coupled to the scan output of the scan cell, and its drain coupled to a lower supply potential; and
the fourth transistor comprises a second NMOS transistor having its gate coupled to the scan enable input, its source coupled to the scan output of the scan cell, and its drain coupled to the output of the flip-flop.

4. The apparatus of claim 3 wherein responsive to a scan enable signal applied to the scan enable input of the scan cell being at a logic high level, the first and second PMOS transistors are turned off and the first and second NMOS transistors are turned on, such that the functional data output of the scan cell is disabled by being disconnected from the flip-flop output via the first PMOS transistor and the scan output of the scan cell is enabled by being connected to the flip-flop output via the second NMOS transistor.

5. The apparatus of claim 3 wherein responsive to a scan enable signal applied to the scan enable input of the scan cell being at a logic low level, the first and second PMOS transistors are turned on and the first and second NMOS transistors are turned off, such that the functional data output of the scan cell is enabled by being connected to the flip-flop output via the first PMOS transistor and the scan output of the scan cell is disabled by being disconnected from the flip-flop output via the second NMOS transistor.

6. An integrated circuit (104) comprising:

scan test circuitry (106) comprising the apparatus of claim 1; and
additional circuitry (108) subject to testing utilizing the scan test circuitry.

7. A disk drive controller comprising the integrated circuit of claim 6.

8. A method of scan testing an integrated circuit, comprising:

providing scan test circuitry (106) comprising at least one scan chain (204) having a plurality of scan cells (206), the scan chain being configured to operate as a serial shift register in a scan shift mode of operation and to capture functional data from at least a portion of additional circuitry of the integrated circuit in a functional mode of operation;
disabling a functional data output of at least a given one of the scan cells in the scan shift mode of operation; and
disabling a scan output of the given scan cell in the functional mode of operation;
wherein a given one of the scan cells comprises:

a functional data input;
a scan input;
a scan enable input;
a multiplexer (300) having a first input coupled to the functional data input, a second input coupled to the scan input, and a select line coupled to the scan enable input; and

a flip-flop (302) having an input coupled to an output of the multiplexer;
the output control circuitry being coupled between an output of the flip-flop and the functional data and scan outputs of the given scan cell; and

CHARACTERIZED IN THAT the disabling steps are performed by output control circuitry comprising one of:

i) a first tri-state buffer (304-1) coupled between the output of the flip-flop and the functional data output of the given scan cell; and a second tri-state buffer (304-2) coupled between the output of the flip-flop and the scan output of the given scan cell;
wherein a scan enable signal is applied to a control input of one of the first and second tri-state buffers and a complemented version of the scan enable signal is applied to the control input of the other one of the first and second tri-state buffers;
ii) a first pair of devices comprising a first transistor and a ***second*** transistor; and
a second pair of devices comprising a ***third*** transistor and a ***fourth*** transistor;
wherein the first pair of devices is configured to disable the functional data output of the given scan cell responsive to a scan enable signal being at a first binary logic level and to enable the functional data output of the given scan cell responsive to a scan enable signal being at a second binary logic level;
wherein the second pair of devices is configured to disable the scan output of the given scan cell responsive to the scan enable signal being at a second binary logic level and to enable the scan output of the given scan cell responsive to the scan enable signal being at a first binary logic level; and
wherein the first transistor and the third transistor are one of NMOS transistors and PMOS transistors and the second and fourth transistors are the other one of NMOS transistors and PMOS transistors; and
iii) a logic gate (500) having a first input coupled to the output of the flip-flop, a second input coupled to the scan enable input of the given scan cell, a first output coupled to the functional data output of the given scan cell and a second output coupled to the scan output of the given scan cell.

9. The method of claim 8 wherein the disabling steps further comprise:

disabling the functional data output of the scan cell and enabling the scan output of the scan cell responsive to a scan enable signal being at a first binary logic level; and
disabling the scan output of the scan cell and enabling the functional data output of the scan cell responsive to the scan enable signal being at a second binary logic level.

10. A computer program product comprising a non-transitory computer-readable storage medium having computer program code embodied therein for use in scan testing an integrated circuit, wherein the computer program code when executed in a testing system (100) causes the testing system to perform the steps of the method of claim 8.

11. A processing system (700) comprising:

a processor (702); and
a memory (704) coupled to the processor and configured to store information ***of the apparatus*** of claim 1.

Patentansprüche

1. Ein Gerät zum Scan-Testen einer integrierten Schaltung (104), das Folgendes umfasst:

eine Scan-Zelle (206), die konfiguriert ist, um mit einer Vielzahl anderer Scan-Zellen zu einer Scan-Kette (204) mit einer Scan-Shift-Betriebsweise und einer funktionellen Betriebsweise angeordnet zu werden;
wobei die Scan-Zelle einen Ausgabesteuerschaltkreis (304-1, 304-2, 305; 400, 402; 500) umfasst, der konfiguriert ist, um eine funktionelle Datenausgabe der Scan-Zelle in der Scan-Shift-Betriebsweise sowie eine Scan-Ausgabe der Scan-Zelle in der funktionellen Betriebsweise zu deaktivieren;
wobei die Scan-Zelle ferner Folgendes umfasst:

eine funktionelle Dateneingabe;
eine Scan-Eingabe;
eine Scan-Aktivierungseingabe;
einen Multiplexer (300), der eine erste, an die funktionelle Dateneingabe gekoppelten Eingabe, eine zweite, an die Scan-Eingabe gekoppelten Eingabe und eine an die Scan-Aktivierungseingabe gekoppelte Auswähllinie hat; sowie
ein Flipflop (302) mit einer Eingabe, die an eine Ausgabe Multiplexers gekoppelt ist;
wobei der Ausgabesteuerschaltkreis zwischen einer Ausgabe des Flipflops und den funktionellen Daten- und Scan-Ausgaben der Scan-Zelle gekoppelt ist; und

DADURCH GEKENNZEICHNET, DASS der Ausgabesteuerkreis eines bzw. einen der Folgenden umfasst:

1.) einen ersten Tristate-Puffer (304-1), der zwischen der Ausgabe des Flipflops und der funktionellen Datenausgabe der Scan-Zelle gekoppelt ist; sowie
einen zweiten Tristate-Puffer (304-2), der zwischen der Ausgabe des Flipflops und der Scan-Ausgabe der Scan-Zelle gekoppelt ist;
wobei einer Steuereingabe eines der ersten und zweiten Tristate-Puffer ein Scan-Aktivierungssignal und der Steuereingabe eines der anderen der ersten und zweiten Tristate-Puffer eine ergänzte Version des Scan-Aktivierungssignals angelegt wird;
2.) ein erstes Paar von Geräten, das einen ersten und einen zweiten Transistor umfasst; und
ein zweites Paar von Geräten, das einen dritten und einen vierten Transistor umfasst;
wobei das erste Paar von Geräten konfiguriert ist, um die funktionelle Datenausgabe der Scan-Zelle in Reaktion auf ein Scan-Aktivierungssignal zu deaktivieren, das sich auf einem ersten binären Logikpegel befindet, sowie um die funktionelle Datenausgabe der Scan-Zelle in Reaktion auf ein Scan-Aktivierungssignal zu aktivieren, das sich auf einem zweiten binären Logikpegel befindet;
wobei das zweite Paar von Geräten konfiguriert ist, um die Scan-Ausgabe der Scan-Zelle in Reaktion auf das Scan-Aktivierungssignal zu desaktivieren, das sich auf einem zweiten binären Logikpegel befindet, und um die Scan-Ausgabe der Scan-Zelle in Reaktion auf das Scan-Aktivierungssignal zu aktivieren, das sich auf einem ersten binären Logikpegel befindet; und
wobei der erste und der dritte Transistor jeweils NMOS- und PMOS-Transistoren und die zweiten und vierten Transistoren jeweils einer der anderen NMOS- und PMOS-Transistoren sind; und
3.) ein Logikgatter (500), wobei eine erste Eingabe an die Ausgabe des Flipflops, eine zweite Eingabe an die Scan-Aktivierungseingabe der Scan-Zelle, eine erste Ausgabe an die funktionelle Datenausgabe der Scan-Zelle und eine zweite Ausgabe an die Scan-Ausgabe der Scan-Zelle gekoppelt sind.

2. Das Anspruch 1 entsprechende Gerät, wobei der Ausgabesteuerschaltkreis die Funktion hat, in Reaktion auf ein Scan-Aktivierungssignal auf einem ersten binären Logikpegel die funktionelle Datenausgabe der Scan-Zelle zu deaktivieren und die Scan-Ausgabe der Scan-Zelle zu aktivieren, sowie in Reaktion auf das Scan-Aktivierungssignal auf einem zweiten binären Logikpegel die Scan-Ausgabe der Scan-Zelle zu deaktivieren und die funktionelle Datenausgabe der Scan-Zelle zu aktivieren.

3. Das Anspruch 1 entsprechende Gerät, wobei:

der erste Transistor einen ersten PMOS-Transistor umfasst, dessen Gatter an die Scan-Aktivierungseingabe, dessen Source an die Ausgabe des Flipflops und dessen Drain an die funktionellen Datenausgabe der Scan-Zelle gekoppelt sind;
wobei der zweite Transistor einen ersten NMOS-Transistor umfasst, dessen Gatter an die Scan-Aktivierungseingabe, dessen Drain an ein oberes Versorgungspotenzial und dessen Source an die funktionelle Datenausgabe der Scan-Zelle gekoppelt sind;
wobei der dritte Transistor einen zweiten PMOS-Transistor umfasst, dessen Gatter an die Scan-Aktivierungseingabe, dessen Source an die Scan-Ausgabe der Scan-Zelle und dessen Drain an ein niedrigeres Versorgungspotenzial gekoppelt sind; und
wobei der vierte Transistor einen zweiten NMOS-Transistor umfasst, dessen Gate an die Scan-Aktivierungseingabe, dessen Source an die Scan-Ausgabe der Scan-Zelle und dessen Drain an die Ausgabe des Flipflops gekoppelt sind.

4. Das Anspruch 3 entsprechende Gerät, wobei die ersten und zweiten PMOS-Transistoren in Reaktion auf ein der Scan-Aktivierungseingabe der Scan-Zelle angelegtes Scan-Aktivierungssignal, während sich diese Zelle auf einem hohen Logikpegel befindet, abgeschaltet und die ersten und zweiten NMOS-Transistoren eingeschaltet werden, sodass die funktionelle Datenausgabe der Scan-Zelle durch Trennung von der Flipflop-Ausgabe über den ersten PMOS-Transistor deaktiviert und die Scan-Ausgabe der Scan-Zelle durch Anschluss an die Flipflop-Ausgabe über den zweiten NMOS-Transistor aktiviert werden.

5. Das Anspruch 3 entsprechende Gerät, wobei die ersten und zweiten PMOS-Transistoren in Reaktion auf ein der Scan-Aktivierungseingabe der Scan-Zelle angelegtes Scan-Aktivierungssignal, während sich diese Zelle auf einem niedrigen Logikpegel befindet, eingeschaltet und die ersten sowie zweiten NMOS-Transistoren abgeschaltet werden, sodass

die funktionelle Datenausgabe der Scan-Zelle durch Anschluss an die Flipflop-Ausgabe über den ersten PMOS-Transistor aktiviert und die Scan-Ausgabe der Scan-Zelle durch Trennung von der Flipflop-Ausgabe über den zweiten NMOS-Transistor deaktiviert werden.

6. Eine integrierte Schaltung (104), die Folgendes umfasst:

Scan-Test-Schaltung (106), die das Anspruch 1 entsprechende Gerät umfasst; sowie
zusätzliche Schaltung (108), vorbehaltlich dessen, dass sie anhand der Scan-Test-Schaltung getestet werden sollte.

7. Ein Diskettenlaufwerk-Controller, der die Anspruch 6 entsprechende integrierte Schaltung umfasst.

8. Ein Verfahren zum Scan-Testen einer integrierten Schaltung, das Folgendes umfasst:

Anordnen einer Scan-Test-Schaltung (106), die mindestens eine Scan-Kette (204) mit einer Vielzahl von Scan-Zellen (206) umfasst, wobei die Scan-Kette konfiguriert ist, um als ein serielles Schieberegister in einer Scan-Shift-Betriebsweise zu funktionieren und von zumindest einem Teil der zusätzlichen Schaltungen der integrierten Schaltung in einer funktionellen Betriebsweise funktionelle Daten zu erfassen;
Deaktivieren einer funktionellen Datenausgabe von zumindest einer bestimmten der Scan-Zellen in der Scan-Shift-Betriebsweise; und
Deaktivieren einer Scan-Ausgabe der bestimmten Scan-Zelle in der funktionellen Betriebsweise;
wobei eine bestimmte dieser Scan-Zellen Folgendes umfasst:

eine funktionelle Dateneingabe;
eine Scan-Eingabe;
eine Scan-Aktivierungseingabe;
einen Multiplexer (300) mit einer ersten, an die funktionelle Dateneingabe gekoppelten Eingabe, einer zweiten, an die Scan-Eingabe gekoppelten Eingabe und einer an die Scan-Aktivierungseingabe gekoppelten Auswähllinie; und
ein Flipflop (302) mit einer an eine Ausgabe des Multiplexers gekoppelten Eingabe;
wobei der Ausgabesteuerschaltkreis zwischen einer Ausgabe des Flipflops und den funktionellen Daten- und Scan-Ausgaben der bestimmten Scan-Zelle gekoppelt ist; und
DADURCH GEKENNZEICHNET, DASS die Deaktivierungsschritte von einem Ausgabesteuerschaltkreis durchgeführt werden, der eines bzw. einen der Folgenden umfasst:

1.) einen ersten Tristate-Puffer (304-1), der zwischen der Ausgabe des Flipflops und der funktionellen Datenausgabe der bestimmten Scan-Zelle gekoppelt ist; sowie
einen zweiten Tristate-Puffer (304-2), der zwischen der Ausgabe des Flipflops und der Scan-Ausgabe der bestimmten Scan-Zelle gekoppelt ist;
wobei einer Steuereingabe eines der ersten und zweiten Tristate-Puffer ein Scan-Aktivierungssignal und der Steuereingabe des anderen der ersten und zweiten Tristate-Puffer eine ergänzte Version des Scan-Aktivierungssignals angelegt werden;
2.) ein erstes Paar von Geräten, das einen ersten und einen zweiten Transistor umfasst; und
ein zweites Paar von Geräten, das einen dritten und einen vierten Transistor umfaßt;
wobei das erste Paar von Geräten konfiguriert ist, um die funktionelle Datenausgabe der bestimmten Scan-Zelle in Reaktion auf ein Scan-Aktivierungssignal zu deaktivieren, das sich auf einem ersten binären Logikpegel befindet, sowie um die funktionelle Datenausgabe der bestimmten Scan-Zelle in Reaktion auf ein Scan-Aktivierungssignal zu aktivieren, das sich auf einem zweiten binären Logikpegel befindet;
wobei das zweite Paar von Geräten konfiguriert ist, um die Scan-Ausgabe der bestimmten Scan-Zelle in Reaktion auf das Scan-Aktivierungssignal zu deaktivieren, das sich auf einem zweiten binären Logikpegel befindet, und um die Scan-Ausgabe der bestimmten Scan-Zelle in Reaktion auf das Scan-Aktivierungssignal zu aktivieren, das sich auf einem ersten binären Logikpegel befindet; und
wobei der erste Transistor und der dritte Transistor jeweils NMOS- und PMOS-Transistoren und die zweiten und vierten Transistoren jeweils die anderen NMOS- und PMOS-Transistoren sind; und
3.) ein Logikgatter (500), wobei eine erste Eingabe an die Ausgabe des Flipflops, eine zweite Eingabe an die Scan-Aktivierungseingabe der bestimmten

Scan-Zelle, eine erste Ausgabe an die funktionelle Datenausgabe der bestimmten Scan-Zelle und eine zweite Ausgabe an die Scan-Ausgabe der bestimmten Scan-Zelle gekoppelt sind.

9. Das Anspruch 8 entsprechende Verfahren, wobei die Deaktivierungsschritte ferner Folgendes umfassen:

Deaktivieren der funktionellen Datenausgabe der Scan-Zelle und Aktivieren der Scan-Ausgabe der Scan-Zelle in Reaktion auf ein Scan-Aktivierungssignal, das sich auf einem ersten binären Logikpegel befindet; und
Deaktivieren der Scan-Ausgabe der Scan-Zelle und Aktivieren der funktionellen Datenausgabe der Scan-Zelle in Reaktion auf das Scan-Aktivierungssignal, das sich auf einem zweiten binären Logikpegel befindet.

10. Ein Computerprogramm-Produkt, das ein nichttransitorisches, computerlesbares Speichermedium mit eingebettetem Computerprogramm-Code umfasst, um beim Scan-Testen einer integrierten Schaltung benutzt zu werden, wobei der Computerprogramm-Code, wenn die Durchführung in einem Testsystem (100) stattfindet, dieses Testsystem veranlasst, die Anspruch 8 entsprechenden Verfahrensschritte durchzuführen.

11. Ein Verarbeitungssystem (700), das Folgendes umfasst:

einen Prozessor (702); und
einen Speicher (704), der an den Prozessor gekoppelt und konfiguriert ist, um Daten des Anspruch 1 entsprechenden Geräts zu speichern,

Revendications

1. Un appareil destiné à être utilisé pour tester par balayage un circuit intégré (104), l'appareil comprenant :

une cellule de balayage (206) configurée pour être agencée avec une pluralité d'autres cellules de balayage dans une chaîne de balayage (204) ayant un mode d'opération de décalage par balayage et un mode d'opération fonctionnel ;
dans lequel la cellule de balayage comprend des circuits de commande de sortie (304-1, 304-2, 305 ; 400, 402 ; 500) qui sont configurés pour désactiver une sortie de données fonctionnelles de la cellule de balayage dans le mode d'opération de décalage par balayage et pour désactiver une sortie de balayage de la cellule de balayage dans le mode d'opération fonctionnel ;
dans lequel la cellule de balayage comprend en outre :

une entrée de données fonctionnelles ;
une entrée de balayage ;
une entrée d'activation de balayage ;
un multiplexeur (300) ayant une première entrée couplée à l'entrée de données fonctionnelles, une seconde entrée couplée à l'entrée de balayage, et une ligne de sélection couplée à l'entrée d'activation de balayage ; et
une bascule bistable (302) ayant une entrée couplée à une sortie du multiplexeur ;

les circuits de commande de sortie étant couplés entre une sortie de la bascule bistable et les sorties de données fonctionnelles et de balayage de la cellule de balayage ; et
CARACTÉRISÉ EN CE QUE les circuits de commande de sortie comprennent un des suivants :

i) un premier tampon à trois états (304-1) couplé entre la sortie de la bascule bistable et la sortie de données fonctionnelles de la cellule de balayage ; et
un second tampon à trois états (304-2) couplé entre la sortie de la bascule bistable et la sortie de balayage de la cellule de balayage ;
dans lequel un signal d'activation de balayage est appliqué à une entrée de commande d'un des premiers et seconds tampons à trois états et une version complétée du signal d'activation de balayage est appliquée à l'entrée de commande de l'autre des premiers et seconds tampons à trois états ;
ii) une première paire de dispositifs comprenant un premier transistor et un second transistor ; et
une seconde paire de dispositifs comprenant un troisième transistor et un quatrième transistor ;
dans lequel la première paire de dispositifs est configurée pour désactiver la sortie de données fonctionnelles de la cellule de balayage en réponse à un signal d'activation de balayage étant à un premier niveau de logique binaire et pour activer la sortie de données fonctionnelles de la cellule de balayage en réponse à un signal d'activation de balayage étant à un second niveau de logique binaire ;
dans lequel la seconde paire de dispositifs est configurée pour désactiver la sortie de

balayage de la cellule de balayage en réponse au signal d'activation de balayage étant à un second niveau de logique binaire et pour activer la sortie de balayage de la cellule de balayage en réponse au signal d'activation de balayage étant à un premier niveau de logique binaire ; et
dans lequel le premier transistor et le troisième transistor sont un des transistors NMOS et des transistors PMOS et le second et le quatrième transistor sont l'autre des transistors NMOS et des transistors PMOS ; et
iii) une porte logique (500) ayant une première entrée couplée à la sortie de la bascule bistable, une seconde entrée couplée à l'entrée d'activation de balayage de la cellule de balayage, une première sortie couplée à la sortie de données fonctionnelles de la cellule de balayage et une seconde sortie couplée à la sortie de balayage de la cellule de balayage.

2. L'appareil de la revendication 1 dans lequel les circuits de commande de sortie sont aptes à désactiver la sortie de données fonctionnelles de la cellule de balayage et à activer la sortie de balayage de la cellule de balayage en réponse à un signal d'activation de balayage étant à un premier niveau de logique binaire et à désactiver la sortie de balayage de la cellule de balayage et à activer la sortie de données fonctionnelles de la cellule de balayage en réponse au signal d'activation de balayage étant à un second niveau de logique binaire.

3. L'appareil de la revendication 1 dans lequel :

le premier transistor comprend un premier transistor PMOS ayant sa porte couplée à l'entrée d'activation de balayage, sa source couplée à la sortie de la bascule bistable, et son drain couplé à la sortie de données fonctionnelles de la cellule de balayage ;
le second transistor comprend un premier transistor NMOS ayant sa porte couplée à l'entrée d'activation de balayage, son drain couplé à un potentiel d'alimentation supérieur et sa source couplée à la sortie de données fonctionnelles de la cellule de balayage ;
le troisième transistor comprend un second transistor PMOS ayant sa porte couplée à l'entrée d'activation de balayage, sa source couplée à la sortie de balayage de la cellule de balayage, et son drain couplé à un potentiel d'alimentation inférieur ; et
le quatrième transistor comprend un second transistor NMOS ayant sa porte couplée à l'entrée d'activation de balayage, sa source couplée à la sortie de balayage de la cellule de balayage, et son drain couplé à la sortie de la bascule bistable.

4. L'appareil de la revendication 3 dans lequel en réponse à un signal d'activation de balayage appliqué à l'entrée d'activation de balayage de la cellule de balayage étant à un niveau élevé de logique, les premiers et seconds transistors PMOS sont mis hors circuit et les premiers et seconds transistors NMOS sont mis sous tension, de telle sorte que la sortie de données fonctionnelles de la cellule de balayage est désactivée en étant déconnectée de la sortie de bascule bistable via le premier transistor PMOS et la sortie de balayage de la cellule de balayage est activée en étant connectée à la sortie de bascule bistable via le second transistor NMOS.

5. L'appareil de la revendication 3 dans lequel en réponse à un signal d'activation de balayage appliqué à l'entrée d'activation de balayage de la cellule de balayage étant à un niveau faible de logique, les premiers et seconds transistors PMOS sont mis sous tension et les premiers et seconds transistors NMOS sont mis hors circuit, de telle sorte que la sortie de données fonctionnelles de la cellule de balayage est activée en étant connectée à la sortie de bascule bistable via le premier transistor PMOS et la sortie de balayage de la cellule de balayage est désactivée en étant déconnectée de la sortie de bascule bistable via le second transistor NMOS.

6. Un circuit intégré (104) comprenant :

des circuits de test de balayage (106) comprenant l'appareil de la revendication 1 ; et
des circuits additionnels (108) soumis à des tests en utilisant les circuits de test de balayage.

7. Un contrôleur de lecteur de disque comprenant le circuit intégré de la revendication 6.

8. Un procédé pour tester par balayage un circuit intégré, comprenant :

fournir des circuits de test par balayage (106) comprenant au moins une chaîne de balayage (204) ayant une pluralité de cellules de balayage (206), la chaîne de balayage étant configurée pour opérer comme un registre à décalage série dans un mode d'opération de décalage par balayage et pour capturer des données fonctionnelles à partir d'au moins une partie des circuits additionnels du circuit intégré dans un mode d'opération fonctionnel ;
désactiver une sortie de données fonctionnelles d'au moins une cellule donnée des cellules de balayage dans le mode d'opération de décalage

par balayage ; et
désactiver une sortie de balayage de la cellule de balayage donnée dans le mode d'opération fonctionnel ;
dans lequel une cellule donnée des cellules de balayage comprend :

une entrée de données fonctionnelles ;
une entrée de balayage ;
une entrée d'activation de balayage ;
un multiplexeur (300) ayant une première entrée couplée à l'entrée de données fonctionnelles, une seconde entrée couplée à l'entrée de balayage, et une ligne de sélection couplée à l'entrée d'activation de balayage ; et
une bascule bistable (302) ayant une entrée couplée à une sortie du multiplexeur ;
les circuits de commande de sortie étant couplés entre une sortie de la bascule bistable et les sorties de données fonctionnelles et de balayage de la cellule de balayage donnée ; et
CARACTÉRISÉ EN CE QUE les étapes de désactivation sont effectuées par des circuits de commande de sortie comprenant un des suivants :

i) un premier tampon à trois états (304-1) couplé entre la sortie de la bascule bistable et la sortie de données fonctionnelles de la cellule de balayage donnée ; et
un second tampon à trois états (304-2) couplé entre la sortie de la bascule bistable et la sortie de balayage de la cellule de balayage donnée ;
dans lequel un signal d'activation de balayage est appliqué à une entrée de commande d'un des premiers et seconds tampons à trois états et une version complétée du signal d'activation de balayage est appliquée à l'entrée de commande de l'autre des premiers et seconds tampons à trois états ;
ii) une première paire de dispositifs comprenant un premier transistor et un second transistor ; et
une seconde paire de dispositifs comprenant un troisième transistor et un quatrième transistor ;
dans lequel la première paire de dispositifs est configurée pour désactiver la sortie de données fonctionnelles de la cellule de balayage donnée en réponse à un signal d'activation de balayage étant à un premier niveau de logique binaire et pour activer la sortie de données fonctionnelles de la cellule de balayage donnée en réponse à un signal d'activation de balayage étant à un second niveau de logique binaire ;
dans lequel la seconde paire de dispositifs est configurée pour désactiver la sortie de balayage de la cellule de balayage donnée en réponse au signal d'activation de balayage étant à un second niveau de logique binaire et pour activer la sortie de balayage de la cellule de balayage donnée en réponse au signal d'activation de balayage étant à un premier niveau de logique binaire ; et
dans lequel le premier transistor et le troisième transistor sont un des transistors NMOS et des transistors PMOS et le second et le quatrième transistor sont l'autre des transistors NMOS et des transistors PMOS ; et
iii) une porte logique (500) ayant une première entrée couplée à la sortie de la bascule bistable, une seconde entrée couplée à l'entrée d'activation de balayage de la cellule de balayage donnée, une première sortie couplée à la sortie de données fonctionnelles de la cellule de balayage donnée et une seconde sortie couplée à la sortie de balayage de la cellule de balayage donnée.

9. Le procédé de la revendication 8 dans lequel les étapes de désactivation comprennent en outre :

désactiver la sortie de données fonctionnelles de la cellule de balayage et activer la sortie de balayage de la cellule de balayage en réponse à un signal d'activation de balayage étant à un premier niveau de logique binaire ; et
désactiver la sortie de balayage de la cellule de balayage et activer la sortie de données fonctionnelles de la cellule de balayage en réponse au signal d'activation de balayage étant à un second niveau de logique binaire.

10. Un produit de programme informatique comprenant un support de stockage lisible par ordinateur non-transitoire ayant un code de programme informatique intégré destiné à être utilisé pour tester par balayage un circuit intégré, dans lequel le code de programme informatique lors de son exécution dans un système de test (100) entraîne le système de test à effectuer les étapes du procédé de la revendication 8.

11. Un système de traitement (700) comprenant :

un processeur (702) ; et
une mémoire (704) couplée au processeur et configurée pour stocker des informations de l'appareil de la revendication 1.

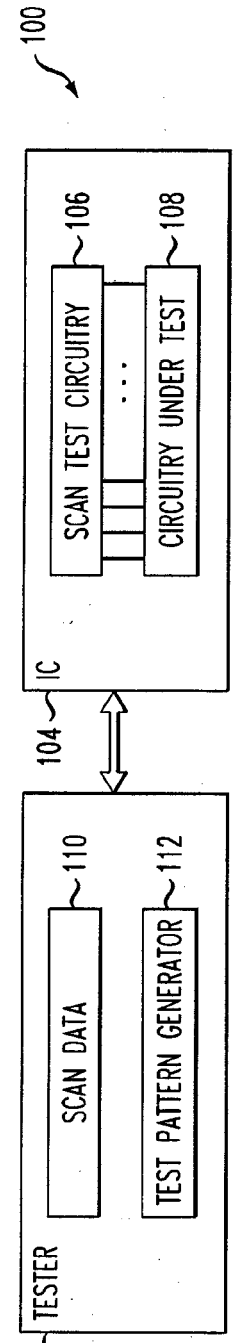

100
IC
SCAN TEST CIRCUITRY
106
CIRCUITRY UNDER TEST
108
104
TESTER
SCAN DATA
110
TEST PATTERN GENERATOR
112
102

FIG. 1

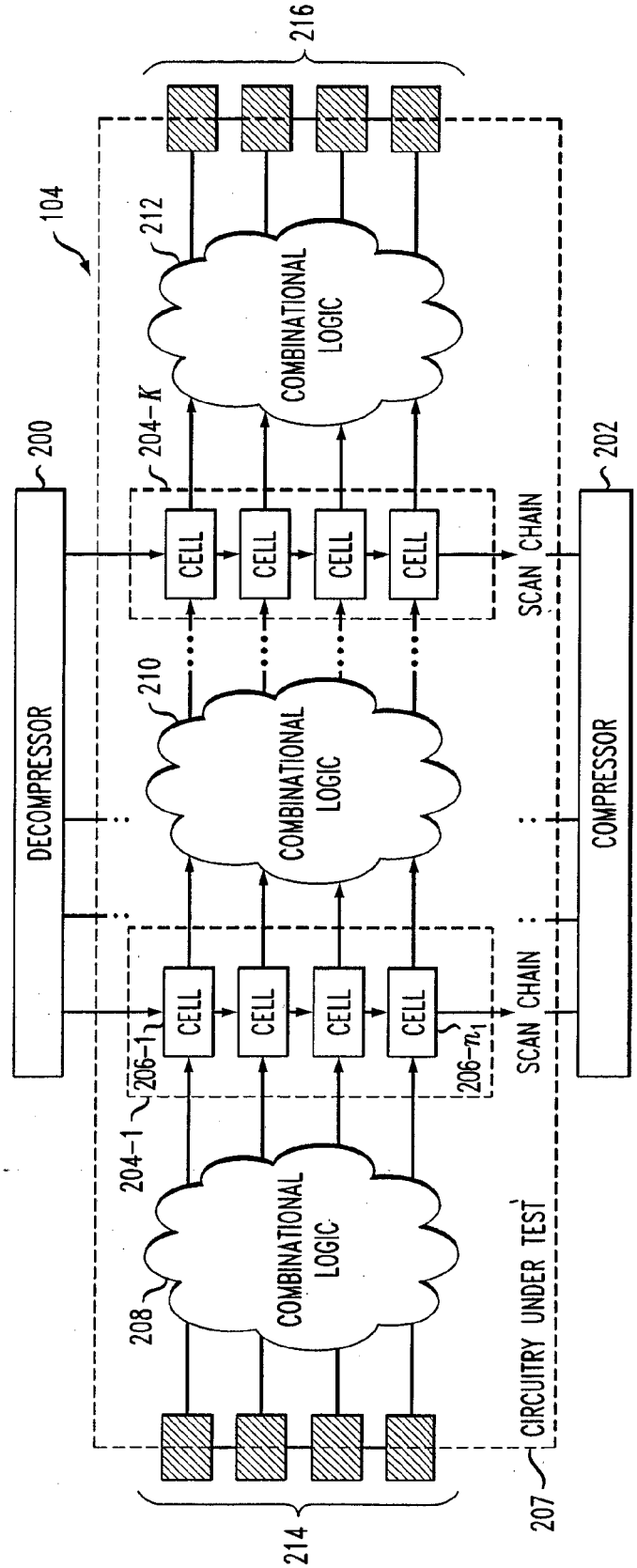

216
104
212
COMBINATIONAL LOGIC
204-K
200
CELL
SCAN CHAIN
202
210
DECOMPRESSOR
COMPRESSOR
206-1
206-n1
204-1
208
214
207
CIRCUITRY UNDER TEST

FIG. 2

FIG. 3

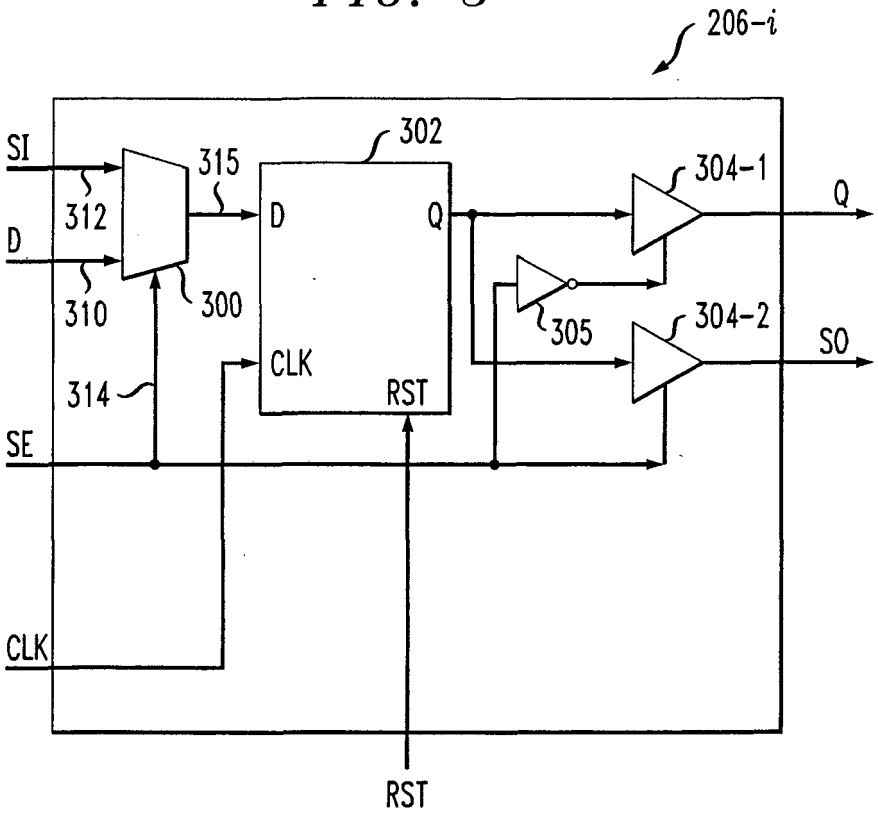

206-i
SI
D
312
310
315
300
302
D
Q
CLK
RST
304-1
Q
305
304-2
SO
314
SE
CLK
RST

FIG. 4

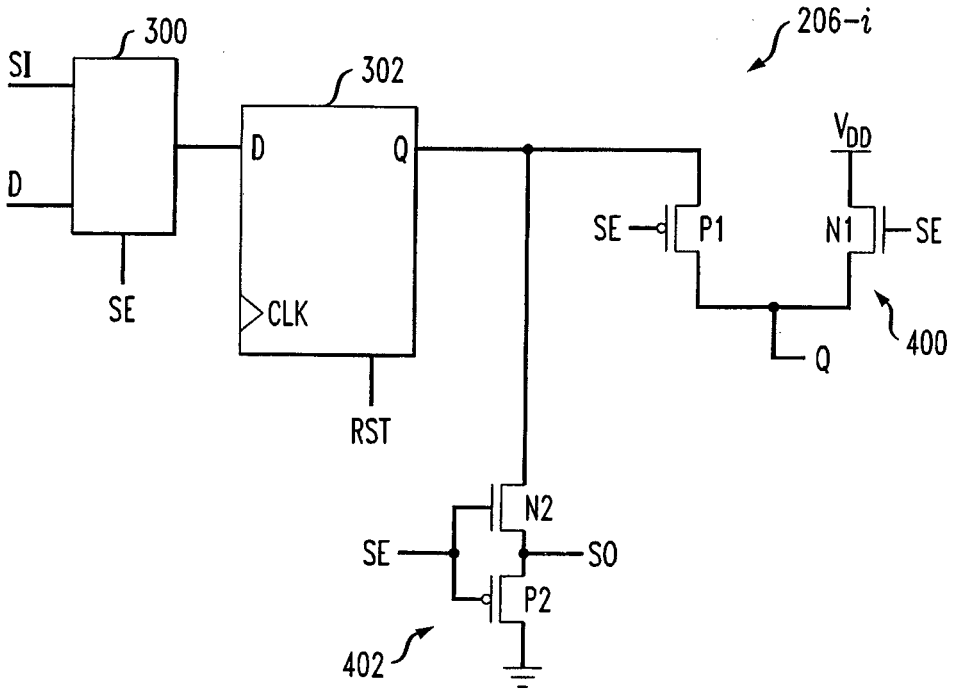

206-i
300
SI
D
SE
302
D
Q
CLK
RST
V_{DD}
SE
P1
N1
SE
Q
400
N2
SE
SO
P2
402

FIG. 5

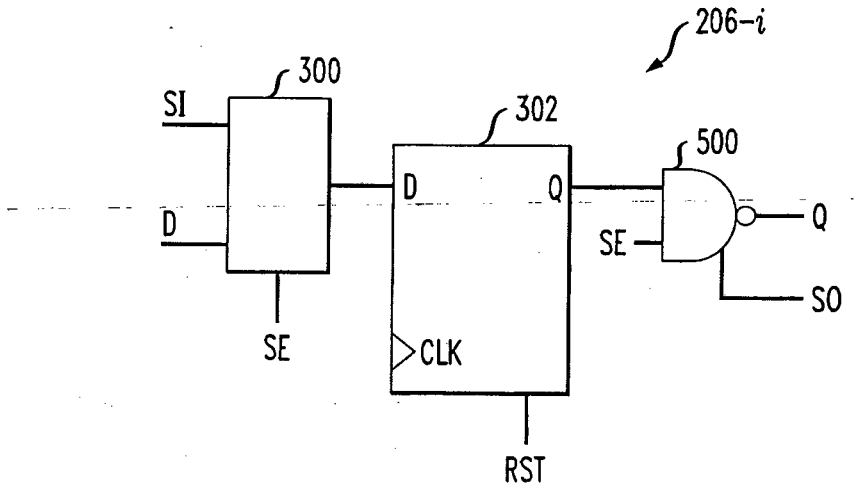

206-i
300
SI
D
SE
302
D
Q
CLK
RST
500
SE
Q
SO

FIG. 6

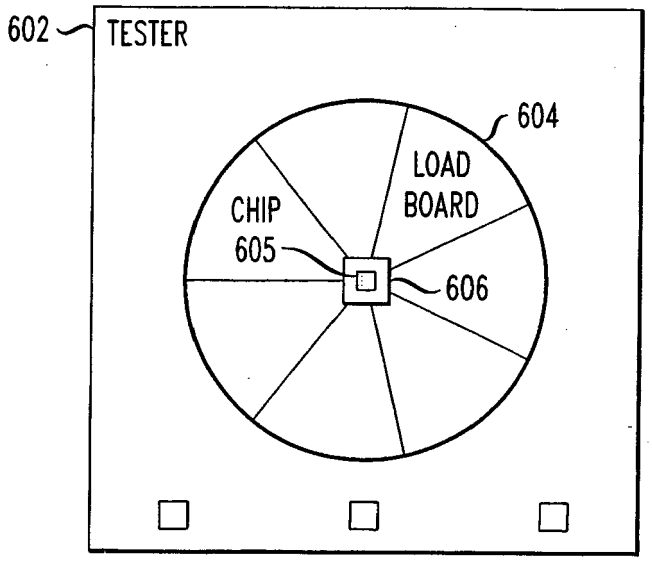
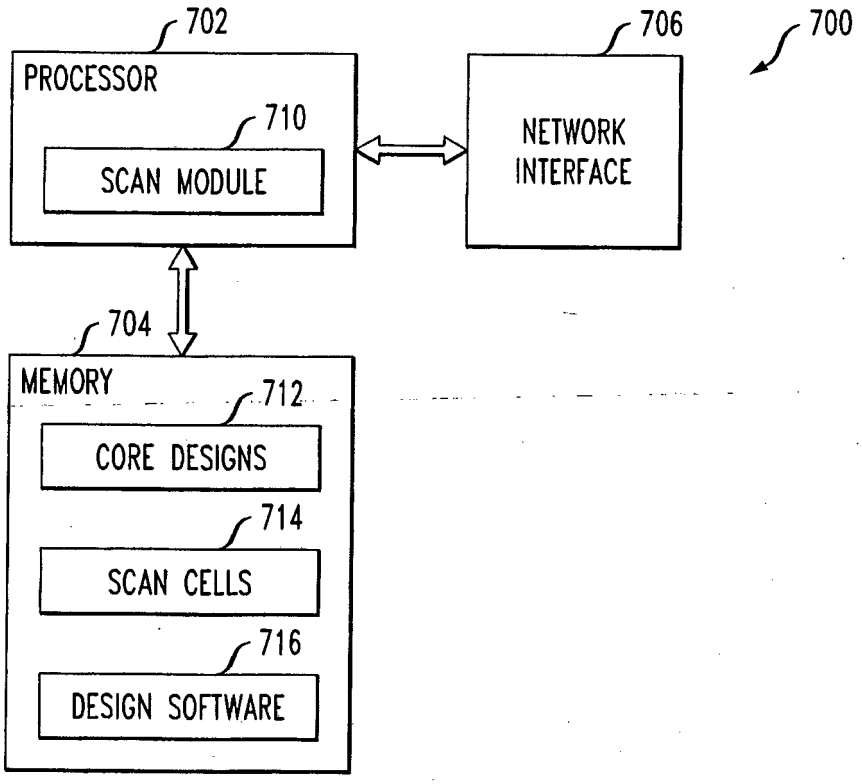

602
TESTER
604
LOAD BOARD
CHIP
605
606

FIG. 7


702
PROCESSOR
710
SCAN MODULE
706
NETWORK INTERFACE
700
704
MEMORY
712
CORE DESIGNS
714
SCAN CELLS
716
DESIGN SOFTWARE

REFERENCES CITED IN THE DESCRIPTION

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