



(11)

EP 2 549 643 B9

(12) **CORRECTED EUROPEAN PATENT SPECIFICATION**

(15) Correction information:
Corrected version no 1 (W1 B1)
Corrections, see
Claims EN 14

(51) Int Cl.:
H03F 1/38 ^(2006.01) **H03F 1/56** ^(2006.01)

(48) Corrigendum issued on:
24.06.2015 Bulletin 2015/26

(45) Date of publication and mention
of the grant of the patent:
05.11.2014 Bulletin 2014/45

(21) Application number: **12176359.3**

(22) Date of filing: **13.07.2012**

(54) **System and method for capacitive signal source amplifier**

System und Verfahren für einen kapazitiven Signalquellenverstärker

Système et procédé pour amplificateur de source de signal capacitif

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR

(30) Priority: **14.07.2011 US 201113183193**

(43) Date of publication of application:
23.01.2013 Bulletin 2013/04

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Description

TECHNICAL FIELD

[0001] This invention relates generally to semiconductor circuits and methods, and more particularly to an amplifier for a capacitive signal source.

BACKGROUND

[0002] Audio microphones are commonly used in a variety of consumer applications such as cellular telephones, digital audio recorders, personal computers and teleconferencing systems. In particular, lower-cost electret condenser microphones (ECM) are used in mass produced cost sensitive applications. An ECM microphone typically includes a film of electret material that is mounted in a small package having a sound port and electrical output terminals. The electret material is adhered to a diaphragm or makes up the diaphragm itself. Most ECM microphones also include a preamplifier that can be interfaced to an audio front-end amplifier within a target application such as a cell phone. The output of the front-end amplifier can be coupled to further analog circuitry or to an A/D converter for digital processing. Because an ECM microphone is made out of discrete parts, the manufacturing process involves multiple steps within a complex manufacturing process. Consequently, a high yielding, low-cost ECM microphone that produces a high level of sound quality is difficult to achieve.

[0003] In a microelectro-mechanical Systems (MEMS) microphone, a pressure sensitive diaphragm is etched directly onto an integrated circuit. As such, the microphone is contained on a single integrated circuit rather than being fabricated from individual discrete parts. The monolithic nature of the MEMS microphone produces a higher yielding, lower cost microphone.

[0004] The interfacing of a MEMS microphone or sensor with an electrical system, however, poses a number of difficulties because of the microphone's very high output impedance. For example, loading by the preamplifier can potentially attenuate the microphone's output signal, and the high resistance nature of the MEMS microphone makes it prone to EMI disturbance and power supply disturbances due to a poor power supply rejection ratio (PSRR).

[0005] Examples for realizations of low noise transducer circuits are given in WO 2005/122392 A1 (TOUMAZ TECHNOLOGY LTD [GB]; NIMMO ROSS [GB]) 22 December 2005 (2005-12-22) and YU-CHUN HSU ET AL: "A Realization of Low Noise Silicon Acoustic Transducer Interface Circuit", VLSI DESIGN, AUTOMATION AND TEST, 2007. VLSI-DAT 2007. INTERNATIONAL SYMPOSIUM ON, IEEE, PI, 1 April 2007 (2007-04-01), pages 1-4, ISBN: 978-1-4244-0582-4.

SUMMARY OF THE INVENTION

[0006] According to an embodiment, a system for amplifying a signal provided by a capacitive signal source includes a first stage and a second stage. The first stage has a voltage follower device including an input terminal configured to be coupled to a first terminal of the capacitive signal source, and a first capacitor having a first end coupled to an output terminal of the voltage follower device, and a second end configured to be coupled to a second terminal of the capacitive signal source. The second stage includes a differential amplifier capacitively coupled to the output terminal of the voltage follower device.

[0007] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

Figures 1 illustrates an amplifier according to the prior art;

Figures 2a-2b illustrate an amplifier according to an embodiment of the present invention;

Figure 3 illustrates an amplifier according to an alternative embodiment of the present invention;

Figure 4 illustrates an amplifier according to a further alternative embodiment of the present invention;

Figure 5 illustrates an embodiment first stage amplifier;

Figure 6 illustrates an embodiment second stage amplifier;

Figures 7a-d illustrate schematics and a timing diagram of an embodiment MEMS microphone bias circuit;

Figure 8 illustrates a system according to an embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0009] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention pro-

vides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0010] The present invention will be described with respect to embodiments in a specific context, namely an amplifier for a capacitive signal source such as a MEMS or an electret condenser microphone (ECM). The invention may also be applied, however, to other types of circuits and systems, such as audio systems, communication systems, sensor systems and other systems that interface to high impedance signal sources.

[0011] In an embodiment, an amplifier for a MEMS microphone has a first stage that includes a capacitively coupled gain boosted source follower stage. This first stage provides a high-impedance interface to the MEMS device and a lowered output impedance at an output of the source follower stage. In addition, the amplifier has a second stage including a capacitively coupled differential amplifier that is coupled to the output of the gain boosted source follower stage. By using a very high resistance biasing network, an amplifier having a bandwidth that spans from a few mHz to tens of KHz and above can be achieved, thereby making embodiments suitable for low frequency sensor and audio applications. It should be appreciated that while some of the described embodiments are directed toward MEMS microphone systems, embodiments of the present invention can also be directed toward MEMS sensors, capacitive sensors, and other capacitive and high impedance signal sources.

[0012] Figure 1a illustrates capacitive sensor amplifier 100 according to the prior art that interfaces with capacitive source 104. Capacitive source 104, which can be a MEMS microphone, an ECM microphone, or other type of capacitive signal source, is represented by voltage source V_{mic} coupled in series with capacitor C_{mic} , which typically has a capacitance between about 1pF and about 10pF. The in-band gain of amplifier 100 is about $A_m = C_1/C_2$. The transfer characteristic of amplifier 100 has a lower corner frequency at about $1/(2\pi C_2 R_2)$ and an upper corner frequency at about $G_m/(2\pi C_1 A_m)$. The value of C_1 is generally much smaller than sensor capacitance C_{mic} to minimize signal attenuation.

[0013] The noise of amplifier 100 is dominated by the noise of resistors R_1 and R_2 at low frequencies, and by the noise of transconductance amplifier 102 at higher frequencies. At higher frequencies the output noise of the amplifier 100 is about $V_{nia} \cdot (C_1 + C_2 + C_{mic})/C_2$, where V_{nia} is the input referred noise of transconductance amplifier 102. It can be seen that large values of C_2 yield a better noise performance. However, the value of C_2 is practically limited because C_1 needs to be large enough in relation to C_2 to achieve a high voltage gain, but cannot be too large in order to avoid attenuating the input signal 101 due to capacitance division between C_{mic} and C_1 .

[0014] Figure 2a illustrates amplification system 200 according to an embodiment of the present invention. MEMS device 202 is coupled to first stage amplifier 204, which is further coupled to second stage 206. First stage amplifier 204 has gain boosted source follower circuit based on transistor M1 and capacitors C_{11} and C_{22} , and second stage amplifier 206 has a fully differential amplifier 224 in a capacitive feedback configuration. MEMS device 202 is modeled by voltage source V_{mic} , microphone capacitance C_{mic} , and parasitic capacitance C_p . In an embodiment, MEMS device 202 is biased by voltage source V_B in series with resistance R_B , which has a resistance in the $G\Omega$ region. Resistance R_B and capacitor C_2 form a lowpass filter that filters noise coming from voltage source V_B . Alternatively, lower resistance values can be used for R_B depending on the particular system and its specifications.

[0015] In an embodiment, bias devices V_B , R_B , first stage 204 and second stage 206 are disposed on a same integrated circuit (IC) 220, and MEMS microphone 202 is interfaced to IC 220 via connection pads 210 and 212. Alternatively, MEMS microphone 202 may also be disposed on the same IC 220 as first stage 204 and second stage 206, in which case the terminals of MEMS microphone 202 may be coupled to first stage 204 and bias resistor R_B internally.

[0016] In an embodiment, one terminal of MEMS microphone 202 is coupled to the gate of transistor M1, and the other terminal is coupled to capacitors C_1 and C_2 and resistance R_B . The combination of transistor M1 and capacitors C_{11} and C_{22} form a gain boosted source follower circuit. In embodiments, M1 is configured as a source follower or voltage follower device in which a signal at the gate of transistor M1 is buffered at the source of transistor M1. Because there is minimal phase shift between the gate of transistor M1 and the source of transistor M1, transistor M1 has a boosting effect on voltage V_{mic} . In an embodiment, the gain of the first stage 204 with respect to V_{mic} is about $G_1 = 1 + C_{11}/C_{22}$ neglecting the effect of C_{mic} , parasitic capacitance C_p , the transconductance of M1, and other parasitic components. In an embodiment, G_1 is set to be between about 0dB and about 20dB. Alternatively, other values for G_1 can be used depending on the particular system and its specifications.

[0017] In an embodiment, M1 is biased in the sub-threshold region via current source I_B in order to reduce thermal and flicker noise. Furthermore, device M1 is sized with a large area in order to further reduce flicker noise.

[0018] In an embodiment, second stage 206 contains differential amplifier 224 with capacitors C_{3P} , C_{3N} , C_{4P} and C_{4N} forming a capacitive feedback network. The voltage gain of second stage 206 is about C_3/C_4 . In an embodiment, the gain of second stage 206 is set to be between about 0 dB and about 20 dB; however, gains outside of this range can also be used. High resistance feedback resistors R_{FB} are used to bias the input of am-

plifier 224. In some embodiments, resistors RFB are in the $G\Omega$ range. Alternatively, lower resistance values can be used depending on the particular application and its specifications. In one embodiment, resistors RFB are implemented using diode connected MOS coupled in series, as shown in Figure 2b. By using diode connected transistors, if the input bias voltages of amplifier 224 in Figure 2a begin to drift, the diode connected transistors will conduct, thereby allowing a temporary DC feedback path to keep the input of amplifier 224 at a proper bias.

[0019] In an embodiment, amplifier 224 is implemented as a fully differential operational transconductance amplifier (OTA) with common mode feedback, however, other amplifier architectures, including, but not limited to a symmetrical amplifier, a folded cascode amplifier, an instrumentation amplifier, and a Miller amplifier can be used in alternative embodiments.

[0020] In an embodiment, the influence of the capacitor size C_{mic} in relation to capacitors present within the amplifier circuit is strongly reduced because of the lower capacitive load realized by driving the opposite end of C11 at the output of first stage 204 in phase with the input signal across terminals 210 and 212. A second low frequency corner of the frequency characteristic is introduced, which is defined by the input capacitance C_{in} of source follower transistor M1 and an additional input resistance R_i that models the biasing network at the gate of M1. In an embodiment, R_i is between about 10 $G\Omega$ and about 1 $T\Omega$. Alternatively, R_i can also be outside of this range. In some embodiments, the implementation depicted in Figure 2a can achieve good noise performance with small sensor capacitor values.

[0021] In one embodiment, the value of C_{mic} is about 5.5pF, the gain of first stage amplifier 204 is about 1, the gain of second stage amplifier 206 is about 5, the 3dB lower corner frequency is about 20 Hz, and the 3dB upper corner frequency is about 20 kHz. Here, output load capacitors CL limit the bandwidth of the amplifier 224 and may act as an anti-aliasing filter for systems having an A/D converter interfaced to the output of second stage 206. In alternative embodiments, the upper corner frequency can be much higher, for example 200 kHz, for higher bandwidth systems, or for systems not requiring filtering.

[0022] In an embodiment, the thermal noise of second stage 206 can be reduced by increasing C22 and C11. Because second stage 206 is buffered by first stage 204, an increase in capacitors C11 and C22 does not directly load the outputs of MEMS microphone 202. In some embodiments, the circuit can be configured such that first stage 204 realizes a maximum gain, for example, 6 dB, and second stage 206 is used for signal mode conversion, for example converting a single ended signal to a differential signal. Second stage 206 may also be used for the adaption of sensitivity, since first stage 204 may not be able to provide 30 dB alone.

[0023] Turning to Figure 3, amplification system 300 is illustrated according to a further embodiment of the

present invention. MEMS microphone 202 is coupled to first stage 304, which is similar to first stage 204 in Figure 2a. Here, boosted source follower transistor M1 is biased by PMOS transistor 320, which mirrors current from current source 322 through transistor 310. A lowpass filter is formed by resistor 312 and capacitor 314 to filter the bias voltage at the gate of transistor 320. In an embodiment, the corner frequency formed by this lowpass filter may range from about 1 mHz to about 1 Hz; however, in alternative embodiments other corner frequencies can be used.

[0024] In second stage 306, the negative input of amplifier 224 is biased by diode connected PMOS devices 330, 331, 332 and 333, and the positive input of amplifier 224 is biased by diode connected PMOS devices 334, 335, 336 and 337. In alternative embodiments, greater or fewer diode connected devices may be coupled in series depending on the nominal expected signal swing of node voltages within second stage 306. Furthermore, other device types besides PMOS devices, for example, triple well NMOS devices, in which the bulk nodes are not coupled to the substrate by default can be used for the feedback bias resistances.

[0025] In an embodiment, MEMS device 202 is biased by voltage source VB followed by low pass filter 302, which nominally has a corner frequency of between 1 mHz and about 1 Hz. Bias voltage VB may be between about 3V and about 60V, although voltages outside of this range are also possible depending on the particular MEMS microphone and/or capacitive sensor used.

[0026] Figure 4 illustrates embodiment amplification system 400 that is suitable for amplifying the output of an ECM microphone that has one terminal coupled to first stage 402. Furthermore, in embodiments using ECM microphones, a microphone bias voltage is not necessary. It should be appreciated that ECM microphones may also be used in other embodiments, such as the embodiment illustrated in Figure 3 Microphone 406, which is represented by V_{mic} and internal capacitance C_{mic} , is coupled to first stage 402. First stage 402 has a source follower PMOS device M1 biased by current source 410. PMOS device M1 is preferably biased in the subthreshold region for better noise performance. In alternative embodiments, a source follower transistor of another transistor type, for example, a NMOS type can be used. Furthermore, in other embodiments, source follower device M1 may be biased in the saturation region.

[0027] In an embodiment, second stage 404 is implemented using a transconductance amplifier having an input differential pair made of PMOS transistors 420 and 422, which are biased by current source 414. The drain currents of transistors 420 and 422 are mirrored to NMOS devices 430 and 428, respectively, via diode connected NMOS devices 424 and 426. Alternatively, the device types of second stage 404 may be inverted. For example, transistors 420 and 422 can be implemented by NMOS devices and/or transistors 430, 424, 426 and 428 can be implemented by PMOS devices or different combinations

of NMOS and PMOS devices thereof. Current sources 412 and 416, which supply current to 430 and 428, are controlled by common mode feedback (CMFB) that sets the common mode voltage of output nodes Voutp and Voutn to a predefined voltage and/or range of voltages. Input transistors 420 and 422 are biased via bias resistors R2, which define the input DC voltage levels for transistors 420 and 422. In some embodiments, bias resistors R2 are variable resistors that are implemented using diode connected transistors, such as those illustrated in Figure 2b. In an embodiment, the gain of second stage 404 is approximately $C1/C2$, and output corner frequency is set by the value of output load capacitance CL and the transconductance of amplifier 404.

[0028] In an embodiment, first stage 402 has a voltage gain about one, and the second stage is set to have a voltage gain of about 5, and ECM microphone 406 has a capacitance C_{mic} of about 5.5pF. In an embodiment, first stage 402 has a high-pass characteristic and second stage 404 has a bandpass characteristic. The composite 3dB bandwidth of first stage 402 cascaded with second stage 404 spans from about 20Hz to about 20 kHz. It should be appreciated that these values are just an example of one embodiment, and that the gains, bandwidths and capacitances of alternative embodiments may be different.

[0029] Figure 5 illustrates an embodiment of first stage amplifier 500 along with its associated bias circuitry. In embodiments, first stage amplifier 500 may be used as a first stage for the embodiments illustrated in Figures 2a, 3 and 4. PMOS source follower device M1 is biased to ground potential via NMOS transistors 534 and 536. In an embodiment, transistors 534 and 536 have a long transistor length to increase the output impedance. These two transistors realize the input biasing resistor for transistor M1. By coupling the gate of device 530 to its drain via resistor 532, the VGS for transistors 534 and 536 is reduced by resistor 532. Due to this construction, the VGS of 534 and 536 is in the mV region, the transistor is in very weak inversion and the output impedance of 536 and 534 is in the $T\Omega$ to $100\text{ G}\Omega$ region. It should be appreciated, however the transistors 536 and 534 are not completely shut off. In one embodiment, resistor 532 is between about $300\text{ K}\Omega$ and about $500\text{ K}\Omega$, and the current of current source is 510 is between about 400nA and about 5uA. In alternative embodiments, other component values, current levels and corner frequencies can be implemented. PMOS device 538 is provided for ESD protection and will conduct current, for example, if input voltage VIN increases above VDD. Alternatively, other ESD protection schemes known in the art may be used depending on the particular application and its specifications.

[0030] In an embodiment, the current of current source 512 is mirrored to PMOS device M2 via PMOS device 520. The voltage at the gate of device 520 is lowpass filtered by and RC lowpass filter network formed by the resistance of PMOS device 526 and the capacitance of

capacitor 528. In an embodiment, the corner frequency of this RC lowpass network is about 100 mHz. PMOS device 526 is biased in the linear region by PMOS device 522 and resistor 524. In an embodiment, optional switches 502 and 504 are closed during startup in order to allow node voltages to settle quickly to their quiescent values prior to operation of the amplifier. Bypassing these resistances avoids a long startup time due to the long time constants. These switches can be closed, for example during the first 100ms or 200ms of operation, however durations outside of this range is also possible. After the switches are opened, the biasing nodes have a high time constant. Switches 502 and 504 can be omitted in situations where startup time is not an issue and/or in circuits having smaller time constants.

[0031] Figure 6 illustrates a circuit level schematic of second stage amplifier 600 according to an embodiment of the present invention. In embodiments, second stage amplifier 600 may be used as a second stage for the embodiments illustrated in Figures 2a, 3 and 4. A fully differential cascoded amplifier has PMOS differential pair made of devices 626 and 628 biased by current source 682. Current from these devices are mirrored to NMOS devices 640 and 638 via diode connected NMOS devices 630 and 632, respectively. High impedance is achieved at output nodes VOUTP and VOUTN by optional cascode transistors 642 and 644 with NMOS devices 642 and 644, respectively. The gate bias voltage of transistors 642 and 644 is represented by voltage VCAS, which can be generated using cascode bias techniques known in the art. In an embodiment, current sources 672 and 670 can also be implemented using cascoded current sources, however, other current source structures known in the art can also be used depending on the particular application and the available headroom.

[0032] In an embodiment, the common mode output level of nodes VOUTP and VOUTN are set to voltage VCM using common mode feedback circuit 690. Voltage VCM can be generated, for example, by using voltage generation techniques known in the art, for example, using a bandgap voltage reference or a resistive voltage divider between the power supply and ground. Common mode feedback circuit 690 has NMOS device 652 and 654 coupled to VCM and NMOS devices 650 and 656 coupled to VOUTN and VOUTP, respectively. Current supplied by current sources 662, 664, 666 and 668 are steered among diode connected NMOS devices 646 and 648 via resistors 658 and 660 and via NMOS devices 650, 652, 654 and 656. Current through NMOS device 646 is conducted from the drains of PMOS devices 626 and 628 via NMOS devices 634 and 636, respectively, thereby forming a closed common mode loop. It should be appreciated that other common mode biasing schemes known in the art can also be applied to embodiment second stages.

[0033] In an embodiment, feedback is provided between outputs VOUTP and VOUTN and the gates of PMOS devices 628 and 626. For example, feedback net-

work 692 has capacitor C4P and diode connected PMOS devices 606 and 608 oriented in a first direction and PMOS devices 610 and 612 oriented in a second direction. Capacitor C4P can be implemented using, for example, poly-poly capacitors, MIM capacitors, and gate capacitors depending on required circuit density and signal linearity.

[0034] In an embodiment, diode connected transistors 606, 608, 610 and 612, which provide a DC bias to the gates of PMOS devices 626 and 628, are oriented in two directions to prevent both positive and negative transients from disturbing the bias point of the amplifier for long periods of time. In some embodiments, greater or less than two diode connected transistors can be connected in series. Embodiments having more transistors coupled in series have a high linear region of amplifier operation and lower total harmonic distortion (THD) at the expense of slower and more difficult recovery from transient disturbances. In embodiments, the number of series biasing devices is selected according to the particular application and its specifications. Feedback network 694, which has capacitor C4N and PMOS device 618, 620, 622 and 624 operates according to the principles of feedback network 692 described above. In an embodiment, optional switches 676, 674, 678 and 680 coupled the inputs and outputs of feedback networks 692 and 694 are closed during startup in order to more quickly bias the amplifier.

[0035] In embodiments, the voltage gain of second stage 600 is approximately $C3P/(C4P)$. Furthermore, in some embodiments, capacitors C4P, and C4N are made to match each other, and capacitors C3P and C3N are made to match each other by using techniques known in the art in order to enhance the power supply rejection ratio (PSRR) and offset of the amplifier. These techniques can include, for example, using unit devices and common centroid layout techniques. PSRR and offset performance can be further enhanced using known layout and sizing techniques to match the remaining active and passive devices within circuit 600.

[0036] Figures 7a-7d illustrate an embodiment bias circuit that may be used to implement voltage source VB shown in Figures 2a and 3. Figure 7a illustrates a top level schematic of MEMS bias circuit 700, which is used to provide a boosted voltage between about 3V and about 60V. Alternatively, voltages outside of this range are also possible depending on the particular MEMS microphone and/or capacitive sensor used. In an embodiment, a Dickson charge pump structure is used to provide boosted output voltage VBIAS. The charge pump is formed by capacitors 740, 742, 744, 746 and 748 coupled to functional diode blocks 704, 706, 708, 710 and 712. In one embodiment, nine functional diode block are used. Alternatively, any number of functional diode blocks may be used depending on the boosted voltage required. In an embodiment, reference voltage VREF is buffered by amplifier 702 and fed into first functional diode 704. Clock generator 716 provides clock signals Q1, Q1N, Q2, Q2N,

Q3 and Q3B that drive capacitors 740, 742, 744, 746 and 748 and functional diode blocks 704, 706, 708, 710 and 712. The output of last functional diode block 712 is coupled to capacitor 750 and lowpass filter 750.

[0037] Figure 7b illustrates embodiment functional diode block 720, which has PMOS devices 722, 724 and 726 and input coupling capacitors 728 and 730. PMOS device 722 is a pass transistor that coupled input IN of functional diode 720 to output OUT of functional diode 720. Cross coupled transistors 724 and 726 and input coupling capacitors 728 730 provides a boosted clock that shuts off transistor 722 at time during which the functional diode is in a nonconducting state. By using circuit 720, inefficiencies due to the threshold voltage of transistor 722 may be avoided. In alternative embodiments, a pn junction diode, a diode connected transistor, or other suitable device may be used in place of functional diode 720.

[0038] Figure 7c illustrates a schematic of embodiment clock generator 716, which provides phased clocks for capacitors 740, 740, 742, 744, 746 and 748, and functional diodes 704, 706, 708, 710 and 712. Figure 7d illustrates a timing diagram of clock generator 716. In an embodiment, clock signals Q1 and Q1N that drive capacitors 740, 740, 742, 744, 746 and 748 have the widest pulse width, clock signals Q2 and Q2N that drive some of the functional diodes have a narrower pulse width, and clock signals Q3 and Q3 that drive the remaining functional diodes have the narrowest pulse width. In an embodiment, the rising edge of Q2 with respect to Q1, the falling edge of Q1 with respect to Q2, the rising edge of Q3 with respect to Q2 and the falling edge of Q2 with respect to Q3 is delayed by Tnovl. By using an embodiment clock phasing scheme, such as the one illustrated in Figure 7d, functional diodes 704, 706, 708, 710 and 712 are in a stable before the signals driving capacitors 740, 740, 742, 744, 746 and 748 are change state. In alternative embodiments, other clock phase relationships may be used.

[0039] Figure 8 illustrates system 900 using embodiments of the present invention. Capacitive sensor 902 is coupled to integrated circuit 904 having first stage 906 and second stage 908 according to embodiments of the present invention described herein. In an embodiment, the differential output of second stage 908 is coupled to A/D converter 910. In some embodiments, A/D converter is implemented as an audio sigma-delta converter. In other embodiments, A/D converter can be, for example, a low frequency A/D suitable for sensor applications. In embodiments, the output of A/D converter is coupled to processor 912 to perform a useful function. Examples of possible applications achievable by system 900 include, but are not limited to telephone systems, digital recorders, and remote sensing systems.

[0040] In some embodiments, for example, capacitive sensor 902 can be a MEMS microphone or other capacitive sensor such as capacitive pressure sensor, an ECM, or another type of floating capacitive signal source. In

alternative embodiments, capacitive sensor 902 can be included on integrated circuit 904. Furthermore, A/D converter 910 and/or processor 912 can be located separately from integrated circuit 904. In some embodiments, the functionality of integrated circuit 904 may be implemented using a single integrated circuit, or using a plurality of integrated circuits.

[0041] According to an embodiment, a system for amplifying a signal provided by a capacitive signal source includes a first stage and a second stage. The first stage has a voltage follower device including an input terminal configured to be coupled to a first terminal of the capacitive signal source, and a first capacitor having a first end coupled to an output terminal of the voltage follower device, and a second end configured to be coupled to a second terminal of the capacitive signal source. The second stage includes a differential amplifier capacitively coupled to the output terminal of the voltage follower device.

[0042] In some embodiments, the voltage follower device of the first stage includes a MOS source follower may be biased in the subthreshold region. The first stage may also include a second capacitor comprising a first end coupled to a reference node and a second end configured to be coupled to the second terminal of the capacitive signal source.

[0043] In an embodiment, the second stage also includes an input capacitor coupled between the output terminal of the voltage follower device and a first input terminal of the differential amplifier, and a reference capacitor coupled between a reference node and a second input terminal of the differential amplifier. The second stage may also include a first feedback capacitor coupled between a first output terminal of the differential amplifier and the first input terminal of the differential amplifier, and a second feedback capacitor coupled between a second output terminal of the differential amplifier and the second input terminal of the differential amplifier.

[0044] In some embodiments, the system may be configured to be coupled to an external capacitive signal source, however, in some embodiments, the capacitive signal source may also be included in the system. In some embodiments, the capacitive signal source resides on the same integrated circuit at the first and second stages. In some embodiments, this capacitive signal source may include a MEMS or ECM microphone, while in other embodiments the capacitive signal source may include a capacitive sensor or other high impedance signal source.

[0045] According to a further embodiment, an amplifier for amplifying a signal provided by a high impedance signal source includes a source follower transistor having a gate configured to be coupled to a first terminal of the high impedance signal source, and a first capacitor having a first terminal coupled to a source of the source follower transistor and a second terminal configured to be coupled to a second terminal of the high impedance signal source. The source follower transistor may be biased

in the subthreshold region in some embodiments. A second capacitor is further coupled between the source of the source follower transistor and a first input of a differential amplifier and a third capacitor coupled between a first output of the differential amplifier and the first input of the differential amplifier. The differential amplifier is configured to produce a negative phase at the first output with respect to the first input, and a low-frequency gain of the differential amplifier is set by a ratio of a capacitance of the second capacitor and a capacitance of the third capacitor. In some embodiments, the amplifier further includes a fourth capacitor coupled between the second terminal of the first capacitor and a voltage reference.

[0046] In some embodiments, the high impedance signal source is a capacitive signal source such as a MEMS or ECM microphone, and the amplifier may also include a biasing network for the high impedance signal source. For example, a MEMS bias circuit may be provided for an amplifier configured to amplify a MEMS microphone. In some embodiments, the MEMS bias circuit is coupled to the second terminal of the first capacitor.

[0047] In an embodiment, a voltage gain from the first and second terminals of the high impedance signal source to the source of the source follower transistor is dependent on a ratio of a capacitance of the first capacitor and a capacitance of the fourth capacitor. This voltage gain may be greater than one in some embodiments.

[0048] In an embodiment, the amplifier also includes a fifth capacitor coupled between a second input of the differential amplifier and a reference voltage and a sixth capacitor coupled between a second output of the differential amplifier and the second input of the differential amplifier. This differential amplifier may comprise a fully differential amplifier with common mode feedback. In some embodiments, the differential amplifier comprises an operational transconductance amplifier (OTA).

[0049] In an embodiment, a bias resistor coupled in parallel with the third capacitor. The bias resistor may have a value of at least 100M Ω , however, in alternative embodiments, a lower value may be used depending on the application and its specifications. In an embodiment, the bias resistor comprises is made of diode connected MOS devices connected in series.

[0050] According to a further embodiment, an integrated circuit for amplifying a signal provided by a floating capacitive source includes a first stage configured to transform a first higher impedance of the floating capacitive source to a second lower impedance at an output of the first stage. The first stage is further configured to increase an input impedance of the first stage by providing positive feedback from the output of the first stage to an input of the first stage via a first capacitor. The amplifier also includes a second stage for transforming the output of the first stage to a differential signal at an output of the second stage. In some embodiments, the integrated circuit also includes a bias network configured to provide a bias voltage to the floating capacitive source.

[0051] In an embodiment, the first stage includes a

boosted source follower circuit comprising a voltage gain greater than one and the second stage comprises a differential amplifier capacitively coupled to an output of the boosted source follower circuit. The first stage may further include a second capacitor coupled between the input of the first stage and a reference node, such that the voltage gain of the boosted source follower circuit is based on a ratio of a capacitance of the first capacitor and a capacitance of the second capacitor.

[0052] According to another embodiment, an integrated circuit for amplifying signal produced by a floating capacitive source includes a boosted source follower circuit configured to be coupled to the floating capacitive source. In some embodiments, the boosted source follower circuit has a voltage gain greater than one. The integrated circuit also includes a differential amplifier capacitively coupled to an output of the source follower circuit and a bias network configured to be coupled to at least one terminal of the floating capacitive source. The differential amplifier may be a fully differential amplifier with a gain set by a capacitive feedback network.

[0053] In an embodiment, the boosted source follower circuit includes a MOS transistor configured to be coupled to a first terminal of the floating capacitive source, a first capacitor having a first terminal coupled to a drain of the MOS transistor and a second terminal configured to be coupled to a second terminal of the floating capacitive source, and a second capacitor coupled between the second terminal of the first capacitor and a reference voltage. In some embodiments, the reference voltage is a ground voltage.

[0054] According to a further embodiment, a method of amplifying a signal provided by a capacitive signal source includes receiving a first signal from a first terminal of the capacitive signal source at a control terminal of a voltage follower and receiving a second signal from a second terminal of the capacitive signal source at a first capacitor coupled to an output node of a voltage follower device. A bias voltage may be provided to the capacitive signal source in some embodiments. The method further includes amplifying the first and second signals by applying a voltage gain based on a ratio of the first capacitor and a second capacitor coupled between the second terminal of the capacitive signal source and a reference node. A third signal is received from the output node of the voltage follower device by a capacitively coupled, fully differential amplifier, and the third signal is amplified to produce a differential output signal. In some embodiments, an analog to digital conversion on the differential output signal.

[0055] Advantages of embodiments include the ability of the amplifier to handle higher signal swings because of the differential structure of embodiment second stage amplifiers. This embodiment differential structure also suppresses even order harmonics. Furthermore, by using two stages in embodiment amplifiers, the sensitivity to amplifier gain variation is small. In some embodiments, this gain variation may be a maximum of about 0.3dB.

Moreover, the gain of the system can be set based on capacitor ratios, thereby reducing the overall gain variation of the systems. In addition, by decoupling the capacitance of the MEMS device with the input capacitor of the second stage, the output of the MEMS device is not attenuated due to a large input capacitor coupled to a virtual ground. The effect of loading the MEMS device with capacitance is further reduced because the MEMS capacitance is coupled in series with the gate of the follower transistors, which converts the high impedance node of the MEMS to a low impedance node for the second stage. In embodiments, the first stage operates like a voltage source with low impedance and the corresponding voltage swing of the sensor.

[0056] A further advantageous aspect of embodiments includes better noise performance. By providing a gain boost at the first stage, the noise contribution of the second stage is reduced.

[0057] A further advantage of embodiments includes the ability to suppress EMI disturbances and light related disturbances experienced by the MEMS sensor, as EMI or power supply disturbances seen by the integrated circuit are suppressed by the differential structure of the second stage differential amplifier. With respect to disturbances seen by the MEMS sensor itself, most EMI disturbances will affect the sensor as a common mode signal. These disturbances are suppressed because both terminals of the sensor are coupled to the first stage of the amplifier. Therefore, any in-phase signal seen at both terminals of the MEMS sensor is rejected or significantly attenuated.

[0058] In embodiments of the invention, the system is an integrated circuit and the capacitive source is a floating capacitive source.

[0059] Embodiments provide for a first implementation of a system for amplifying a signal provided by a capacitive signal source, the system comprising:

a first stage comprising:

a voltage follower device comprising an input terminal configured to be coupled to a first terminal of the capacitive signal source, and a first capacitor comprising a first end coupled to an output terminal of the voltage follower device, and a second end configured to be coupled to a second terminal of the capacitive signal source; and a second stage capacitively coupled to the output terminal of the voltage follower device, the second stage comprising a differential amplifier.

[0060] In a second implementation of the first implementation, the second stage further comprises:

an input capacitor coupled between the output terminal of the voltage follower device and a first input terminal of the differential amplifier;

a reference capacitor coupled between a reference node and a second input terminal of the differential amplifier;
 a first feedback capacitor coupled between a first output terminal of the differential amplifier and the first input terminal of the differential amplifier; and
 a second feedback capacitor coupled between a second output terminal of the differential amplifier and the second input terminal of the differential amplifier.

[0061] In a third implementation of the first implementation, the voltage follower device comprises a MOS source follower.

[0062] In a fourth implementation of the third implementation, the source follower device is biased in a sub-threshold region.

[0063] In a fifth implementation of the first implementation, the first stage further comprises a second capacitor comprising a first end coupled to a reference node and a second end configured to be coupled to the second terminal of the capacitive signal source.

[0064] A sixth implementation of the first implementation further comprises the capacitive signal source.

[0065] In a seventh implementation of the sixth implementation, the capacitive signal source comprises a MEMS microphone.

[0066] Embodiments provide for an eighth implementation of an amplifier for amplifying a signal provided by a high impedance signal source, the amplifier comprising:

a source follower transistor having a gate configured to be coupled to a first terminal of the high impedance signal source;
 a first capacitor having a first terminal coupled to a source of the source follower transistor and a second terminal configured to be coupled to a second terminal of the high impedance signal source;
 a second capacitor coupled between the source of the source follower transistor and a first input of a differential amplifier; and
 a third capacitor coupled between a first output of the differential amplifier and the first input of the differential amplifier, wherein
 the differential amplifier is configured to produce a negative phase at the first output with respect to the first input, and
 a low-frequency gain of the differential amplifier is set by a ratio of a capacitance of the second capacitor and a capacitance of the third capacitor.

[0067] A ninth implementation of the eighth implementation further comprises a fourth capacitor coupled between the second terminal of the first capacitor and a voltage reference, wherein a voltage gain from the first and second terminals of the high impedance signal source to the source of the source follower transistor is

dependent on a ratio of a capacitance of the first capacitor and a capacitance of the fourth capacitor.

[0068] In a tenth implementation of the ninth implementation, the voltage gain from the first and second terminals of the high impedance signal source to the source of the source follower transistor is greater than one.

[0069] An eleventh implementation of the eighth implementation further comprises:

a fifth capacitor coupled between a second input of the differential amplifier and a reference voltage; and
 a sixth capacitor coupled between a second output of the differential amplifier and the second input of the differential amplifier.

[0070] In a twelfth implementation of the eighth implementation, the differential amplifier comprises a fully differential amplifier with common mode feedback.

[0071] In a thirteenth implementation of the eighth implementation, the source follower transistor is biased in a sub-threshold region.

[0072] A fourteenth implementation of the eighth implementation further comprises a bias resistor coupled in parallel with the third capacitor, the bias resistor comprising a value of at least $100\text{M}\Omega$.

[0073] In a fifteenth implementation of the fourteenth, the bias resistor comprises a plurality of diode connected MOS devices connected in series.

[0074] In a sixteenth implementation of the eighth implementation, the high impedance signal source comprises a capacitive signal source.

[0075] In a seventeenth implementation of the sixteenth implementation, the capacitive signal source comprises a MEMS microphone.

[0076] An eighteenth implementation of the seventeenth implementation, further comprises a MEMS bias circuit coupled to the second terminal of the first capacitor.

[0077] In a nineteenth implementation of the eighth implementation, the differential amplifier comprises an operational transconductance amplifier (OTA).

[0078] Embodiments of the method further comprise performing an analog to digital conversion on the differential output signal. Embodiments of the method further comprise providing a bias voltage to the capacitive signal source.

[0079] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

Claims

1. A system for amplifying a signal provided by a capacitive source, the system circuit comprising:

a first stage (204) configured to transform a first impedance of the capacitive source (202) to a second impedance at an output of the first stage, the first impedance being greater than the second impedance, wherein the first stage is configured to increase an input impedance of the first stage by providing positive feedback from the output of the first stage to an input of the first stage via a first capacitor (C11); and

a second stage (206) for transforming the output of the first stage to a differential signal at an output of the second stage.
2. The system of claim 1, further comprising a bias network (R_B, V_B) configured to provide a bias voltage to the capacitive source.
3. The system of claim 1 or 2, wherein the first stage comprises a boosted source follower circuit comprising a voltage gain greater than one.
4. The system of claim 3, wherein:

the first stage further comprises a second capacitor (C22) coupled between the input of the first stage and a reference node; and

the voltage gain is based on a ratio of a capacitance of the first capacitor and a capacitance of the second capacitor.
5. The system of one of claims 1 to 4, wherein the signal source is a capacitive signal source, the first stage comprises a voltage follower device comprising an input terminal configured to be coupled to a first terminal of the capacitive signal source, the first capacitor comprises a first end coupled to an output terminal of the voltage follower device, and a second end configured to be coupled to a second terminal of the capacitive signal source, and the second stage (206) is capacitively coupled to the output terminal of the voltage follower device, the second stage comprising a differential amplifier (A2).
6. The system of claim 5, wherein the second stage further comprises:

an input capacitor (C3P) coupled between the output terminal of the voltage follower device and a first input terminal of the differential amplifier;

a reference capacitor (C3N) coupled between a reference node and a second input terminal of the differential amplifier;
7. The system of claim 5 or 6, wherein the voltage follower device comprises a MOS source follower (M1).
8. The system of claim 7, wherein the source follower device is biased in a sub-threshold region.
9. The system of one of claims 5 to 8, wherein the first stage further comprises a second capacitor comprising a first end coupled to a reference node and a second end configured to be coupled to the second terminal of the capacitive signal source.
10. The system of claim 1, wherein the capacitive signal source is a high impedance signal source, the first stage comprises a source follower transistor (M1) having a gate configured to be coupled to a first terminal of the high impedance signal source, the first capacitor has a first terminal coupled to a source of the source follower transistor and a second terminal configured to be coupled to a second terminal of the high impedance signal source, the second capacitor is coupled between the source of the source follower transistor and a first input of a differential amplifier of the second stage, a third capacitor is coupled between a first output of the differential amplifier and the first input of the differential amplifier, the differential amplifier is configured to produce a negative phase at the first output with respect to the first input, and a low-frequency gain of the differential amplifier is set by a ratio of a capacitance of the second capacitor and a capacitance of the third capacitor.
11. The system of claim 10, further comprising a fourth capacitor coupled between the second terminal of the first capacitor and a voltage reference, wherein a voltage gain from the first and second terminals of the high impedance signal source to the source of the source follower transistor is dependent on a ratio of a capacitance of the first capacitor and a capacitance of the fourth capacitor.
12. The system of claim 10 or 11, further comprising:

a fifth capacitor (C3N) coupled between a second input of the differential amplifier and a reference voltage; and

a sixth capacitor (C_L) coupled between a second output of the differential amplifier and the second input of the differential amplifier.

13. The system of one of claims 10 to 12, wherein the differential amplifier comprises a fully differential amplifier with common mode feedback and/or an operational transconductance amplifier (OTA) and/or wherein the source follower transistor is biased in a sub-threshold region.

14. The amplifier of one of claims 10 to 13, further comprising a bias resistor coupled in parallel with the third capacitor, the bias resistor comprising a value of at least 100M Ω .

15. A method of amplifying a signal provided by a capacitive signal source, the method comprising:

receiving a first signal from a first terminal of the capacitive signal source at a control terminal of a voltage follower;
receiving a second signal from a second terminal of the capacitive signal source at a first capacitor coupled to an output node of a voltage follower device;
amplifying the first and second signals, amplifying comprising applying a voltage gain based on a ratio of the first capacitor and a second capacitor coupled between the second terminal of the capacitive signal source and a reference node;
receiving a third signal from the output node of the voltage follower device by a capacitively coupled, fully differential amplifier; and
amplifying the third signal, amplifying comprising producing a differential output signal.

Patentansprüche

1. System zum Verstärken eines Signals, das durch eine kapazitive Quelle bereitgestellt wird, wobei die Systemschaltung umfasst:

eine erste Stufe (204), die so ausgelegt ist, dass sie eine erste Impedanz der kapazitiven Quelle (202) in eine zweite Impedanz an einem Ausgang der ersten Stufe umwandelt, wobei die erste Impedanz größer als die zweite Impedanz ist, wobei die erste Stufe so ausgelegt ist, dass sie eine Eingangsimpedanz der ersten Stufe durch Bereitstellen von positiver Rückkopplung vom Ausgang der ersten Stufe über einen ersten Kondensator (C11) zu einem Eingang der ersten Stufe erhöht; und
eine zweite Stufe (206) zum Umwandeln des Ausgangs der ersten Stufe in ein Differenzsignal an einem Ausgang der zweiten Stufe.

2. System nach Anspruch 1, ferner umfassend ein Vorspannungsnetz (R_B , V_B), das so ausgelegt ist, dass es eine Vorspannung für die kapazitive Quelle bereitstellt.

3. System nach Anspruch 1 oder 2, wobei die erste Stufe eine Sourcefolger-Verstärkungsschaltung umfasst, die eine Spannungsverstärkung von über eins umfasst.

4. System nach Anspruch 3, wobei:

die erste Stufe ferner einen zweiten Kondensator (C22) umfasst, der zwischen den Eingang der ersten Stufe und einen Referenzknoten gekoppelt ist; und

die Spannungsverstärkung auf einem Verhältnis einer Kapazität des ersten Kondensators und einer Kapazität des zweiten Kondensators basiert.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei die Signalquelle eine kapazitive Signalquelle ist, die erste Stufe eine Spannungsfolgervorrichtung umfasst, die einen Eingangsanschluss umfasst, der so ausgelegt ist, dass er mit einem ersten Anschluss der kapazitiven Signalquelle gekoppelt wird, der erste Kondensator ein erstes Ende, das mit einem Ausgangsanschluss der Spannungsfolgervorrichtung gekoppelt ist, und ein zweites Ende umfasst, das so ausgelegt ist, dass es mit dem einem zweiten Anschluss der kapazitiven Signalquelle gekoppelt wird, und
die zweite Stufe (206) kapazitiv mit dem Ausgangsanschluss der Spannungsfolgervorrichtung gekoppelt ist, wobei die zweite Stufe einen Differenzverstärker (A2) umfasst.

6. System nach Anspruch 5, wobei die zweite Stufe ferner umfasst:

einen Eingangskondensator (C3P), der zwischen den Ausgangsanschluss der Spannungsfolgervorrichtung und einen ersten Eingangsanschluss des Differenzverstärkers gekoppelt ist; einen Referenzkondensator (C3N), der zwischen einen Referenzknoten und einen zweiten Eingangsanschluss des Differenzverstärkers gekoppelt ist;

einen ersten Rückkopplungskondensator (C4P), der zwischen einen ersten Ausgangsanschluss des Differenzverstärkers und den ersten Eingangsanschluss des Differenzverstärkers gekoppelt ist;

einen zweiten Rückkopplungskondensator (C4N), der zwischen einen zweiten Ausgangsanschluss des Differenzverstärkers und den zweiten Eingangsanschluss des Differenzver-

stärkers gekoppelt ist.

7. System nach Anspruch 5 oder 6, wobei die Spannungsfolgervorrichtung einen MOS-Sourcefolger (M1) umfasst. 5
8. System nach Anspruch 7, wobei die Sourcefolgervorrichtung in einer Unterschwellenregion vorgespannt ist. 10
9. System nach einem der Ansprüche 5 bis 8, wobei die erste Stufe ferner einen zweiten Kondensator umfasst, der ein erstes Ende, das mit einem Referenzknoten gekoppelt ist, und ein zweites Ende umfasst, das so ausgelegt ist, dass es mit dem zweiten Anschluss der kapazitiven Signalquelle gekoppelt wird. 15
10. System nach Anspruch 1, wobei die Signalquelle eine hochohmige Signalquelle ist, die erste Stufe einen Spannungsfolgertransistor (M1) umfasst, der ein Gate aufweist, das so ausgelegt ist, dass es mit einem ersten Anschluss der hochohmigen Signalquelle gekoppelt wird, der erste Kondensator einen ersten Anschluss, der mit einer Source des Sourcefolgertransistors gekoppelt ist, und einen zweiten Anschluss umfasst, der so ausgelegt ist, dass er mit dem einem zweiten Anschluss der hochohmigen Signalquelle gekoppelt wird, 20
der zweite Kondensator zwischen die Source des Sourcefolgertransistors und einen ersten Eingang eines Differenzverstärkers der zweiten Stufe gekoppelt ist, 30
ein dritter Kondensator zwischen einen ersten Ausgang des Differenzverstärkers und den ersten Eingang des Differenzverstärkers gekoppelt ist, der Differenzverstärker so ausgelegt ist, dass er eine negative Phase am ersten Ausgang in Bezug auf den ersten Eingang erzeugt, und 35
die Niederfrequenzverstärkung des Differenzverstärkers durch ein Verhältnis einer Kapazität des zweiten Kondensators und einer Kapazität des dritten Kondensators festgelegt ist. 40
45
11. System nach Anspruch 10, ferner umfassend einen vierten Kondensator, der zwischen den zweiten Anschluss des ersten Kondensators und eine Spannungsreferenz gekoppelt ist, wobei eine Spannungsverstärkung aus den ersten und zweiten Anschlüssen der hochohmigen Signalquelle zur Source des Sourcefolgertransistors von einem Verhältnis einer Kapazität des ersten Kondensators und einer Kapazität 50
des vierten Kondensators abhängt. 55
12. System nach Anspruch 10 oder 11, ferner umfassend:

einen fünften Kondensator (C3N), der zwischen einen zweiten Eingang des Differenzverstärkers und eine Referenzspannung gekoppelt ist; einen sechsten Kondensator (C_L), der zwischen einen zweiten Ausgang des Differenzverstärkers und den zweiten Eingang des Differenzverstärkers gekoppelt ist.

13. System nach einem der Ansprüche 10 bis 12, wobei der Differenzverstärker einen voll differenziellen Verstärker mit Gleichtaktrückkopplung und/oder einen Transkonduktanz-Operationsverstärker (OTA) umfasst, und/oder wobei der Sourcefolgertransistor in einer Unterschwellenregion vorgespannt ist.
14. Verstärker nach einem der Ansprüche 10 bis 13, ferner umfassend einen Vorspannungswiderstand, der parallel zum dritten Kondensator gekoppelt ist, wobei der Vorspannungswiderstand einen Wert von mindestens 100 MΩ umfasst.
15. Verfahren zum Verstärken eines Signals, das durch eine kapazitive Quelle bereitgestellt wird, wobei das Verfahren umfasst:

Empfangen eines ersten Signals aus einem ersten Anschluss der kapazitiven Signalquelle an einem Steueranschluss eines Spannungsfolgers;
Empfangen eines zweiten Signals aus einem zweiten Anschluss der kapazitiven Signalquelle an einem ersten Kondensator, der mit einem Ausgangsknoten einer Spannungsfolgervorrichtung gekoppelt ist;
Verstärken der ersten und zweiten Signale, wobei das Verstärken ein Anwenden einer Spannungsverstärkung umfasst, die auf einem Verhältnis des ersten Kondensators und eines zweiten Kondensators beruht, der zwischen den zweiten Anschluss der kapazitiven Signalquelle und einen Referenzknoten gekoppelt ist;
Empfangen eines dritten Signals vom Ausgangsknoten der Spannungsfolgervorrichtung durch einen kapazitiv gekoppelten, vollständig differenziellen Verstärker; und
Verstärken des dritten Signals, wobei das Verstärken ein Erzeugen eines differenziellen Ausgangssignals umfasst.

Revendications

1. Système d'amplification d'un signal fourni par une source capacitive, le système du circuit comprenant :

un premier étage (204) configuré pour transformer une première impédance de la source (202)

- capacitive en une deuxième impédance à une sortie du premier étage, la première impédance étant plus grande que la deuxième impédance, le premier étage étant configuré pour augmenter une impédance d'entrée du premier étage en fournissant une réaction positive de la sortie du premier étage à une entrée du premier étage par l'intermédiaire d'un premier condensateur (C11) ; et
un deuxième étage (206) pour transformer la sortie du premier étage en un signal différentiel à une sortie du deuxième étage.
2. Système suivant la revendication 1, comprenant, en outre, un réseau (R_B , V_B) de polarisation configuré pour fournir une tension de polarisation à la source capacitive.
3. Système suivant la revendication 1 ou 2, dans lequel le premier étage comprend un circuit amplifié à suiveur de source ayant un gain en tension plus grand que un.
4. Système suivant la revendication 3, dans lequel :
- le premier étage comprend, en outre, un deuxième condensateur (C22) monté entre l'entrée du premier étage et un noeud de référence ; et le gain en tension repose sur un rapport d'une capacité du premier condensateur et d'une capacité du deuxième condensateur.
5. Système suivant l'une des revendications 1 à 4, dans lequel :
- la source de signal est une source de signal capacitive,
le premier étage comprend un dispositif suiveur de tension, comprenant une borne d'entrée configurée pour être reliée à une première borne de la source de signal capacitive,
le premier condensateur comprend une première extrémité reliée à une borne de sortie du dispositif suiveur de tension et une deuxième extrémité configurée pour être reliée à une deuxième borne de la source de signal capacitive, et le deuxième étage (206) est relié capacitivement à la borne de sortie du dispositif suiveur de tension, le deuxième étage comprenant un amplificateur (A2) différentiel.
6. Système suivant la revendication 5, dans lequel le deuxième étage comprend, en outre :
- un condensateur (C3P) d'entrée, monté entre la borne de sortie du dispositif suiveur de tension et une première borne d'entrée de l'amplificateur différentiel ;
- un condensateur (C3N) de référence, monté entre un noeud de référence et une deuxième borne d'entrée de l'amplificateur différentiel ;
un premier condensateur (C4P) de réaction, monté entre une première borne de sortie de l'amplificateur différentiel et la première borne d'entrée de l'amplificateur différentiel ; et
un deuxième condensateur (C4N) de réaction, monté entre une deuxième borne de sortie de l'amplificateur différentiel et la deuxième borne d'entrée de l'amplificateur différentiel.
7. Système suivant la revendication 5 ou 6, dans lequel le dispositif suiveur de tension comprend un suiveur (M1) de source MOS.
8. Système suivant la revendication 7, dans lequel le dispositif suiveur de source est polarisé dans une région de sous-seuil.
9. Système suivant l'une des revendications 5 à 8, dans lequel le premier étage comprend, en outre, un deuxième condensateur comprenant une première extrémité reliée à un noeud de référence et une deuxième extrémité configurée pour être reliée à la deuxième borne de la source de signal capacitive.
10. Système suivant la revendication 1, dans lequel :
- la source de signal capacitive est une source de signal à grande impédance,
le premier étage comprend un transistor (M1) à suiveur de source ayant une grille configurée pour être reliée à une première borne de la source de signal à grande impédance,
le premier condensateur a une première borne reliée à une source du transistor à suiveur de source et une deuxième borne configurée pour être reliée à une deuxième borne de la source de signal à grande impédance,
le deuxième condensateur est monté entre la source du transistor à suiveur de source et une première entrée d'un amplificateur différentiel du deuxième étage,
un troisième condensateur est monté entre une première sortie de l'amplificateur différentiel et la première entrée de l'amplificateur différentiel, l'amplificateur différentiel est configuré pour produire une phase négative à la première sortie par rapport à la première entrée, et
un gain à basse fréquence de l'amplificateur différentiel est réglé par un rapport d'une capacité du deuxième condensateur et une capacité du troisième condensateur.
11. Système suivant la revendication 10, comprenant, en outre, un quatrième condensateur monté entre la deuxième borne du premier condensateur et une

tension de référence, un gain en tension des première et deuxième bornes de la source de signal à grande impédance à la source du transistor à suiveur de source, dépendant d'un rapport d'une capacité du premier condensateur et d'une capacité du quatrième condensateur. 5

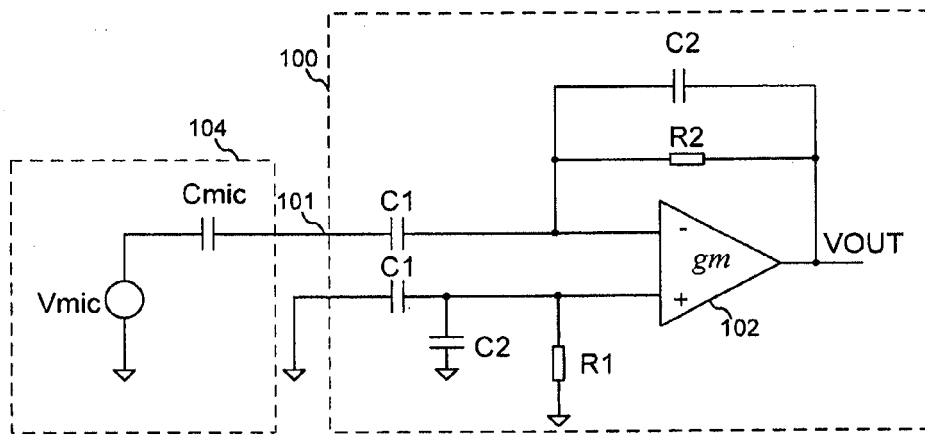
12. Système suivant la revendication 10 ou 11, comprenant, en outre :

un cinquième condensateur (C3N) monté entre une deuxième entrée de l'amplificateur différentiel et une tension de référence ; et
un sixième condensateur (C_L) monté entre une deuxième sortie de l'amplificateur différentiel et la deuxième entrée de l'amplificateur différentiel. 10 15

13. Système suivant l'une des revendications 10 à 12, dans lequel l'amplificateur différentiel comprend un amplificateur pleinement différentiel à réaction en mode commun et/ou un amplificateur opérationnel à transconductance (OTA) et/ou dans lequel le transistor à suiveur de source est polarisé dans une région de sous-seuil. 20 25

14. Système suivant l'une des revendications 10 à 13, comprenant, en outre, une résistance de polarisation montée en parallèle au troisième condensateur, la résistance de polarisation comprenant une valeur d'au moins 100 MΩ. 30

15. Procédé d'amplification d'un signal fourni par une source de signal capacitive, le procédé comprenant : 35
la réception d'un premier signal d'une première borne de la source de signal capacitive à une borne de commande d'un suiveur de tension ;
la réception d'un deuxième signal d'une deuxième borne de la source de signal capacitive à un premier condensateur relié à un noeud de sortie d'un dispositif suiveur de tension ; 40
l'amplification du premier et du deuxième signal, l'amplification comprenant appliquer un gain de tension reposant sur un rapport du premier condensateur et d'un deuxième condensateur monté entre la deuxième borne de la source de signal capacitive et un noeud de référence ; 45
la réception d'un troisième signal du noeud de sortie du dispositif suiveur de tension par un amplificateur entièrement différentiel monté capacitivement ; et 50
l'amplification du troisième signal, l'amplification comprenant la production d'un signal de sortie différentiel. 55



Prior Art

FIG. 1

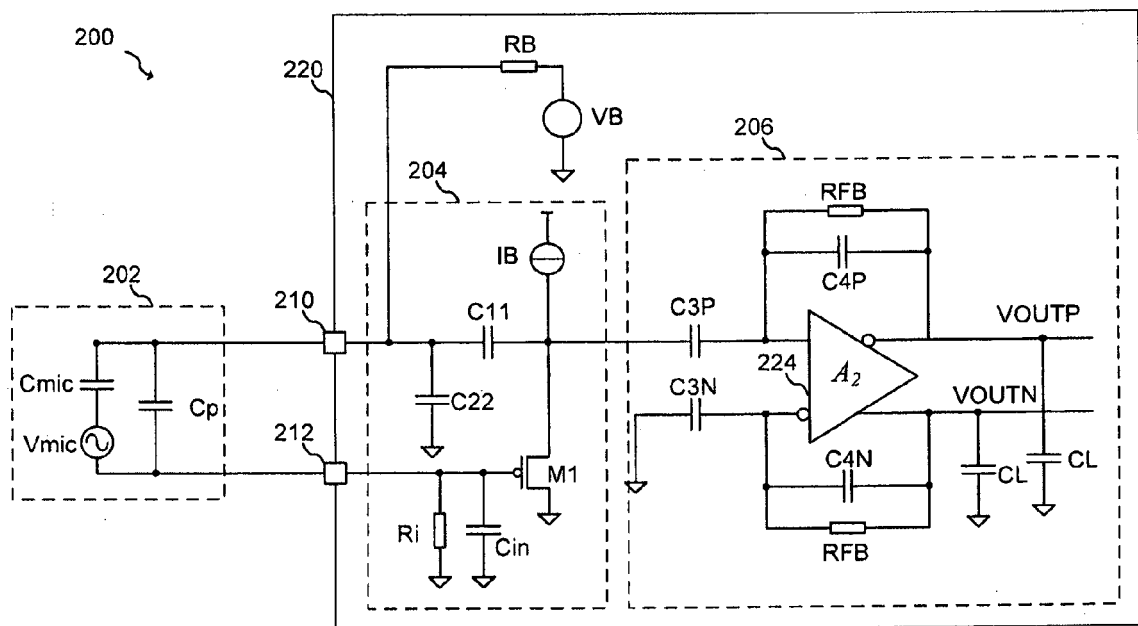


FIG. 2a

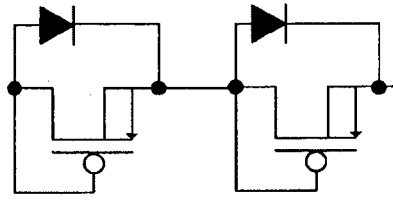


FIG. 2b

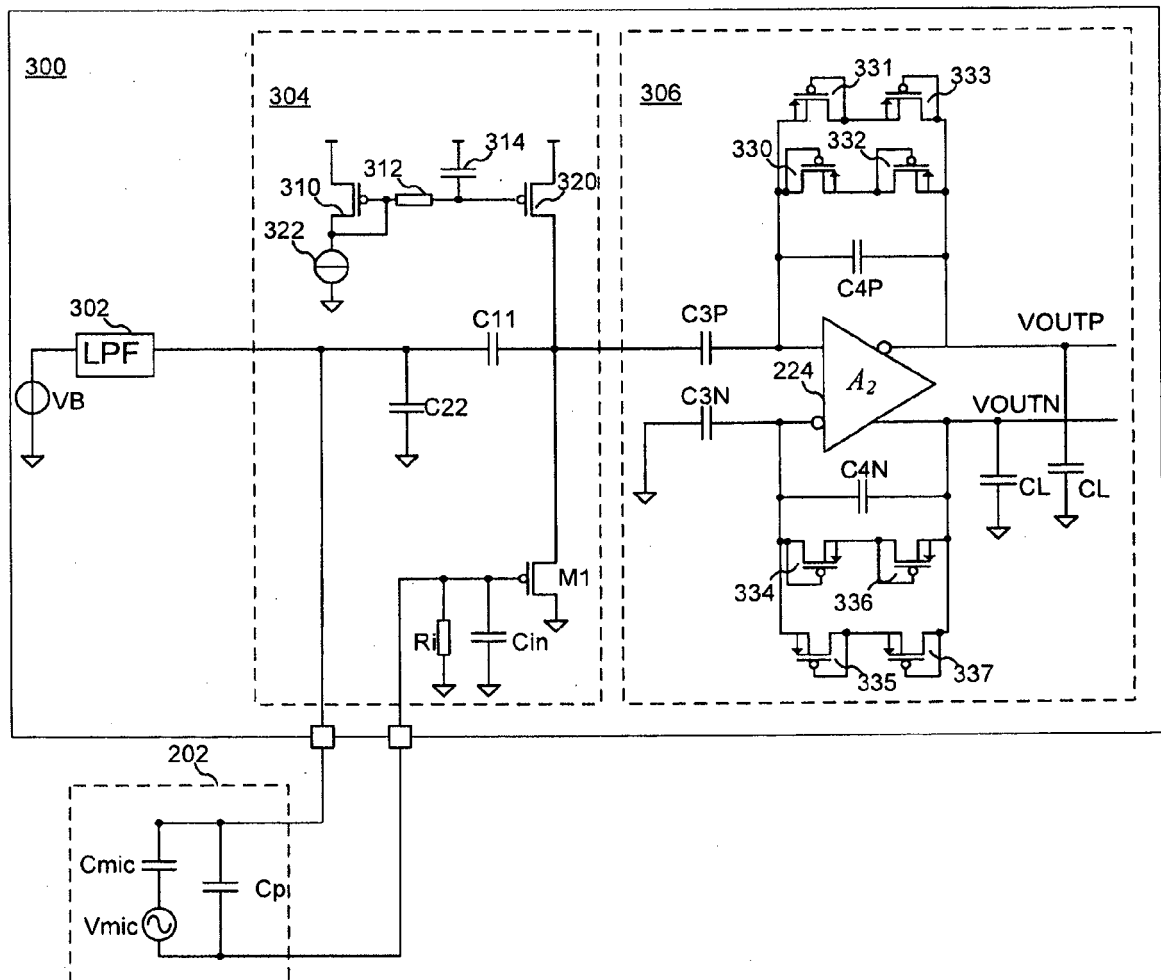


FIG. 3

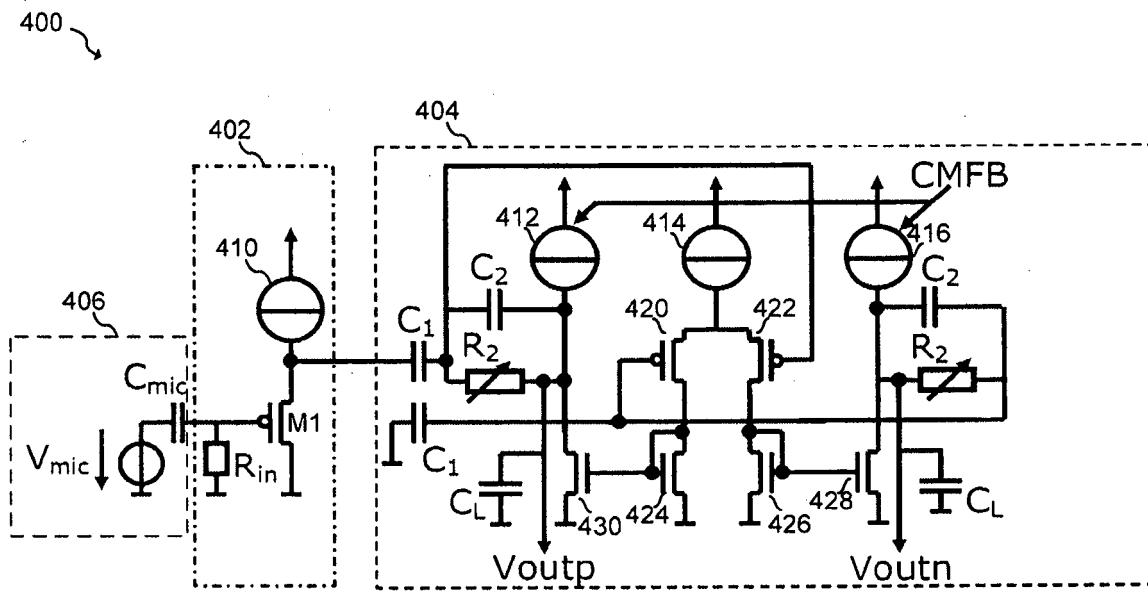


FIG. 4

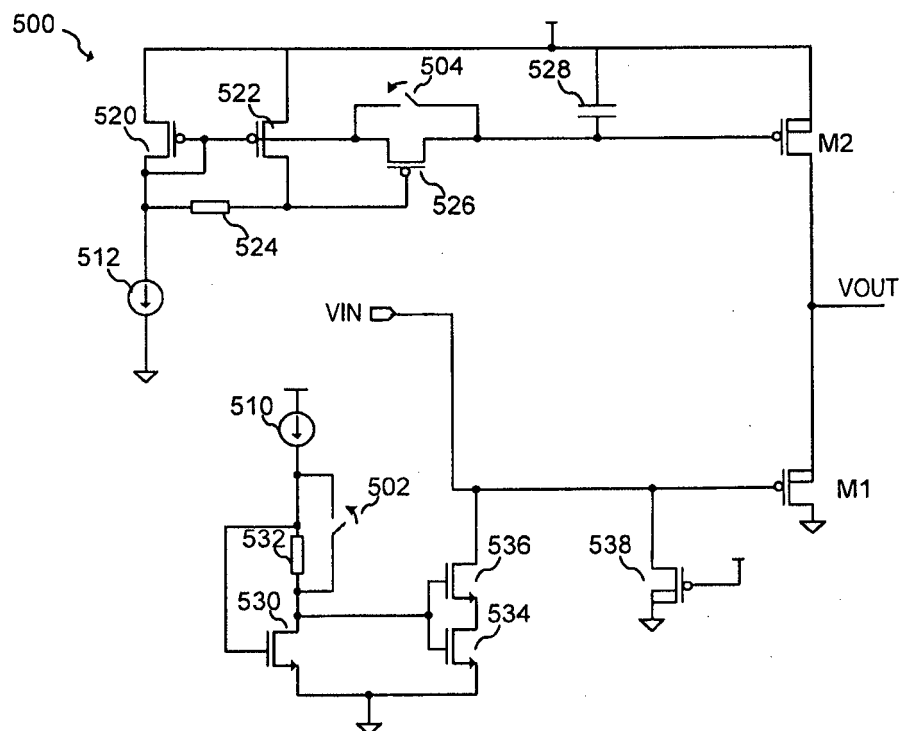


FIG. 5

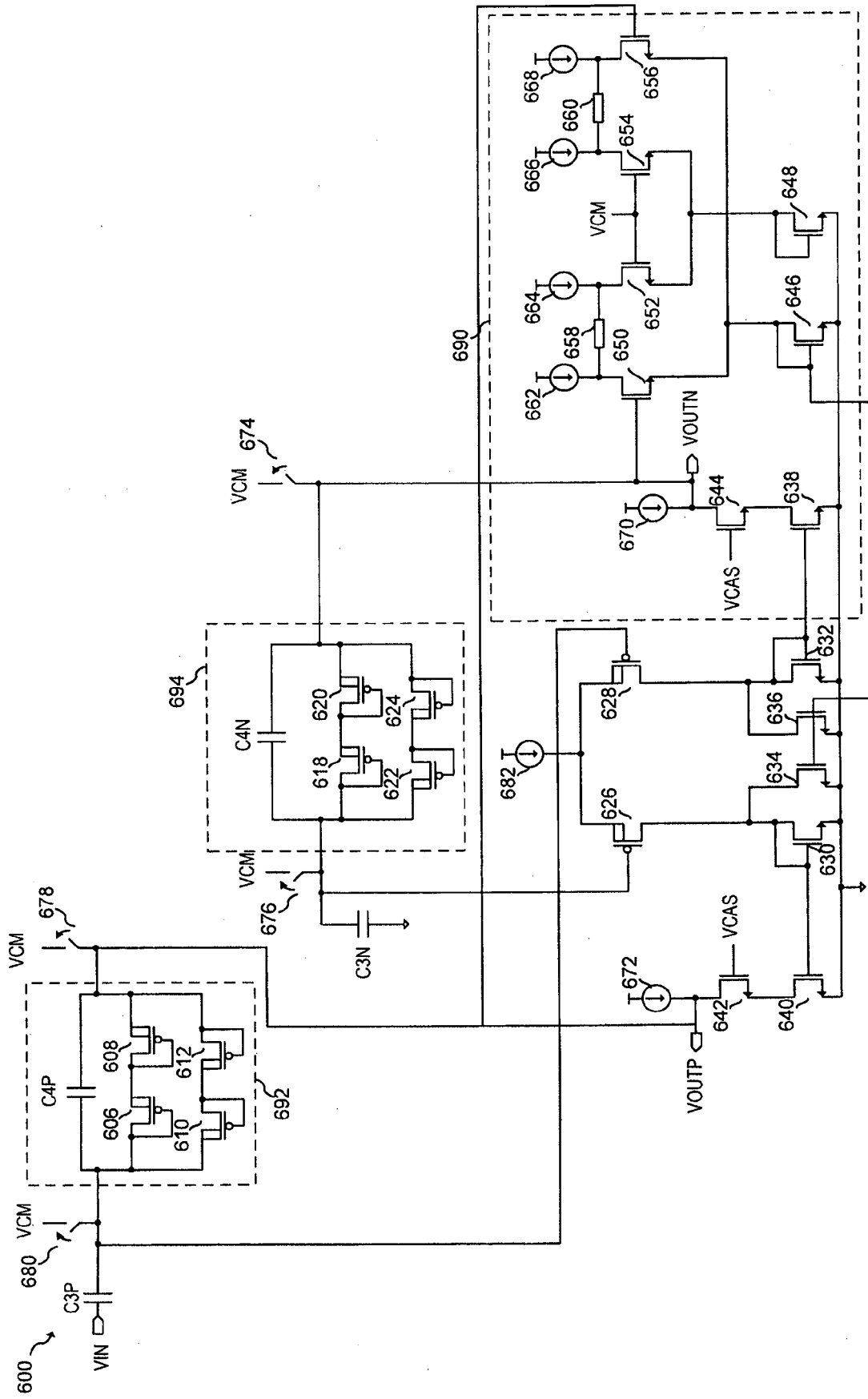


FIG. 6

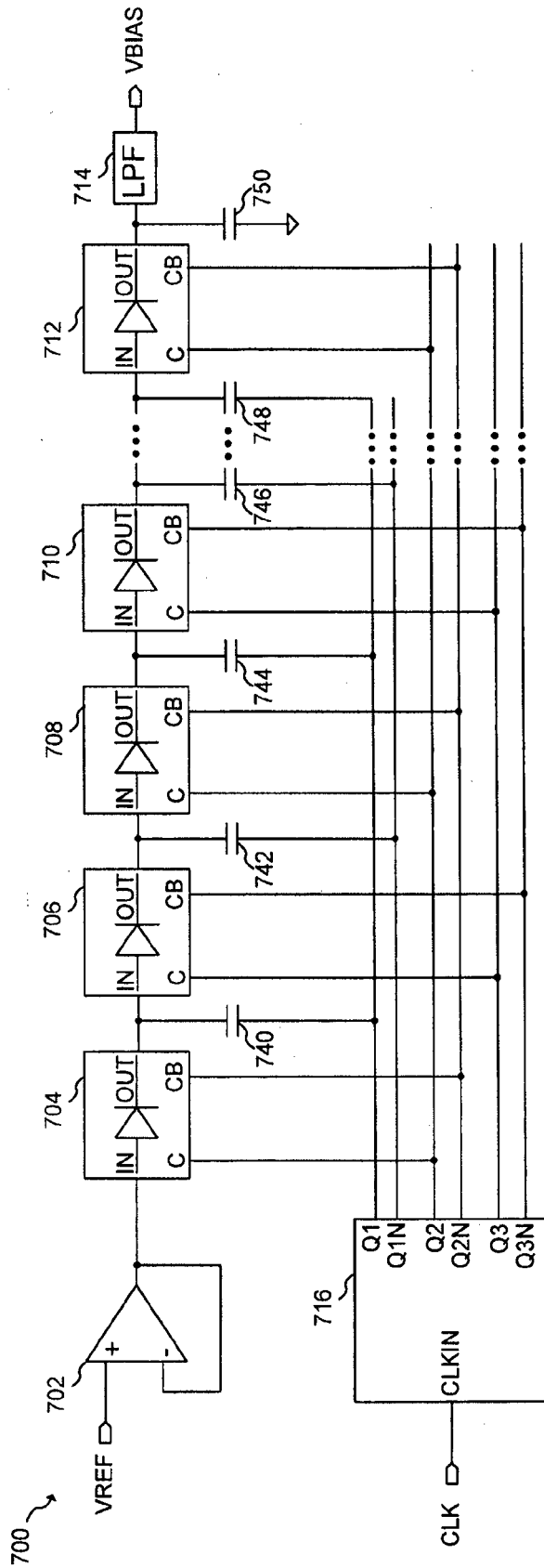


FIG. 7a

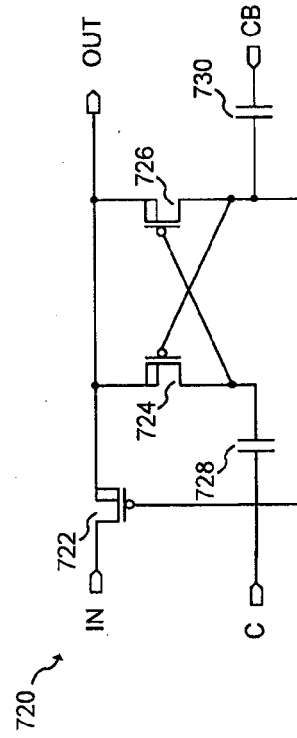


FIG. 7b

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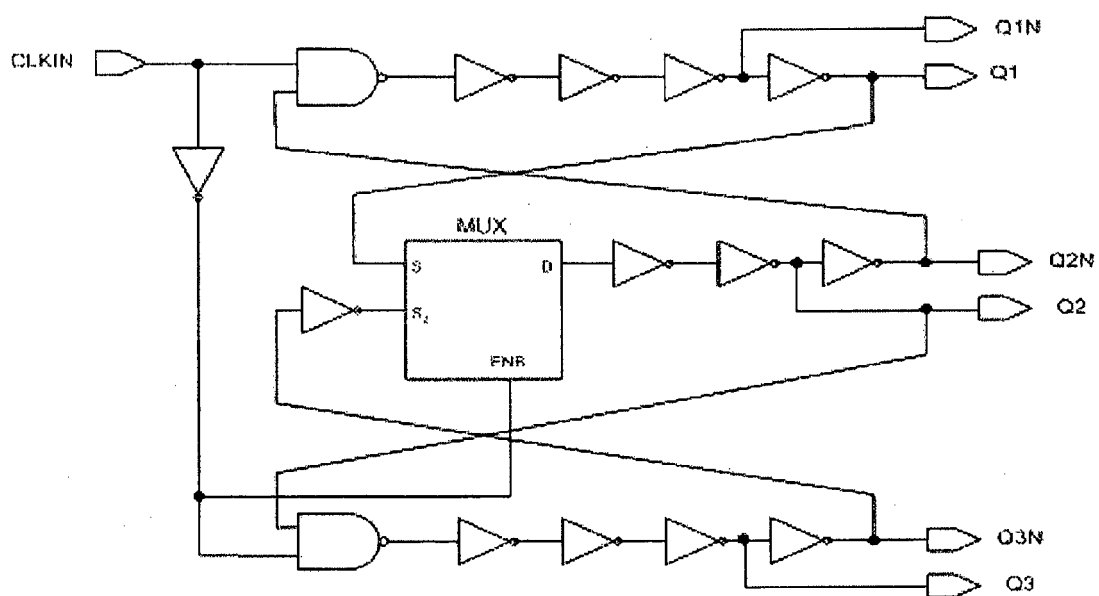


FIG. 7c

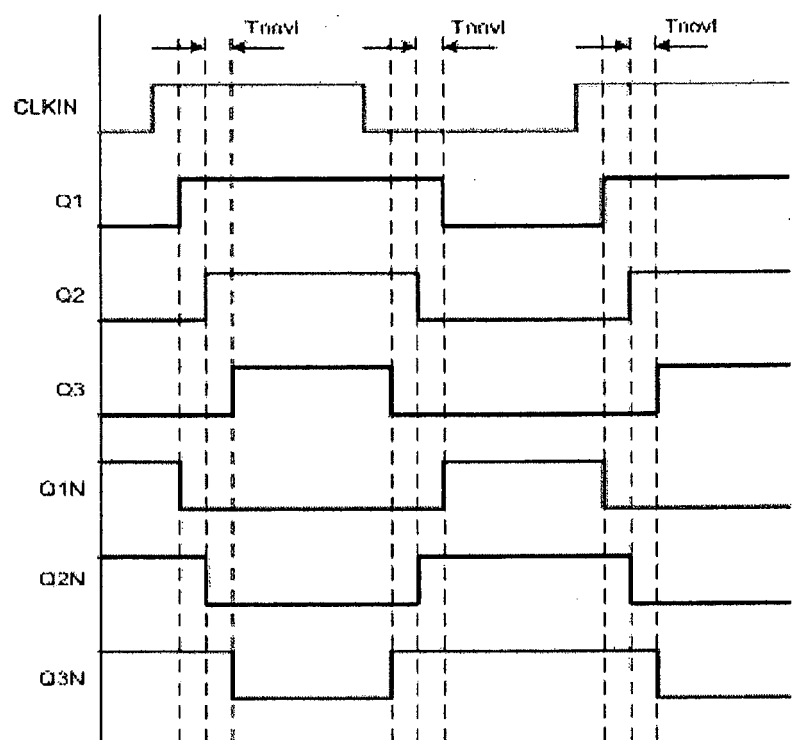


FIG. 7d

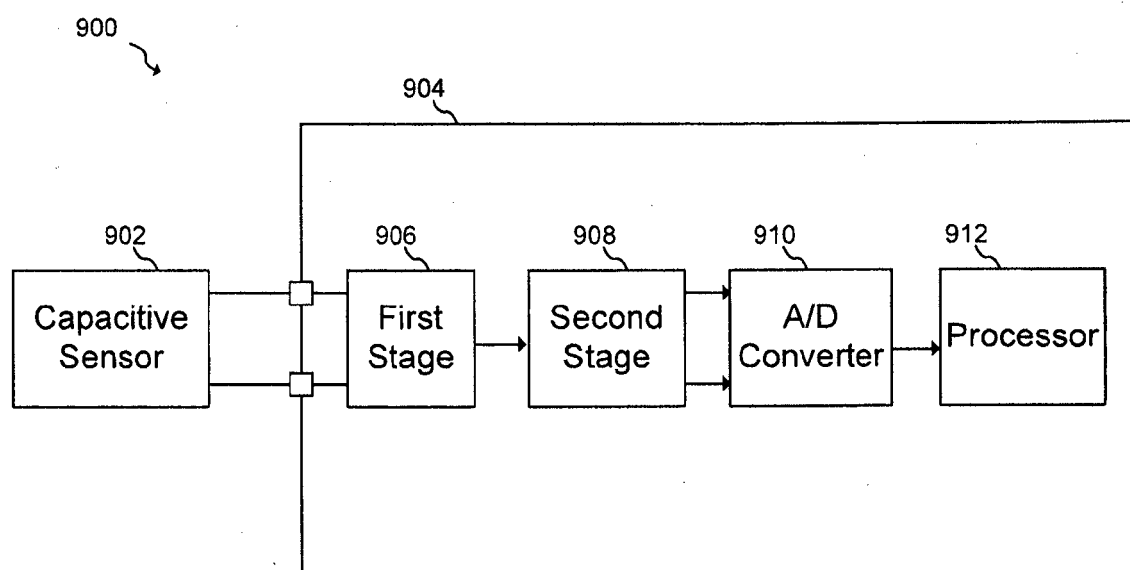


FIG. 8

REFERENCES CITED IN THE DESCRIPTION

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Non-patent literature cited in the description

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