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(54) **A PHASED ARRAY ANTENNA SIGNAL PROCESSING STRUCTURE, A METHOD AND A COMPUTER PROGRAM PRODUCT**

PHASENARRAY-ANTENNENSIGNALVERARBEITUNGSSTRUKTUR, VERFAHREN UND
COMPUTERPROGRAMMPRODUKT

STRUCTURE DE TRAITEMENT DE SIGNAUX D'ANTENNE RÉSEAU À COMMANDE DE PHASE,
PROCÉDÉ ET PRODUIT PROGRAMME D'ORDINATEUR

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Description

[0001] The invention relates to a phased array antenna signal processing structure, comprising a processor that includes a digital beam forming unit for generating partial beam data from digitized samples of a set of phased array antenna elements.

[0002] Digital beam forming in active electronic antenna arrays is complex. When the beam forming is performed in the digital domain, a central processor is heavily loaded both in terms of processing load and in communication load. Current implementations of analog and digital beam formers are very inflexible and poorly scalable. When the number of (phased array) antenna elements increases, the computational requirements of the used processor increases exceptionally.

[0003] It is noted that patent publication WO 2004/030145 discloses a method of producing a digital beamformer signal by a number of antenna modules that are alike, as well as a system implementing the method.

[0004] It is an object of the invention to provide a more efficient signal processing structure according to the preamble for processing phased array antenna element data. Thereto, according to the invention, a phased array antenna signal processing structure according to claim 1 is provided.

[0005] By both generating partial beam data and adding intermediate beam data from another processor, the processing capacity as well as the communication load of the signal processing structure can be distributed, thereby optimally exploiting the processor capacity. Especially when the processors are communicatively connected in a ring structure for cyclically performing the adding function, all processors can in principle be loaded equally.

[0006] The processing functions that are needed for computing a digital beam can be effectively distributed over the available processors. Further, the processor according to the invention allows a highly scalable ring structure wherein the number of processors increases linearly with number of phased array antenna elements and the communication load remains the same. The structure is thus fully scalable regarding the number of digital beams, the number of phased array antenna elements and the number of processors. In addition, since only intermediate results are transmitted, there is a low communication load on array level while the communication between the processors is minimal. Further, a hierarchical beam forming structure can be realized without a hierarchy in the processor structure.

[0007] Further, the invention relates to a method according to claim 11.

[0008] In addition, the invention relates to a computer program product according to claim 16. A computer program product may comprise a set of computer executable instructions stored on a data carrier, such as a flash memory, a CD or a DVD. The set of computer executable instructions, which allow a programmable computer to

carry out the method as defined above, may also be available for downloading from a remote server, for example via the Internet.

[0009] Other advantageous embodiments according to the invention are described in the following claims.

[0010] By way of example only, embodiments of the present invention will now be described with reference to the accompanying figures in which

Fig. 1 shows a schematic view of a phased array antenna signal processing structure according to the invention;

Fig. 2 shows a schematic view of a compressor in the structure of Fig. 1;

Fig. 3 shows a schematic view of three subsequent processors in the structure of Fig. 1; and

Fig. 4 shows a flow chart of a method according to the invention.

[0011] The figures are merely schematic views of a preferred embodiment according to the invention. In the figures, the same reference numbers refer to equal or corresponding parts.

[0012] Figure 1 shows a schematic view of a phased array antenna signal processing structure 1 according to the invention. The structure 1 includes a multiple number of identical processors 2a-h that are communicatively connected in a ring structure. In the shown embodiment, the ring structure is composed of eight processors 2a-h and a central unit that are interconnected via two sets of communication lines 4, viz. a set of communication lines 4a transmitting intermediate beam data and a set of communication lines 4b transmitting final beam data. The set of communication lines 4a,b can be physically distinct lines or logically distinct lines.

[0013] Figure 2 shows a schematic view of a processor 2 from the ring structure 1. The processor 2, also called tile, includes a digital beam forming unit 5, also called beam former, for generating partial beam data from digitized samples of a set of phased array antenna elements. Further, the processor 2 includes a first adder 6, also called samples adder, for adding the generated partial beam data. In addition, the processor 2 includes a number of terminals for communication with other devices.

[0014] More specifically, the processor 2 includes a first set of input terminals 7 for receiving intermediate beam data 44a from a preceding processor in the ring 1, a first set of output terminals 8 for transmitting new intermediate beam data 44a to a subsequent processor in the ring 1, a second set of input terminals 9 for receiving digitized samples 12 of a phased array antenna set, a third set of input terminals 10 for receiving digital beam coefficients 11, a fourth set of input terminals 13 and a second set of output terminals 14 for receiving and transmitting, respectively, final beam data 44b.

[0015] In order to obtain the ring structure, the first set of input terminals 7 of a particular processor 2c are con-

nected the first set of output terminals 8 of a preceding processor 2b in the ring 1. Similarly, the first set of output terminals 8 of the particular processor 2c are connected to the set of input terminals 7 of a subsequent processor 2d in the ring 1. Analogously, the fourth set of input terminals 13 and the second set of output terminals 14 of subsequent processors 2 in the ring structure 1 form the second set of communication lines for the final beam data 44b.

[0016] Each processor 2 contains the same number of input terminals in the second set of input terminals 9, so that each processor can process the same number of samples 12. In the shown example, the processor 2 includes 32 first input terminals 9, also called sample input channels. Then, the ring structure 1, including in the shown example 8 processors 2, is able to process 256 channels of digital samples. Thereto, a phased array antenna structure is split into 8 sets of phased array antenna elements, each feeding a corresponding processor 2.

[0017] Also the central unit 3 is provided with corresponding sets of input terminals and output terminals for receiving the intermediate beam data 44a and the final beam data 44b.

[0018] During operation of the ring structure 1 according to the invention, each processor 2a-h receives, via the second set of input terminals 9 digitized samples 12 from the corresponding set of phased array antenna elements. Thereto, the samples have been digitized using analog to digital converters ADC's. Each processor 2 processes the samples 12 to generate partial beam data. In this process, digital beam coefficients 11 are received via the third set of input terminals 10. The digital beam forming unit 5 includes a set of multipliers for multiplying the received samples 12 with corresponding digital beam coefficients 11. Further, the digital beam forming unit 5 includes a second adder for adding corresponding multiplied samples to generate partial beam data.

[0019] In order to obtain a digital beam, each sample is multiplied with a corresponding coefficient. Then, all multiplied samples are added. Thus, in each processor 2 receiving, in the shown embodiment, 32 samples, 32 multiplied samples are added. However, according to an aspect of the invention, a multiple number of digital beams can be computed. Thereto, the same samples 12 are also multiplied with other digital beam coefficients 11 to arrive at a second set of digital beam data. Preferably, the number of digital beams is in the same order as the total number of samples, in this example, 256 digital beams. The data that is generated in the digital beam forming unit 5 are called partial beam data, since the adding process has not yet been performed over all samples, but only over the samples that are received by a common processor 2. In the following, the process of adding the partial beam data is described.

[0020] The partial beam data 15 is internally transmitted to the first adder 6 that receives also intermediate beam data 44a from the preceding processor 2 in the ring structure 1, via the first set of input terminals 9. Using

the first adder, the partial beam data 15 generated by the digital beam forming unit 5 is added to the intermediate beam data 44a to get a new update of the intermediate beam data 44a. Corresponding digital beam data are added, i.e. a summation is performed over partial beam data that relate to the same digital beam. The new update of the intermediate beam data 44a is transmitted to the next processor 2 in the ring structure 1. When this process is repeated, subsequently, by the eight processors 2, all digital beams have been computed. The data of the complete digital beams are called final beam data 44b.

[0021] According to an aspect of the invention, final beam data are generated by adding intermediate beam data received at a processor to corresponding partial beam data generated by the processor, wherein the intermediate beam data are based on corresponding partial beam data generated by all other processors in the ring 1. The final beam data 44b is transmitted via the second set of output terminals.

[0022] Figure 3 shows a schematic view of three subsequent processors 2a-c in the structure 1. According to an advantageous embodiment of the invention, the computation of the final beam data 44b is evenly distributed over the processors 2, so that each processor 2 performs a similar task. In the exemplary embodiment, each processor 2 generates 32 different final digital beams adding up to the total number of 256 digital beams. In the shown embodiment, the first processor 2a computes a block 80 of final digital beams, viz. digital beams 225-256, and seven blocks 81 of 32 intermediate digital beam data each. Similarly, the second processor 2 b computes a single block 80 of other final digital beams, viz. digital beams 193-224, and seven blocks 81 of 32 intermediate digital beam data each. The block 80 that is added, by a particular processor 2, to the communication line 4b of final data, is not changed by the other processors 2.

[0023] The central unit 3 obtains all blocks of final data 44b for further processing. The fully beam formed data referred to as final beam data available for further processing can be transmitted to units outside the ring structure. In a first embodiment, the final beam data can be transmitted to a single processor unit. However, the communication load is herewith locally increased. In a further embodiment, the final beam data are transmitted to a dedicated processor node embedded at any location in the ring structure. In yet a further embodiment, one or a few beam data sets are allocated to a single processor, so that the communication load is distributed over available processors. The latter method of communicating final beam data has the added advantage that any additional processing required per final beam data set (e.g. range-doppler processing) can be equally divided over processors as well.

[0024] In order to facilitate a proper time management of the data to be processed and transmitted, a number of further input terminals and output terminals can be provided. As an example, the processor might include terminals for time controlling signals and/or for reading

data such as multiplication coefficients that have been input to the processor.

[0025] It is noted that, preferably, the number of first and second input terminals, and the number of first and second output terminals coincides to optimally benefit from digital I/O terminals in the processor 2. In a different embodiment the data passed between processors can contain time stamp data to align partial beam data and intermediate beam data.

[0026] As an example, the digital samples are received at a rate of 96 K samples per second, per ADC, each sample having 8 bits that are transmitted serially.

[0027] According to a further aspect of the invention, a defect in the performance of a specific processor in the ring structure can be detected. Then, the intermediate data and the final data can be transmitted by a preceding processor in the ring, towards a subsequent processor in the ring, thus circumventing the processor having the defect. Apparently, measures have to be taken to properly delay the data or time stamp the data, so that the other processors continue in meaningfully processing the intermediate results. Advantageously, by applying a data transfer by-pass, the ring structure can continue processing phased array antenna data, also with a defect processor, albeit with a reduced performance since the functionally eliminated processor and connected antenna element data do not contribute anymore in computing a digital beam.

[0028] In this respect it is noted that the steps of detecting a defect in the performance of a specific processor, and forwarding the intermediate data and final data transmitted by a preceding processor towards a subsequent processor can not only be performed in combination with a phased array antenna signal processing structure wherein a multiple number of processors are communicatively connected in a ring structure, but also, in combination with a more general phased array antenna signal processing structure wherein a multiple number of processors are communicatively connected in a chain structure.

[0029] The processor can be implemented in various ways, e.g. as an FPGA, an ASIC, a DSP or a general purpose processor, e.g. using a laptop.

[0030] Figure 4 shows a flow chart of an embodiment of the method according to the invention. The method is used for processing phased array antenna digitized samples. The method comprises the steps of generating (100) partial beam data using a processor processing a digitized samples received from a set of phased arrays, receiving (110), at the processor, intermediate beam data from another processor processing digitized samples received from another set of phased array antenna elements, generating (120) new intermediate beam data by adding the partial beam data to the corresponding received intermediate beam data, and transmitting (130) the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased arrays.

[0031] The method of processing phased array antenna digitized samples can be performed using dedicated hardware structures, such as FPGA and/or ASIC components. Otherwise, the method can also at least partially be performed using a computer program product comprising instructions for causing a processor of the computer system to perform the above described steps of the method according to the invention. All steps can in principle be performed on a single processor. However it is noted that at least one step can be performed on a separate processor, e.g. the step of transmitting the new intermediate beam data to yet a further processor processing digitized samples received from a further set of phased arrays.

[0032] The invention is not restricted to the embodiments described herein. It will be understood that many variants are possible.

[0033] It is noted that another number of processors and another total number of samples can be chosen. Further, another number of input terminals in the second set of input terminals of the processors can be chosen.

[0034] In addition, the processor can include further processing functions such as analog-digital conversion, calibration etc. Calibration can be implemented as an additional multiplication, for the sake of a simple design, or as an additional addition, for the sake of computational efficiency.

[0035] The digital beam forming unit can process on the real and imaginary part of the samples. Otherwise, also the amplitude and phase components can be processed. Further, by signal decomposition in frequency and phase components, an efficient Hilbert operation can optionally be applied.

[0036] Other such variants will be apparent for the person skilled in the art and are considered to lie within the scope of the invention as determined in the following claims.

Claims

1. A phased array antenna signal processing structure (1), comprising a processor (2) that includes a digital beam forming unit (5) for generating partial beam data (15) from digitized samples (12) of a set of phased array antenna elements, and wherein the processor further comprises:

- a first set of input terminals (7) for receiving intermediate beam data (44a) from another processor processing digitized samples received from another set of phased array antenna elements;
- a first adder (6) for generating new intermediate beam data by adding partial beam data (15) generated by the digital beam forming unit to the corresponding received intermediate beam data (44a);

- a first set of output terminals (8) for transmitting the new intermediate beam data;
 - a second set of input terminals (9) for receiving said digitized samples (12) of said set of phased array antenna elements;
 - a third set of input terminals (10) for receiving digital beam coefficients (11); and wherein the digital beam forming unit (5) comprises a set of multipliers for multiplying said received digitized samples (12) with corresponding received digital beam coefficients (11); and a second adder for adding corresponding multiplied samples to generate said partial beam data (15).
2. A structure according to claim 1, wherein the partial beam data and the intermediate beam data include data relating to multiple digital beams.
 3. A structure according to any of the preceding claims, comprising a multiple number of processors communicatively connected in a ring structure.
 4. A structure according to claim 3, wherein the first set of input terminals of a particular processor are connected to the first set of output terminals of a preceding processor in the ring, and wherein the first set of output terminals of the particular processor are connected to the first set of input terminals of a subsequent processor in the ring.
 5. A structure according to claim 3 or 4, wherein each of the processors are arranged for processing digitized samples of a corresponding set of phased array antenna elements.
 6. A structure according to any of claims 3-5, wherein each processor contains the same number of input terminals in the second set of input terminals.
 7. A structure according to any of claims 3-6, further comprising a central unit, included in the ring, for receiving final beam data (44b).
 8. A structure according to any of claims 3-7, wherein the processors further include a fourth set of input terminals and a second set of output terminals for receiving and transmitting, respectively, final beam data (44b).
 9. A structure according to any of claims 3-8, wherein the first adder in each processor is arranged for generating final beam data (44b) by adding received intermediate beam data to corresponding partial beam data generated by the digital beam forming unit wherein the intermediate beam data is based on corresponding partial beam data generated by all other processors in the ring.
 10. A structure according to any of claims 3-9, wherein the processors are identical.
 11. A method for processing digitized samples (12) of a set of phased array antenna elements, comprising the steps of:
 - generating partial beam data (15) using a processor (2) processing digitized samples (12) received from a set of phased array antenna elements;
 - receiving, at the processor (2), intermediate beam data (44a) from another processor processing digitized samples received from another set of phased array antenna elements;
 - generating new intermediate beam data (44a) by adding the partial beam data (15) to the corresponding received intermediate beam data (44a), using a first adder (6); and
 - transmitting the new intermediate beam data (44a) to yet a further processor processing digitized samples received from a further set of phased array antenna elements,
 wherein the step of generating partial beam data (15) includes multiplying said received digitized samples (12) with corresponding digital beam coefficients (11), using a set of multipliers, and adding corresponding multiplied samples, using a second adder, to generate said partial beam data (15).
 12. A method according to claim 11, further comprising the steps of:
 - splitting the digitized samples of the sets of phased array antenna elements into a multiple number of N digitized sample sets;
 - generating partial beam data using N processors communicatively connected in a ring structure, each processor processing a corresponding digitized sample set;
 - receiving, at each processor, intermediate beam data from a preceding processor in the ring;
 - generating, by each processor, new intermediate beam data by adding the intermediate beam data that is received at each processor to corresponding partial beam data generated by said processor; and
 - transmitting all new intermediate beam data to the subsequent processor in the ring.
 13. A method according to claim 12, further comprising generating final beam data by performing the steps of:
 - adding intermediate beam data received at a processor to corresponding partial beam data

generated by the processor wherein the intermediate beam data are based on corresponding partial beam data generated by all other processors in the ring; and

- deciding whether the added intermediate beam data is complete and can be transferred as final beam data instead of intermediate beam data.

14. A method according to claim 13, further comprising a step of performing additional processing on the final beam data.

15. A method according to claim 14, further comprising detecting a defect in the performance of a specific processor in the ring structure, and forwarding the intermediate data and final data transmitted by a preceding processor in the ring, to a subsequent processor in the ring.

16. A computer program product for processing digitized samples (12) of a set of phased array antenna elements, the computer program product comprising computer readable code causing a processor (2) to perform the steps of:

- generating partial beam data (15) using a processor (2) processing digitized samples (12) received from a set of phased array antenna elements;

- receiving, at the processor, intermediate beam data (44a) from another processor processing digitized samples received from another set of phased array antenna elements;

- generating new intermediate beam data (44a) by adding the partial beam data (15) to the corresponding received intermediate beam data (44a), using a first adder (6); and

- transmitting the new intermediate beam data (44a) to yet a further processor processing digitized samples received from a further set of phased array antenna element antenna elements,

wherein the step of generating partial beam data (15) includes multiplying said received digitized samples (12) with corresponding digital beam coefficients (11), using a set of multipliers, and adding corresponding multiplied samples, using a second adder, to generate said partial beam data (15).

Patentansprüche

1. Phasengesteuerte Gruppenantennensignal-Verarbeitungsstruktur (1), mit einem Prozessor (2), der eine digitale Strahlformungseinheit (5) zum Erzeugen von Teilstrahl-
daten (15) aus digitalisierten Proben (12) eines Satzes

phasengesteuerter Gruppenantennenelemente enthält, und wobei der Prozessor weiter Folgendes umfasst:

- einen ersten Satz von Eingangsanschlüssen (7) zum Empfangen von Zwischenstrahl-
daten (44a) von einem anderen Prozessor, der digitalisierte Proben verarbeitet, die von einem anderen Satz phasengesteuerter Gruppenantennenelemente empfangen werden;

- einen ersten Addierer (6) zum Erzeugen neuer Zwischenstrahl-
daten durch Hinzufügen der von der digitalen Strahlformungseinheit erzeugten Teilstrahl-
daten (15) zu den entsprechenden empfangenen Zwischenstrahl-
daten (44a);

- einen ersten Satz von Ausgangsanschlüssen (8) zum Übertragen der neuen Zwischenstrahl-
daten;

- einen zweiten Satz von Eingangsanschlüssen (9) zum Empfang der digitalisierten Proben (12) des Satzes von phasengesteuerten Gruppen-
antennenelementen;

- einen dritten Satz von Eingangsanschlüssen (10) zum Empfangen von digitalen Strahlkoeffizienten (11); und wobei die digitale Strahlformungseinheit (5) einen Satz von Multiplizierern zum Multiplizieren der empfangenen digitalisierten Proben (12) mit entsprechenden empfangenen digitalen Strahlkoeffizienten (11) umfasst; und einen zweiten Addierer zum Hinzufügen von entsprechenden multiplizierten Proben, um die Teilstrahl-
daten (15) zu erzeugen.

2. Struktur nach Anspruch 1, wobei die Teilstrahl-
daten und die Zwischenstrahl-
daten Daten enthalten, die sich auf mehrere digitale Strahlen beziehen.

3. Struktur nach einem der vorhergehenden Ansprüche, umfassend eine Vielzahl von Prozessoren, die kommunikativ in einer Ringstruktur verbunden sind.

4. Struktur nach Anspruch 3, wobei der erste Satz von Eingangsanschlüssen eines bestimmten Prozessors mit dem ersten Satz von Ausgangsanschlüssen eines vorhergehenden Prozessors in dem Ring verbunden ist und wobei der erste Satz von Ausgangsanschlüssen des bestimmten Prozessors mit dem ersten Satz von Eingangsanschlüssen eines nachfolgenden Prozessors im Ring verbunden ist.

5. Struktur nach Anspruch 3 oder 4, bei jeder der Prozessoren zum Verarbeiten digitalisierter Proben eines entsprechenden Satzes phasengesteuerter Gruppenantennenelemente angeordnet ist.

6. Struktur nach einem der Ansprüche 3 bis 5, wobei jeder Prozessor die gleiche Anzahl von Eingangsanschlüssen im zweiten Satz von Eingangsanschlüssen

schlüssen enthält.

7. Struktur nach einem der Ansprüche 3 bis 6, weiter umfassend eine in dem Ring enthaltene Zentraleinheit zum Empfangen der Endstrahldaten (44b). 5
8. Struktur nach einem der Ansprüche 3 bis 7, wobei die Prozessoren weiter einen vierten Satz von Eingangsanschlüssen und einen zweiten Satz von Ausgangsanschlüssen zum Empfangen bzw. Übertragen von Endstrahldaten (44b) enthalten. 10
9. Struktur nach einem der Ansprüche 3 bis 8, wobei der erste Addierer in jedem Prozessor zum Erzeugen von Endstrahldaten (44b) durch Hinzufügen von empfangenen Zwischenstrahldaten zu entsprechenden Teilstrahldaten angeordnet ist, die von der digitalen Strahlformungseinheit erzeugt werden, wobei die Zwischenstrahldaten auf entsprechenden Teilstrahldaten basieren, die von allen anderen Prozessoren im Ring erzeugt werden. 15 20
10. Struktur nach einem der Ansprüche 3 bis 9, wobei die Prozessoren identisch sind. 25
11. Verfahren zum Verarbeiten digitalisierter Proben (12) eines Satzes phasengesteuerter Gruppenantennenelemente, welches die folgenden Schritte umfasst: 30
 - Erzeugen von Teilstrahldaten (15) unter Verwendung eines Prozessors (2), der digitalisierte Proben (12) verarbeitet, die von einem Satz phasengesteuerter Gruppenantennenelemente empfangen werden; 35
 - Empfangen, an dem Prozessor (2), von Zwischenstrahldaten (44a) von einem anderen Prozessor, der digitalisierte Proben verarbeitet, die von einem anderen Satz phasengesteuerter Gruppenantennenelemente empfangen werden; 40
 - Erzeugen neuer Zwischenstrahldaten (44a) durch Addieren der Teilstrahldaten (15) zu den entsprechenden empfangenen Zwischenstrahldaten (44a) unter Verwendung eines ersten Addierers (6); und 45
 - Übertragen der neuen Zwischenstrahldaten (44a) an einen weiteren Prozessor, der digitalisierte Proben verarbeitet, die von einem weiteren Satz phasengesteuerter Gruppenantennenelemente empfangen werden, wobei der Schritt des Erzeugens von Teilstrahldaten (15) das Multiplizieren der empfangenen digitalisierten Proben (12) mit entsprechenden digitalen Strahlkoeffizienten (11) umfasst, unter Verwendung eines Satzes von Multiplizierern und Hinzufügen entsprechender multiplizierter Proben unter Verwendung eines zweiten Addierers, um 50 55

die Teilstrahldaten (15) zu erzeugen.

12. Verfahren nach Anspruch 11, welches weiter folgende Schritte umfasst:
 - Aufteilen der digitalisierten Proben der Sätze von phasengesteuerten Gruppenantennenelementen in eine Vielzahl von N digitalisierten Probensätzen;
 - Erzeugen von Teilstrahldaten unter Verwendung von N Prozessoren, die kommunikativ in einer Ringstruktur verbunden sind, wobei jeder Prozessor einen entsprechenden digitalisierten Probensatz verarbeitet;
 - Empfangen, an jedem Prozessor, von Zwischenstrahldaten von einem vorhergehenden Prozessor in dem Ring;
 - Erzeugen, durch jeden Prozessor, von neuen Zwischenstrahldaten durch Addieren der an jedem Prozessor empfangenen Zwischenstrahldaten zu entsprechenden, von dem Prozessor erzeugten Teilstrahldaten; und
 - Übertragen aller neuen Daten des Zwischenstrahls an den nachfolgenden Prozessor im Ring.
13. Verfahren nach Anspruch 12, weiter umfassend das Erzeugen von Endstrahldaten durch Ausführen der folgenden Schritte:
 - Hinzufügen von an einem Prozessor empfangenen Zwischenstrahldaten zu entsprechenden Teilstrahldaten, die von dem Prozessor erzeugt werden, wobei die Zwischenstrahldaten auf entsprechenden Teilstrahldaten basieren, die von allen anderen Prozessoren im Ring erzeugt werden; und
 - Entscheiden, ob die hinzugefügten Zwischenstrahldaten vollständig sind und als Endstrahldaten anstelle von Zwischenstrahldaten übertragen werden können.
14. Verfahren nach Anspruch 13, welches weiter einen Schritt des Durchführens einer zusätzlichen Verarbeitung der Endstrahldaten umfasst.
15. Verfahren nach Anspruch 14, weiter umfassend das Erkennen eines Fehlers in der Leistung eines bestimmten Prozessors in der Ringstruktur, und das Weiterleiten der Zwischendaten und der Enddaten, die von einem vorhergehenden Prozessor im Ring übertragen werden, an einen nachfolgenden Prozessor im Ring.
16. Computerprogrammprodukt zum Verarbeiten digitalisierter Proben (12) eines Satzes phasengesteuerter Gruppenantennenelemente, wobei das Computerprogrammprodukt computerlesbaren Code um-

fasst, der bewirkt, dass ein Prozessor

(2) die folgenden Schritte ausführt:

Erzeugen von Teilstrahl-
daten (15) unter Verwen-
dung eines Prozessors (2), der digitalisierte Proben
(12) verarbeitet, die von einem Satz phasengesteu-
erter Gruppenantennenelemente empfangen wer-
den;

- Empfangen, an dem Prozessor, von Zwischen-
strahl-
daten (44a) von einem anderen Prozes-
sor, der digitalisierte Proben verarbeitet, die von
einem anderen Satz phasengesteuerter Grup-
penantennenelemente empfangen werden;

- Erzeugen neuer Zwischenstrahl-
daten (44a)
durch Addieren der Teilstrahl-
daten (15) zu den
entsprechenden empfangenen Zwischenstrahl-
daten (44a) unter Verwendung eines ersten Ad-
dierers (6); und

- Übertragen der neuen Zwischenstrahl-
daten (44a) an einen weiteren Prozessor, der digitali-
sierte Proben verarbeitet, die von einem weite-
ren Satz von Gruppenantennenelementen mit
phasengesteuertem Gruppenantennenelement
empfangen werden,

wobei der Schritt des Erzeugens von Teilstrahl-
daten (15) das Multiplizieren der empfangenen digitalisierten
Proben (12) mit entsprechenden digitalen Strahl-
koeffizienten (11) unter Verwendung eines Satzes
von Multiplizierern und das Hinzufügen entspre-
chender multiplizierter Proben unter Verwendung ei-
nes zweiten Addierers umfasst, um Teilstrahl-
daten (15) zu erzeugen.

Revendications

1. Structure de traitement de signal d'antenne réseau à commande de phase (1), comprenant un proces-
seur (2) comprenant une unité de formation de fais-
ceau numérique (5) pour générer des données de
faisceau partielles (15) à partir d'échantillons numé-
risés (12) d'un ensemble d'éléments d'antennes ré-
seau à commande de phase, et dans lequel le pro-
cesseur comprend en outre :

- un premier ensemble de bornes d'entrée (7)
pour recevoir des données de faisceau intermé-
diaires (44a) à partir d'un autre processeur traitant
des échantillons numérisés reçus d'un autre
ensemble d'éléments d'antenne réseau à com-
mande de phase ;
- un premier additionneur (6) pour générer de
nouvelles données de faisceau intermédiaires
en ajoutant des données de faisceau partielles
(15) générées par l'unité de formation de fais-
ceau numérique aux données de faisceau inter-
médiaires reçues correspondantes (44a) ;

- un premier ensemble de bornes de sortie (8)
pour transmettre les nouvelles données de fais-
ceau intermédiaires ;

- un deuxième ensemble de bornes d'entrée (9)
pour recevoir lesdits échantillons numérisés
(12) dudit ensemble d'éléments d'antenne ré-
seau à commande de phase ;

- un troisième ensemble de bornes d'entrée (10)
pour recevoir des coefficients de faisceau nu-
mériques (11) ; et dans laquelle l'unité de for-
mation de faisceau numérique (5) comprend un
ensemble de multiplicateurs pour multiplier les-
dits échantillons numérisés reçus (12) avec des
coefficients de faisceau numérique reçus cor-
respondants (11) ; et un second additionneur
pour ajouter des échantillons multipliés corres-
pondants afin de générer lesdites données de
faisceau partielles (15).

2. Structure selon la revendication 1, dans laquelle les
données de faisceau partielles et les données de
faisceau intermédiaires comprennent des données
relatives à plusieurs faisceaux numériques.

3. Structure selon l'une quelconque des revendications
précédentes, comprenant un nombre multiple de
processeurs connectés en communication dans une
structure en boucle.

4. Structure selon la revendication 3, dans laquelle le
premier ensemble de bornes d'entrée d'un proces-
seur particulier est connecté au premier ensemble
de bornes de sortie d'un processeur précédent dans
la boucle, et dans laquelle le premier ensemble de
bornes de sortie du processeur particulier est con-
necté au premier ensemble de bornes d'entrée d'un
processeur ultérieur dans la boucle.

5. Structure selon la revendication 3 ou 4, dans laquelle
chacun des processeurs est agencé pour traiter des
échantillons numérisés d'un ensemble correspon-
dant d'éléments d'antenne réseau à commande de
phase.

6. Structure selon l'une quelconque des revendications
3 à 5, dans laquelle chaque processeur contient le
même nombre de bornes d'entrée dans le second
ensemble de bornes d'entrée.

7. Structure selon l'une quelconque des revendications
3 à 6, comprenant en outre une unité centrale, inclu-
se dans l'anneau, pour recevoir des données de fais-
ceau finales (44b).

8. Structure selon l'une quelconque des revendications
3 à 7, dans laquelle les processeurs comprennent
en outre un quatrième ensemble de bornes d'entrée
et un second ensemble de bornes de sortie pour

recevoir et transmettre, respectivement, des données de faisceau finales (44b).

9. Structure selon l'une quelconque des revendications 3 à 8, dans laquelle le premier additionneur dans chaque processeur est agencé pour générer des données de faisceau finales (44b) en ajoutant des données de faisceau intermédiaires reçues à des données de faisceau partielles correspondantes générées par l'unité de formation de faisceau numérique, dans laquelle les données de faisceau intermédiaires sont basées sur des données de faisceau partielles correspondantes générées par tous les autres processeurs de la boucle. 5 10
10. Structure selon l'une quelconque des revendications 3 à 9, dans laquelle les processeurs sont identiques. 15
11. Procédé de traitement d'échantillons numérisés (12) d'un ensemble d'éléments d'antenne réseau à commande de phase, comprenant les étapes consistant à : 20

- générer des données de faisceau partielles (15) en utilisant un processeur (2) traitant des échantillons numérisés (12) reçus à partir d'un ensemble d'éléments d'antenne réseau à commande de phase ; 25
- recevoir, au niveau du processeur (2), des données de faisceau intermédiaires (44a) provenant d'un autre processeur, traitant des échantillons numérisés reçus d'un autre ensemble d'éléments d'antenne réseau à commande de phase ; 30
- générer de nouvelles données de faisceau intermédiaires (44a) en ajoutant les données de faisceau partielles (15) aux données de faisceau intermédiaires reçues correspondantes (44a), en utilisant un premier additionneur (6) ; et 35
- transmettre les nouvelles données de faisceau intermédiaires (44a) à encore un processeur supplémentaire traitant des échantillons numérisés reçus d'un ensemble supplémentaire d'éléments d'antenne réseau à commande de phase, 40

dans lequel l'étape de génération de données de faisceau partielles (15) comprend la multiplication desdits échantillons numérisés reçus (12) avec des coefficients de faisceau numériques correspondants (11) en utilisant un ensemble de multiplicateurs, et l'ajout d'échantillons multipliés correspondants, en utilisant un second additionneur, afin de générer lesdites données de faisceau partielles (15). 50

12. Procédé selon la revendication 11, comprenant en outre les étapes consistant à : 55

- diviser les échantillons numérisés des ensembles d'éléments d'antenne réseau à commande de phases en un nombre multiple de N ensembles d'échantillons numérisés ;
- générer des données de faisceau partielles en utilisant N processeurs connectés en communication dans une structure en boucle, chaque processeur traitant un ensemble d'échantillons numérisés correspondant ;
- recevoir, au niveau de chaque processeur, des données de faisceau intermédiaires provenant d'un processeur précédent dans la boucle ;
- générer, via chaque processeur, de nouvelles données de faisceau intermédiaires en ajoutant les données de faisceau intermédiaires qui sont reçues au niveau de chaque processeur aux données de faisceau partielles correspondantes générées par ledit processeur ; et
- transmettre toutes les nouvelles données de faisceau intermédiaires au processeur suivant dans la boucle.

13. Procédé selon la revendication 12, comprenant en outre la génération de données de faisceau finales en effectuant les étapes consistant à : 25

- ajouter des données de faisceau intermédiaires reçues au niveau d'un processeur aux données de faisceau partielles correspondantes générées par le processeur, dans lequel les données de faisceau intermédiaires sont basées sur des données de faisceau partielles correspondantes générées par tous les autres processeurs de la boucle ; et
- décider si les données de faisceau intermédiaires ajoutées sont complètes et peuvent être transférées en tant que données de faisceau finales au lieu de données de faisceau intermédiaires. 35 40

14. Procédé selon la revendication 13, comprenant en outre une étape consistant à effectuer un traitement supplémentaire sur les données de faisceau finales. 45

15. Procédé selon la revendication 14, comprenant en outre la détection d'un défaut de performance d'un processeur spécifique dans la structure en boucle, et l'envoi des données intermédiaires et des données finales transmises par un processeur précédent dans la boucle, à un processeur suivant dans la boucle. 50

16. Produit programme informatique destiné à traiter des échantillons numérisés (12) d'un ensemble d'éléments d'antenne réseau à commande de phase, le produit programme informatique comprenant un code lisible par ordinateur amenant un processeur (2) à effectuer les étapes consistant à : 55

- générer des données de faisceau partielles (15) en utilisant un processeur (2) traitant des échantillons numérisés (12) reçus à partir d'un ensemble d'éléments d'antenne réseau à commande de phase ; 5
- recevoir, au niveau du processeur, des données de faisceau intermédiaires (44a) provenant d'un autre processeur traitant des échantillons numérisés reçus à partir d'un autre ensemble d'éléments d'antenne réseau à commande de phase ; 10
- générer de nouvelles données de faisceau intermédiaires (44a) en ajoutant les données de faisceau partielles (15) aux données de faisceau intermédiaires reçues correspondantes (44a), en utilisant un premier additionneur (6) ; et 15
- transmettre les nouvelles données de faisceau intermédiaire (44a) à encore un processeur supplémentaire traitant des échantillons numérisés reçus à partir d'un autre ensemble d'éléments d'antenne réseau à commande de phase, 20

dans lequel l'étape de génération de données de faisceau partielles (15) comprend la multiplication desdits échantillons numérisés reçus (12) avec des coefficients de faisceau numérique correspondants (11), en utilisant un ensemble de multiplicateurs, et l'ajout d'échantillons multipliés correspondants, en utilisant un second additionneur, afin de générer lesdites données de faisceau partielles (15). 25 30

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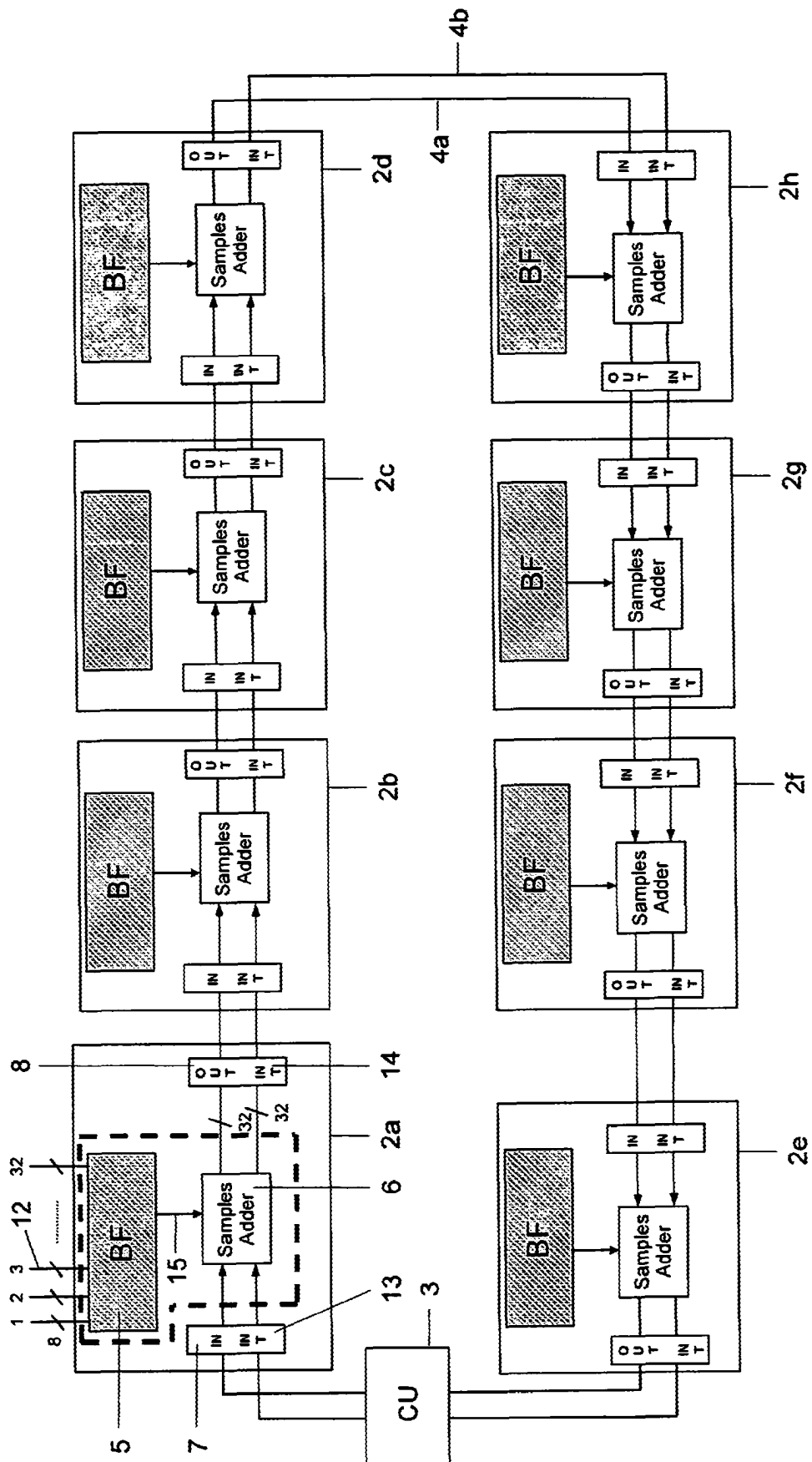


Fig. 1

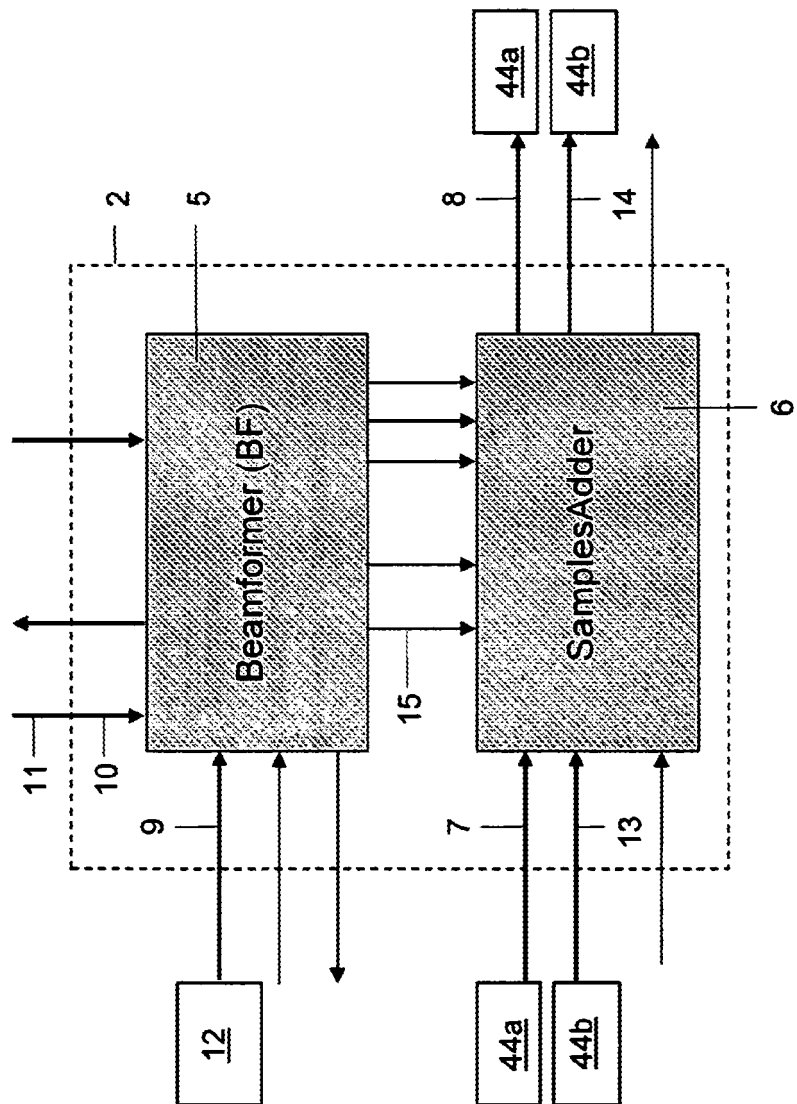


Fig. 2

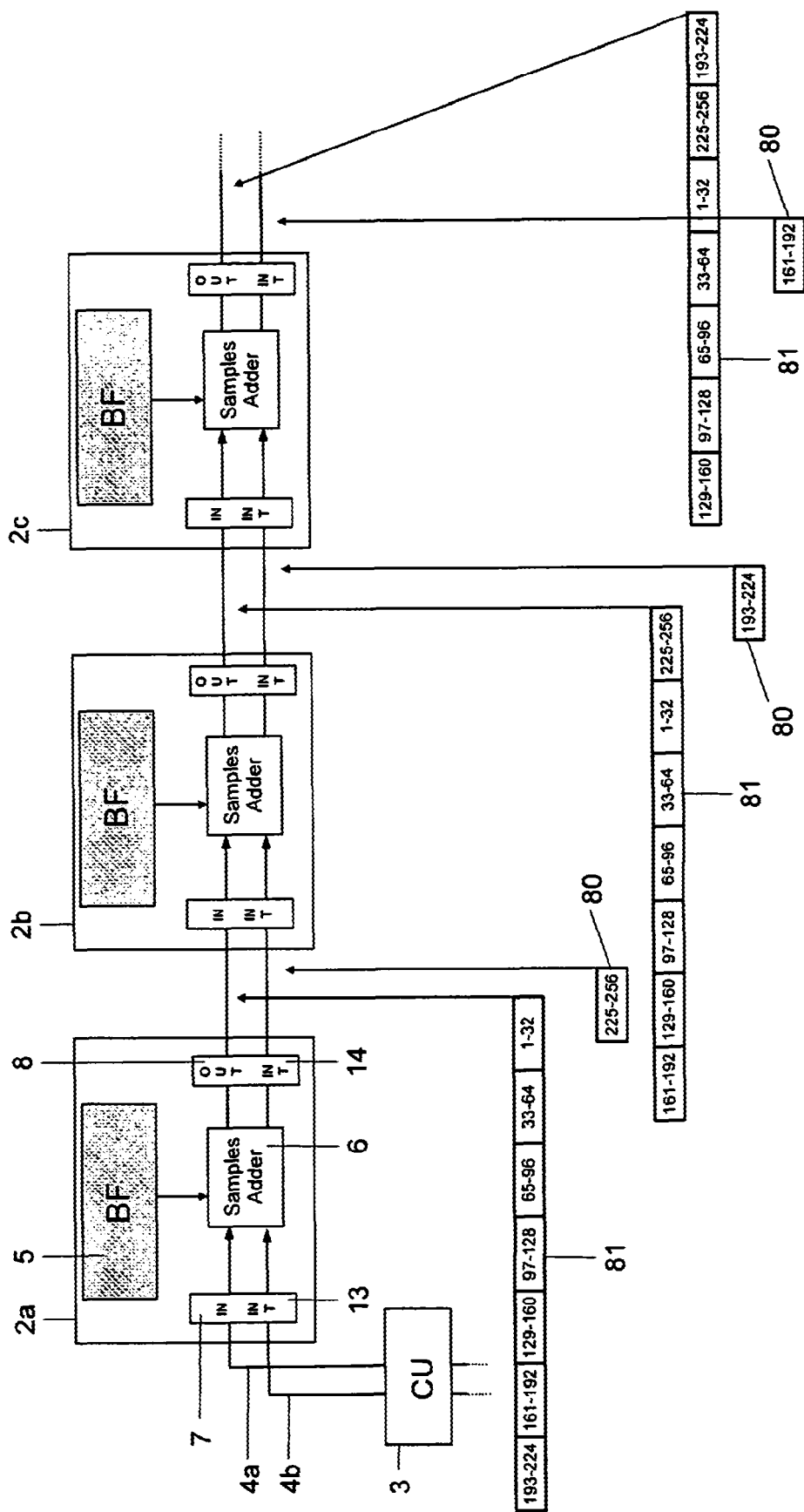


Fig. 3

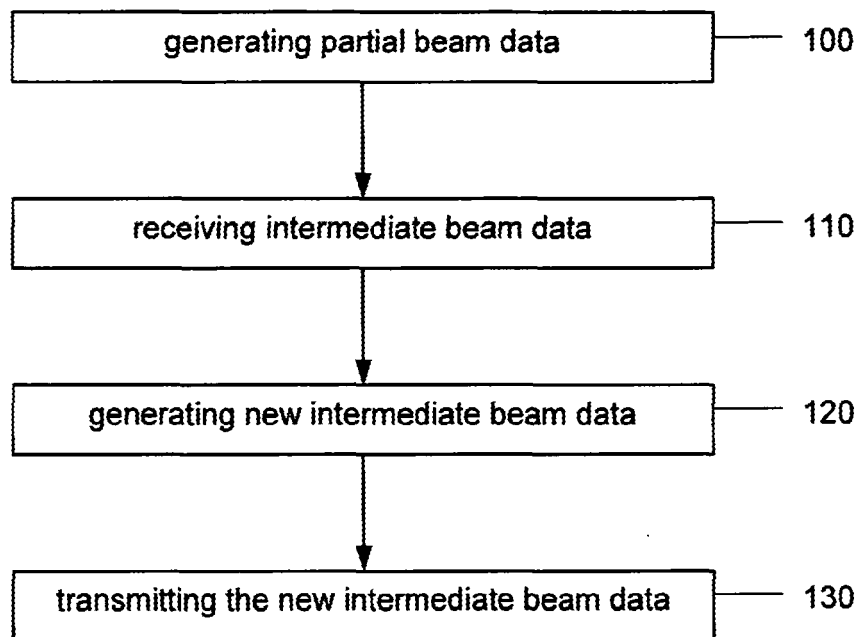


Fig. 4

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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