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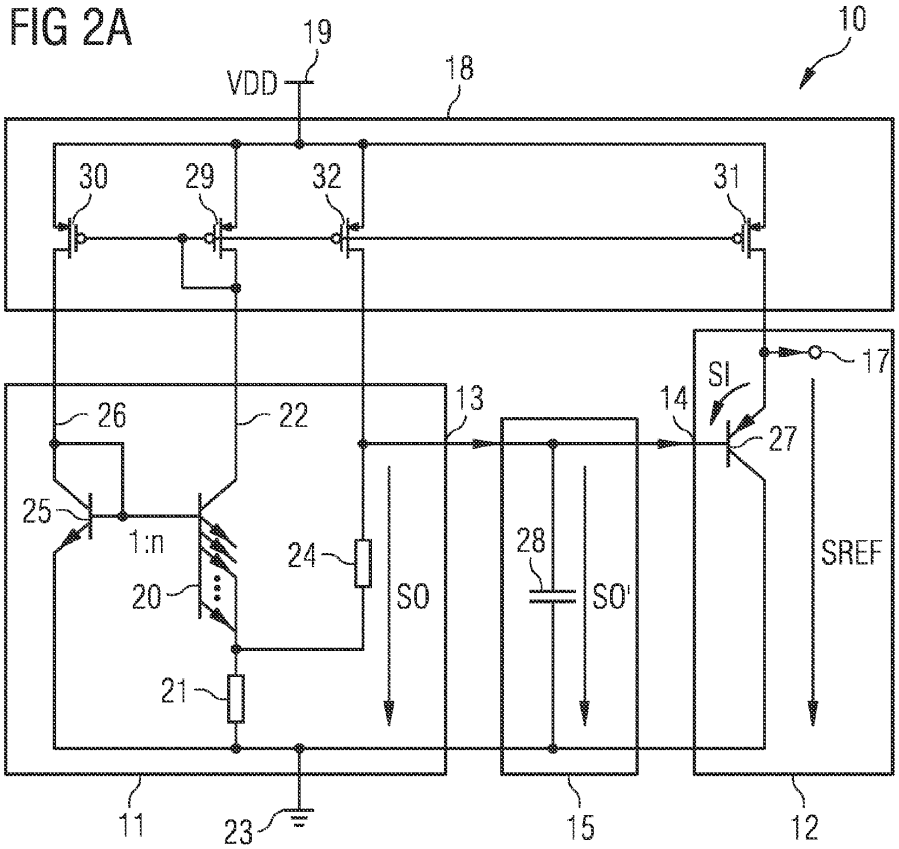
(54) Signal generator and method for signal generation

(57) A signal generator (10) comprises a signal source (11) that is configured for generating a source signal (SO) and a buffer (12, 56). The buffer (12, 56) is configured for generating an internal signal (SI) and for generating a reference signal (SREF, SBG) by summing the internal signal (SI) to the source signal (SO) or to a signal (SO') derived from the source signal (SO). The sign of the temperature coefficient of the source signal (SO) is opposite to the sign of the temperature coefficient of the internal signal (SI).

FIG 2A



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Description

[0001] The present invention is related to a signal generator and to a method for signal generation.

[0002] Integrated circuits often comprise a signal generator which generates a reference signal. The reference signal can be a constant and temperature-independent signal.

[0003] The publication "A simple three-terminal IC bandgap reference", A. Brokaw, IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, 1974, pp. 388-393, describes a reference circuit which generates a voltage signal that is independent from the temperature.

[0004] In the publication "A low-voltage CMOS bandgap reference", E. Vittoz et al., IEEE Journal of Solid-State Circuits, Vol. SC-14, No. 3, 1979, pp. 573-577, a voltage source for generating a voltage that is proportional to the absolute temperature and a further voltage which has only a small temperature dependency is described.

[0005] Document US 7,224,210 B2 refers to a voltage reference generator circuit subtracting two currents with different temperature coefficients. Thus, a reference voltage is achieved that has a low temperature coefficient. The circuit is able to drive a small load.

[0006] It is an object of the present application to provide a signal generator and a method for signal generation which can drive a high load.

[0007] This object is solved by a signal generator according to claim 1 and a method for signal generation according to claim 14. Preferred embodiments are presented in the respective dependent claims.

[0008] In an embodiment, a signal generator comprises a signal source and a buffer. The signal source is configured to generate a source signal. The buffer is configured to generate an internal signal and to generate a reference signal by means of summing the internal signal to the source signal or by means of summing the internal signal to a signal that is derived from the source signal. The sign of the temperature coefficient of the source signal is opposite to the sign of the temperature coefficient of the internal signal.

[0009] It is an advantage of the signal generator that the buffer inside the signal generator is able to drive a high load. Since the buffer is used for generating the reference signal by superimposing the internal signal and the source signal or the signal derived from the source signal, respectively, only a small number of transistors are required for the implementation of the signal generator. The signal generator has a high driving ability and can be realized on a small area of a semiconductor body. Due to the small number of transistors, the current consumption of the signal generator is low.

[0010] The signal generator can also be referred to as a reference signal generator. The reference signal can be a constant signal. The reference signal is nearly independent from the temperature.

[0011] In an embodiment, the source signal is proportional to the absolute temperature. The internal signal is complementary to the source signal in relation to the absolute temperature. A signal which is proportional to the absolute temperature can be abbreviated as a PTAT signal. A signal that is complementary to said signal in relation to the absolute temperature can be referred to as a complementary to the absolute temperature signal, abbreviated as a CTAT signal. The source signal is a PTAT signal, whereas the internal signal is the corresponding CTAT signal. The source signal is inversely proportional to the temperature in comparison to the internal signal.

[0012] In an alternative embodiment, the source signal is a linear or quadratic function of the temperature. The source signal can be a polynomial function of the temperature.

[0013] In an embodiment, the internal signal is a linear or quadratic function of the temperature. The internal signal can be a polynomial function of the temperature.

[0014] In an embodiment, the source signal has a positive temperature coefficient and the internal signal has a negative temperature coefficient. Alternatively, the source signal has a negative temperature coefficient and the internal signal has a positive temperature coefficient. By superimposing the source signal and the internal signal, a reference signal is achieved with a nearly zero temperature coefficient. The amount of the temperature coefficient of the source signal and the amount of the temperature coefficient of the internal signal are approximately equal.

[0015] In an embodiment, the source signal and the internal signal are summed up in voltage mode for the generation of the reference signal. The internal signal is superimposed on top of the source signal. The source signal is a voltage with reference to the reference potential terminal. The internal signal is a voltage that is added on top of the source signal. The source signal and the internal signal have the same signs.

[0016] In an embodiment, the source signal and the internal signal are voltage signals. The reference signal is the sum of the source signal and the internal signal or the sum of the signal derived from the source signal and the internal signal.

[0017] In an embodiment, the signal source comprises an output for providing the source signal. The output of the signal source is coupled to an input of the buffer. The internal signal is generated with reference to the input of the buffer. The source signal is tapped off at the input of the buffer. The output of the signal source can directly be connected to the input of the buffer.

[0018] Alternatively, the signal generator comprises a low-pass filter that couples the output of the signal source to the input of the buffer. Advantageously, an improved noise performance of the signal generator is achieved by the low-pass filter.

[0019] In an alternative embodiment, the signal generator comprises a further buffer that couples the output of the signal source to the input of the buffer. Preferably, the output of the signal source is coupled via the low-

pass filter to the further buffer and the further buffer is connected to the input of the buffer. The filter and/or the further buffer generate the signal which is derived from the source signal. The signal derived from the source signal is generated by filtering, buffering and/or amplification of the source signal.

[0020] In an embodiment, the sign of the temperature coefficient of the signal derived from the source signal is opposite to the sign of the temperature coefficient of the internal signal. The amount of the temperature coefficient of the signal derived from the source signal and the amount of the temperature coefficient of the internal signal are approximately equal.

[0021] In an embodiment, the internal signal is added on top of the signal that is derived from the source signal. The signal that is derived from the source signal is a voltage with reference to a reference potential terminal.

[0022] In an embodiment, the buffer comprises a buffer transistor. The buffer transistor can be a bipolar transistor. The buffer transistor may be operated in an emitter-follower configuration.

[0023] Alternatively, the buffer transistor is implemented as a field-effect transistor. Thus, the buffer transistor may be operated in a source-follower configuration.

[0024] In an embodiment, the buffer transistor has a control terminal which is coupled to the input of the buffer. Furthermore, a first terminal of the buffer transistor may be connected to an output of the buffer. At the output of the buffer, the reference signal is provided.

[0025] In an embodiment, the internal signal is a voltage between the control terminal and the first terminal of the buffer transistor. In case of the buffer transistor being a bipolar transistor, the internal signal usually has a negative temperature coefficient.

[0026] In an embodiment, the signal source comprises a first source transistor and a first resistor. A first current path comprises a controlled section of the first source transistor and the first resistor. The first current path is arranged between a supply voltage terminal and a reference potential terminal. A node between the controlled section of the first source transistor and the first resistor is coupled to the output of the signal source.

[0027] In a further development, the signal source comprises a second resistor. The second resistor couples the output of the signal source to the node between the controlled section of the first source transistor and the first resistor. The second resistor may be implemented for scaling of the PTAT coefficient of the source signal. Since the second resistor is separated in another branch in comparison to the first current path, more headroom for the first source transistor is achieved. This results in an improvement of the power-supply rejection ratio, abbreviated PSRR.

[0028] In an embodiment, the signal source comprises a second source transistor. The second source transistor controls the first source transistor. The second source transistor is designed such that the second source transistor has a smaller current driving capability in comparison to the first source transistor. A second current path of the signal source comprises a controlled section of the second source transistor and is arranged between the supply voltage terminal and the reference potential terminal. A first terminal of the second source transistor is connected to a control terminal of the second source transistor and to a control terminal of the first source transistor.

[0029] In an embodiment, the signal generator comprises a current mirror that couples the signal source to the supply voltage terminal as well as the buffer to the supply voltage terminal. The current mirror generates at least one current for the signal source and at least one current for the buffer. The current mirror controls the current in the first and second current path of the signal source and of the current flowing through the controlled section of the buffer transistor. Advantageously, the current supply for the signal source and the current supply for the buffer are controlled in common by the current mirror.

[0030] In a further development, the signal generator comprises a current generator and a current source. The current generator generates a first signal. The current generator may be coupled to the buffer. The current source generates a second signal. The current source may be coupled to the current mirror. The sign of the temperature coefficient of the first signal is opposite to the sign of the temperature coefficient of the second signal. The second signal may be proportional to the absolute temperature. The first signal may be complementary to the second signal in relation to the absolute temperature. The second signal is a PTAT signal and the first signal is a CTAT signal. An output of the current generator and an output of the current source are connected to a reference current output. A reference output signal is flowing through the reference current output. The reference output signal is the sum of the first and the second signal. The first, the second and the reference output signal are realized as currents.

[0031] In an embodiment, the buffer comprises an output, a first output and a voltage divider that is connected to the output. The first output of the buffer is connected to a tap of the voltage divider. The reference signal can be tapped at the output of the buffer. A first reference signal is provided at the first output of the buffer.

[0032] In an embodiment, the signal generator is realized as a universal voltage/current reference generator which has no application limitation and can be used in any type of analog circuits.

[0033] In an embodiment, the signal generator is realized as a mixed bipolar transistor/field-effect transistor circuit. The signal generator is fabricated by a BiCMOS technology.

[0034] In an embodiment, a method for signal generation comprises generating a source signal and generating an internal signal. Furthermore, a reference signal is generated by adding the internal signal and the source signal or by adding the internal signal and a signal which

is derived from the source signal. A buffer generates the internal signal and the reference signal. The sign of the temperature coefficient of the source signal is opposite to the sign of the temperature coefficient of the internal signal.

[0035] Advantageously, the buffer is designed such as to drive a high load. Since the buffer in addition is able to provide the internal signal and to superimpose the internal signal and the source signal, the method for signal generation can be implemented with a small number of transistors.

[0036] The following description of figures of exemplary embodiments may further illustrate and explain the invention. Devices and circuit blocks with the same structure and the same effect, respectively, appear with equivalent reference symbols. In so far as circuit blocks or devices correspond to one another in terms of their function in different figures, the description thereof is not repeated for each of the following figures.

FIG. 1 shows an exemplary embodiment of a block diagram of a signal generator according to the principle presented and

FIGs. 2A and 2B show exemplary embodiments of a signal generator according to the principle presented.

[0037] FIG. 1 shows an exemplary embodiment of a block diagram of a signal generator 10 according to the principle presented. The signal generator 10 comprises a signal source 11 and a buffer 12. An output 13 of the signal source 11 is coupled to an input 14 of the buffer 12. Moreover, the signal generator 10 comprises a low-pass filter 15 that is arranged between the output 13 of the signal source 11 and the input 14 of the buffer 12. Further on, a further buffer 16 of the signal generator 10 is arranged between the low-pass filter 15 and the input 14 of the buffer 12. The further buffer 16 may be implemented as a low-cost buffer.

[0038] The signal source 11 generates a source signal SO with a first temperature coefficient. The source signal SO is proportional to the absolute temperature. The source signal SO can be named as a PTAT signal. The source signal SO is filtered by the low-pass filter 15, buffered by the further buffer 16 and provided to the input 14 of the buffer 12. Thus, a derived source signal SO' which is derived from the source signal SO by means of the low-pass filter 15 and the further buffer 16 is provided to the input 14 of the buffer 12. The buffer 12 internally generates an internal signal SI with a second temperature coefficient. The first and the second temperature coefficients have opposite signs. The internal signal SI is complementary to the source signal SO in relation to the absolute temperature. The internal signal SI can be named as a CTAT signal. The source signal SO and the internal signal SI have the form of voltages. The source signal SO and the internal signal SI are superimposed by the buffer 12 such that a reference signal SREF is provided by the buffer 12 at an output 17 of the buffer 12.

[0039] The signal generator 10 is implemented as a band gap reference. The signal generator 10 is realized as a reference signal generator. The reference signal SREF has the form of a voltage. The reference signal SREF is constant and nearly independent from the temperature. Since the signal generator 10 for the realization of the bandgap voltage reference comprises the generation of a voltage with a PTAT coefficient and of a voltage having a CTAT coefficient, the two circuit blocks for generation of the different temperature coefficients can be separated. The voltage having the CTAT coefficient is generated in a buffering manner, such that a strong driving ability is achieved. Therefore, an additional buffer is not needed. The buffer 12 incorporates the property of a good line regulation to obtain satisfactory PSRR so that the PSRR of the signal generator 10 is good.

[0040] The low-pass filter 15 advantageously can be inserted between the PTAT and CTAT circuit block to improve the noise performance. Since it only needs to filter out the noise from the signal source 11, the design of the low-pass filter 15 is less demanding.

[0041] In an alternative, not shown embodiment, the signal generator 10 does not comprise the further buffer 16. The low-pass filter 15 is directly connected to the input 14 of the buffer 12.

[0042] In an alternative, not shown embodiment, the signal generator 10 does not comprise the low-pass filter 15. Thus, the output 13 of the signal source 11 is directly connected to the further buffer 16.

[0043] In an alternative, not shown embodiment, the signal generator 10 does not comprise the low-pass filter 15 and the further buffer 16. Thus, the output 13 of the signal source 11 is directly connected to the input 14 of the buffer 12.

[0044] FIG. 2A shows an exemplary embodiment of the signal generator 10 according to the principle presented, which is a further development of the block diagram of the signal generator of FIG. 1. The signal generator 10 comprises a current mirror 18 which connects the signal source 11 to a supply voltage terminal 19. The current mirror 18 also connects the buffer 12 to the supply voltage terminal 19.

[0045] The signal source 11 comprises a first source transistor 20 and a first resistor 21. A first current path 22 comprises the first source transistor 20 and the first resistor 21. The first current path 22 is arranged between the current mirror 18 and a reference potential terminal 23. The output 13 of the signal source 11 is connected to a node between the first source transistor 20 and the first resistor 21. Furthermore, the signal source 11 comprises a second resistor 24 which couples the output 13 of the signal source 11 to the node between the first source transistor 20 and the first resistor 21. Further on, the signal source 11 comprises a second source transistor 25. The second source transistor 25 is arranged in a

second current path 26 of the signal source 11. The second current path 26 couples the current mirror 18 to the reference potential terminal 23. A first terminal of the second source transistor 25 is connected to a control terminal of the second source transistor 25. The first terminal of the second source transistor 26 is connected to the current mirror 18. A second terminal of the second source transistor 25 is connected to the reference potential terminal 23. Moreover, a control terminal of the second source transistor 25 is connected to a control terminal of the first source transistor 20.

[0046] The buffer 12 comprises a buffer transistor 27. The buffer transistor 27 is a bipolar transistor. The buffer transistor 27 is realized as a PNP transistor. The buffer transistor 27 is operated in an emitter-follower configuration and controlled by the signal source 11. A control terminal of the buffer transistor 27 is coupled to the input 14 of the buffer 12. A first terminal of the buffer transistor 27 is connected to the output 17 of the buffer 12. Further on, the first terminal of the buffer transistor 27 is connected to the current mirror 18. A second terminal of the buffer transistor 27 is connected to the reference potential terminal 23. The buffer transistor 27 is arranged in a current path between the current mirror 18 and the reference potential terminal 23.

[0047] The low-pass filter 15 comprises a filter capacitor 28. The filter capacitor 28 couples the output 13 of the signal source 11 to the reference potential terminal 23. The current mirror 18 comprises a first, a second, a third and a fourth mirror transistor 29 to 32. The first mirror transistor 29 is arranged in the first current path 22 and couples the supply voltage terminal 19 to the first source transistor 20. The second mirror transistor 30 is located in the second current path 26 and couples the supply voltage terminal 19 to the second source transistor 25. The third mirror transistor 31 couples the supply voltage terminal 19 to the buffer 12. The third mirror transistor 31 is arranged in series to the buffer transistor 27. The output 17 of the buffer 12 is connected to a node between the third mirror transistor 31 and the buffer transistor 27. The output 13 of the signal source 11 is connected to a node between the current mirror 18 and the second resistor 24. The fourth mirror transistor 32 is arranged between the supply voltage terminal 19 and the output 13 of the signal source 11. A control terminal of the first mirror transistor 29 is connected to a first terminal of the first mirror transistor 29. The first mirror transistor 29 provides current to the first source transistor 20. The second mirror transistor 30 generates current for the second source transistor 25. The third mirror transistor 31 supplies current for the operation of the buffer transistor 27. Further on, the fourth mirror transistor 32 generates current that mainly flows through the second resistor 24.

[0048] The first and the second source transistors 20, 25 are realized as bipolar transistors. Both transistors are implemented as NPN transistors. The first source transistor 20 has an n-fold current density in comparison to the second source transistor 25. The first source transistor 20 has different dimensions in comparison to the second source transistor 25. The first to the fourth current mirror transistors 29 to 32 are realized as field-effect transistors. The four mirror transistors 29 to 32 are designed as p-channel metal-oxide-semiconductor field-effect transistors. The value of a current that flows through the first current path 22 is equal to the value of a current which flows through the second current path 26.

[0049] A supply voltage VDD is applied to the supply voltage terminal 19. The internal signal SI is generated between the first terminal of the buffer transistor 27 and the control terminal of the buffer transistor 27. The signal generator 10 of FIG. 2A shows a basic circuit realization of a voltage/current reference generator with inherently high PSRR and high driving ability. The first and the second source transistors 20, 25, the first and the second mirror transistors 29, 30 and the first resistor 21 form a basic voltage/current reference generator. The second resistor 24 effects the PTAT coefficient scaling and is separated from the first resistor 21 into another branch to ensure more headroom of first source transistor 20 for PSRR improvement. The CTAT coefficient is acquired by the buffer transistor 27 that is added on top of the PTAT coefficient in a source follower manner.

[0050] Since the output impedance of the buffer transistor 27 is low, the PSRR as well as the driving ability are automatically enhanced. The noise of the signal generator 10 is also low, because the PTAT coefficient generation does not involve any other active regulation for example with an amplifier and the number of noise sources is minimized. The filter capacitor 28 can be added to form a low-pass filtering to further improve the noise performance by utilizing the impedance provided by the drain node of fourth mirror transistor 32 and the second resistor 24.

[0051] The output impedance of the signal generator 10 is low, which offers a high driving ability, fast transient regulation as well as direct access to obtain other reference voltages lower than the typical bandgap voltage of 1.23 V. Consequently, no additional buffer is needed for buffering the reference signal SREF and a significant current and area saving can be acquired. Another advantage is that the signal generator 10 has an inherently high PSRR, even without any other additional regulation techniques. Also, low noise design can be easily achieved. The transient regulation operates fast. The signal generator 10 can be obtained by a simple and compact design.

[0052] In an alternative, not shown embodiment, the first and the second source transistors 20, 25 are implemented as field-effect transistors.

[0053] In an alternative, not shown embodiment, the first to the fourth current mirror transistors 29 to 32 are realized as bipolar transistors.

[0054] In an alternative, not shown embodiment, the buffer transistor 27 is realized as a field-effect transistor. The buffer transistor 27 may be a P-channel metal-oxide-semiconductor field-effect transistor.

[0055] FIG. 2B shows a further exemplary embodiment of a signal generator 10 according to the principle presented, which is a further development of the signal generator shown in FIGs. 1 and 2A. The signal source 11 comprises a first and a second cascode transistor 40, 41. The first cascode transistor 40 is arranged in the first current path 22, whereas the second cascode transistor 41 is arranged in the second current path 26. The first cascode transistor 40 is located between the current mirror 18 and the first source transistor 20. The second cascode transistor 41 is arranged between the second source transistor 25 and the current mirror 18. The first and the second cascode transistors 40, 41 are implemented as field-effect transistors. Moreover, the signal source 11 comprises a third resistor 42 which is arranged in the second current path 26 between the second cascode transistor 41 and the current mirror 18.

[0056] Further on, the signal source 11 comprises a first amplifier 43 that controls the first cascode transistor 40. A first input of the first amplifier 43 is connected to a node between the second source transistor 25 and the second cascode transistor 41. A second input of the first amplifier 43 is connected to a node between the first source transistor 20 and the first cascode transistor 40. A control terminal of the second cascode transistor 41 is connected to a node between the third resistor 42 and the current mirror 18. The control terminals of the first and the second source transistors 20, 25 are connected to a node between the second cascode transistor 41 and the third resistor 42.

[0057] The current mirror 18 is realized as a cascoded current mirror. To each of the first, second, third and fourth mirror transistor 29 to 32, a further mirror transistor is connected in series. Thus, the current mirror 18 comprises a fifth, sixth and seventh mirror transistor 44 to 46. The fifth, sixth and seventh mirror transistors 44 to 46 work as cascode transistors for the first, second and fourth mirror transistors 29, 30, 32. The fifth, sixth and seventh mirror transistors 44 to 46 and the further mentioned mirror transistors are realized as field-effect transistors. The fifth and sixth current mirror transistors 44, 45 are arranged in the first and the second current path 22, 26. Moreover, the current mirror 18 comprises a mirror resistor 47 that is integrated in the first current path 22. The fifth mirror transistor 44 is connected to the first mirror transistor 29, whereas the mirror resistor 47 is connected to the first cascode transistor 40. The control terminal of the first mirror transistor 29 is connected to a node between the fifth mirror transistor 44 and the mirror resistor 47. A control terminal of the fifth mirror transistor 44 is connected to a node between the mirror resistor 47 and the first cascode transistor 40. The sixth mirror transistor 45 is arranged between the second mirror transistor 30 and the third resistor 42.

[0058] The current mirror 18 comprises a second amplifier 48 which controls the sixth mirror transistor 45. A first input of the second amplifier 48 is connected to a node between the first and the fifth mirror transistor 29, 44, whereas a second input of the second amplifier 48 is connected to a node between the second and the sixth mirror transistor 30, 45.

[0059] The low-pass filter 15 comprises a filter resistor 49 which is arranged between the output 13 of the signal source 11 and the filter capacitor 28. A node between the filter resistor 49 and the filter capacitor 28 is coupled to the input 14 of the buffer 12. The filter resistor 49 and the filter capacitor 28 form a low-pass RC filter.

[0060] Moreover, the signal generator 10 comprises the further buffer 16. The further buffer 16 is realized in the form of a differential amplifier. The further buffer 16 is connected via the current mirror 18 to the supply voltage terminal 19. Thus, the current mirror 18 comprises an eighth and a ninth mirror transistor 50, 51 which are connected as cascode transistors. The further buffer 16 comprises a first to a fourth amplifier transistor 52 to 55. The first to fourth amplifier transistors 52 to 55 are implemented as field-effect transistors .The output 13 of the signal source 11 is coupled via the low-pass filter 15 to a control terminal of the first amplifier transistor 52. The first and the second amplifier transistors 52, 53 are connected in series. The second and the third amplifier transistors 53, 54 are arranged in the form of a current mirror. The third and the fourth amplifier transistors 54, 55 are connected in series.

[0061] The series connection of the first and the second amplifier transistors 52, 53 is arranged in parallel to the series connection of the third and the fourth amplifier transistors 54, 55. A node between the third amplifier transistor 54 and the fourth amplifier transistor 55 is connected to the input 14 of the buffer 12 and, in addition, also to a control terminal of the fourth amplifier transistor 54. A current that flows through the first amplifier transistor 52 is mirrored into a current flowing through the fourth amplifier transistor 55. The first to the fourth amplifier transistors 52 to 55 implement a small buffer biased with very low current.

[0062] The signal generator 10 comprises an additional buffer 56. The output 13 of the signal source 11 is coupled via an input 14' of the additional buffer 56 to a control terminal of a first buffer transistor 57. A first terminal of the first buffer transistor 57 is connected via a second buffer transistor 58 to the supply voltage terminal 19. The first terminal of the first buffer transistor 57 is coupled to an additional output 64 of the additional buffer 56. A control terminal of the second buffer transistor 58 is coupled via a buffer capacitor 59 to the reference potential terminal 23. A second terminal of the first buffer transistor 57 is connected via a third buffer transistor 60 to the reference potential terminal 23. A fourth buffer transistor 61 is arranged between the third buffer transistor 60 and the current mirror 18. The second terminal of the first buffer transistor 57 is connected to a node between the third and the fourth buffer transistors 60, 61. The second buffer transistor 58 has a control terminal that is connected to a node between the current mirror 18 and the fourth buffer transistor 61.

[0063] Moreover, the additional buffer 56 comprises a buffer resistor 62 and a fifth buffer transistor 63 that are connected in series. The third and the fifth buffer transistors 60, 63 form a current mirror. The buffer resistor 62 connects the fifth buffer transistor 63 to the current mirror 18. The additional output 64 is connected to the node between the first and the second buffer transistor 57, 58. A load capacitor 65 couples the additional output 64 to the reference potential terminal 23.

[0064] The current mirror 18 comprises a tenth, eleventh, twelfth and thirteenth mirror transistor 66 to 69. Hence, the eleventh mirror transistor 67 is arranged in cascode form to the tenth mirror transistor 66 such that it provides a current to the third and the fourth buffer transistor 60, 61. The eleventh and the twelfth mirror transistor 68, 69 are also arranged in cascode form and provide a current to the series circuit of the buffer resistor 62 and the fifth buffer transistor 63. The first buffer transistor 57 is realized as a bipolar transistor. The bipolar transistor is a PNP bipolar transistor. The second to the fifth buffer transistors 58, 60, 61, 63 are designed as field-effect transistors.

[0065] The current mirror 18 comprises a fourteenth mirror transistor 70 which is arranged in cascode form to the fourth mirror transistor 31. The fourth mirror transistor 31 and fourteenth mirror transistor 70 provide a current to the buffer transistor 27. The buffer 12 comprises a voltage divider 71. The voltage divider 71 couples the output 17 of the buffer 12 to the reference potential terminal 23. The voltage divider 71 has at least a first and a second divider resistor 72, 73 which are connected in series. A first output 74 of the buffer 12 is connected to a node between the first and the second divider resistors 72, 73. A third divider resistor 75 is connected in series to the first and the second voltage divider resistors 72, 73. A second output 76 of the buffer 12 is connected to a node between the second and the third divider resistors 73, 75. A fourth divider resistor 77 is arranged between the third divider resistor 75 and the reference potential terminal 23. A third output 78 of the buffer 12 is connected to a node between the third and the fourth divider resistors 75, 77.

[0066] In addition, the signal generator 10 comprises a current source 80 which connects the supply voltage terminal 19 to a reference current output 81. The current source 80 is connected to the current mirror 18. The current source 80 has a first and a second current source transistor 82, 83 which are connected in series and are controlled by the current mirror 18. The first current source transistor 82 has a control terminal connected to the control terminal of the first mirror transistor 29. Furthermore, a control terminal of the second current source transistor 83 is connected to the control terminal of the fifth mirror transistor 44. The first and the second current source transistors 82, 83 are implemented as field-effect transistors.

[0067] Moreover, the signal generator 10 comprises a current generator 84 which couples the supply voltage terminal 19 to the reference current output 81. The current generator 84 comprises a first and a second generator transistor 85, 86 that are connected in series and arranged between the supply voltage terminal 19 and the reference current output 81. The first generator transistor 85 is connected to the supply voltage terminal 19 and the second generator transistor 86 is connected to the reference current output 81. A control terminal of the second generator transistor 86 is connected to a control terminal of the fifth mirror transistor 44. A control terminal of the first generator transistor 85 is coupled to an output of the additional buffer 56. For this reason, the control terminal of the first generator transistor 85 is coupled to the control terminal of the third buffer transistor 60.

[0068] A series circuit of a third and a fourth generator transistor 87, 88 of the current generator 84 couples the supply voltage terminal 19 to the reference potential terminal 23. The control terminal of the first generator transistor 85 is connected to a node between the third and the fourth generator transistor 87, 88. A control terminal of the fourth generator transistor 88 is connected to the control terminal of the third buffer transistor 60. A fifth, sixth and seventh generator transistor 89 to 91 as well as a generator resistor 92 are arranged in series and couple the supply voltage terminal 19 to the reference potential terminal 23. The node between the third and the fourth generator transistors 87, 88 is also connected to a control terminal of the fifth generator transistor 89. A node between the sixth and the seventh current generator transistor 90, 91 is connected to a control terminal of the third generator transistor 87. Moreover, the current generator 84 comprises an eighth generator transistor 93 that couples the current mirror 18 to the reference potential terminal 23.

[0069] The current mirror 18 comprises a fifteenth and a sixteenth mirror transistor 94, 95 that are arranged in cascode form and provide a current to the eighth generator transistor 93. A current generator capacitor 96 of the current generator 84 couples a control terminal of the eighth generator transistor 93 to the reference potential terminal 23. The control terminal of the eighth generator transistor 93 is connected to a node between the seventh generator transistor 91 and the current generator resistor 92. A control terminal of the seventh generator transistor 91 is connected to a node between the eighth generator transistor 93 and the current mirror 18. A control terminal of the sixth generator transistor 90 is connected to the control terminal of the fifth mirror transistor 44. The current generator 84 is realized as a CTAT current generator. The first to the seventh generator transistors 85 to 91 are designed as field-effect transistors. The eighth generator transistor 93 is implemented as a bipolar transistor.

[0070] The source signal SO having the PTAT voltage component is obtained at the drain of seventh mirror transistor 46. The source signal SO is filtered by the low-pass filter 15 and buffered by the further buffer 16 and provided to the input 14' of the additional buffer 56 and to the input

14 of the buffer 12 in the form of the derived source signal SO'. The derived source signal SO' is realized as a voltage. The amplification factor provided by the further buffer 16 is approximately 1. Since the buffer 12 for the realization of the CTAT coefficient is implemented by the PNP bipolar transistor 27, the further buffer 16 can be added as a small low-cost buffer in order to eliminate the load to the signal source 11 which is created by the base impedance of the buffer transistor 27. Most of the time, the beta of the PNP bipolar buffer transistor 27 is large enough such that the further buffer 16 can optionally be omitted. Besides, since no load regulation is required at that node, the further buffer 16 only needs to provide an impedance transfer, hence the further buffer 16 can operate with a small current value.

[0071] The additional buffer 56 generates an additional reference signal SBG. The additional reference signal SBG has the form of a voltage. The first buffer transistor 57 offers the CTAT voltage component such that the additional reference signal SBG is generated. The additional reference signal SBG effects as a bandgap voltage. The first buffer transistor 57 is a PNP bipolar transistor. The internal signal SI is generated between the first terminal of the first buffer transistor 57 and the control terminal of the first buffer transistor 57. The first buffer transistor 57 is embedded in a flipped-voltage-follower configuration composed by the second, third and fourth buffer transistors 58, 60, 61 as well as the tenth and eleventh mirror transistors 66, 67, in which the fourth buffer transistor 61 acts as a current buffer and provides a voltage level shifting, as well as an enhancement of PSRR, as the supply voltage VDD is isolated from the first buffer transistor 57. The buffer capacitor 59 is a compensation capacitor. The load capacitor 65 represents the load. This flipped-voltage-follower serves as a buffer, which offers a high transient class-AB output current for fast load regulation. Besides, the low impedance at the emitter of the first buffer transistor 57 makes the driving ability of the additional reference signal SBG strong.

[0072] The buffer 12 not only generates the reference signal SREF, but also a first, a second and a third reference signal SREF1, SREF2, SREF3 at the first, second and third outputs 74, 76, 78 of the buffer 12 by means of the voltage divider 71. The first, second and third reference signals SREF1, SREF2, SREF4 are smaller in comparison to the reference signal SREF. The first, second and third reference signals SREF1, SREF2, SREF3 have the form of voltages such as the reference signal SREF.

[0073] The source signal SO having the PTAT voltage component can be used multiple times by adding different CTAT component buffers such as the buffer 12 and the additional buffer 56, because the signal source 11 providing the PTAT component does not need to be duplicated. More than one buffer 12, 56 can be coupled to the output 13 of the signal source 11. The different buffers such as the buffer 12 and the additional buffer 56 can be designed with different topologies, depending on the block requirements. For instance, the derived source signal SO' can be tapped off at a gate of the fourth amplifier transistor 55 and is a PTAT voltage. The derived source signal SO' can be fed into the buffer 12 that is a simple P-type source follower stage to introduce other reference voltages. Here the reference signal SREF has strong driving ability, but slower load regulation as the buffer 12 is a class-A buffer to drive a load which does not need fast transient settling. The divider resistors 72, 73, 75, 77 realize the voltage divider 71 to present the first, second and third reference signals SREF1, SREF2, SREF in the form of voltages. The divider resistors 72, 73, 75, 77 can be implemented by area-efficient high resistive resistors. A matching of the divider resistors 72, 73, 75, 77 and the resistors 21, 24 is not required.

[0074] The current source 80 generates a second signal I2. The second signal 12 is proportional to the absolute temperature. A buffer signal SB1 generated by the additional buffer 56 is provided to the current generator 84 such that a first signal I1 is provided at the output of the current generator 84. The buffer signal SB1 has the form of a voltage. The first signal I1 is complementary to the second signal I2 in respect of the absolute temperature. The first and the second signals I1, 12 are added and provided as a reference output signal IREF to the reference current output 81. The reference output signal IREF is nearly independent from the temperature. The first and the second signal I1, I2 as well as the reference output signal IREF are currents.

[0075] The fifth to eighth generator transistors 89, 90, 91, 93, the fifteenth and eighteens mirror transistors 94, 95 as well as the generator resistor 92 compose the CTAT current generator 84 to compensate the temperature coefficient of the second signal I2 so that the performance variation cross corner is reduced. The reference output signal IREF is provided to a not shown further circuit. The performance of the further circuit has at most small variations related to the fabrication process and temperature due to the high stability of the reference output signal IREF. The fifth generator transistor 89 receives the CTAT current. The first and the second signals I1, I2 which are the PTAT and CTAT currents are summed by the first current source transistor 82 and the first generator transistor 85. The third and fourth generator transistors 87, 88 have the effect of level shifters and suit the low voltage operation. The temperature coefficient compensation of the reference output signal IREF can be adjusted by the ratio of the generator resistor 92 and the first resistor 21.

[0076] A cascode circuit couples the current mirror 18 to the first and the second source transistor 20, 25. The currents through the first and the second current path 22, 26 are stabilized by the cascode circuit. The cascode circuit comprises the first and the second cascode transistor 40, 41, the first and the second amplifier 43, 48, the third resistor 42 and the mirror resistor 47.

[0077] The first and the second cascode transistors 40, 41, the fifth and the sixth mirror transistors 44, 45 as well as the first and the second amplifiers 43, 48 are

adapted to further improve the PSRR. The first and the second amplifiers 43, 48 are implemented as gain boosting amplifiers. This kind of regulated cascode is achievable by the feature of the signal source 11 having the second resistor 24 split to another branch. The second resistor 24 is a PTAT scaling resistor. The third resistor 42 and the mirror resistor 47 work as level shifter to provide enough headroom for the cascode transistors 40, 41, 44, 45. As the third resistor 42 and the mirror resistor 47 do not need to be well matched, they can be realized by high resistive poly resistors and are not area consuming.

[0078] The signal generator 10 is a voltage/current reference generator. The signal generator 10 can be designed for a microphone interface ASIC. The not shown microphone can be a digital micro electro mechanical systems microphone, abbreviated MEMS microphone. The signal generator 10 can be implemented in versatile and flexible configurations. The signal source 11 has to be realized only once and provides the source signal SO, respectively, the derived source signal SO' to different buffers 12, 56 such that the different reference signals SBG, SREF, SREF1, SREF2, SREF3 in the form of voltages or the reference output signal IREF can be generated.

[0079] Alternatively, the amplification factor provided by the further buffer 16 is different from 1. If the further buffer 16 is designed with an amplification factor larger than 1, the ratio of the second resistor 24 to the first resistor 21 can be reduced, correspondingly.

[0080] In an alternative, not shown embodiment, the current generator 84 and the current source 80 are omitted. Thus, the signal generator 10 comprises the buffer 12 and the additional buffer 56.

[0081] In an alternative, not shown embodiment, the current generator 84, the current source 80 and the additional buffer 56 are omitted. The signal generator 10 comprises the buffer 12.

[0082] In an alternative, not shown embodiment, the buffer 12 is omitted. The signal generator 10 comprises the additional buffer 56. The current generator 84 and the current source 80 can optionally also be omitted.

[0083] In an alternative, not shown embodiment, the voltage divider 71 only comprises the first and the second divider resistors 72, 73 and only generates the first reference signal SREF1. Alternatively, the voltage divider 71 comprises more than four divider resistors and generates further reference signals.

Reference numerals

[0084]

10	signal generator
11	signal source
12	buffer
13	output
14, 14'	input
15	low-pass filter
16	further buffer
17	output
18	current mirror
19	supply voltage terminal
20	first source transistor
21	first resistor
22	first current path
23	reference potential terminal
24	second resistor
25	second source transistor
26	second current path
27	buffer transistor
28	filter capacitor
29	first mirror transistor
30	second mirror transistor
31	third mirror transistor
32	fourth mirror transistor
40	first cascode transistor
41	second cascode transistor
42	third resistor
43	first amplifier
44	fifth mirror transistor
45	sixth mirror transistor
46	seventh mirror transistor
47	mirror resistor
48	second amplifier

49	filter resistor
50	eighth mirror transistor
51	ninth mirror transistor
52 to 55	first to fourth amplifier transistor
56	additional buffer
57	first buffer transistor
58	second buffer transistor
59	buffer capacitor
60	third buffer transistor
61	fourth buffer transistor
62	buffer resistor
63	fifth buffer transistor
64	additional output
65	load capacitor
66 to 69	tenth to thirteenth mirror transistor
70	fourteenth mirror transistor
71	voltage divider
72	first divider resistor
73	second divider resistor
74	first output
75	third divider resistor
76	second output
77	fourth divider resistor
78	third output
80	current source
81	reference current output
82	first current source transistor
83	second current source transistor
84	current generator
85	first generator transistor
86	second generator transistor
87	third generator transistor
88	fourth generator transistor
89	fifth generator transistor
90	sixth generator transistor
91	seventh generator transistor
92	generator resistor
93	eighth generator transistor
94	fifteenth mirror transistor
95	sixteenth mirror transistor
96	current generator capacitor
IREF	reference output signal
I1	first signal
I2	second signal
SB1	buffer signal
SBG	additional reference signal
SI	internal signal
SO	source signal
SO’	derived source signal
SREF	reference signal
SREF1	first reference signal
SREF2	second reference signal
SREF3	third reference signal

Claims

1. Signal generator, comprising:

- a signal source (11) that is configured for generating a source signal (SO) and
- a buffer (12, 56) that is configured for generating an internal signal (SI) and a reference signal (SREF, SBG) by summing the internal signal

(SI) to the source signal (SO) or to a signal (SO') derived from the source signal (SO), wherein the sign of the temperature coefficient of the source signal (SO) is opposite to the sign of the temperature coefficient of the internal signal (SI).

2. Signal generator according to claim 1, wherein the source signal (SO) and the internal signal (SI) are voltage signals and the reference signal (SREF, SBG) is the sum of the source signal (SO) and the internal signal (SI) or the sum of the signal (SO') derived from the source signal (SO) and the internal signal (SI).

3. Signal generator according to claim 1 or 2, comprising a current mirror (18) that couples the signal source (11) to a supply voltage terminal (19) and couples the buffer (12) to the supply voltage terminal (19).

4. Signal generator according to one of claims 1 to 3, wherein the signal source (11) comprises an output (13) for providing the source signal (SO), wherein the output (13) of the signal source (11) is coupled to an input (14) of the buffer (12).

5. Signal generator according to claim 4, wherein the buffer (12, 56) comprises a buffer transistor (27, 57) operating in a source follower configuration or an emitter follower configuration.

6. Signal generator according to claim 5, the buffer transistor (27, 57) having

- a control terminal that is connected to the input (14, 14') of the buffer (12, 56) and
- a first terminal that is coupled to an output (17, 64) of the buffer (12, 56) at which the reference signal (SREF, SBG) is provided,

wherein the internal signal (SI) is a voltage between the control terminal and the first terminal of the buffer transistor (27, 57).

7. Signal generator according to one of claims 4 to 6, comprising a low-pass filter (15) that is arranged between the output (13) of the signal source (11) and the input (14, 14') of the buffer (12, 56).

8. Signal generator according to one of claims 4 to 7, comprising a further buffer (16) that is arranged between the output (13) of the signal source (11) and the input (14, 14') of the buffer (12, 56).

9. Signal generator according to one of claims 1 to 8, the signal source (11) comprising a first source transistor (20) and a first resistor (21) such that a first current path (22) comprises the first source transistor (20) and the first resistor (21) and a node between the first source transistor (20) and the first resistor (21) is coupled to an output (13) of the signal source (11) at which the source signal (SO) is provided.

10. Signal generator according to claim 9, the signal source (11) comprising a second resistor (24) that couples the output (13) of the signal source (11) to the node between the first source transistor (20) and the first resistor (21).

11. Signal generator according to claim 9 or 10, the signal source (11) comprising a second source transistor (25) controlling the first source transistor (20) and having a smaller current driving capability in comparison to the first source transistor (20).

12. Signal generator according to one of claims 1 to 11, the buffer (12) comprising an output (17) for providing the reference signal (SREF), a first output (74) for providing a first reference signal (SREF1) and a voltage divider (71), wherein the voltage divider (71) is connected to the output (17) of the buffer (12) and the first output (74) of the buffer (12) is connected to a tap of the voltage divider (71).

13. Signal generator according to one of claims 1 to 12, comprising

- a current generator (84) for generating a first signal (I1) and
- a current source (80) for generating a second signal (I2),

wherein the sign of the temperature coefficient of the first signal (I1) is opposite to the sign of the temperature coefficient of the second signal (I2) and a reference output signal (IREF) is provided by summing the first and the second signal (I1, I2) .

14. Method for signal generation, comprising

- generating a source signal (SO),
- generating an internal signal (SI), wherein the sign of the temperature coefficient of the source signal (SO) is opposite to the sign of the temperature coefficient of the internal signal (SI) and
- generating a reference signal (SREF, SBG) by summing the internal signal (SI) and the source signal (SO) or summing the internal signal (SI) and a signal (SO') that is derived from the source signal (SO), wherein a buffer (12, 56) generates the internal signal (SI) and the reference signal (SREF, SBG).

15. Method according to claim 15, wherein the source signal (SO) is a voltage with ref-

erence to a reference potential terminal (23) and the internal signal (SI) is a voltage that is added on top of the source signal (SO) or the signal (SO') that is derived from the source signal (SO).

FIG 1

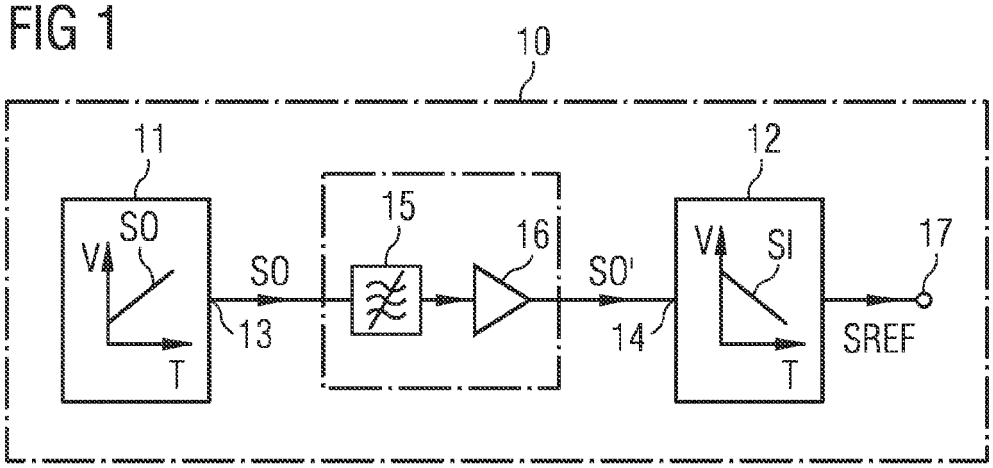
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FIG 2A

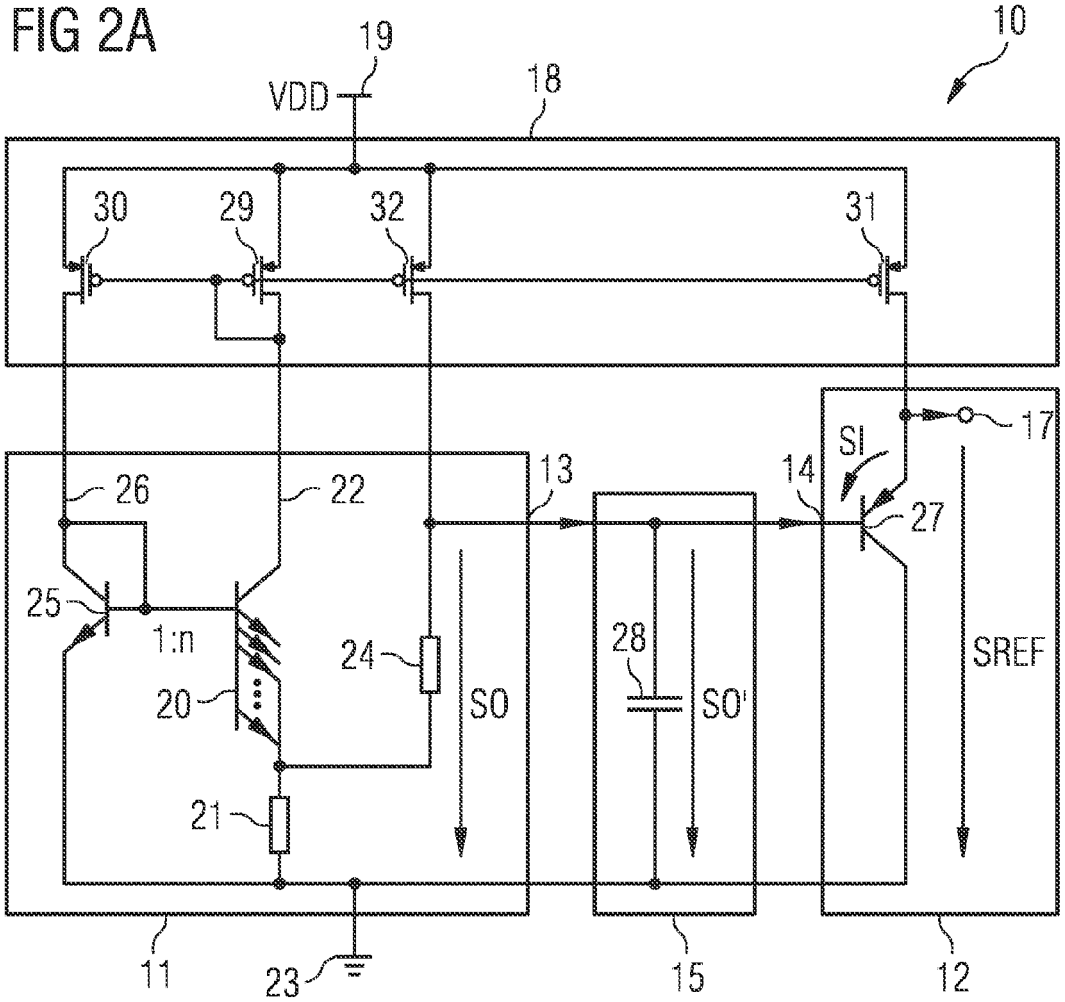
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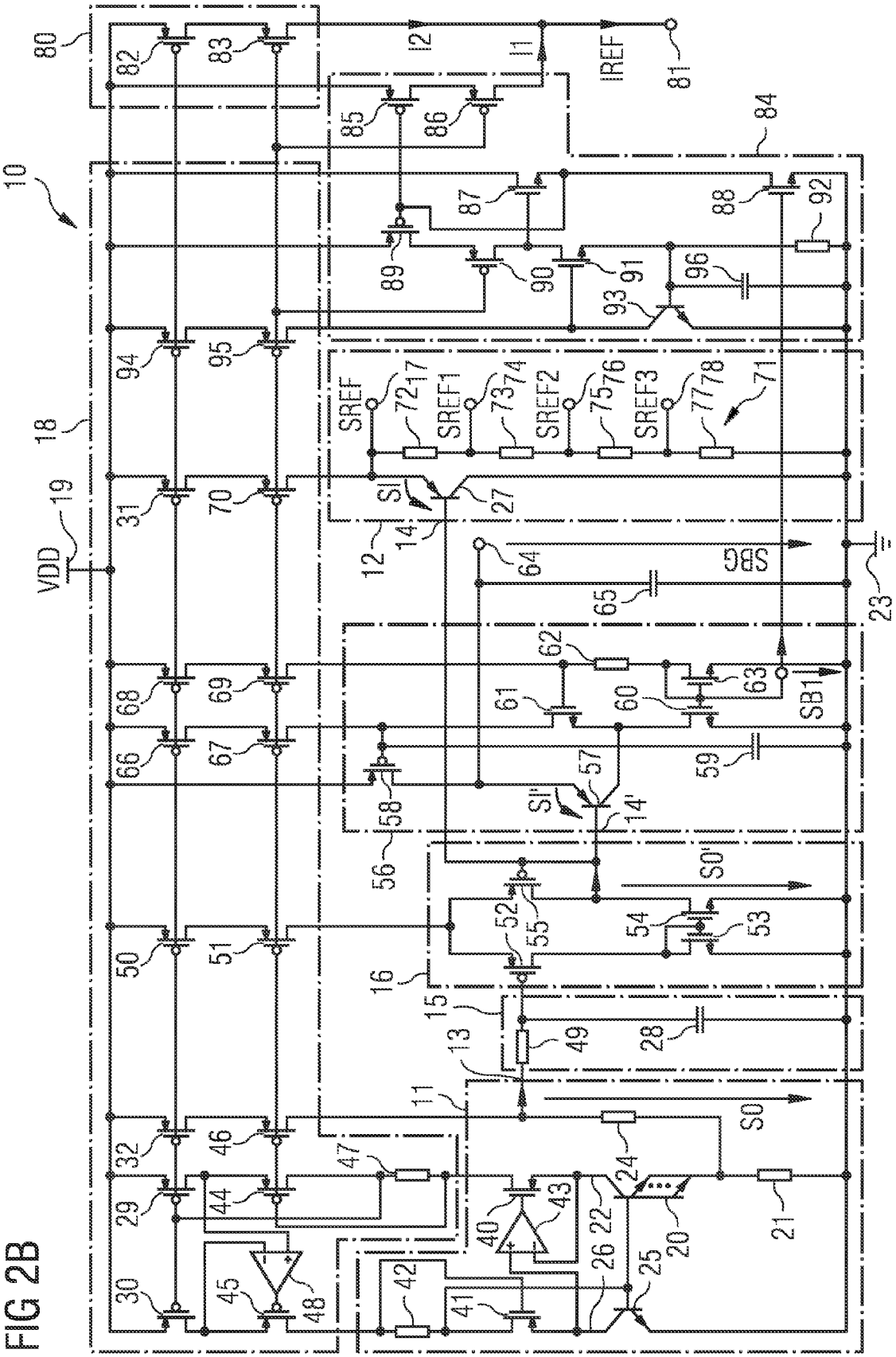
FIG 2B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EUROPEAN SEARCH REPORT

Application Number
EP 11 17 7486

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	28 February 2012	Arias Pérez, Jagoba

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EUROPEAN SEARCH REPORT

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