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(54) MICROMACHINED ON-WAFER PROBES AND RELATED METHOD

MIKROGEFERTIGTE ON-WAFER-SONDEN UND VERFAHREN DAFÜR

SONDES SUR TRANCHE MICRO-USINÉES ET PROCÉDÉ CONNEXE

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(56) References cited:
EP-A1- 2 012 131
US-A- 5 408 188
US-A1- 2004 017 215
US-A1- 2005 194 961
US-A1- 2008 068 034
US-A1- 2008 265 919
US-A1- 2009 189 623
US-A1- 2009 206 369
US-A1- 2010 026 331

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Description

BACKGROUND OF THE INVENTION

[0001] While significant progress has been made in the range of 0.5-2 terahertz integrated circuit fabrication, the measurement infrastructure for characterizing such components remains largely undeveloped. Currently, individual devices must be diced, or separated by other means, and mounted to a fixture for measurement. Further, for commercial probes that are currently available up to 340 GHz, their associated manufacturing techniques would not be transferable for higher frequency designs.

[0002] Probe structures that interface with integrated circuits exist commercially up to 500GHz, but are very expensive since they typically rely on hand assembly of several components. At higher frequencies hand assembly becomes increasingly difficult to the point where a different approach is necessary. Moreover, even at 500GHz and lower, for instance, it is a difficult assembly and yields a fragile product.

[0003] The conventional means of using fixtures for calibrated measurements of integrated circuits is extremely time-consuming and expensive (e.g., both in having to make the fixture and then assemble the device into the fixture and then make the measurement). By mounting a device in a fixture, additional "parasitic" effects are created that can mask the true response of the device itself. De-embedding the device response from the effects of the fixture is often difficult. It is preferable to measure the bare device on wafer prior to dicing and mounting. Moreover, a variety of calibration techniques have been developed to remove measurement errors due to probes and allow direct on-wafer measurements. Applying this to a fixtured device is difficult if not impossible.

[0004] Accordingly, there is a need in the art for direct on-wafer probing that allows rapid prototyping and characterization and also eliminates parasitic effects and responses associated with fixtures

[0005] Accordingly, there is a need in the art for calibrated on-wafer measurements of submillimeter-wave devices (about 300 GHz to about 3,000 GHz) and Terahertz devices (about 100 GHz to about 10,000 GHz), which in turn would significantly reduce the effort and cost required to characterize a wafer of devices while increasing the accuracy of the measurement by eliminating errors and effects associated with the fixture.

[0006] Moreover, there is a need in the art for improved manufacturing and reliability of probe structures pertaining to millimeter-wave devices (about 30 GHz to about 300 GHz).

[0007] EP 2 012 131 A1 describes a contact probe which can be electrically connected with a measurement apparatus to measure a high speed and high frequency signal. The probe includes a first printed wiring board having a signal electrode and a ground electrode used as a contact part with respect to a measuring object. The signal electrode and the ground electrode are formed of a metal wiring pattern on a substrate. A second printed wiring board has a coaxial line structure with shield electrodes which enclose a signal line. The signal electrode of the first printed wiring board and the signal line of the second printed wiring board are electrically connected together, and the ground electrode of the first printed wiring board and the shield electrodes of the second printed wiring board are electrically connected together.

[0008] US 2009/0189623 A1 describes a wafer probe comprising a contact conductively interconnected with the wall of a waveguide channel and supported by a substrate that projects from an end of a waveguide channel.

[0009] US 2008/0265919 A1 describes scalable wideband probes, fixtures, and sockets for high speed IC testing and interconnects.

[0010] US 2008/0068034 A1 describes a probe array wafer including a substrate, upon which a plurality of compliant probes are mounted. Pairs of axially aligned probes may be electrically connected together to provide a pass through power connection from the test equipment to the device under test.

[0011] US 5,408,188 discloses a wafer probe for high frequency single-ended signals in which a waveguide transitions directly to a coplanar line at the probe tip. The probe tip comprises a dielectric blade having a centrally located (laterally) signal conductor affixed to the lower surface of the blade. The blade is clamped between separable upper and lower portions of the waveguide with the ground conductors in contact with the lower interior surface of the waveguide's wall.

SUMMARY OF THE INVENTION

[0012] The present invention relates to a device for probing a structure on a surface of an object substrate and to a method of testing such a structure using the device. The invention is defined by the independent claims 1 and 12; further features are defined in their corresponding dependent claims. Additional aspects of the invention are presented in the description and the drawings.

[0013] An aspect of an embodiment of the present disclosure provides, but not limited thereto, a micromaching process to fabricate a single chip that simply drops into a supporting structure. Micromachining includes processes based on integrated circuit fabrication techniques that create structures with dimensions on the order of microns. Since much of the technology from integrated circuits can be leveraged, a higher volume of devices at a lower cost can be produced with the parallel processing techniques commonly used in industry.

[0014] An aspect of an embodiment of the present disclosure provides, but not limited thereto, a micromaching process to create a probe that will interface with integrated circuits operating at frequencies of 100GHz and higher. This approach creates a silicon structure (or other applicable choice of material) that provides mechanical force for probing while supporting the transfer of the high frequency energy between a measurement system and an integrated circuit, individual device or material. The integrated circuit, individual device or material may be, for example, at the micron-scale, as well as sub-micron scale such as nano-scale. Moreover, related components of the system and device of the embodiments may be micron or sub-micron scale as well.

[0015] An aspect of an embodiment provides the mechanical design and characterization of a micromachined on-wafer probe scalable to submillimeter-wave frequencies. The design may comprise a silicon micromachined probe (i.e., microfabricated compliant chip, and which may be of other suitable materials) with a ground-signal-ground (**GSG**) configuration on a silicon substrate. In an approach, the silicon substrate may be about 15 μm thick, or the silicon substrate could be thicker or thinner within reason, as desired or required. This micromachined chip is housed in a metal waveguide block that provides mechanical support for the probe and enables coupling to a waveguide flange. In an exemplary embodiment, loadcell measurements of the microfabricated compliant chip (i.e., probe) show a DC contact resistance below 0.07 Ω with an applied force of 1 mN.

[0016] As mentioned above, the substrate of the probe may be thicker or thinner within reason even at a design frequency of 500 GHz. Moreover, as the system design moves to higher frequencies, a thinner Silicon substrate may be implemented. For example, in an approach a 5um thick substrate is utilized for a higher frequency.

[0017] As will be discussed later, while Silicon may have been selected for a substrate material for a number of design reasons, it should be appreciated that the substrate may be realized utilizing alternative materials. For instance, besides Silicon the substrate may be anyone of the following materials: Polyimide, Fused Quartz, Gallium Arsenide, Alumina, Silicon Nitride, Kapton HN Polyimide, Single Crystalline Quartz, or synthetic diamond, as well as any other suitable synthetic materials as desired or required.

[0018] An aspect of an embodiment of the present disclosure provides a new approach to making millimeter-wave (about 30 GHz to about 300 GHz), submillimeter-wave (about 300 GHz to about 3,000 GHz) and Terahertz frequency (about 100 GHz to about 10,000 GHz) on-wafer probes. A micromaching process is applied to create more accurate probe structures so that frequencies as high as the Terahertz range (about 100 GHz to about 10,000 GHz) can be on-wafer probes. Moreover, the mechanically active component is easy to replace so repairs to the probes are feasible and economical.

[0019] Moreover, it should be appreciated that an aspect of an embodiment of the present disclosure provides a new approach to making on-wafer probes for direct current (DC), i.e., zero frequency.

[0020] An aspect of various embodiments of the present disclosure may provide a number of features, elements and characteristics, such as but not limited thereto, the following:

- Integration of the waveguide probe with the probe tip in a single chip.
- Use of a thin chip, such as but not limited to a silicon chip, as the mechanically active component.
- Avoids expensive and challenging hand assembly of the devices that commercial probes currently rely upon.
- Capability to be made smaller since the critical components are defined with microfabrication processes, and therefore can operate at frequencies higher than existing commercial probes.

[0021] Further, an embodiment of the present disclosure allows a design and fabrication to registrate/align the different features of the probe to tighter/better specifications. For example, an embodiment includes two outer ground tips/lines and an inner signal tip/line. These are all put down in one material and their registration to each other is better than 0.1um. Whereas, in conventional practice, the features that are put down in different layers are typically registered to better than 2um to each other. As a result, an aspect of an embodiment of the present disclosure also provides the capability to, among other things, operate at frequencies higher than existing commercial probes.

[0022] Moreover, currently there are no commercial on-wafer probes available above 500GHz.

[0023] Further yet, an embodiment of the present disclosure provides an approach that may also be produced at lower frequencies for a probe at a lower cost.

[0024] Further still, an embodiment of the present disclosure allows the fixture (e.g. housing or block) to be used over and over again while the probe can be easily replaced. In an approach, the housing or block may be relatively more expensive compared to the probe and therefore a replaceable/disposable probe in conjunction with reusable or more permanent block would lead to economic savings.

[0025] An aspect of an embodiment of the present disclosure provides a device for probing a structure on a surface of an object substrate. The device comprises: a microfabricated compliant chip, wherein the microfabricated compliant chip comprises integrated electrical interconnects.

[0026] An aspect of an embodiment of the present disclosure provides a device for probing a structure on a surface of an object substrate. The device being configured to be secured by a housing that is configured to be able to electrically

interconnect to a measurement instrument. The device comprises: a microfabricated compliant chip, wherein the microfabricated compliant chip comprises integrated electrical interconnects.

[0027] An aspect of an embodiment of the present disclosure provides a housing that is configured to be able to electrically interconnect to a measurement instrument. The housing comprises: an aperture that is configured to detachably engage with a microfabricated compliant chip that is used for probing a structure on a surface of an object substrate.

[0028] An aspect of an embodiment of the present disclosure provides a method of fabricating a device for probing a structure on a surface of an object substrate. The method may comprise: providing a substrate; and integrating electrical interconnects in the substrate to provide a microfabricated compliant chip.

[0029] An aspect of an embodiment of the present disclosure provides a method of fabricating a device used for probing a structure on a surface of an object substrate. The device being configured to be secured by a housing that is configured to be able to electrically interconnect to a measurement instrument. The method comprises: providing a substrate; and integrating electrical interconnects in the substrate to provide a microfabricated compliant chip.

[0030] An aspect of an embodiment of the present disclosure provides a method of testing a structure on a surface of an object substrate. The testing method comprises probing the surface of an object substrate with a device, wherein the device includes a microfabricated compliant chip, wherein the microfabricated compliant chip comprises integrated electrical interconnects.

[0031] A micromaching process to fabricate a single chip that simply drops into a supporting structure. The micromaching process provides the ability to create a probe that will interface with integrated circuits, for example, operating at frequencies in the range of about 100GHz to about 3,000 GHz (3 THz), or greater. This approach creates a silicon structure (or other applicable choice of material) that provides mechanical force for probing while supporting the transfer of the high frequency energy between a measurement system and the integrated circuit, individual device or material.

[0032] These and other objects, along with advantages and features of various aspects of embodiments of the disclosure disclosed herein, will be made more apparent from the description, drawings and claims that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The foregoing and other objects, features and advantages of the present invention, as well as the invention itself, will be more fully understood from the following description of preferred embodiments, when read together with the accompanying drawings

Fig. 1A provides a schematic diagram of a device **10** for probing a structure (not shown) on a surface of an object substrate **1.**

Fig. 1B provides a schematic diagram of a device **10** for probing a structure **2** on a surface of an object substrate.

Fig. 2A schematically illustrates a waveguide block housing the microfabricated compliant chip.

Fig. 2B schematically illustrates an enlarged partial view of **Fig. 2A** including the micro fabricated compliant chip in relation to waveguide block housing. The top half of the block is removed for clarity. Not visible on the underside of the chip is the conductor connecting the waveguide to the compliant beam.

Fig. 3 schematically illustrates the compliant beam of the microfabricated compliant chip pressing against the device under test (DUT). As the chip is lowered from a first position to a second position onto the DUT, a stress σ is introduced into the chip.

Fig. 4 schematically illustrates a side view of waveguide showing the effect of the angle on the coupling to the input waveguide.

Fig. 5A schematically represents a simulation demonstrating the effect of the angle of approach (θ) coupling between the input waveguide and the chip's related waveguide block.

Fig. 5B graphically represents a simulation demonstrating the effect of the angle of approach (θ) coupling between the input waveguide and chips's related waveguide block.

Fig. 6 schematically represents dimensions of a cantilever beam.

Fig. 7 provides a graphical comparison of the materials in **Table I** in a cantilever structure. These results are for a cantilever 350 μm long, 15 μm wide and 15 μm thick. Lines of constant strain-energy density for the cantilever are indicated.

Fig. 8 schematically illustrates a side view of a clamping recess with the silicon chip in place. When the two halves of the waveguide block are pressed together, the total chip thickness of 25 μm is compressed down to 21 μm. This compressed gold protects the silicon from the waveguide block while fixing the chip in place, providing mechanical support for the chip.

Fig. 9 schematically illustrates at op view of the W-Band compliant beam indicating the clamped area and relevant dimensions. The outline of the substrate is visible through the beamlead so the shape of the silicon can be observed.

Fig. 10 provides a plot of the stress under a 1 mN load at each tip. Not shown is the 2.3 μm deflection of the tips under this load.

Fig. 11 graphically represents the maximum stress induced into the microfabricated compliant chip (e.g., probe) under a 3 mN load as the fillet radius is varied between 15 μm and 75 μm. The total width is held constant at 750 μm.
Fig. 12A is a photomicrograph depiction of the front view and back view of each of the micromachined W-Band chip as it relates to a transmission line of the coaxial design.
Fig. 12B is a photomicrograph depiction of the front view and back view of each of the micromachined W-Band chip as it relates to a transmission line of the microstrip design.
Fig. 13 is micrographic depiction of the microfabricated compliant chip mounted in the waveguide block housing (right side of figure) shown next to a commercial probe for comparison (left side of figure).
Fig. 14A provides scanning electron micrograph (SEM) depiction of the tip of the compliant beam before numerous contact cycles, i.e, before contact test.
Fig. 14BA provides scanning electron micrograph (SEM) depiction of the tip of the compliant beam after 10,000 contact cycles at 10 mN. It also shows wear of the silicon contact point as well as wear and displacement of the electroplated gold.
Fig. 15 provides a schematic diagram showing how the contact resistance is measured between the microfabricated compliant chip (i.e., probe) designed with one contact point and the silicon substrate's contact pad. Connections for the four-wire measurement are indicated by the overlayed circuit diagram.
Fig. 16 graphically illustrates the measurement of the contact resistance plotted against the contact force of the microfabricated compliant chip (i.e., probe). Note that a contact resistance below 0.1 Ω is achieved at 1 mN.
Fig. 17 graphically illustrates minimum contact resistance for each contact cycle highlighting the effect of excessive contact force on the probe's lifetime. The higher contact force of 25 mN (dashed line) drastically decreased the lifetime of probe to 700 contact cycles. Differences in low resistance measurements resulted from variations in the two-wire measurement setup between devices.
Fig. 18 schematically illustrates the microfabricated compliant chip in relation to waveguide block housing. The top half of the block is removed for clarity. Not visible on the underside of the chip is the conductor connecting the waveguide to the compliant beam.
Figs. 19A-19B schematically illustrate the microstrip and coaxial-based probe chips, respectively.
Figs. 20A-20B schematically illustrate the transmission line designs for the microstrip and coaxial-based probe chips, respectively.
Fig.21A schematically illustrates the 625 GHz waveguide to transmission line simulation model.
Fig.21B graphically illustrates the results of waveguide to transmission line simulation model.
Fig.22A schematically illustrates the 625 GHz rectangular coaxial to the probed substrate simulation model. The inset schematically shows the necessary break in the substrate required to form the contact tips.
Fig.22B graphically illustrates the return loss over a set of different contact tip lengths.
Fig.23A schematically illustrates a full simulation of 625 GHz probe from waveguide to the probed substrate, whereby the simulation model being for the unbiased probed.
Fig.23B graphically illustrates the results of the simulation model of **Fig. 23A** for the Microstrip design.
Fig.23C graphically illustrates the results of the simulation model of **Fig. 23A** for the coaxial design.
Fig.24A graphically illustrates the one-port measurements of the 625 GHz waveguide probes for the microstrips design.
Fig.24B graphically illustrates the one-port measurements of the 625 GHz waveguide probes for the coaxial design.
Fig.25A graphically illustrates the measurements of offset short lines with calibrated on-wafer probes, which shows the position of the four offset shorts on the Smith chart.
Fig.25B graphically illustrates the measurements of offset short lines with calibrated on-wafer probes, which shows the phase of the verification offset short lines comparing the measured (solid) to the expected (dashed) value.
Fig. 26A schematically illustrates a waveguide block housing the microfabricated compliant chip.
Fig. 26B provides an enlarged partial view of the area identified in **Fig. 26A. Fig. 26C** schematically illustrates the front side of the micro fabricated compliant chip (i.e., probe chip).
Fig. 27 schematically represents a mechanical test setup whereby the load cell is used to measure the amount of contact force being generated by the micro fabricated compliant chip (i.e., probe chip).
Fig. 28 schematically represents the mechanical test results of the microfabricated compliant chip (i.e., micromachined probe) using the setup shown in **Fig. 27.** Contact force vs. vertical motion of the stage.
Fig. 29 graphically illustrates the measurement results of a microfabricated compliant chip (i.e., micromachined on-wafer probe).
Figs. 30A-30C graphically illustrate the measured S-parameters of the same microfabricated compliant chip (i.e., micromachined probe chip) mounted in the waveguide block three times for (a) Magnitude of S_{11} (Waveguide port); (b) Magnitude of $S_{21;}$ and (c) Magnitude of S_{22} (CPW port), respectively.
Figs. 31A-31C graphically illustrate the measured S-parameters of three different microfabricated compliant chips (i.e., micromachined probe chips) for: (a) Magnitude of S_{11} (Waveguide port); (b) Magnitude of $S_{21;}$ and(c) Magnitude

of S_{22} (CPW port), respectively.

Figs.32A-32C graphically illustrate the measured S-parameters of the microfabricated compliant chip (i.e., micromachined probe) doing lifetime testing for: (a) Magnitude of S_{11} (Waveguide side); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW side), respectively.

Figs. 33A-33C provide scanning electron micrograph (SEM) depictions of images of the tips of the microfabricated compliant chip (i.e., micromachined probe) after: (a) 10 contacts; (b) 3000 contacts; and (c) 6000 contacts, respectively.

[0034] The accompanying drawings, which are incorporated into and form a part of the instant specification, illustrate several aspects and embodiments of the present invention and, together with the description herein, serve to explain the principles of the invention. The drawings are provided only for the purpose of illustrating select embodiments of the invention and are not to be construed as limiting the invention.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS OF THE INVENTION

[0035] An aspect of an embodiment provides a scalable approach to wafer probe development that integrates a rectangular waveguide probe and coplanar waveguide (**CPW**) wafer probe onto a single chip, such as but not limited to, a silicon chip. In an embodiment, this silicon structure can support submillimeter-wave (about 300 GHz to about 3,000 GHz) or terahertz frequency (about 100 GHz to about 10,000 GHz) transmission lines as the substrate can be made about 1 μm to about 15 μm thick to suppress coupling to parasitic substrate modes. It should be appreciated that the substrate may be less than 1 μm thick or greater than about 15 μm thick. Alternatively, the structure may be provided to support millimeter-wave (about 30 GHz to about 300 GHz) transmission lines. The mechanical characteristics of single-crystal silicon allows for a robust probe to be fabricated which supplies sufficient force for low-resistance contacts, enabling low-insertion loss coupling to the device under test (**DUT**) and DC biasing of probed circuits.

[0036] **Fig. 1A** provides a schematic diagram of a device **10** for probing a structure (not shown) on a surface of an object substrate **1.** The device **10** is a microfabricated compliant chip, wherein said microfabricated compliant chip includes integrated electrical interconnects **12** (shown in **Fig. 1B**). Accordingly, in an embodiment the microfabricated compliant chip is monolithic due to its single-piece circuit construction. The structure or area on the object substrate **1** may be anyone one of one or more of the following: integrated circuit or any type of microelectronic device, microelectromechanical (MEM) device , non-electronic device, or a sample of material with appropriate contacts or some other geometric feature that has been fabricated on the substrate surface. The structure may be of interest for purpose of characterizing a material on the object substrate rather than characterizing a device on the object substrate. For instance, the material of interest for characterizing may be a biological material, such as DNA, RNA, proteins, etc. or any other biological materials as desired or required. Moreover, the material of interest for characterizing may be graphene, an atomic scale lattice structure, or an atomic scale lattice structure, as well as any other applicable structure or material. The structure or area on the object substrate may be, for example, an integrated circuit, electric device, non-electric device, individual device or material that may be at, for example, the micron-scale, as well as sub-micron scale such as nano-scale. Still referring to **Fig. 1A,** in an embodiment, the integrated electrical interconnects **12** (shown in **Fig. 1B**) of the microfabricated compliant chip **10** may generally comprise one of the following: at least one compliant beam **50,** at least one transmission circuit **30;** and a waveguide transition element **20,** whereby the transmission circuit **30** is suitable to electrically interconnect the compliant beam **50** with the waveguide transition element **20.** The waveguide transition element **20** is configured to be electrically interconnected with a measurement instrument **22,** by way of a waveguide **24,** for example. The measurement instrument **22** may be a network analyzer or vector network analyzer (VNA), or any system or device capable of measuring, analyzing, storing, processing and/or recording the data. Although not shown, the integrated electrical interconnects **12** may be further configured to supply a bias current (or bias voltage as well) to the object substrate. Moreover, other active and passive circuit components may be added to the integrated electrical interconnects **12** as desired or required.

[0037] As shown in **Fig.** 1**B,** the microfabricated compliant chip device **10** is configured to be secured by a housing **23** by an aperture **26** (or other retention mechanisms or means) provided by the housing **23** or it's related components. The aperture **26** may be a block split, or other available configurations such as a slot, groove, recess, channel, tunnel, indentation, passage, slit, or port. Further yet, the microfabricated compliant chip **10** may be secured to the housing in a manner that is deatachably engaged with the housing (e.g., so as to be releasable from the housing). For instance, if the microfabricated compliant chip device is damaged then the chip may be readily removed and replaced. Alternatively, the chip may be substituted with a different chip or device if desired or required. Compressive forces induced by the housing or it's related components will secure and align the microfabricated compliant chip **10** in place. And further, the amount of compressive force may be altered (as desired or required) by increasing or decreasing its magnitude, as well as changing the area or location of the applied force. The housing may be configured to be reusable, but not necessarily.

[0038] As will be discussed in greater detail below, the microfabricated compliant chip **10** is configured whereby when

it is presented to a structure **2** on a surface of an object substrate **1** and when the prerequisite force is applied, then the entire structure (or at least substantially) of the microfabricated compliant chip **10** (that is not clamped in the housing) deflects. The thickness and length of the structure of the microfabricated compliant chip **10,** as well as the angle that it is presented to the structure **2** on a surface of an object substrate **1,** is optimally designed such that enough force is generated with a modest amount of flexure of the microfabricated compliant chip **10.** The force exerted by the microfabricated compliant chip **10** on the object substrate **1** is what is needed to insure a good electrical contact.

[0039] As illustrated in **Fig. 2,** a housing **23** is provided, such as a waveguide block. In an embodiment, the waveguide block may be an E-plane split waveguide block type having a split **26** that houses the microfabricated compliant chip **10,** such as silicon chip. **Fig. 2B** schematically shows tabs **71** of silicon, for example, that are electroplated with gold which are clamped between the two halves of the waveguide block, providing mechanical support and alignment of the chip **10** (e.g., wafer probe) to the housing **23.** The chip **10** couples from waveguide **24,** through a waveguide probe **25,** such as a radial probe (e.g., radial E plane waveguide probe,) into the transmission circuit **30,** e.g., a transmission line channel. This channel emerges from the block **23** where the mode is converted to the Ground-Signal-Ground (**GSG**) of the compliant beam **50** of the microfabricated compliant chip **10** (e.g., wafer probe).

[0040] In an embodiment, silicon may be used (as opposed to alumina or polyimide or other suitable material, for example) because it is more compatible with micromachining processes and its high elastic modulus produces significant force for low-resistance contacts, even with the thin substrates required at submillimeter-wave or terahertz frequencies. Secondly, the fabrication process allows for full lithographic control over the extents of the silicon substrate, allowing excellent matching between functional transmission lines and precise control of the geometry of the probe. Finally, use of a split waveguide block design and drop-in probe chip modules allow for user friendly replacement of any worn, damaged or unwanted microfabricated compliant chips **10.**

EXAMPLES

[0041] Practice of an aspect of an embodiment (or embodiments) of the invention will be still more fully understood from the following examples and experimental results, which are presented herein for illustration only and should not be construed as limiting the invention in any way.

Example and Experimental Results Set No. 1

[0042] An exemplary embodiment presented in this Example and Experimental Set provides the mechanical design and performance of a microfabricated compliant chip **10** (i.e., a micromachined probe) for a W-Band (75-110 GHz) prototype and a waveguide probe **25** (e.g., WR-1.5 (500-750 GHz)) developed to measure emerging planar submillimeter-wave devices. The electromagnetic design is presented in the Example and Experimental Results Set No. 2 that is found later in this disclosure.

I. MECHANICAL DESIGN

[0043] The structure of microfabricated compliant chip **10** must provide sufficient force to create a low resistance electrical contact to the device (e.g., planar or non planar device) that is being measured. This minimizes insertion loss and enables biasing of active devices. Commercial probes quote contact resistances at or below 0.1 Ω. Based on microactuator measurements it is hypothesized that at least 0.2 mN of force per tip is required between the probe and the device under test (DUT) to achieve this contact resistance for gold-to-gold contacts.

[0044] This force is generated by the cantilever beam formed by fixing the microfabricated compliant chip **10** (e.g., silicon chip) to the housing **23** (e.g., waveguide block) in the areas indicated in **Fig. 2.** As the compliant beam **50** of the microfabricated compliant chip device presses against the device under test (DUT) 2, the deflection of the compliant beam **50** (or applicable portion of the microfabricated compliant chip) generates the contact force, as illustrated in **Fig. 3.** The reaction to this force is the stress, σ, induced in the beam. If this stress exceeds the yield strength of the material used in the microfabricated compliant chip **10,** the chip will fail. **Table I** lists the yield strengths of several materials compatible with micromachining processes. **Fig. 3** illustrates the chip being lowered from an initial position to a subsequent position, whereby the compliant beam **50** is shown deflected or flexed.

A. Angle of Approach and Microfabricated Compliant Chip Length

[0045] The angle of the microfabricated compliant chip **10** with respect to the object substrate **1** (θ in **Fig. 4**) impacts several critical elements of the microfabricated compliant chip **10** design. First, the compliant beam **50** must be sufficiently long to extend beyond the block **23** so as to be visible from an overhead microscope (not shown) or other instrument. Second, the compliant beam **50** must reach below the level of the waveguide block **23** so that the micro fabricated

compliant chip **10** makes contact with sufficient margin as to prevent the waveguide block **23** from touching the object substrate **1** or DUT. Finally, the coupling from the input waveguide **24** to the split-waveguide probe housing **23** is an important factor in choosing θ.

[0046] A direct connection between the input waveguide **24** and the angled waveguide of the split block **23,** illustrated in **Fig. 4,** is analyzed to simplify the design of the housing **23. Fig. 5** shows a finite element model of the two waveguides connected at an angle θ. The angled waveguide is simply cut flush at the end of the waveguide block, exposing a cross section of the waveguide that is $\alpha/\cos(\theta)$ long, and centered on the input waveguide. Using HFSS™, simulations of this transition show that the return loss is better than 20 dB for angles less than or equal to 30°. Consequently, 30° is chosen as the angle of approach for the microfabricated compliant chip **10** so that no additional transition structures are necessary to couple to the input waveguide **24.**

[0047] The length of the microfabricated compliant chip **10** is chosen based on the constraints shown in **Fig. 3,** for example. The channel **32** enclosing the transmission line **31** of the microfabricated compliant chip **10** is 100 μm high, so the vertical projection of the distance from the center of the microfabricated compliant chip **10** to the base of the channel **32** is 25 μm. A minimum of 40 μm is left between the bottom of the block and the transmission line channel **32** to avoid deformation of the machined material. Lapping the bottom of the waveguide block after milling permits the block thickness below the channel to be set to 40 ± 3 μm. A separation of at least 110 μm between the block and the DUT **2** is left when the probe initially contacts the DUT, so the length of microfabricated compliant chip **10** (i.e., probe length) is calculated as:

$$l = (40\ \mu m + 110\ \mu m + 25\ \mu m)/\sin(30^\circ) = 350\ \mu m \quad (1)$$

B. Beam Analysis and Material Selection

[0048] Many different materials compatible with micro fabrication processes are available to form the microfabricated compliant chip **10,** with some of the more common listed in **Table I** along with their relevant material properties. To compare these materials, the maximum deflection and force of a prismatic cantilever beam for each are calculated. Although the actual micro fabricated compliant chip **10** structure is more complex, this simple structure can be analyzed directly, and allows straightforward comparison between the materials. **Fig. 6** shows a cantilever beam with a single point force, *F,* on the end of the beam. The maximum stress, $\frac{max}{x}$, is at the base of the beam and given by :

$$\sigma_x^{max} = \frac{Flt}{2I}. \quad (2)$$

TABLE I

MATERIAL PROPERTIES OF CANDIDATE BEAM MATERIALS. *E* IS THE ELASTIC MODULUS AND σ^{yield} IS THE YIELD STRENGTH.

Material	*E* (GPa)	σ^{yield} (MPa)	E_r	Modulus of Resilience (kJ/m^3)
Gold	80	220	N/A	302
Nickel	207	320	N/A	447
Fused Quartz	73	50	3.8	17
Gallium Arsenide	118	85	12.9	30
Alumina	300	330	9.1	181
Silicon Nitride	310	830	5-8	1,111
Kapton HN Polyimide	2.5	230	3.2	10,580
Single Crystalline Quartz	97	1700	4.6	14,897
Silicon	185	4500	11.9	54,730

[0049] By setting $\sigma \frac{max}{x} = \sigma^{\text{yield}}$ (the yield stress) we can solve for the maximum force and deflection the beam can withstand at the point of failure

$$F^{max} = \frac{wt^2}{6l}\sigma^{yield} \qquad (3)$$

$$y^{max} = \frac{-2l^2}{3Et}\sigma^{yield} \qquad (4)$$

for a rectangular cross section.

[0050] It should be noted that this analysis assumes the force applied is perpendicular to the beam, along the y-axis in **Fig. 6.** As can be seen in **Fig. 3** this is not quite correct since the microfabricated compliant chip **10** approaches the probed DUT **2** at an angle (It should be appreciated that the angle may vary as desired or required).. This will generate an additional component of the force along the length of the cantilever. However, by comparing simulations of the probe with experiment, it has been found that this axial force is largely relieved as the probe slides against the probed DUT. Therefore we neglect the axial component of the stress in the remaining analysis.

[0051] The beam material must support a high maximum force for a given deflection. This is to ensure the probe is rugged and will not easily break during normal use. It is noted that a higher yield strength is preferable, but the elastic modulus has a diminishing effect on the maximum deflection, based on equation (4). A figure of merit that is related to these two material parameters is the modulus of resilience. The modulus of resilience, u^y, is defined as the amount of strain-energy density that a material can support before failure :

$$u^y = \frac{(\sigma^{yield})^2}{2E} \quad \left(\frac{J}{m^3}\right). \qquad (5)$$

The modulus of resilience for different materials is listed in **Table I** and allows for direct comparison of the various candidate substrates.

[0052] The modulus of resilience allows for comparison independent of the geometry, but it fails to provide a sense of the material's performance with respect to the maximum force and deflection. Choosing a specific geometry for the beam allows these maximums to be calculated and different probe materials to be compared. This comparison is shown in **Fig. 7** for a beam that is 350 μm long with a width and thickness of 15 μm. Contours of constant strain-energy density for the cantilever are indicated on the plot, for comparison to the modulus of resilience.

[0053] From this most of the materials listed in **Table I** can be eliminated compared to the performance of polyimide, single crystalline quartz and silicon. The anisotropic nature of single crystalline quartz may complicate the electromagnetic design of the probe so this is eliminated. Polyimide has a lower maximum force for this particular geometry due to its relatively low elastic modulus. If the polyimide beam is made thicker it can provide a maximum force on the same order as silicon, with the tradeoff being that the maximum deflection is reduced. For instance, a polyimide beam 66 μm thick would generate a maximum force of 7 mN with a corresponding deflection of 96 μm, which is similar to the performance of a 15 μm thick silicon beam.

[0054] For high frequency operation, we wish to minimize the electrical thickness of the dielectric to avoid coupling to substrate or surface modes. A 15 μm thick silicon beam (ε_r = 11:9) will be λ_d/10 thick at 625 GHz (the center of the WR-1.5 waveguide band), while the 66 μm thick polyimide beam (ε_r = 3:2) will be λ_d/4 thick. Although the dielectric constant of polyimide is lower than silicon, its smaller elastic modulus forces the beam to be electrically thicker than silicon to achieve comparable contact forces. In addition, the higher modulus of resilience of silicon allows for greater design freedom over that of polyimide, helping ease other design constraints. For these reasons silicon is chosen as the substrate material of the microfabricated compliant chip **10.**

C. Drop-In microfabricated compliant chip **10** Assembly

[0055] To facilitate assembly, the microfabricated compliant chip **10** is secured to the housing **23** by clamping the microfabricated compliant chip **10** between the two halves of the waveguide block **23,** eliminating the need for adhesives or the like during assembly. As schematically shown in **Fig. 8,** recesses are milled into one half of the waveguide block to a depth sufficient to support the thickness of the silicon substrate tabs, but compress the 5 μm of electroplated gold

that is applied to both sides of the microfabricated compliant chip **10.** This gold provides a cushion between the silicon and the relatively rough surface of the waveguide block, preventing chipping or cracking of the microfabricated compliant chip **10.** This approach simultaneously provides alignment of the chip to the waveguide block and mechanical support for the chip. The gold must be sufficiently thick to compensate for variations in the depth of the recess, but with modern machining techniques a tolerance of ± 3 μm can be achieved. Other materials besides gold may be implemented if desired or required, such as but not limited thereto Indium (could be plated), various alloys of gold, as well as other suitable materials.

D. Additional Design and Stress Analysis

[0056] Additional considerations of shape of the microfabricated compliant chip **10** may be guided by two goals, for example. First, the geometry of the microfabricated compliant chip **10** must reduce the concentration of the stress induced into the microfabricated compliant chip **10** by the contact force. A minimum of 0.2 mN of force must be applied to create a low-resistance gold-to-gold contact. The force applied is to the entire structure of the compliant beam **50,** but it is the force at the contact tip **51** that we measure with our load cell. This force at the contact tip **51** is what is needed to insure a good electrical contact. As a margin of safety, 1 mN of force per contact tip **51** is chosen for this design. The maximum stress induced under this force must not exceed the yield strength of silicon, 4.5 GPa. Second, the mechanical design must allow for a transmission line **31** to connect the waveguide **24** to the microfabricated compliant chip **10.** Therefore, the microfabricated compliant chip **10** is designed to be 750 μm wide (i.e. have a width of 750 μm) to support a transmission line while allowing sufficient area for the silicon to be clamped to the housing in a region that is far from the electromagnetically active portion of the microfabricated compliant chip **10.** This results in the clamped areas **53** being located at the edges of the microfabricated compliant chip **10** so that the transmission line can emerge from the waveguide block along the center, as shown in **Fig. 9.**

[0057] A substrate thickness of 15 μm is chosen for this design as it will ensure sufficient contact force and is electrically thin at W-Band. It is noted that at this W-band, we could have obtained a working design with modestly thicker and certainly with thinner Si. Therefore, it is not the case that 15 μm is the only or necessarily the perfect thickness at W-band. For the submillimeter probe operating at 625 GHz and above, this thickness is greater than $\lambda_d/10$. Although this electrical thickness is greater than the design guideline, full-wave electromagnetic simulations verify that there is not excessive radiation into the substrate. Once characterized, the mechanical performance of this design will inform the use of thinner substrates for higher frequency probes.

[0058] The mechanical performance of the structure of the microfabricated compliant chip **10** is analyzed with ANSYS, a finite element simulator. **Fig. 10** shows simulation results for the compliant beam **50** of the microfabricated compliant chip **10** structure under a load of 1 mN per contact tip **51.**

[0059] Fillets **54** are used adjacent to the clamped areas **53** to avoid high stress concentrations in the microfabricated compliant chip **10. Fig. 11** shows the maximum stress induced in the probe by a 3 mN force as the radius of the fillet curve is varied from 15 μm to 75 μm. The total width of the microfabricated compliant chip **10** is held constant at 750 μm. For small radii, the stress is concentrated into a tight corner, increasing the maximum stress. For the larger radii, the fillet curve consumes a large proportion of the total width of the beam and reduces the area of the clamping region **53,** again driving the maximum stress up.

[0060] A radius of 55 μm is chosen for this exemplary design. Although it is not optimum, the difference in the maximum stress from the optimum fillet radius of 35 μm is only 4 MPa. This results in the clamped areas being 220 μm wide, distributing the force over a broad area. Final dimensions of the exemplary embodiment of the microfabricated compliant chip **10** design are shown in **Fig. 9.**

[0061] The maximum stress in the silicon under this 3x1 mN load is 98 MPa. Accordingly, a deflection of 2.3 μm is produced at the tip **51.** Assuming fracture will occur at 4.5 GPa there is a safety factor of 46. This wide safety margin provides a degree of protection against user error. For instance, an excessive 20 μm deflection imposed on the microfabricated compliant chip **10** would result in a stress of 1 GPa which is still well below the expected failure point of the silicon. However, excessive deflection will result in higher forces being placed on at the contact tips **51.** This drastically reduces the lifetime of the microfabricated compliant chip **10,** and this aspect shall be discussed later in the disclosure at Example and Experimental Set No. 3.

II. FABRICATION AND MEASUREMENTS

[0062] The microfabricated compliant chips **10** were fabricated using a silicon-on insulator process developed to produce thin substrates for submillimeter-wave components, although it may be applicable for substrates greater than or less than submillimeter-wave components as well. And this process may be augmented to include vias and allow patterning of both front-side and back-side electroplated gold.

[0063] The fabrication process begins with a silicon-on-insulator wafer with a 15 μm thick device layer. Gold conductors

and beamlead areas **52** are electroplated to a thickness of 6 μm. The wafer is subsequently bonded to a carrier wafer and the handle area is removed with a combination of lapping and plasma etching. Backside alignment is used to define and etch the 20 μm wide via-holes (not shown). Gold is then plated on the backside to a thickness of 4 μm. Finally, a substrate extents etch is performed and the devices are released from the carrier wafer. Representative microfabricated compliant chips **10** are shown in **Fig. 12.**

[0064] The waveguide probe housing was machined with a Kern MMP 5-axis CNC-micromachining tool. The bottom face of the block is lapped after milling so that the distance between the probe transmission line channel and the base of the block can be precisely controlled to ±3 μm.

[0065] Mounting of the microfabricated compliant chip **10** in the waveguide block is done by handling the chips by the beamlead **52** (e.g., gold beamleads or other material as desired or required), thus avoiding damage to the silicon substrate **11.** The depth of the clamping recesses were within design specification and the probe chips were readily aligned to the block by observing when the chip dropped into place. An assembled waveguide block **23** with the mounted microfabricated compliant chip **10** (e.g., probe chip) protruding from the front face of the block is shown in **Fig. 13.** Next to it is a commercial probe provided for comparison (left side of figure).

A . Contact Resistance Measurement

[0066] Sufficient force for a low contact resistance is critical for maintaining low insertion loss and enabling DC biasing through the wafer probes. To verify that the mechanical design provides sufficient force to achieve a low contact resistance, a microfabricated compliant chip **10** with a single tip **51** was fabricated. This enables a fourwire measurement of a single contact point. The test probe is the same as shown in **Fig. 9** and scanning electron micrographs (SEMs) of worn probe tips **51** indicate a contact area 40 μm wide and 5 to 10 μm long (see **Fig. 14**). A load cell (Futek FSH02534) capable of measuring forces in the 0.2 mN to 100 mN range was fitted with a silicon substrate with gold contact pads. **Fig. 15** shows how the probe and contact substrate are designed to enable a four-wire measurement of the probe's contact resistance, $R_{contact}$. The measurements in **Fig. 16** demonstrate that a contact resistance of 0.07 Ω is achieved at 1 mN and that this resistance continues to decrease with additional force, approaching a minimum of 0.02 Ω at 55 mN.

[0067] The microfabricated compliant chip **10** fails at contact forces between 60 and 70 mN, generally cracking around the simulated point of maximum stress on the fillet. However, the failures are rarely observed as the bottom of the waveguide housing contacts the probed substrate before this force can be applied.

[0068] Clearly more than sufficient force is generated by the 15 μm thick silicon with this mechanical design. This suggests that the thinner probes required for higher frequency operation are feasible. **Table II** lists the amount of deflection required to produce 1 mN of force using this probe design with different substrate thicknesses and indicates that 5 μm thick silicon can be used if a sufficient amount of deflection can be tolerated in the landing of the microfabricated compliant chip **10.** Using the guideline that a maximum thickness of $< \lambda_d/0$ is needed to eliminate substrate mode loss, 5 μm substrates can potentially be used to 1.7 THz.

B. DC Contact Lifetime Study

[0069] An initial lifetime study was conducted to characterize the wear and damage to the gold contacts resulting from multiple contact cycles. A computer controlled stage was assembled to bring a silicon wafer coated with gold into contact with the micromachined probe while monitoring the contact force and resistance. For simplicity, a two-wire measurement was used in this study. **Fig. 17** graphically shows the measured contact resistance plotted against the number of contact cycles. The probe contact failed (indicated by the large increase in resistance) after 10,000 cycles with an applied contact force of 10 mN, whereas the lifetime is reduced to 700 cycles when a force of 25 mN is applied. The SEM photos in **Fig. 14** show the probe tip **51** before (**Fig. 14B**) the lifetime study and after failure (**Fig. 14C**). These images indicate that the failure is due to a combination of displacement of the electroplated gold and wear of the silicon supporting the contact tip. The displacement of the gold is of particular concern since the material will be pushed into the area between the ground and signal contact tips. This leads to shorting of the ground-signal-ground (GSG) probe tips **51** before the contact metal is abrasively removed, reducing the RF lifetime compared to the DC contact lifetime characterized here. This issue can be addressed by using a harder metal (such as a Gold/Cobalt alloy or Ruthenium) to form the probe tip **51,** reducing the amount of material displaced during each contact cycle.

TABLE II

BEHAVIOR OF microfabricated compliant chip (PROBE) DESIGN WITH THINNER SUBSTRATES.		
Substrate Thickness (μm)	Maximum Deflection Before Failure (μm)	Deflection for 1 mN of force (μm)
15	103	1.3

(continued)

BEHAVIOR OF microfabricated compliant chip (PROBE) DESIGN WITH THINNER SUBSTRATES.		
Substrate Thickness (μm)	Maximum Deflection Before Failure (μm)	Deflection for 1 mN of force (μm)
10	154	4.4
8	193	8.5
5	306	35
3	503	160

III. CONCLUSIONS

[0070] This Example and Experimental Set provides the design of microfabricated compliant chip **10** (i.e., micromachined probes) that can operate at submillimeter-wave frequencies. The mechanical design and characterization of the microfabricated compliant chip **10** presented here provides the foundation for the electromagnetic design, that shall be discussed later in this disclosure at Example and Experimental Set No. 2. By employing a silicon micromachining process, excellent mechanical characteristics are achieved by the choice of silicon as the mechanical material and photolithographic control over the substrate extents, enabling a robust mechanical design. Contact resistances below 0.1 Ω are measured at contact forces below 1 mN, comparable with lower frequency commercial probes. A lifetime study shows the probes are capable of forming this DC contact for over 9000 contact cycles.

Example and Experimental Results Set No. 2

I. INTRODUCTION

[0071] This Example and Experimental Set provides for, among other things, the design and characterization of a micromachined on-wafer probe for submillimeter-wave integrated circuit measurement. The Example and Experimental Set No. 1 (as provided in this disclosure above) presented the mechanical design and demonstrated that the probe produced thousands of low-resistance contacts. In this Example and Experimental Set, the RF design and performance of the probe is presented. The finite element simulation tool HFSS™ is used to model and design the various transitions required to couple from WR-1.5 rectangular waveguide to a probed object substrate. One-port measurements of the probes (microfabricated compliant chips) are presented at the WR-1.5 (500-750 GHz) band.

[0072] Two RF designs are pursued that are compatible with the same waveguide block. The designs primarily differ in the transmission line used to couple from the rectangular waveguide to the Ground-Signal-Ground (GSG) probe. Microstrip is one choice, as it is well characterized and less susceptible to loaded waveguide modes. The second design uses a lower-loss rectangular-coaxial transmission line, but is more susceptible to exciting resonances along the line.

[0073] **Fig. 18** schematically shows a detail of the coaxial probe chip **10** (i.e., microfabricated compliant chip) resting on the bottom-half of the E-plane split waveguide housing **23.** The conductors on the probe chip **10** are not visible in **Fig. 18** as they face downwards to allow contact to the probed substrate **1.** The submillimeter-wave signal couples from the rectangular waveguide **24** through an E-plane radial stub (i.e., waveguide probe) into the enclosed transmission line of the transmission circuit **30.** The transmission line emerges from the housing **23** and transitions to the coplanar waveguide probe tips **51.**

[0074] Microphotograph-like depictions of the probe chip layouts are schematically shown for the microstrip-based and coaxial-based probe chips in **Figs. 19A and 19B,** respectively.

[0075] Characterization of the micro fabricated compliant chip (probe) is done with one-port offset short measurements. Insertion loss of the probes over the WR-1.5 band (500-750 GHz) is found to be 6-10 dB and the corresponding return loss from 10-15 dB. Accordingly, the coaxial design exhibits and insertion loss 2 dB over better than the microstrip probe design.

II. PROBE DESIGN

[0076] Design of the microfabricated compliant chip (probe) primarily consists of two electromagnetic transitions: one from rectangular waveguide to a channel supported transmission line and a second from transmission line to the CPW on the probe tips. Because low insertion loss is critical to maintaining the dynamic range of the on-wafer measurement, two designs based on different transmission lines are pursued so that a lower loss design can be evaluated while still having a lower risk alternative. Details of these designs are described in the following sections of this Example and

Experimental Set.

A. Microstrip Probe Design

[0077] As described in the Example and Experimental Set No. 1 (above), the substrate **11** of the micro fabricated compliant chip (probe) is chosen to be 15 μm thick to avoid excitation of substrate modes while maintaining sufficient mechanical strength. A 50 Ω microstrip line silicon of this thickness has a conductor 12 μm wide (transmission line **31**), as schematically shown in **Fig. 20A.** To allow the same waveguide block to be compatible with both transmission line designs, the microstrip line is suspended in the channel by beam leads, and a gold layer on the backside of the substrate is used to form the ground-plane. For these dimensions and using a conductivity of electroplated gold of 6 x 10^6 (S/m), the loss is found by HFSS simulation to be 3.7 dB/mm at 625 GHz. Although this amount of loss is high, it does not prohibit the use of microstrip as the probe tips and rectangular waveguide are separated by less than 1 mm.

[0078] To couple to the GSG probe tips, a via-based microstrip to CPW transition is used. This transition is simulated to have a return loss below 15 dB from 500 to 750 GHz.

B. Coaxial Probe Design

[0079] As schematically shown in **Fig. 20B,** the coaxial-based micro fabricated compliant chip (probe) design uses a suspended substrate **11** to create a quasi-rectangular coax transmission line **31** with the channel formed by the waveguide housing as the outer conductor. To realize a 50 Ω line in this configuration the center conductor must be 35 μm wide, as shown in **Fig. 20B.** Assuming conductivities of 6 x 10^6 (S/m) for the gold center conductor and the 2 x10^7 (S/m) for the aluminum channel, a line loss of 1.5 dB/mm at 625 GHz is expected, less than half than that of the microstrip line.

[0080] A disadvantage of the coaxial line is that it suffers from coupling to spurious modes at discontinuities in the substrate width. This is an important issue because silicon tabs are placed along the length of the probe chip to align and fix the chip to the waveguide block. The shortest clamping tab length possible, 75 μm, is set by the limits of the machining process used to fabricate the waveguide blocks. For the coaxial transmission line, this length is $\lambda_g/4$ at 625 GHz, and the discontinuity in the impedance is a concern.

C. Waveguide to Transmission Line Transition

[0081] Coupling to the micro fabricated compliant (probe) chip transmission line from rectangular waveguide is accomplished by, for example, an E-plane radial-stub probe **25.** For the coaxial design, the clamping tabs are moved away from the transmission line channel in order to prevent the resonances induced by a discontinuity in the substrate width. The microstrip design, which does not suffer from this moding issue, is clamped along the length of microstrip, avoiding the need to extend the substrate across the waveguide. This allows the use of a transition similar to that used for the lower frequency prototype probe.

[0082] By extending the substrate across the waveguide for the coaxial design, the clamping area can be placed in an area away from the signal path, as shown in **Fig. 21A.** To ensure high isolation in this clamping channel, a 40 μm wide by 45 μm long via is placed at the edge of the waveguide wall. This allows the clamping tabs to be placed 150 μm back from the waveguide without significantly affecting the performance of the transition.

[0083] The clamping channel is 85 μm wide by 30 μm deep. This depth allows enough space for the 15 μm silicon with the 4 μm thick gold layers on the front and backside of the chip to be housed but does not couple to the rectangular waveguide mode. One side of the channel is designed to contact the backside gold and ground the via to the block. The channel leaves a 10 μm gap between the front side gold and the block so that future designs can incorporate built-in DC biasing by passing current through this channel to the center conductor of the probe.

[0084] The additional silicon in the waveguide makes optimization of the transition more difficult since it adds additional inductance to the total structure. A capacitive step 30 μm high and 62.5 μm wide is introduced in the waveguide wall 140 μm away from the center of the transition to compensate for the additional inductance of the waveguide structure. The back short is placed at 145 μm from the center of the radial probe. The minimum tool diameter for milling the rectangular waveguide is 75 μm, so the backshort and capacitive step have a corner rounding radius of 37.5 μm.

[0085] **Fig. 21B** schematically shows the simulated scattering parameters with reference planes the waveguide and the transmission line ports. The transmission line wave-port (Port 2 in **Fig. 21A**) is placed 300 μm away from the rectangular waveguide transition to allow energy coupled to cutoff modes at the transition to decay. The solid line shows the coaxial-based design is expected to have a -15 dB fractional bandwidth of 28% with an average insertion loss of 0.4 dB. The microstrip design shows a wider bandwidth of 32%. These simulations assume a gold conductivity for the conductors of 6x10^6 (S/m). Loss on the rectangular waveguide walls is neglected.

D. Probe to Substrate Coupling

[0086] The coupling from the CPW probe tips to the substrate's transmission line is very sensitive at submillimeter wavelengths. In particular, the length of the contact tips that extend from the probe to the DUT plays a strong role in the matching of this section. As both designs use CPW to couple to the probed substrate, only simulations for the coax design are shown. **Fig. 22A** shows the model of the coaxial line transition to the CPW probe tips contacting a probed substrate. Radiation boundaries are applied around the volume of air surrounding the probe tip to simulate an unenclosed environment and an odd-mode symmetry plane is used to reduce the model size in half.

[0087] The probe pitch is chosen to be 30 μm, center to center, based on the maximum CPW gap widths that can operate at these frequencies without excessive radiation into the substrate. The calibration wafer used in this work uses CPW dimensions of 52.5/5/10/5/52.5 μm on a silicon substrate (ε_r = 11:9) to achieve a 50 Ω line. HFSS simulations of the CPW dimension along the probe show that the width of the conductors must be 18 μm at the contact tip **51** as shown in **Fig. 22A.**

[0088] Coupling to the substrate supported CPW line is sensitive to the contact tip length. The tips must extend from the bulk of the probe, as shown in the inset of **Fig. 22A,** to focus the force of the probe onto the metal to metal interface. This break in the substrate between the conductors increases the impedance of the CPW in that region, thus creating a mismatched section of transmission line at the interface between the probe and the substrate.

[0089] The influence of the contact tip length on the coupling to the probed substrate is studied by varying the tip lengths from 5 μm to 25 μm in the model and observing the return loss at the coaxial port. **Fig. 22B** shows that for any length greater than 10 μm the return loss is greater than -15 dB. Following the trend, the best performance should be achieved with no tips. However, without tip structures to increase the pressure at the gold-to-gold contacts it will be difficult to achieve a sufficient force to achieve a low-resistance contact on all three conductors simultaneously if the probe is not perfectly parallel to the probed substrate. To verify this claim, two tip lengths, 0 μm and 10 μm, were fabricated and tested. No successful calibrations were achieved with the 0 μm tip length probes. Consequently, the 10 μm contact tip length is used for the remainder of the design.

E. Full Probe Simulation

[0090] **Fig. 23A** shows the full simulation model for the coaxial design which combines the rectangular waveguide transition and the transition to the probed substrate. The microstrip simulation is similar. A gold conductivity of $6x10^6$ (S/m) is assumed. Radiation boundaries surround the probe and probed substrate to simulate an unenclosed environment. Also may be included is the simulated s-parameters with reference planes at the rectangular waveguide ports and the CPW line on the probed substrate. The 130 μm of CPW on the substrate is de-embedded to remove the line loss from the results. Neglecting loss in the rectangular waveguide and the probe housing, the average simulated insertion losses are 1.3 dB and 2.8 dB for the coaxial and microstrip-based probe, respectively.

III. ONE-PORT PROBE CHARACTERIZATION

[0091] The submillimeter s-parameter measurement system at the University of Virginia currently consists of a one-port VNA system consisting of a Virginia Diodes Inc. WR-1.5 frequency extender module (VDI WR1.5 VNAXTXRX) interfaced to a Rohde & Schwarz ZVA40 network analyzer. Full s-parameters of the probes are characterized by de-embedding with a two-tier offset short calibration.

[0092] The initial reference plane is set at the waveguide flange of the frequency extender by measuring four waveguide standards supplied with the VDI frequency extender: a short, an eighth-wavelength offset short, a quarter-wavelength offset short and a load. The error terms of the VNA system are calculated from the over-determined system by a least-squares fit. A second reference plane is set by mounting the probe block to the frequency extender and measuring five on-wafer offset shorts with the VNA calibrated to the waveguide flange. The lengths and effective electrical length at 625 GHz are listed in **Table III.** Each reflection standard is separated by 60° at mid-band so that the five calibration standards achieve equal coverage around the Smith chart. 70 μm of CPW line between the contact pads and the calibration reference plane is included in the calibration adding approximately 0.5 dB of loss to the de-embedded S_{21} of the probes.

TABLE III

CALIBRATION STANDARD PHYSICAL AND ELECTRICAL DELAY OF THE 52.5/5/10/5/52.5 μM (ε_{eff} = 6:68) CPW DELAY SHORT LINES USED FOR CALIBRATION.		
Standard Number	Physical Length	Electrical Length at 625 GHz
1	0 μm	0°
2	18 μm	70°
3	36 μm	140°
4	54 μm	210°
5	72 μm	280°

[0093] The error parameters of the probe are extracted with the least-squares method so that all five line lengths plus redundant measurements of the same standard can be included in the calibration. **Fig. 24** shows the resulting de-embedded scattering parameters for the microstrip and coaxial probe designs, respectively. The mean insertion-loss for the coaxial design is 7.2 dB and for the microstrip design is 9.5 dB.

[0094] **Table IV** provides a detailed breakdown of the loss mechanisms of the probe from the waveguide flange to the calibrated reference plane on the probed substrate, comparing the predicted and the measured insertion loss at 625 GHz for the two probe designs. The rectangular waveguide loss of 0.076 dB/mm is a measured value and corresponds to other published waveguide losses that these frequencies. Conductor loss on the calibration substrate is modeled by HFSS and radiation into the substrate is calculated. These three losses are included in both the microstrip and coaxial designs' loss calculations.

[0095] Transmission line losses are calculated with densely meshed wave-port simulations of the transmission line geometries. Conductivities are assumed to be 6 x 10^6 (S/m) for the electroplated gold conductors and 2 x10^7 (S/m) for the milled aluminum housing.

[0096] Probe radiation losses accounts for miscellaneous loss mechanisms separate from conductor losses. This value is found by analyzing the model in **Fig. 22A** without any conductor losses. Therefore, any energy lost into this model is radiated from the probe tip, injected into the substrate or coupled to other modes when the signal transfers from the probe to the probed substrate.

[0097] The measured values differ from the expected values by 1.3- 1.8 dB. This discrepancy is likely due to the surface roughness of the structures (which was neglected in the simulations) as well as errors in the calibration producing uncertainty in the measurement of the probe. An error analysis shows that if the variation in the alignment of the probe to the standards and the repeatability of the probe is taken into account uncertainties of $\pm$1.2 dB in S_{21} at 625 GHz can be expected.

[0098] The most significant sources of loss are the rectangular waveguide (2.65 dB) and the conductor loss of the probe tips (1.2 dB). Shortening the probe tip length would reduce the associated conductor loss along the probe tip's CPW line, but this would impact the mechanical performance of the probe. The length of rectangular waveguide is largely dictated by the size of the waveguide flange used since the probe tip has to extend beyond the bottom of the waveguide flange to contact the substrate (See Example and Experimental Set No. 1). Significant reductions in the length of waveguide could be realized if a smaller flange, such as the Grammer miniature interface described by Hesler (See J. Hesler, A. Kerr, W. Grammer, and E. Wollack, "Recommendations for waveguide interfaces to 1 THZ," in 18th International Symposium on Space Terahertz Technology, 2007). This flange would reduce the diameter by half and consequently reduce the necessary length of waveguide by half.

IV. ONE-PORT CALIBRATION VERIFICATION

[0099] The de-embedded s-parameters of the probes indicate a reasonable match and insertion loss from the waveguide to the DUT. To demonstrate the probes can support a calibration on a probed substrate, a set of verification measurements were performed. The coaxial probe design is chosen as its lower insertion loss provides for greater dynamic range of the measurement. As the current measurement instrumentation in our laboratory is a one port system, we choose to measure offset shorts not included the calibration are used to verify and assess the probe performance. Five offset short-circuited lines are measured, but only four of them are used in the calibration. The last standard is de-embedded with the resulting calibration and compared against the expected phase of the offset short.

[0100] **Fig. 25A** shows different verification standards plotted on a Smith chart. This shows that there is some uncertainty in the magnitude response, but the measurement largely correspond to what is expected for the five offset short lines that are designed to be approximately 60° apart. In **Fig. 25B,** the measured phase of each line is plotted against

its corresponding simulated phase. These measurements closely follow the modeled values, with the measured response varying from the model by 6° on average. The maximum variation from the expected value of the magnitude is 3.3 dB and the phase is 30°. These discrepancies are at the upper end of frequency band, where the insertion loss of the probe increases substantially. This results in a lower accuracy for this system at these frequencies.

TABLE IV

LOSSES IN UNBIASED PROBE AT 625 GH_Z				
Design	**Structure**	**Length**	**Attenuation**	**Total Loss**
	Waveguide	34.8 mm	0.076 dB/mm	2.65 dB
	Calibration Substrate CPW (Conductor)	70 μm	5.8 dB/mm	0.41 dB
	Calibration Substrate CPW (Radiation)	70 μm	1.6 dB/mm	0.11 dB
Microstrip	Enclosed Microstrip	450 μm	3.7 dB/mm	1.7 dB
	Microstrip to CPW transition (Simulation)	N/A	N/A	0.4 dB
	Probe Microstrip	330 μm	3.6 dB/mm	1.2 dB
	Probe CPW (Conductor)	70 μm	5.3 dB/mm	0.4 dB
	Probe CPW (Radiation - Sim)	120 μm	N/A	0.1 dB
	Expected loss			7.0 dB
	Measured Loss			8.8 dB
Coaxial	Coaxial line	450 μm	1.5 dB/mm	0.68 dB
	Probe CPW (Conductor)	400 μm	3.08 dB/mm	1.23 dB
	Probe CPW (Radiation - Sim)	400 μm	N/A	0.3 dB
	Expected loss			5.4 dB
	Measured Loss			6.6 dB

V. CONCLUSIONS

[0101] This Example and Experimental Set (as well as Example and Experimental Set No.1 provided above) demonstrate, among other things, the design and measurement of the first on-wafer probe operating at 500 to 750 GHz. A silicon micromachined design is applied to achieve the necessary tolerances at these high frequencies. This Example and Experimental Set follows the design of the electromagnetic coupling structures that are compatible with the mechanical design presented in Example and Experimental Set No.1. Two designs are tested that are based on different transmission line topologies. The microstrip design resulted in higher losses, due to the thin substrate and via-based transition required to couple to the GSG probe tips. The coaxial design required a more complex rectangular waveguide coupling structure to allow for the clamped areas to be moved away from the coaxial line, but one-port measurements show insertion losses to be 1-2 dB lower than the microstrip design. Overall, insertion losses for both designs are between 6-10 dB. The microfabricated compliant chip (probe) is shown to be able to support calibrated measurements in both one and two-port configurations.

Example and Experimental Results Set No. 3

I. INTRODUCTION

[0102] As schematically shown in **Fig. 26,** the microfabricated compliant chip **10** (i.e., micromachined probe chip) is housed in an E-plane split-waveguide metal-machined block **23.** To contact the device, structure or material (not shown) on the probed substrate (not shown), the microfabricated compliant chip **10** (i.e., probe chip) extends beyond the metal housing **23** by 400 μm (chip extends beyond the housing a length of 400 μm) and terminates in coplanar waveguide (CPW) to form Ground-Signal-Ground (GSG) probe tips **51.**

[0103] A notable feature of this design is the simple, self-aligning mounting process of the microfabricated compliant chip **10** (i.e., probe chip), which does not require any adhesives (or the like). Recesses (not shown) are milled into the waveguide block **23** with a depth precision of $\pm 3\mu$m. The probe chip drops into these recesses and is subsequently

aligned to the block to better than ±5 μm precision.

[0104] **Fig. 26B** provides an enlarged partial view of the area identified in **Fig. 26A. Fig. 26C** schematically illustrates the front side of the microfabricated compliant chip **10** (i.e., probe chip). In order to provide mechanical support to the chip as pressure is applied to the probe tip **51,** the silicon substrate of the microfabricated compliant chip is clamped in or to the housing **23** (or between sections of the housing) by compressing electroplated gold **52** (e.g., beam leads) on both sides of the substrate **11.** The substrate **11** is identified by the dashed lines in **Fig. 26B**). The recesses are used to align the microfabricated compliant chip **10** (i.e., probe chip) to effectively provide Port-I, which is the waveguide connection and Port-II, which is the CPW probe tips. As noted, the waveguide **24** height b=190 μm, which is half of the waveguide (WR-1.5) width a.

[0105] This Example and Experimental Set presents the repeatability of the mounting process and the lifetime of the micro fabricated compliant chip (probe). In Experimental Set No.2 above, two designs were evaluated that couple between waveguide and the probe tips with either a microstrip or a coaxial transmission line. The results presented in this Example and Experimental Set reflect the microstrip-based design, but both designs share a similar mechanical design, so the coaxial-based design should exhibit similar behavior.

II. MECHANICAL TEST

[0106] The ultra-thin silicon is used as a substrate for the microstrip line and as a support for the mechanically active compliant beam **50.** When compliant beam **50** of the probe contacts the test wafer, the silicon deflects and generates a force at the tip **51.** The force induced by the micro fabricated compliant chip (probe) with respect to the vertical distance the probe traveled can be modeled as a linear spring, K_1 (see **Fig. 27**)

[0107] The setup as schematically shown in **Fig. 27** is used to measure the spring constant, K_1. A test wafer (i.e., object substrate **1**) is attached to a load cell (Futek® FSH0234) that is used to monitor the contact force. A motor-driven stage **81** is used to move the test wafer **1** vertically. As the stage **81** rises, the microfabricated compliant chip **50** (silicon chip) contacts with the wafer **1** and generates force at the tip **51** of the compliant beam **50** that is measured by the load cell. During this process, the load cell also deflects and can be modeled as another spring, K_2. This setup is therefore a series connected two-spring system.

[0108] Measuring the contact force with respect to the vertical motion of the stage **81** gives the total spring constant, K_{total}. A linear regression of the measured results are shown in **Fig. 28** and give K_{total} = 0:40 ± 0:02 mN/μm.

[0109] For the series connected two-spring system,

$$\frac{1}{K_{total}} = \frac{1}{K_1} + \frac{1}{K_2}.$$

The spring constant of the load cell, K_2, is independently measured, using a similar setup, to be 1.07 ± 0.07 mN/μm. Therefore, the spring constant of the probe is K_1 = 0.65 ± 0.08 mN/μm.

[0110] Previous measurements (as shown in Example and Experimental Set No. 1 above) have shown that a micromachined silicon chip achieves a low contact resistance of 0.07 Ω at 1 mN per tip. However, higher contact force (>3 mN) may be required to ensure that all three tips **51** on the GSG **55** of the microfabricated compliant chip (probe) simultaneously contact to the CPW probing pads (not shown) with low resistance of the Device Under Test (DUT) (not shown) on the object wafer, given possible non-planarity of the probe with the Device Under Test (DUT).

[0111] To determine the minimum force required for good Radio Frequency (RF) contact, the microfabricated compliant chip (e.g., micromachined probe) is connected to a one-port WR-1.5 frequency extension unit from Virginia Diodes Inc. (VDI WR1.5 VNAXTXRX) with a Rhode and Schwarz ZVA- 40 network analyzer as the backend. The network analyzer (not shown) is used to measure the reflection coefficient at the waveguide connection, Port-I of the microfabricated compliant chip (i.e., probe).

[0112] The gold contact pad on the test wafer shorts the CPW probe GSG tips as the stage moves up and the wafer contacts the probe. The phase of the reflection coefficient at Port-I responds to the change in probe tip contact and settles during this process. The contact force where the reflection coefficient settles is defined as the minimum contact force required for RF probing. Test results show that there is a dramatic change in the phase of the measured reflection coefficient when the contact force increases from 0 to 0.2 mN, and as the contact force increases, the reflection coefficient gradually settles. At 15 mN, the phase change in reflection coefficient with respect to contact force is within the phase measurement uncertainty.

III. RF MEASUREMENT

[0113] A two-tier calibration technique is used to obtain the scattering parameters of the microfabricated compliant chip (probe). With this method, the network analyzer is initially calibrated to a reference plane coincident with the frequency extension unit test port, using a waveguide short and delayed shorts of four different lengths. Because waveguide loads are generally unavailable in the WR-1.5 band, only waveguide delayed shorts, which can be accurately characterized from their dimensions, are used as calibration standards.

[0114] After the first tier in the calibration procedure, the microfabricated compliant chip (probe) is attached to the network analyzer test port. The second-tier calibration is performed by terminating the CPW probe tips with on-wafer calibration standards, a CPW short and four CPW delayed shorts that can also be accurately characterized from their dimensions. During second-tier calibration, a 20 mN contact force is used to ensure any non-planarity is overcome. The reflection coefficient measured at the network analyzer test port, Γ^M, is related to the scattering parameters of the probe, S_{ij}, and the reflection coefficient of the CPW short, Γ_{l}, by the bilinear transform,

$$\Gamma^M = S_{11} + \frac{S_{21}S_{12}\Gamma_{\mathrm{l}}}{1 - S_{22}\Gamma_{\mathrm{l}}}.$$

[0115] By measuring the reflection coefficient of the microfabricated compliant chip (probe) with these on-wafer calibration standards, and noting that the probe is a reciprocal network, the scattering parameters of the probe are obtained. The S-parameters of a micromachined probe obtained by this one-port two-tier calibration method are shown in **Fig. 29.**

[0116] The insertion loss varies from 8 to 12 dB and the return loss is larger than 10 dB over most of the band from 500 to 750 GHz. The ripple in S_{11} is due to a standing wave in the rectangular waveguide because of misalignment at the waveguide connection. The uncertainty in this measurement is due to positioning error and noise in the network analyzer and can be quantified by the method detailed in reference T. Reck, L. Chen, C. Zhang, C. Groppi, H. Xu, A. Arsenovic, S. Barker, A. Lichtenberger, and R. Weikle, "Calibration accuracy of a 625 GHz on-wafer probe," in 76th ARFTG Microwave Measurement Conference Digest, Dec. 2010. The uncertainty in S_{21} is calculated and shown in **Fig. 29.**

IV. REPEATABILITY

[0117] As shown in **Fig. 26,** the microfabricated compliant chip **10** (i.e., probe chip) is aligned by the recesses in the waveguide block **23** to within ± 5 μm. The fabrication process also introduces probe chip variations across the wafer, especially from misalignment in lithography.

[0118] The uncertainty both in chip fabrication and assembly will result in variations in the probe performance. The sensitivity of the probe to the alignment precision is measured by mounting the same probe chip to a waveguide block three times and measuring the corresponding scattering parameters. These measurement results are shown in **Fig. 30.** The probe performance changes slightly but within the measurement uncertainty. The return loss at the CPW port (**Fig. 30C**) is degraded because of slightly oversized pins used in these measurements to align the two halves of the waveguide block.

[0119] The microfabricated compliant chip (probe) performance with three different probe chips of the same design is shown in **Fig. 31.** The performance variations are due to the uncertainty both in chip fabrication and assembly. Therefore the variations are slightly larger but still within the measurement uncertainty. In these measurements the oversized pins were replaced resulting in better matching at the CPW port (**Fig. 31C**).

V. RELIABILITY TESTS

[0120] The microfabricated compliant chip (on-wafer probes) are designed to skate on the contact pad to break through surface contamination and to ensure a low resistance contact. However, this skating action adds to the wear of the probes. How fast the probes wear depends on factors including contact force as well as probe tip and bond pad materials. As shown in **Fig. 26,** the CPW probe tips **51** are fabricated on the ultra-thin silicon substrate **11** by plated gold, which is 4μm thick. Most contact pads of submillimeter-wave integrated circuits also use plated gold.

[0121] The setup in **Fig. 27** is used again to test the lifetime of the microfabricated compliant chip **10** (e.g., micromachined probes). The motor stage **81** is raised up gradually until the contact force reaches 20 mN. Then the motor stage **81** is lowered until compliant beam **50** of the microfabricated compliant chip **10** (probe) and object substrate **1** are separated. This completes one contact cycle. The scattering parameters of the micromachined probe **10** are measured initially and after every 1,000 contact cycles by a one-port two-tier calibration. The measured results are shown in **Fig. 32.** The microfabricated compliant chip (micromachined probe) maintained consistent performance through 5,000 con-

tacts and then was found to have degraded upon testing after 6,000 contacts.

[0122] Scanning electron microscope images of the probe tips **51** after 10, 3,000 and 6,000 contacts are shown in **Figs. 33A, 33B, and 33C,** respectively. The images show that the probe tips **51** picked up debris from the contact pad (of the DUT) and that this debris built up in the gap between the GSG probe tips **51,** which eventually will cause the micro fabricated compliant chip (probe) to fail in a short circuit.

VI. CONCLUSION

[0123] These particular measured results prove the feasibility of a reliable microfabricated compliant chip (on-wafer probe) in the terahertz frequency range (e.g., 500-750 GHz). At 20 mN contact force, the microfabricated compliant chip (micromachined probe) is capable of more than 5,000 contacts with consistent RF performance. This microfabricated compliant chip (probe) will significantly reduce the time and cost of submillimeter-wave and terahertz frequency monolithic integrated circuits testing.

REFERENCES

[0124]

[1] W. Deal, "Solid-state amplifiers for terahertz electronics," in Proceedings of the IEEE MTT-S International Microwave Symposium, 2010.

[2] J. Hacker, M. Seo, A. Young, Z. Griffith, M. Urteaga, T. Reed, and M. Rodwell., "THz MMICs based on InP HBT technology," in Proceedings of the IEEE MTT-S International Microwave Symposium, 2010.

[3] A. Fung, D. Dawson, L. Samoska, K. Lee, T. Gaier, P. Kangaslahti, C. Oleson, A. Denning, Y. Lau, and G. Boll, "Two-port vector network analyzer measurements in the 218-344 and 356-500-GHz frequency bands," Microwave Theory and Techniques, IEEE Transactions on, vol. 54, no. 12, pp. 4507 -4512, dec. 2006.

[4] S. Liu and G. Boll, "A new probe for w-band on-wafer measurements," in Microwave Symposium Digest, 1993., IEEE MTT-S International, 1993, pp. 1335 - 1338 vol.3.

[5] R. Bass, A. Lichtenberger, R. Weikle, S. Pan, E. Bryerton, J. Kooi, and C. Walker, "Ultra-thin silicon chips for submillimeter-wave applications," in Proceedings of the Fifteenth International Symposium on Space THz Technology, mar. 2004.

[6] J. W. Kooi, G. Chattopadhyay, S. Withington, F. Rice, J. Zmuidzinas, C. Walker, and G. Yassin, "A full-height waveguide to thinfilm microstrip transition with exceptional RF bandwidth and coupling efficiency," International Journal of Infrared and Millimeter Waves, vol. 24, no. 3, pp. 261-284, mar. 2003.

[7] E. M. Godshalk, "Wafer probing at w-band," sep. 1993, pp. 848 -850.

[8] "The infinity probe for on-wafer device characterization and modeling to 110 GHZ," Cascade Microtech, Tech. Rep., 2004.

[9] "Infinity probe: high-frequency performance with low, stable contact resistance," Cascade Microtech, Inc, Beaverton, Oregon 97006, Tech. Rep., 2008.

[10] J. Schimkat, "Contact measurements providing basic design data for microrelay actuators," Sensors and Actuators A: Physical, vol. 73, no. 1-2, pp. 138 - 143, 1999. [Online]. Available: http://www.sciencedirect.com/science/article/B6THG- 3WWKPDW-1F/2/27c17f2b6bd61b893f706210565ca324

[11] I. Chasiotis, C. Bateson, K. Timpano, A. McCarty, N. Barker, and J. Stanec, "Strain rate effects on the mechanical behavior of nanocrystalline Au films," Thin Solid Films, vol. 515, no. 6, pp. 3183 - 3189, 2007, tMS 2005 - Mechanical Behaviour of Thin Films and Small Structures - TMS 2005. [Online]. Available: http://www.sciencedirect.com/science/article/B6TW0- 4JCBN4F-5/2/0d8c70a8e8b0fc0b3ac34377f55b75bb.

[12] D. Son, J.-J. Kim, T. W. Lim, and D. Kwon, "Evaluation of fatigue strength of LIGA nickel film by microtensile tests," Scripta Materialia, vol. 50, pp. 1265-1269, May 2004.

[13] "Fused silica," Del Mar Ventures, Tech. Rep., 2007, http://www.sciner.com/Opticsland/FS.htm. [Online]. Available: http://www.sciner.com/Opticsland/FS.htm

[14] K. Hjort, J. Soderkvist, and J. A. Schweitz, "Gallium arsenide as a mechanical material," Journal of Micromechanics and Microengineering, vol. 4, no. 1, p. 1, 1994. [Online]. Available: http://stacks.iop.org/0960-1317/4/i=1/a=001

[15] H. Belsinger and et al., "A fracture criterion for gallium arsenide wafers," Engineering Fracture Mechanics, vol. 48, no. 2, pp. 199-205, May 1994.

[16] "Aluminum oxide," Accuratus, Tech. Rep., 2002, http://www.accuratus.com/alumox.html. [Online]. Available: http://www.accuratus.com/alumox.html

[17] "Silicon nitride," Accuratus, Tech. Rep., 2002, http://www.accuratus.com/silinit.html. [Online]. Available: http://www.accuratus.com/silinit.html

>Kap "Kapton polyimide film," Du Pont, Tech. Rep., 2010, http://www2.dupont.com/Kapton/. [Online]. Available: http://www2.dupont.com/Kapton/

[19] J. S. Danel and G. Delapierre, "Quartz: a material for microdevices," Journal of Micromechanics and Microengineering, vol. 1, no. 4, p. 187, 1991. [Online]. Available: http://stacks.iop.org/0960-1317/1/i=4/a=001

[20] X. Li, T. Kasai, S. Nakao, H. Tanaka, T. Ando, M. Shikida, and K. Sato, "Measurement for fracture toughness of single crystal silicon film with tensile test,"Sensors and Actuators A: Physical, vol. 119, no. 1, pp. 229 - 235, 2005. [Online]. Available: http://www.sciencedirect.com/science/article/B6THG-4CY0GYV - 1/2/390b1252940707c4776e9761c6cc3a5b

[21] M. Afsar, H. Chi, and X. Li, "Millimeter wave complex refractive index, complex dielectric permittivity and loss tangent of high purity and compensated silicon," in Precision Electromagnetic Measurements, 1990. CPEM '90 Digest., Conference on, 11-14 1990, pp. 238 -239.

[22] F. P. Beer, J. E. Russell Johnston, and J. T. DeWolf, Mechanics of Materials. McGraw-Hill, 2002.

[23] M. Riaziat, R. Majidi-Ahy, and I.-J. Feng, "Propagation modes and dispersion characteristics of coplanar waveguides," Microwave Theory and Techniques, IEEE Transactions on, vol. 38, no. 3, pp. 245 -251, mar. 1990.

[24] L. Chen, C. Zhang, T. J. Reck, C. Groppil, A. Arsenovic, A. Lichtenberger, R. M. Weikle, and N. S. Barker, "Terahertz micromachined onwafer probes: Repeatability and robustness," in International Microwave Symposium, 2011, accepted.

[25] E. Rabinowicz, Friction and Wear of Materials. John Wiley & Sons, Inc., 1995.

[26] A. Broue, J. Dhennin, F. Courtade, P.-L. Charvet, P. Pons, X. Lafontan, and R. Plana, "Thermal and topological characterization of Au, Ru and Au/Ru based MEMS contacts using nanoindenter," pp. 544 -547, 2010.

[27] Z. Zhou and K. Melde, "Development of a broadband coplanar waveguide-to-microstrip transition with vias," Advanced Packaging, IEEE Transactions on, vol. 31, no. 4, pp. 861 -872, nov. 2008.

[28] T. Reck, L. Chen, C. Zhang, C. Groppi, H. Xu, A. Arsenovic, S. Barker, A. Lichtenberger, and R. Weikle, "Micromachined on-wafer probes," Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International, pp. 65 -68, may 2010.

[29] C. Risacher, V. Vassilev, A. Pavolotsky, and V. Belitsky, "Waveguideto-microstrip transition with integrated bias-T," IEEE Microwave and Wireless Components Letters, vol. 13, no. 7, pp. 262-264, jul. 2003.

[30] D. Kasilingam and D. Rutledge, "Surface-wave losses of coplanar tranmission lines," Microwave Symposium Digenst, MTT-S International, vol. 83, no. 1, pp. 113-116, may 1983.

[31] J. Ou and M. Caggiano, "Determine two-port s-parameters from oneport measurements using calibration substrate standards," may. 2005, pp. 1765 - 1768 Vol. 2.

[32] K. Wong, "Uncertainty analysis of the weighted least squares VNA calibration," ARFTG Microwave Measurements Conference, Fall 2004. 64th, pp. 23 - 31, Dec 2004.

[33] "Virginia Diodes Inc. waveguide band designations," Virginia Diodes Inc., Tech. Rep., 2009, http://www.virginiadiodes.com/.

[34] T. Reck, L. Chen, C. Zhang, C. Groppi, H. Xu, A. Arsenovic, S. Barker, A. Lichtenberger, and R. Weikle, "Calibration accuracy of a 625 GHZ on-wafer probe," in 76th ARFTG Microwave Measurement Conference Digest, Dec. 2010.

[35] J. Hesler, A. Kerr, W. Grammer, and E. Wollack, "Recommendations for waveguide interfaces to 1 THZ," in 18th International Symposium on Space Terahertz Technology, 2007.

[36] P. Siegel, "Terahertz technology," Microwave Theory and Techniques, IEEE Transactions on, vol. 50, pp. 910-928, Mar 2002.

[37] R. Lai, X. Mei, W. Deal, W. Yoshida, Y. Kim, P. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, et al., "Sub 50 nm InP HEMT Device with fmax Greater than 1 THz," in IEEE International Electron Devices Meeting, 2007. IEDM 2007, pp. 609-611,2007.

[38] L. Samoska, W. Deal, G. Chattopadhyay, D. Pukala, A. Fung, T. Gaier, M. Soria, V. Radisic, X. Mei, and R. Lai, "A Submillimeter-Wave HEMT Amplifier Module With Integrated Waveguide Transitions Operating Above 300 GHz," Microwave Theory and Techniques, IEEE Transactions on, vol. 56, pp. 1380 -1388, june 2008.

[39] A. Fung, D. Dawson, L. Samoska, K. Lee, C. Oleson, and G. Boll, "On-wafer vector network analyzer measurements in the 220-325 GHz frequency band," in Microwave Symposium Digest, 2006. IEEE MTT-S International, pp. 1931-1934, IEEE, 2007.

[40] T. J. Reck, L. Chen, C. Zhang, C. Groppi, H. Xu, A. Arsenovic, N. S. Barker, A. Lichtenberger, and R. M. Weikle, "Micromachined on wafer probes," in Microwave Symposium Digest, 2010., IEEE MTT-S International, June 2010.

[41] R. Bass, A. Lichtenberger, R. Weikle, S. Pan, E. Bryerton, J. Kooi, and C. Walker, "Ultra-thin silicon chips for submillimeter-wave applications," in Proceedings of the Fifteenth International Symposium on Space THz Technology, March 2004

[42] U.S. Patent No. US 4,727,319, Shahriary, I., "Apparatus for On-Wafer Tasting of Electrical Circuits", February 23, 1988.

[43] U.S. Patent No.US 5,003,253, Majidi-Ahy, et al., "Millimeter-Wave Active Probe System", March 26, 1991.
[44] U.S. Patent No. US 6,759,859 B2, Deng, et al., "Resilient and Rugged Multi-Layered Probe", July 6, 2004.
[45] U.S. Patent No. US 6,930,497 B2, Deng, et al., "Flexible Multi-Layered Probe for Measuring a Signal from an Object", August 16, 2005.
[46] U.S. Patent Application Publication No. US 2003/0112024 A1, Deng, et al., "Resilient and Rugged Probe", June 19, 2003.
[47] U.S. Patent Application Publication No. US 2004/0189334 A1, Deng, et al., "Flexible Multi-Layered Probe", September 30, 2004.
[48] U.S. Patent Application Publication No. US 2005/0201683 A1, Ghiron, et al., September 15, 2005.
[49] U.S. Patent No. 7,233,160 B2, Hayden, et al., "Wafer Probe", June 19, 2007.
[50] U.S. Patent No. 7,456,646 B2, Hayden, et al., "Wafer Probe", November 25, 2008.
[51] U.S. Patent No. 7,495,461, B2, Hayden, et al., "Wafer Probe", February 24, 2009.
[52] U.S. Patent No. 6,242,930 B1, Matsunaga, et al., "High-Frequency Probe Capable of Adjusting Characteristic Impedance in End Part and Having the End Part Detachable", June 5, 2001.
[53] U.S. Patent No. 4,849,689, Gleason, et al., "Microwave Wafer Probe Having Replaceable Probe Tip", July 18, 1989.
[54] U.S. Patent No. 7,619,419 B2, Campbell, R., "Wideband Active-Passive Differential Signal Probe", November 17, 2009.
[55] U.S. Patent No. 4,641,140, Heckaman, et al., "Miniaturized Microwave Transmission Link", February 3, 1987.
[56] U.S. Patent No. 4,894,612, Drake, et al., "Soft Probe for Providing High Speed On-Wafer Connections to a Circuit", January 16, 1990.
[57] U.S. Patent No. 7,504,842 B2, Schwindt, R., "Probe Holder for Testing of a Test Device", March 17, 2009.
[58] U.S. Patent No. 5,477,159, Hamling, D., "Integrated Circuit Probe Fixture with Detachable High Frequency Probe Carrier", December 19, 1995.
[59] U.S. Patent No. 5,231,349, Majidi-Ahy, et al., "Millimeter-Wave Active Probe System", July 27, 1993.
[60] EP Patent Application Publication No. 0 367 542 A3, Gleason, et al., "Microwave Wafer Probe Having Replaceable Probe Tip", May 9, 1990; Application No. 89311203.7, filed October 30, 1989.
[61] EP Patent Application Publication No. 0 367 542 A2, Gleason, et al., "Microwave Wafer Probe Having Replaceable Probe Tip". May 9, 1990; Application No. 89311203.7, filed October 20, 1989.
[62] U.S. Patent No. 7,427,868, B2, Strid, et al., "Active Wafer Probe", September 23, 2008.
[63] U.S. Patent No. 7,449,899 B2, Campbell, et al., "Probe for High Frequency Signals", November 11, 2008.
[64] U.S. Patent No. 4,827,211 B2, Strid, et al., "Wafer Probe", May 2, 1989.
[65] U.S. Patent No. 7,304,488 B2, Gleason, et al., "Shielded Probe for High-Frequency Testing of a Device Under Test", December 4, 2007.
[66] U.S. Patent No. 7,436,194 B2, Gleason, et al., "Shielded Probe with Low Contact Resistance for Testing a Device Under Test", October 14, 2008.
[67] U.S. Patent No. 7,501,842, B2, Gleason, et al., "Shielded Probe for Testing a Device Under Test", March 10, 2009.
[68] U.S. Patent Application Publication No. US2008/0042671 A1, Gleason, et al., "Probe for Testing a Device Under Test", February 21, 2008; U.S. Patent Application Serial No. 11/975,471, filed October 19, 2007.
[69] International Patent Application Publication No. WO 2004/107401 A2, Gleason, et al., "Probe for Testing a Device Under Test", December 9, 2004; International Patent Application Serial No. PCT/US2004/012806, filed April 26, 2004.
[70] U.S. Patent No. 5,565,788, Burr, et al., "Coaxial Wafer Probe with Tip Shielding", October 15, 1996.
[71] U.S. Patent No. 7,498,829 B2, Gleason, et al., "Shielded Probe for Testing a Device Under Test", March 3, 2009.
[72] U.S. Patent No. 7,394,269 B2, Gleason, et al., "Probe for Testing a Device Under Test", July 1, 2008.
[73] U.S. Patent No. 7,271,603 B2, Gleason, et al., "Shielded Probe for Testing a Device Under Test", September 18, 2007.
[74] U.S. Patent No. 7,057,404 B2, Gleason, et al., "Shielded Probe for Testing a Device Under Test", June 6, 2006.
[75] U.S. Patent No. 7,688,097 B2, Hayden, et al., "Wafer Probe", March 30, 2010.
[76] U.S. Patent No. 7,898,273, B2, "Gleason, et al., "Probe for Testing a Device Under Test", March 1, 2011.

[0125] It should be understood that the above dimensions are exemplary for the illustrated applications, and should not be construed as limiting the invention. While remaining within the scope of the present invention, actual dimensions may vary and may be influenced by a variety of factors and limitations-including the present invention system, devices and methods as well as environmental factors or device under test (DUT) factors. Accordingly, various systems, methods, and devices (including dimensions) may be employed within the context of the present invention.

[0126] Unless clearly specified to the contrary, there is no requirement for any particular described or illustrated activity or element, any particular sequence or such activities, any particular size, speed, material, duration, contour, dimension

or frequency, or any particularly interrelationship of such elements. Moreover, any activity can be repeated, any activity can be performed by multiple entities, and/or any element can be duplicated. Further, any activity or element can be excluded, the sequence of activities can vary, and/or the interrelationship of elements can vary. It should be appreciated that aspects of the present invention may have a variety of sizes, contours, shapes, compositions and materials as desired or required.

[0127] In summary, while the present invention has been described with respect to specific embodiments, many modifications, variations, alterations, substitutions, and equivalents will be apparent to those skilled in the art. Indeed, various modifications of the present invention, in addition to those described herein, will be apparent to those of skill in the art from the foregoing description and accompanying drawings. The scope of the invention is defined by the appended claims.

[0128] Still other embodiments will become readily apparent to those skilled in this art from reading the above-recited detailed description and drawings of certain exemplary embodiments. Moreover, any activity can be repeated, any activity can be performed by multiple entities, and/or any element can be duplicated. Further, any activity or element can be excluded, the sequence of activities can vary, and/or the interrelationship of elements can vary. Unless clearly specified to the contrary, there is no requirement for any particular described or illustrated activity or element, any particular sequence or such activities, any particular size, speed, material, dimension or frequency, or any particularly interrelationship of such elements. Accordingly, the descriptions and drawings are to be regarded as illustrative in nature, and not as restrictive. Moreover, when any number or range is described herein, unless clearly stated otherwise, that number or range is approximate. When any range is described herein, unless clearly stated otherwise, that range includes all values therein and all sub ranges therein.

Claims

1. A device for probing a structure on a surface of an object substrate (1), said device comprising:
a monolithic microfabricated compliant chip (10), wherein said microfabricated compliant chip comprises integrated electrical interconnects (20, 30, 50), and said microfabricated compliant chip is configured to:

   be secured to a housing (23) by clamping said microfabricated compliant chip in the housing (23);
   be electrically interconnected to a measurement instrument (22); and
   contact the structure on a surface of an object substrate (1).

2. The device of claim 1, wherein said microfabricated compliant chip is provided with clamping tabs (71).

3. The device of claim 1, wherein said integrated electrical interconnects of said microfabricated compliant chip comprise:

   at least one compliant beam (50);
   at least one transmission circuit (30); and
   a waveguide transition element (20), wherein said at least one transmission circuit is a transmission line channel suitable to electrically interconnect said at least one compliant beam with said waveguide transition element, and wherein the waveguide transition element (20) is configured to be electrically interconnected with the measurement instrument (22) by way of a waveguide (24).

4. The device of claim 3, wherein said at least one compliant beam comprises:
at least one contact tip (51), wherein said at least one contact tip is electrically interconnected with said at least one compliant beam, and wherein said at least one contact tip is configured to contact the structure on a surface of an object substrate when pressed against it.

5. The device of claim 4, wherein said at least one contact tip is configured to be compliant when said contact tip contacts the structure on a surface of an object

6. The device of claim 4, further comprising a plurality of said contact tips configured as a coplanar waveguide, "CPW", in communication with said at least one transmission circuit.

7. The device of claim 3, wherein said at least one compliant beam comprises a Ground-Signal-Ground, "GSG", configuration.

8. The device of claim 3, wherein said integrated electrical interconnects of said microfabricated compliant chip further comprise:
at least one of at least one bias current circuit or at least one bias voltage circuit, wherein said at least one bias current circuit or at least one bias voltage circuit is configured to electrically interconnect with the structure on a surface of an object substrate when said at least one compliant beam makes contact with said structure on a surface of an object substrate.

9. The device of claim 1, further comprising:
a secondary device for probing the structure on a surface of an object substrate, said secondary device comprising a secondary microfabricated compliant chip, wherein said secondary microfabricated compliant chip comprises secondary integrated electrical interconnects, and wherein said secondary microfabricated compliant chip being configured to be secured by a secondary housing.

10. The device of claim 1, wherein the microfabricated compliant chip (10) is configured to be secured to the housing (23) by detachably engaging it.

11. The device of claim 1 or 10, wherein said housing is configured to be reusable when said microfabricated compliant chip is detached and replaced with another microfabricated compliant chip.

12. A method of testing a structure on a surface of an object substrate, wherein said testing method comprises:

electrically probing the surface of an object substrate using a device according to any one of the preceding claims; and
electrically interconnecting the device to a measurement instrument.

13. The method of claim 12, wherein said housing is configured to be reusable when said microfabricated compliant chip is detached and replaced with another microfabricated compliant chip.

Patentansprüche

1. Vorrichtung zum Sondieren einer Struktur auf einer Fläche eines Objektsubstrats (1), wobei die Vorrichtung Folgendes umfasst:
einen monolithischen mikrogefertigten konformen Chip (10), wobei der mikrogefertigte konforme Chip integrierte elektrische Leiterbahnen (20, 30, 50) umfasst und der mikrogefertigte konforme Chip dazu ausgelegt ist:

durch Klemmen des mikrogefertigten konformen Chips in einem Gehäuse (23) in dem Gehäuse (23) befestigt zu sein;
mit einem Messinstrument (22) elektrisch verbunden zu sein und
die Struktur auf einer Fläche eines Objektsubstrats (1) zu berühren.

2. Vorrichtung nach Anspruch 1, wobei der mikrogefertigte konforme Chip mit Klemmlaschen (71) versehen ist.

3. Vorrichtung nach Anspruch 1, wobei die integrierten elektrischen Leiterbahnen des mikrogefertigten konformen Chips Folgendes umfassen:

mindestens einen konformen Strahl (50);
mindestens eine Übertragungsschaltung (30) und
ein Lichtwellenleiterübergangselement (20), wobei die mindestens eine Übertragungsschaltung ein Übertragungsleitungskanal ist, der geeignet ist, den mindestens einen konformen Strahl mit dem Lichtwellenleiterübergangselement zu verbinden, und wobei das Lichtwellenleiterübergangselement (20) dazu ausgelegt ist, mit dem Messinstrument (22) mittels eines Lichtwellenleiters (24) elektrisch verbunden zu sein.

4. Vorrichtung nach Anspruch 3, wobei der mindestens eine konforme Strahl Folgendes umfasst:
mindestens eine Kontaktspitze (51), wobei die mindestens eine Kontaktspitze mit dem mindestens einen konformen Strahl elektrisch verbunden ist und wobei die mindestens eine Kontaktspitze dazu ausgelegt ist, die Struktur auf einer Fläche eines Objektsubstrats zu berühren, wenn sie dagegen gedrückt wird.

5. Vorrichtung nach Anspruch 4, wobei die mindestens eine Kontaktspitze dazu ausgelegt ist, konform zu sein, wenn die Kontaktspitze die Struktur auf einer Fläche eines Objektsubstrats berührt, wenn sie dagegen gedrückt wird.

6. Vorrichtung nach Anspruch 4, die ferner eine Vielzahl der Kontaktspitzen umfasst, die als ein koplanarer Lichtwellenleiter, "CPW", ausgelegt sind, der mit der mindestens einen Übertragungsschaltung in Kommunikation steht.

7. Vorrichtung nach Anspruch 3, wobei der mindestens eine konforme Strahl eine Masse-Signal-Masse("GSG")-Auslegung umfasst.

8. Vorrichtung nach Anspruch 3, wobei die integrierten elektrischen Leiterbahnen des mikrogefertigten konformen Chips ferner Folgendes umfassen:
mindestens eines von mindestens einer Vorstromschaltung oder mindestens einer Vorspannungsschaltung, wobei die mindestens eine Vorstromschaltung oder die mindestens eine Vorspannungsschaltung dazu ausgelegt ist, mit der Struktur auf einer Fläche eines Objektsubstrats elektrisch verbunden zu sein, wenn der mindestens eine konforme Strahl die Struktur auf einer Fläche eines Objektsubstrats berührt.

9. Vorrichtung nach Anspruch 1, die ferner Folgendes umfasst:
eine sekundäre Vorrichtung zum Sondieren der Struktur auf einer Fläche eines Objektsubstrats, wobei die sekundäre Vorrichtung einen sekundären mikrogefertigten konformen Chip umfasst, wobei der sekundäre mikrogefertigte konforme Chip sekundäre integrierte elektrische Leiterbahnen umfasst und wobei der sekundäre mikrogefertigte konforme Chip dazu ausgelegt ist, durch ein sekundäres Gehäuse befestigt zu sein.

10. Vorrichtung nach Anspruch 1, wobei der mikrogefertigte konforme Chip (10) dazu ausgelegt ist, durch lösbares Eingreifen darin am Gehäuse (23) befestigt zu sein.

11. Vorrichtung nach Anspruch 1 oder 10, wobei das Gehäuse dazu ausgelegt ist, wiederverwendbar zu sein, wenn der mikrogefertigte konforme Chip gelöst und durch einen anderen mikrogefertigten konformen Chip ersetzt wird.

12. Verfahren zum Testen einer Struktur auf einer Fläche eines Objektsubstrats, wobei das Testverfahren Folgendes umfasst:

elektrisches Sondieren der Fläche eines Objektsubstrats unter Verwendung einer Vorrichtung gemäß einem der vorstehenden Ansprüche und
elektrisches Verbinden der Vorrichtung mit einem Messinstrument.

13. Verfahren nach Anspruch 12, wobei das Gehäuse dazu ausgelegt ist, wiederverwendbar zu sein, wenn der mikrogefertigte konforme Chip gelöst und durch einen anderen mikrogefertigten konformen Chip ersetzt wird.

Revendications

1. Dispositif destiné à sonder une structure sur une surface d'un substrat d'objet (1), ledit dispositif comprenant :
une puce souple micro-fabriquée monolithique (10), dans lequel ladite puce souple micro-fabriquée comprend des interconnexions électriques intégrées (20, 30, 50), et ladite puce souple micro-fabriquée est configurée de manière à :

être fixée à un boîtier (23), en serrant ladite puce souple micro-fabriquée dans le boîtier (23) ;
être interconnectée électriquement à un instrument de mesure (22) ; et
entrer en contact avec la structure sur une surface d'un substrat d'objet (1).

2. Dispositif selon la revendication 1, dans lequel ladite puce souple micro-fabriquée est munie de languettes de serrage (71).

3. Dispositif selon la revendication 1, dans lequel lesdites interconnexions électriques intégrées de ladite puce souple micro-fabriquée comprennent :

au moins une barre souple (50) ;
au moins un circuit de transmission (30) ; et
un élément de transition de guide d'ondes (20), dans lequel ledit au moins un circuit de transmission est un

canal de ligne de transmission pertinent pour interconnecter électriquement ladite au moins une barre souple avec ledit élément de transition de guide d'ondes, et dans lequel l'élément de transition de guide d'ondes (20) est configuré de manière à être interconnecté électriquement avec l'instrument de mesure (22) au moyen d'un guide d'ondes (24).

4. Dispositif selon la revendication 3, dans lequel ladite au moins une barre souple comprend :
au moins une pointe de contact (51), dans lequel ladite au moins une pointe de contact est électriquement interconnectée avec ladite au moins une barre souple, et dans lequel ladite au moins une pointe de contact est configurée de manière à entrer en contact avec la structure sur une surface d'un substrat d'objet lorsqu'elle est pressée contre celui-ci.

5. Dispositif selon la revendication 4, dans lequel ladite au moins une pointe de contact est configurée de manière à être déformable lorsque ladite pointe de contact entre en contact avec la structure sur une surface d'un substrat d'objet lorsqu'elle est pressée contre celui-ci.

6. Dispositif selon la revendication 4, comprenant en outre une pluralité desdites pointes de contact configurées en tant qu'un guide d'ondes coplanaire, « CPW », en communication avec ledit au moins un circuit de transmission.

7. Dispositif selon la revendication 3, dans lequel ladite au moins une barre souple comprend une configuration « Terre-Signal-Terre », « GSG ».

8. Dispositif selon la revendication 3, dans lequel lesdites interconnexions électriques intégrées de ladite puce souple micro-fabriquée comprennent en outre :
au moins un circuit parmi au moins un circuit de courant de polarisation et au moins un circuit de tension de polarisation, dans lequel ledit au moins un circuit de courant de polarisation ou ledit au moins un circuit de tension de polarisation est configuré de manière à s'interconnecter électriquement avec la structure sur une surface d'un substrat d'objet lorsque ladite au moins une barre souple entre en contact avec ladite structure sur une surface d'un substrat d'objet.

9. Dispositif selon la revendication 1, comprenant en outre :
un dispositif secondaire destiné à sonder la structure sur une surface d'un substrat d'objet, ledit dispositif secondaire comprenant une puce souple micro-fabriquée secondaire, dans lequel ladite puce souple micro-fabriquée secondaire comprend des interconnexions électriques intégrées secondaires, et dans lequel ladite puce souple micro-fabriquée secondaire est configurée de manière à être fixée par un boîtier secondaire.

10. Dispositif selon la revendication 1, dans lequel la puce souple micro-fabriquée (10) est configurée de manière à être fixée au boîtier (23) en la mettant en prise de manière détachable.

11. Dispositif selon la revendication 1 ou 10, dans lequel ledit boîtier est configuré de manière à être réutilisable lorsque ladite puce souple micro-fabriquée est détachée et remplacée par une autre puce souple micro-fabriquée.

12. Procédé de test d'une structure sur une surface d'un substrat d'objet, dans lequel ledit procédé de test comprend les étapes ci-dessous consistant à :

sonder électriquement la surface d'un substrat d'objet en utilisant un dispositif selon l'une quelconque des revendications précédentes ; et
interconnecter électriquement le dispositif avec un instrument de mesure.

13. Procédé selon la revendication 12, dans lequel ledit boîtier est configuré de manière à être réutilisable lorsque ladite puce souple micro-fabriquée est détachée et remplacée par une autre puce souple micro-fabriquée.

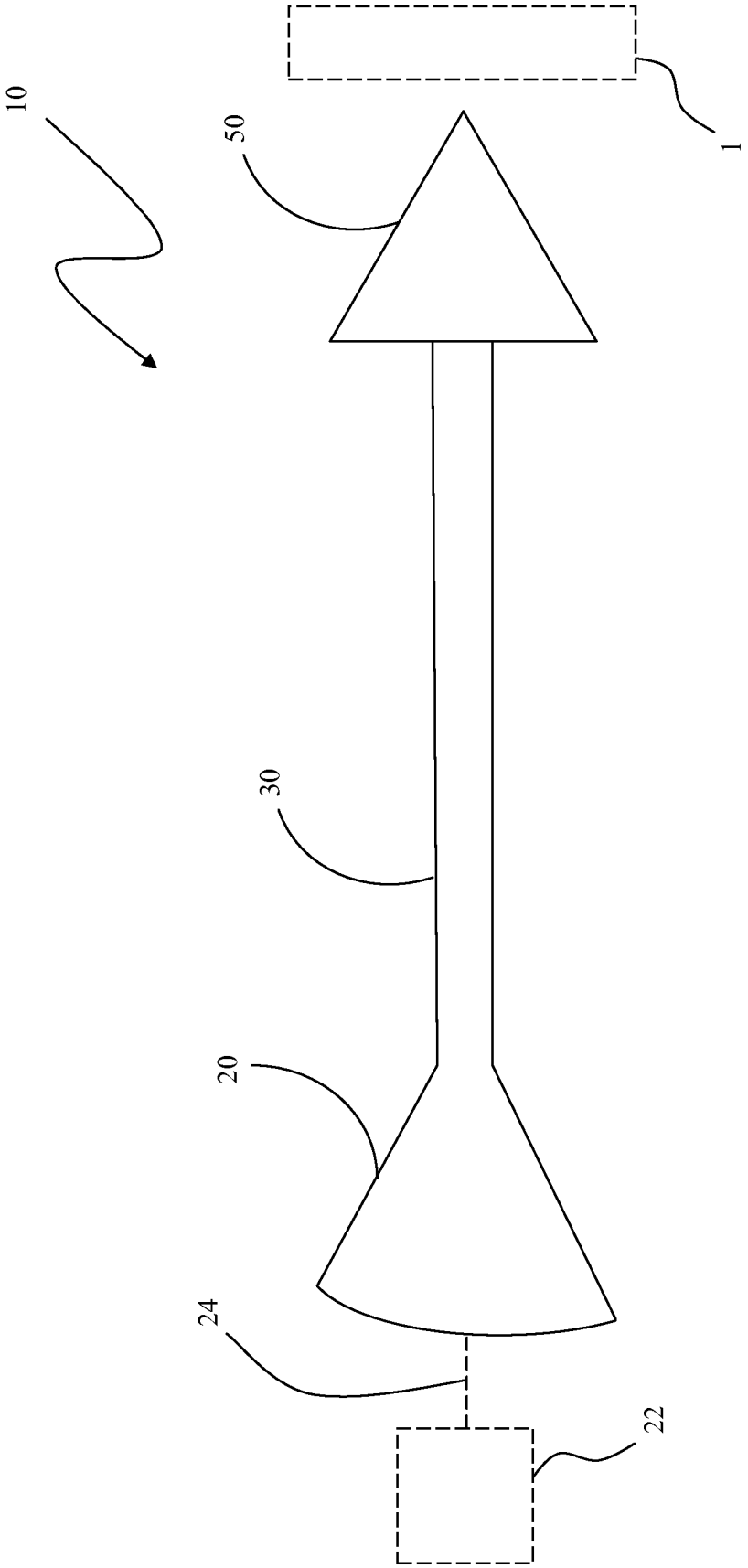


FIG. 1A

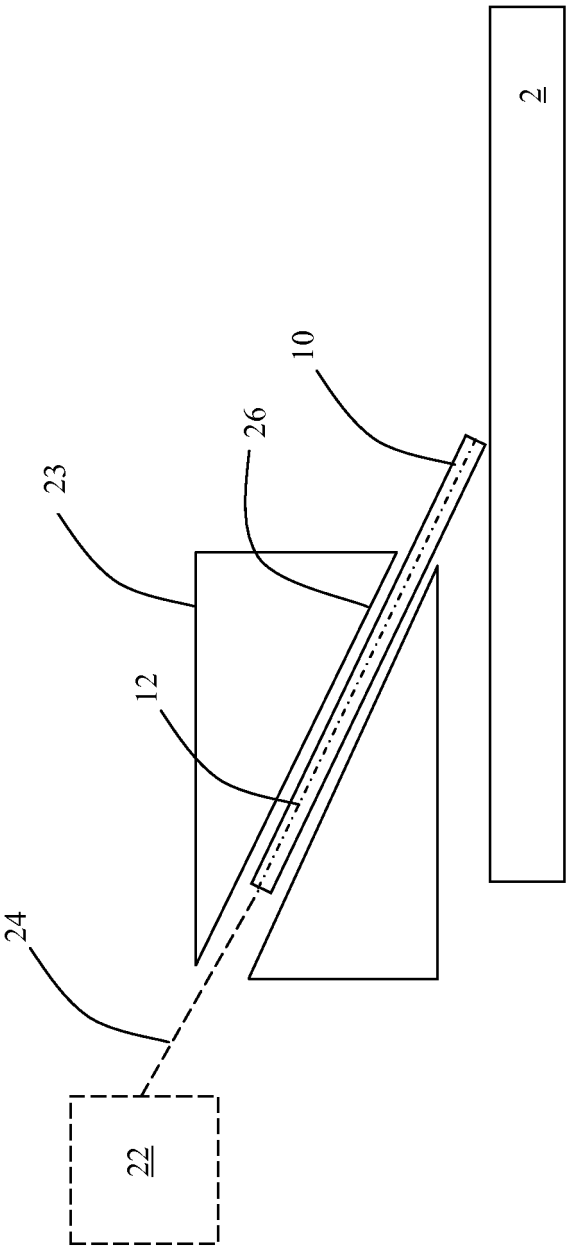


FIG. 1B

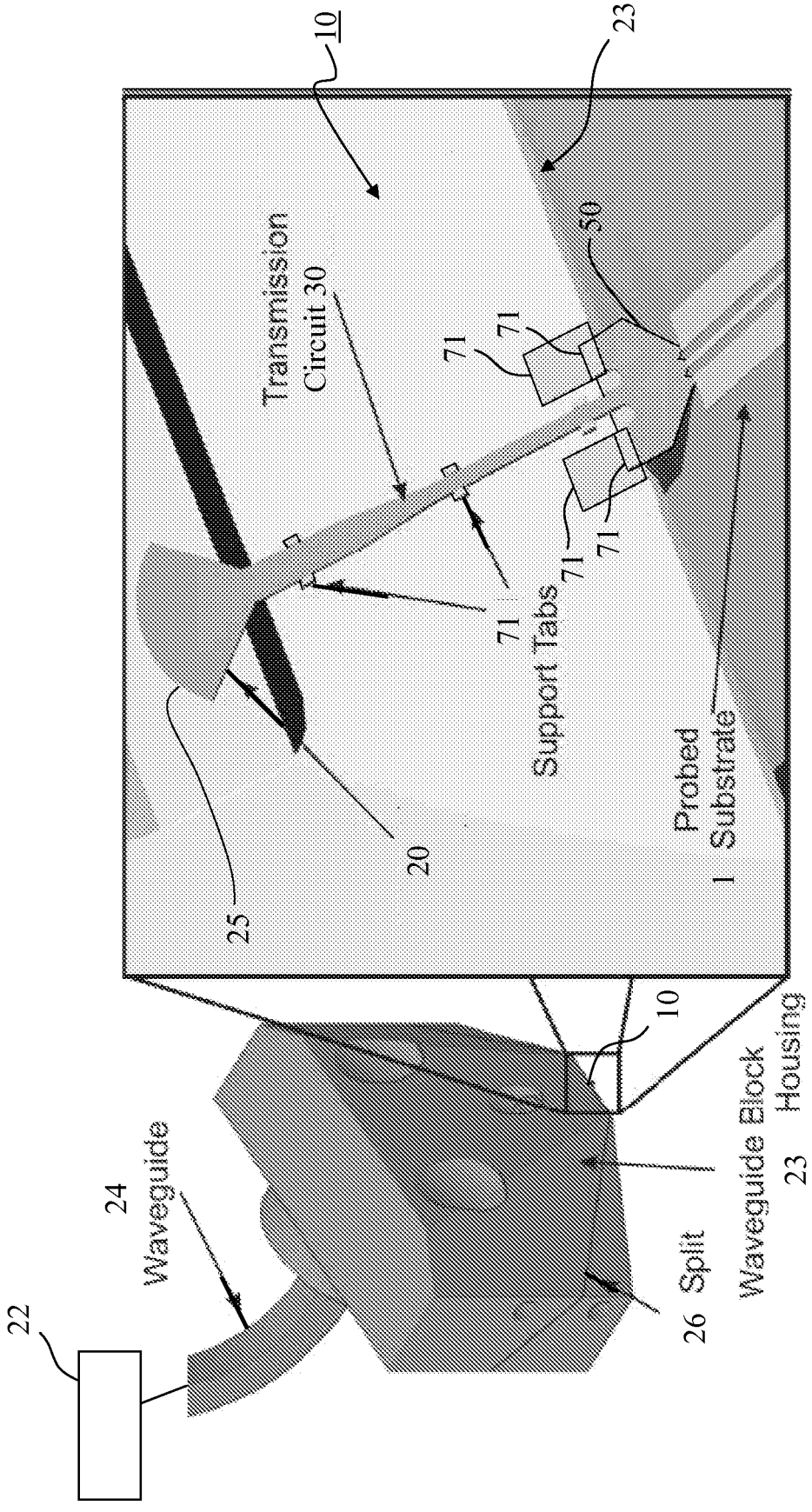

22
24
Waveguide
26
Split
Waveguide Block
23
Housing
10
1
Probed
Substrate
Support Tabs
71
71
71
71
71
30
Transmission
Circuit 30
20
25
10
23

FIG. 2A

FIG. 2B

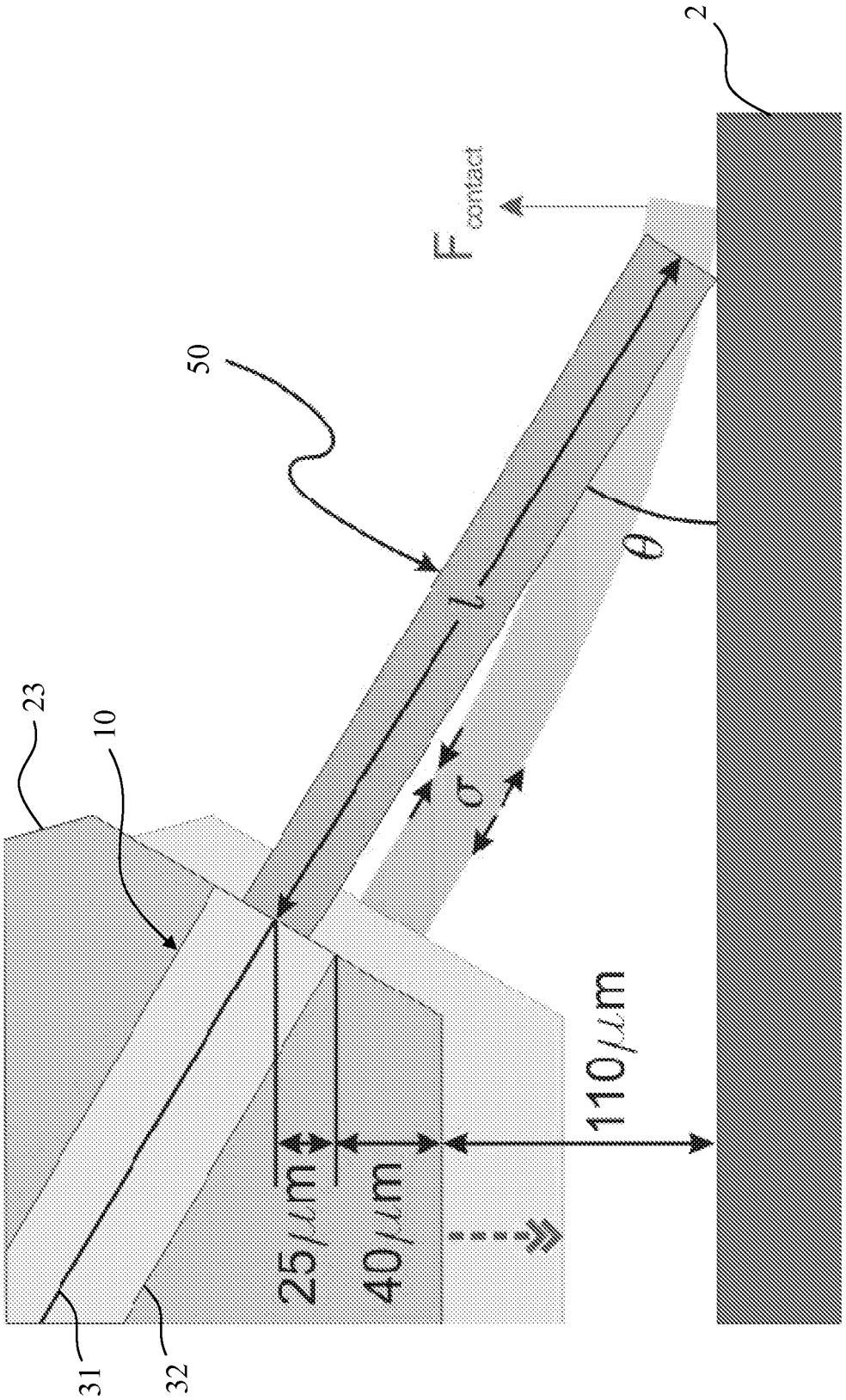


FIG. 3

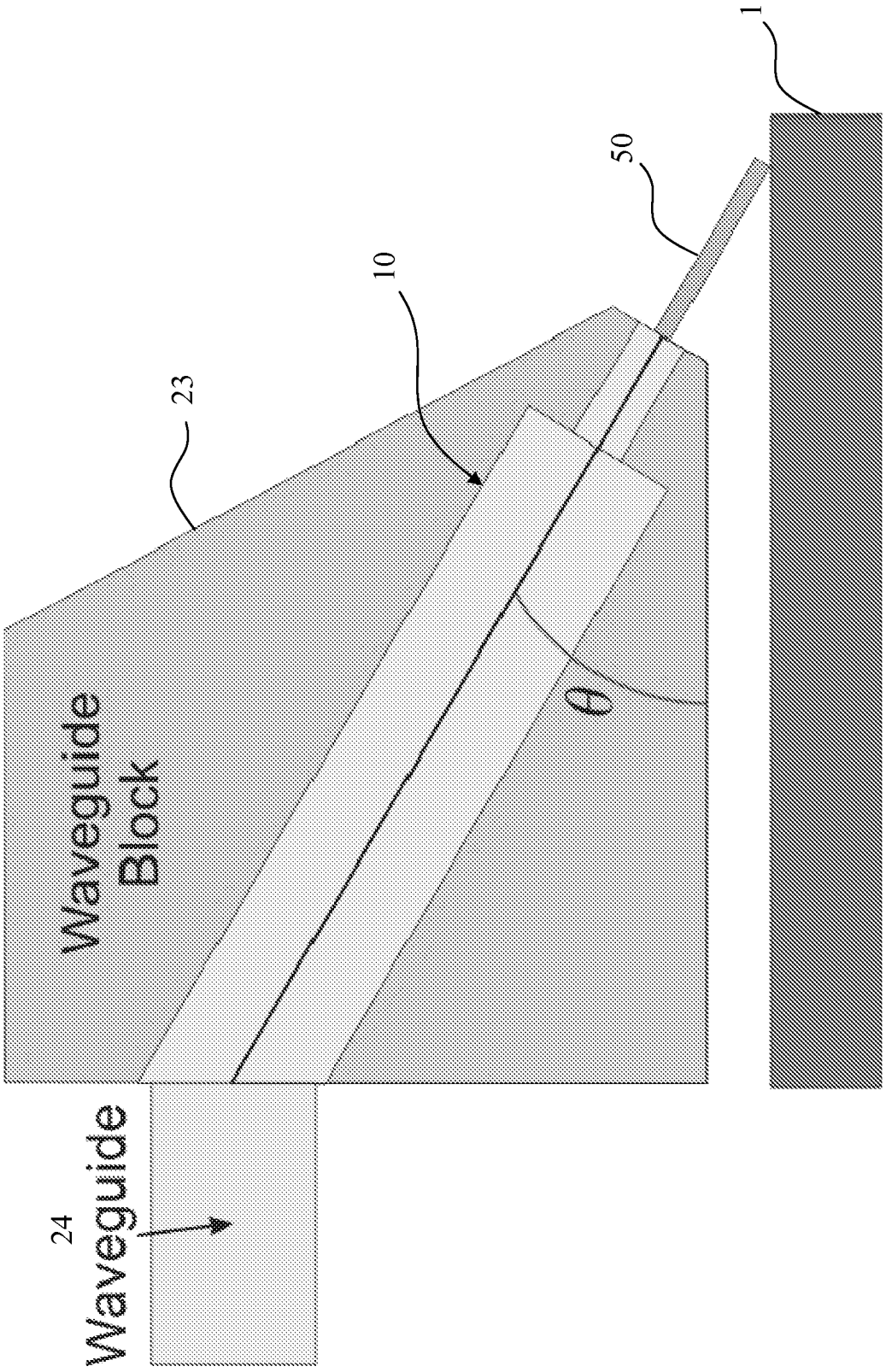


FIG. 4

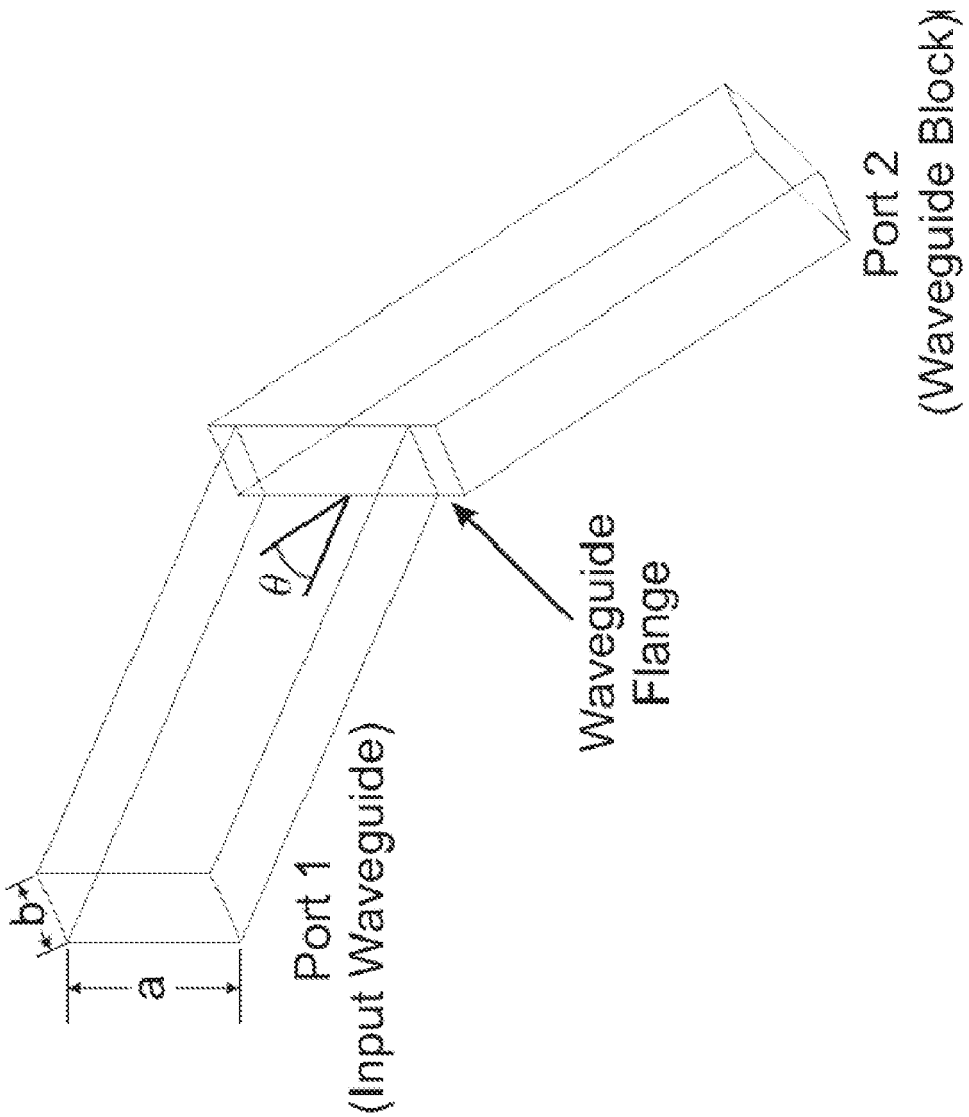

Port 2
(Waveguide Block)
θ
Waveguide
Flange
Port 1
(Input Waveguide)
a
b

FIG. 5A

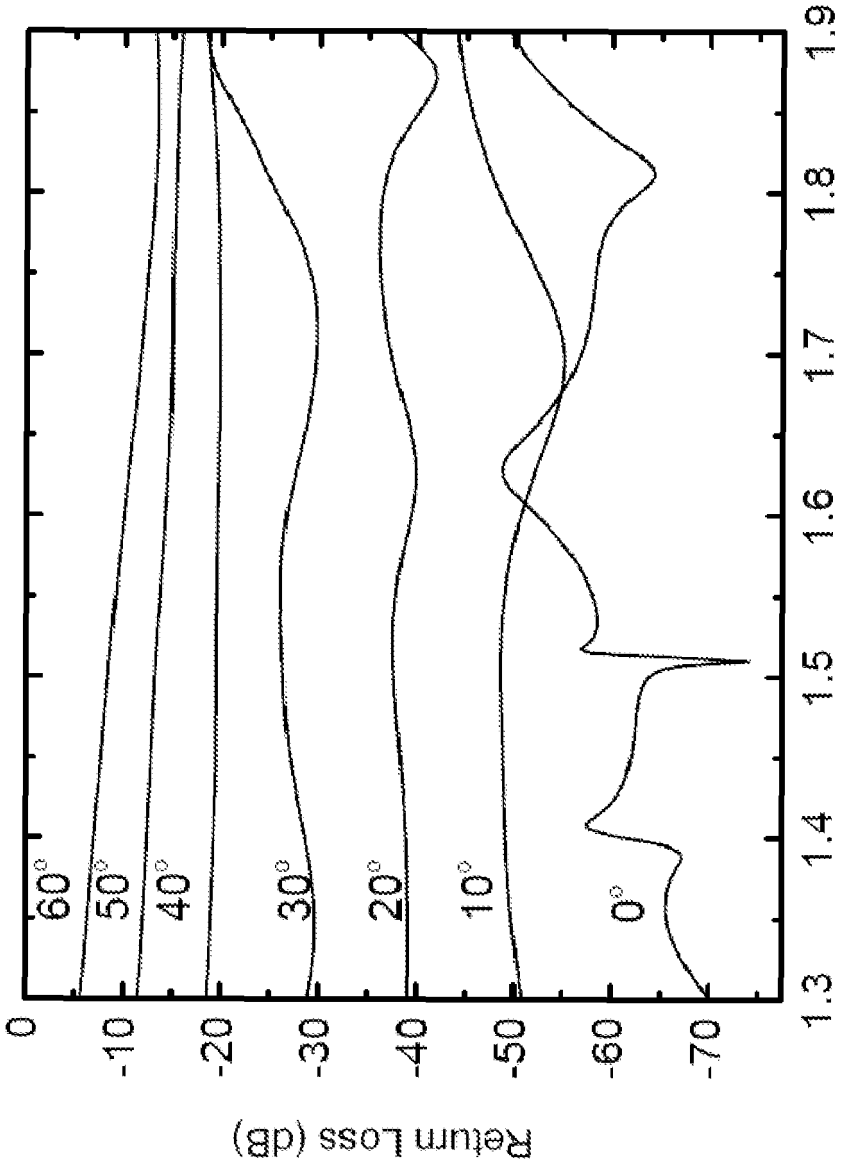

Return Loss (dB)
0
-10
-20
-30
-40
-50
-60
-70
1.3
1.4
1.5
1.6
1.7
1.8
1.9
f/f_c
60°
50°
40°
30°
20°
10°
0°

FIG. 5B

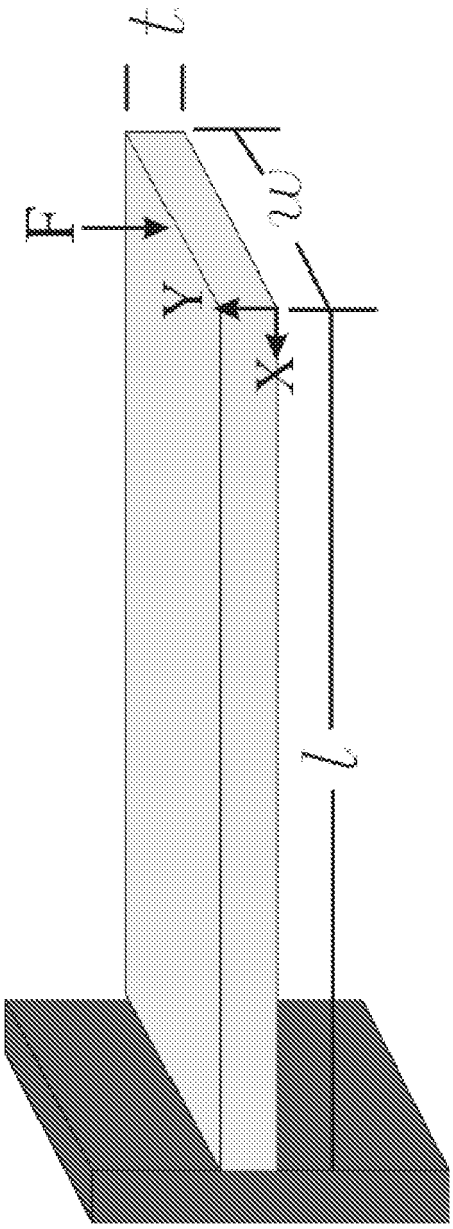


FIG. 6

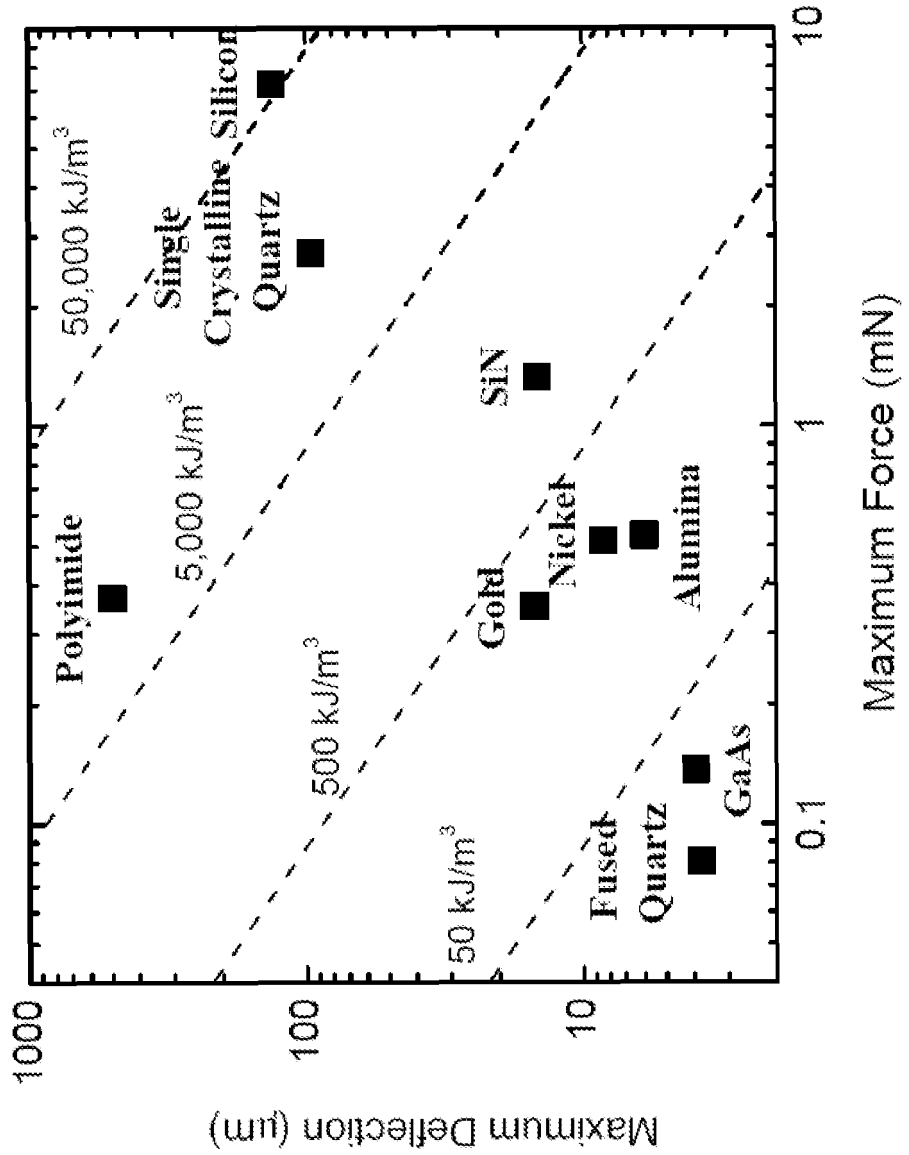

Maximum Deflection (μm)
1000
100
10
Maximum Force (mN)
0.1
1
10
50,000 kJ/m3
5,000 kJ/m3
500 kJ/m3
50 kJ/m3
Polyimide
Single Crystalline Silicon
Quartz
SiN
Gold
Nickel
Alumina
Fused Quartz
GaAs

FIG. 7

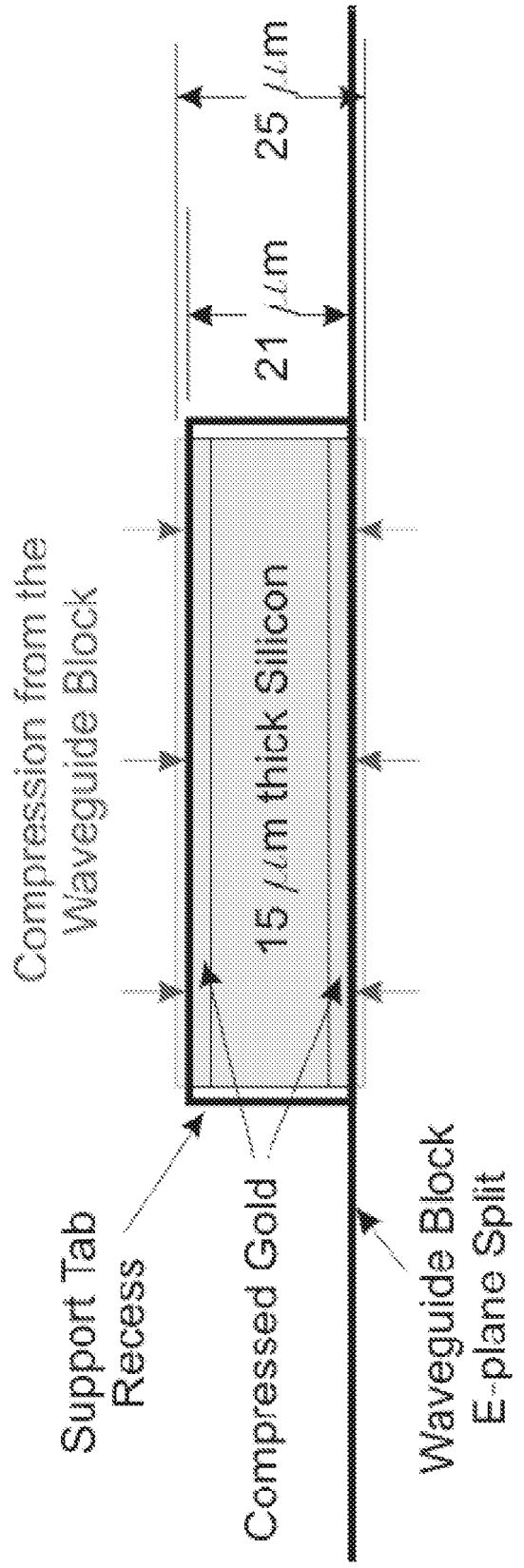

Compression from the Waveguide Block
Support Tab Recess
Compressed Gold
15 μm thick Silicon
Waveguide Block E-plane Split
21 μm
25 μm

FIG. 8

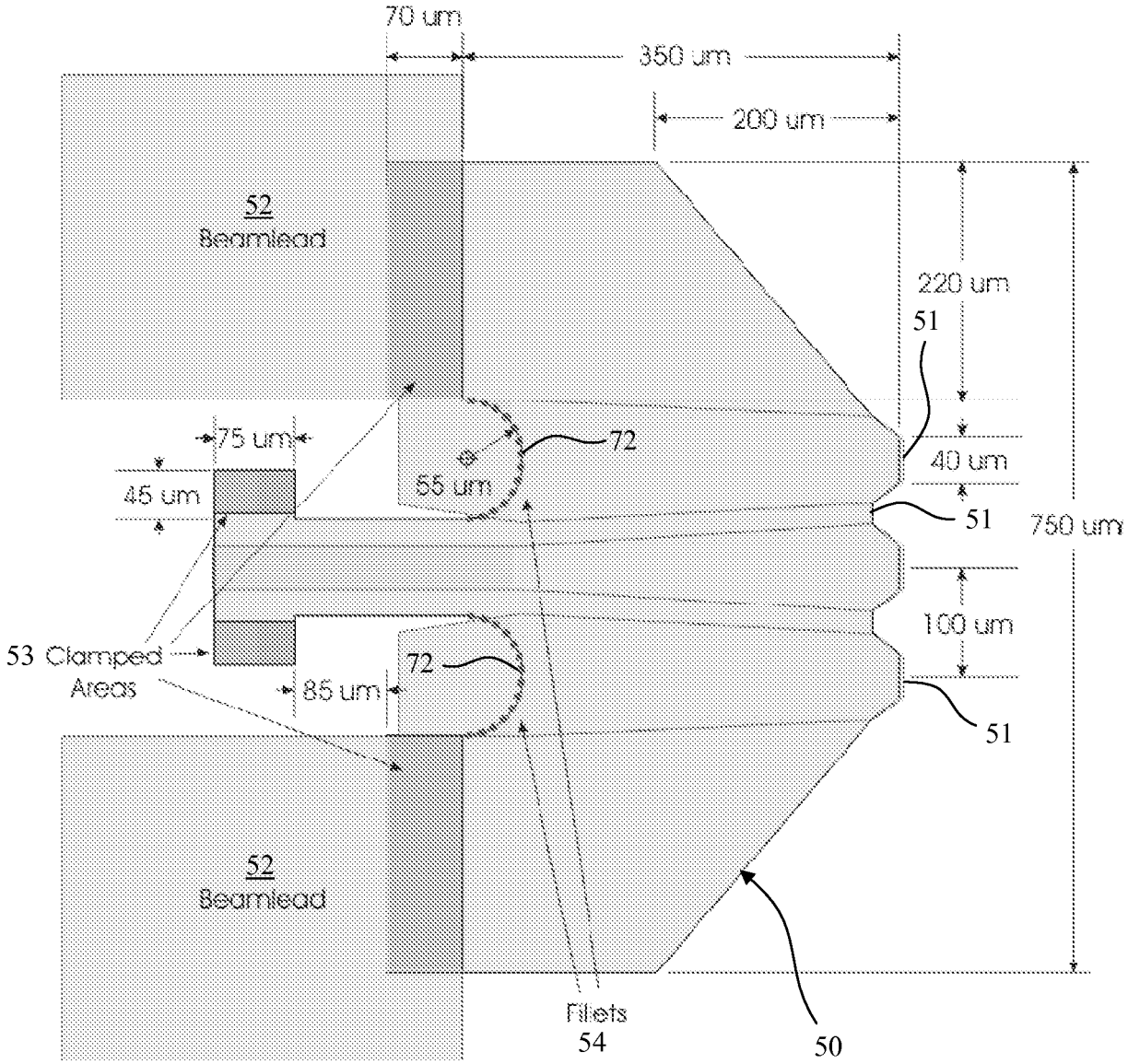

70 um
350 um
200 um
52
Beamlead
220 um
51
75 um
72
40 um
45 um
55 um
51
750 um
100 um
53 Clamped
Areas
72
85 um
51
52
Beamlead
Fillets
54
50

FIG. 9

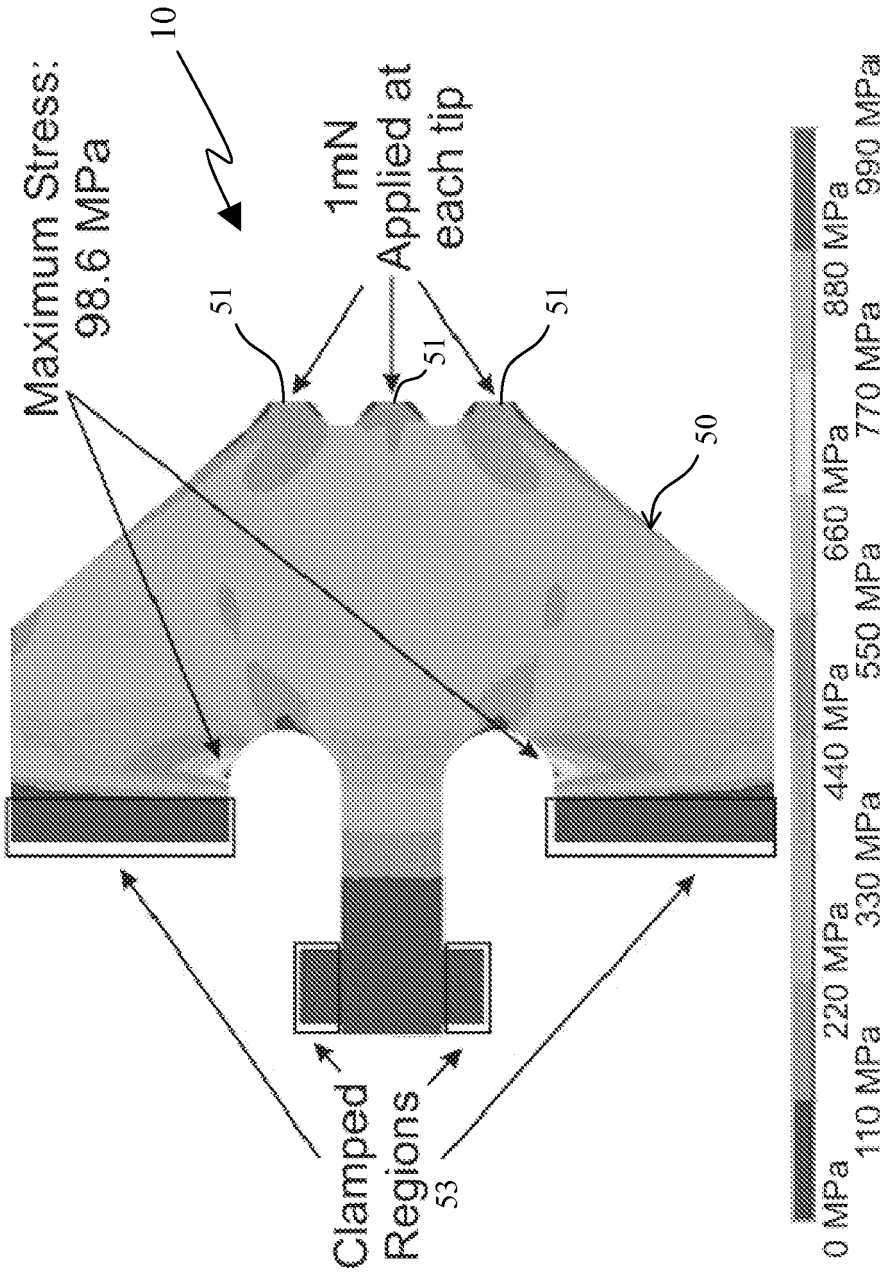

Maximum Stress:
98.6 MPa
10
1mN
Applied at
each tip
51
51
51
50
Clamped
Regions
53
0 MPa
110 MPa
220 MPa
330 MPa
440 MPa
550 MPa
660 MPa
770 MPa
880 MPa
990 MPa

FIG. 10

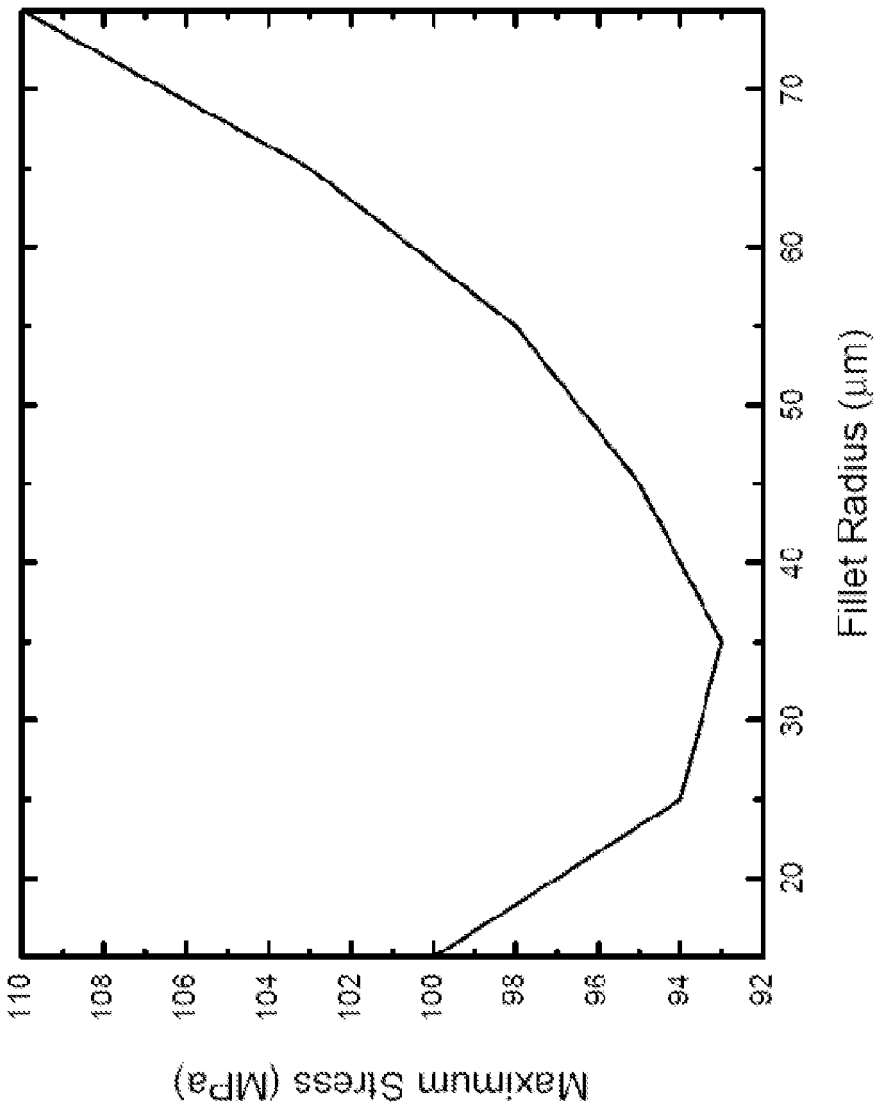

Maximum Stress (MPa)
110
108
106
104
102
100
98
96
94
92
Fillet Radius (μm)
20
30
40
50
60
70

FIG. 11

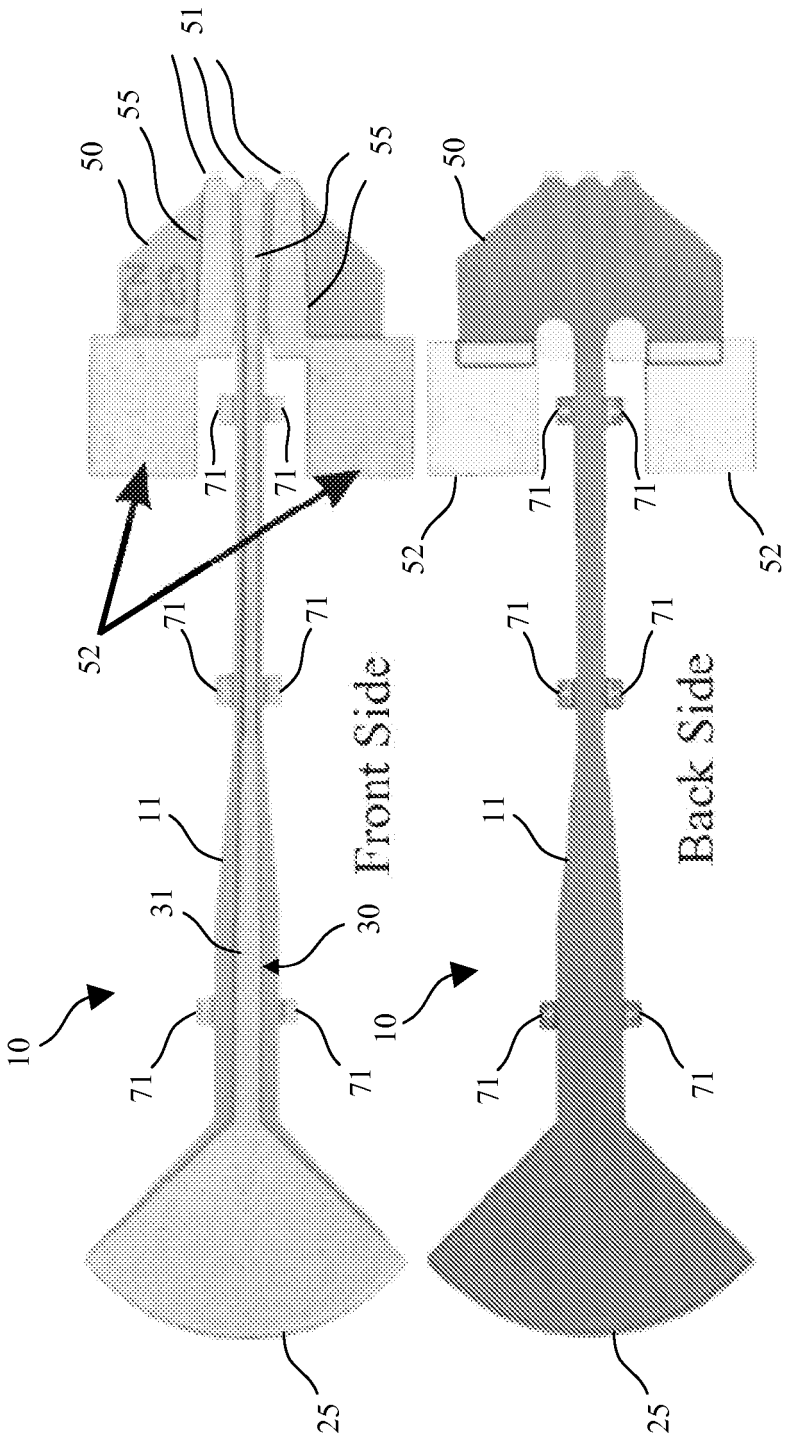

51
55
50
55
50
71
71
71
71
52
52
52
71
71
71
71
Front Side
Back Side
11
11
31
30
10
10
71
71
71
71
25
25

FIG. 12A

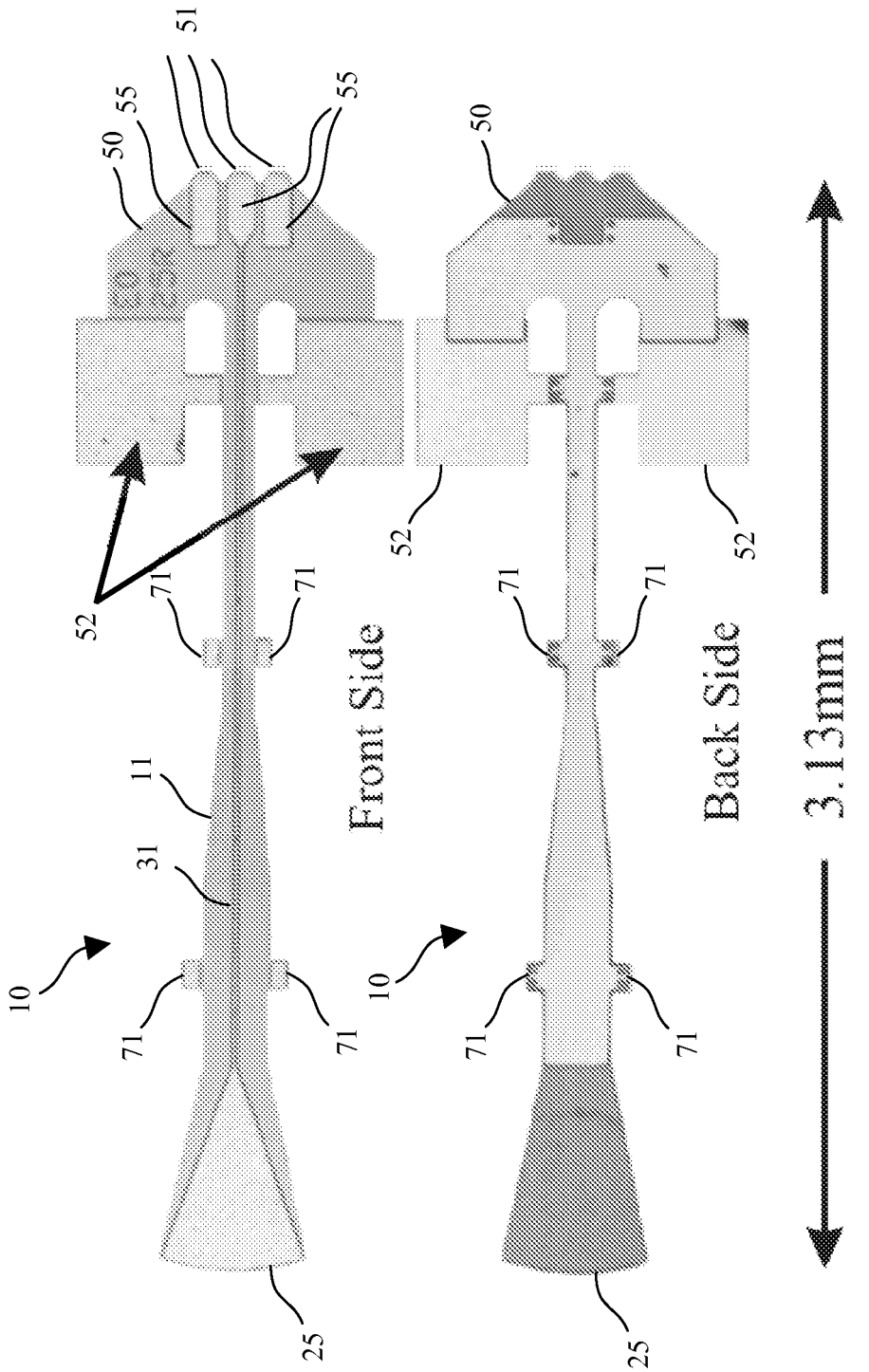

10
11
31
71
71
71
71
25
52
50
55
55
51
Front Side
10
71
71
71
71
25
52
50
52
Back Side
3.13mm

FIG. 12B

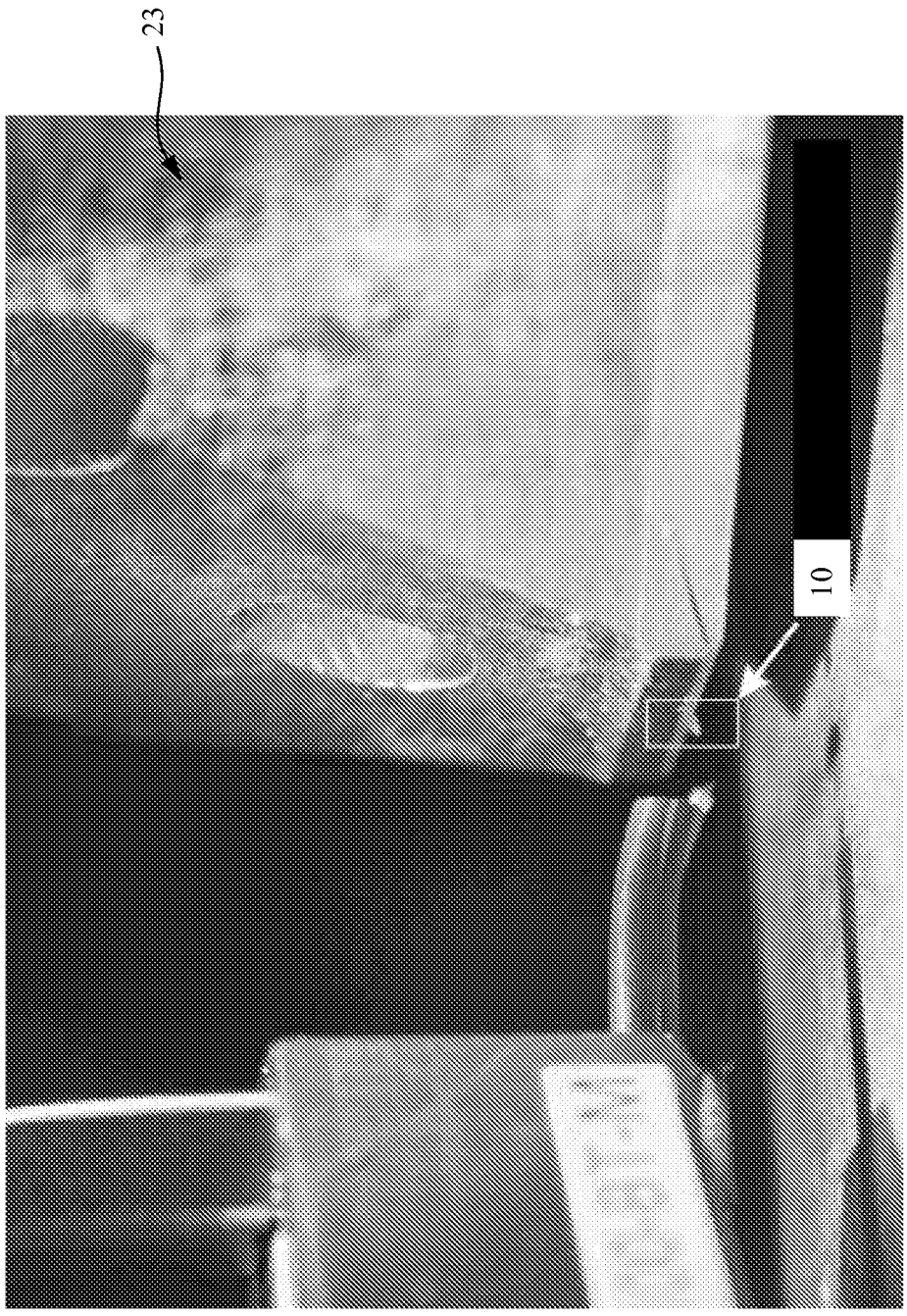


FIG. 13

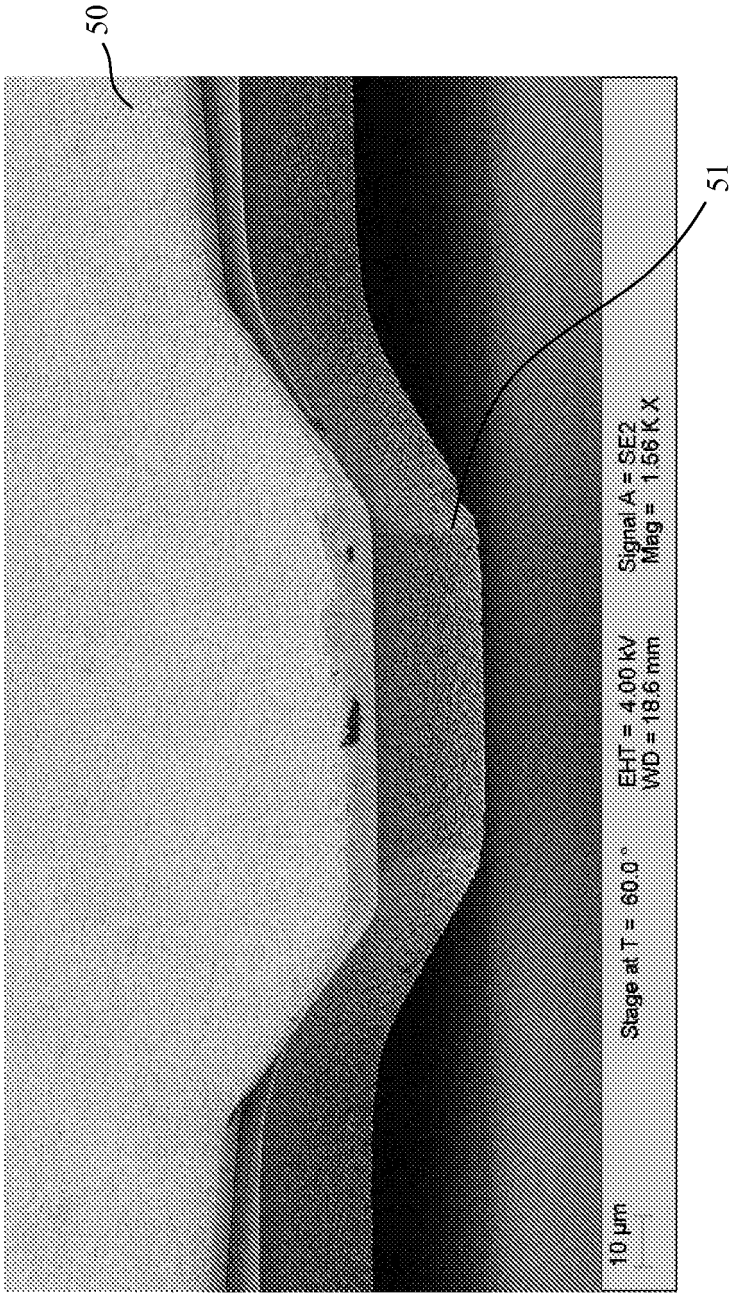

50
51
10 µm
Stage at T = 60.0 °
EHT = 4.00 kV
WD = 18.6 mm
Signal A = SE2
Mag = 1.56 K X

FIG. 14A

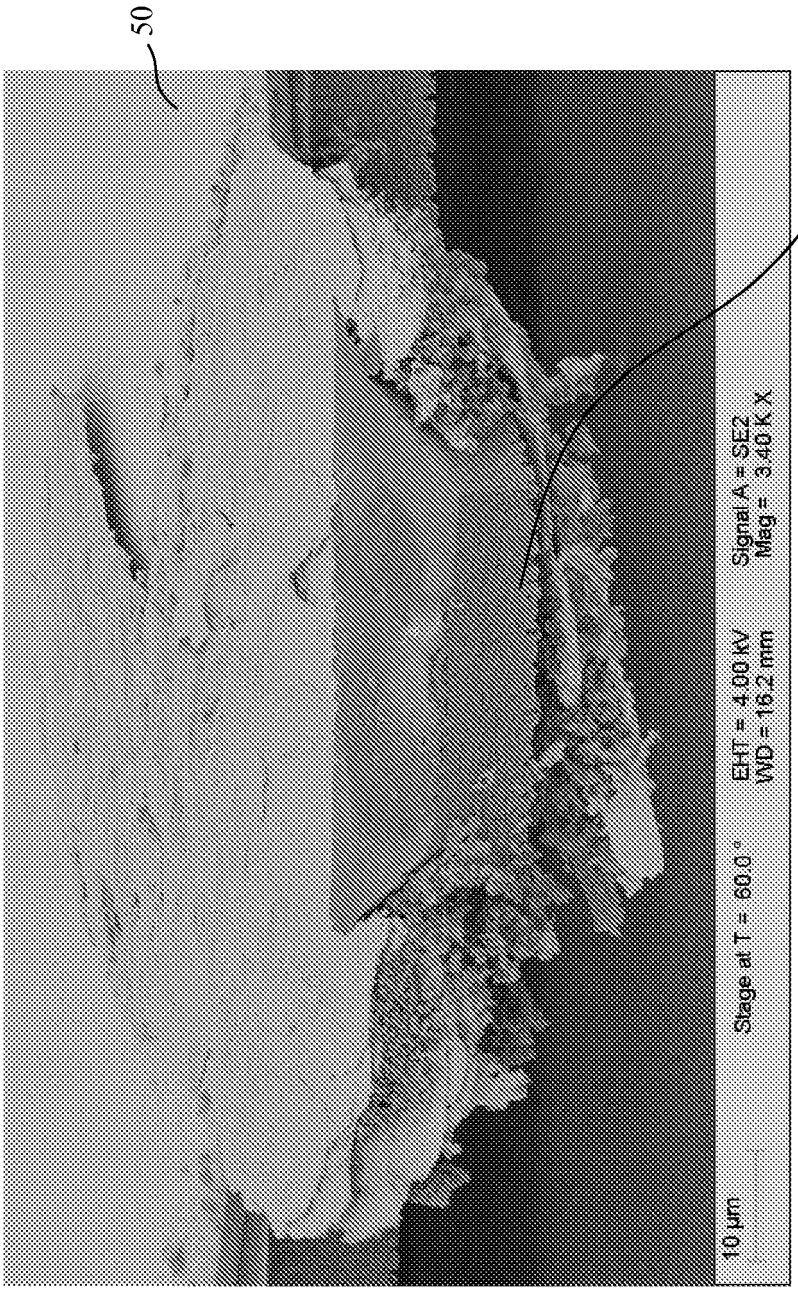

50
51
10 µm
Stage at T = 60.0 °
EHT = 4.00 kV
WD = 16.2 mm
Signal A = SE2
Mag = 3.40 K X

FIG. 14B

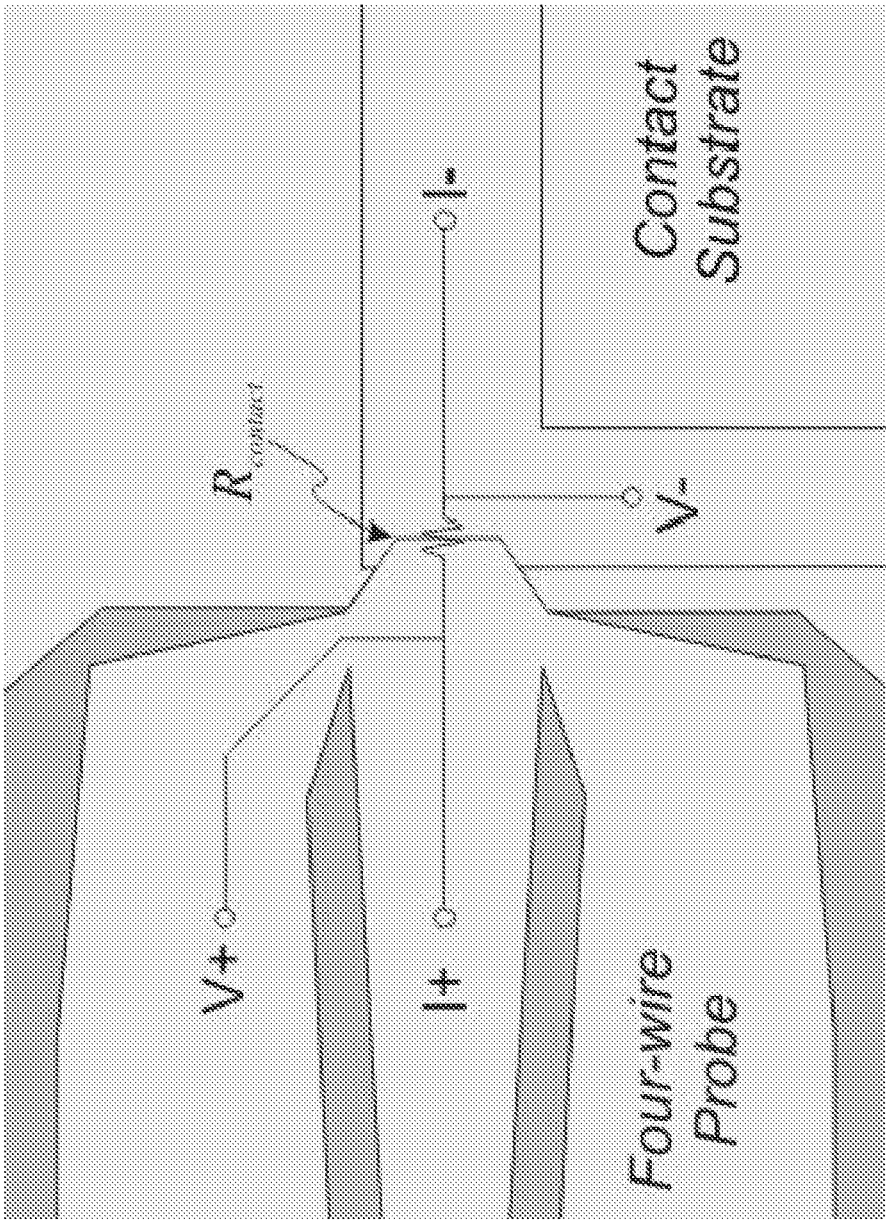


FIG. 15

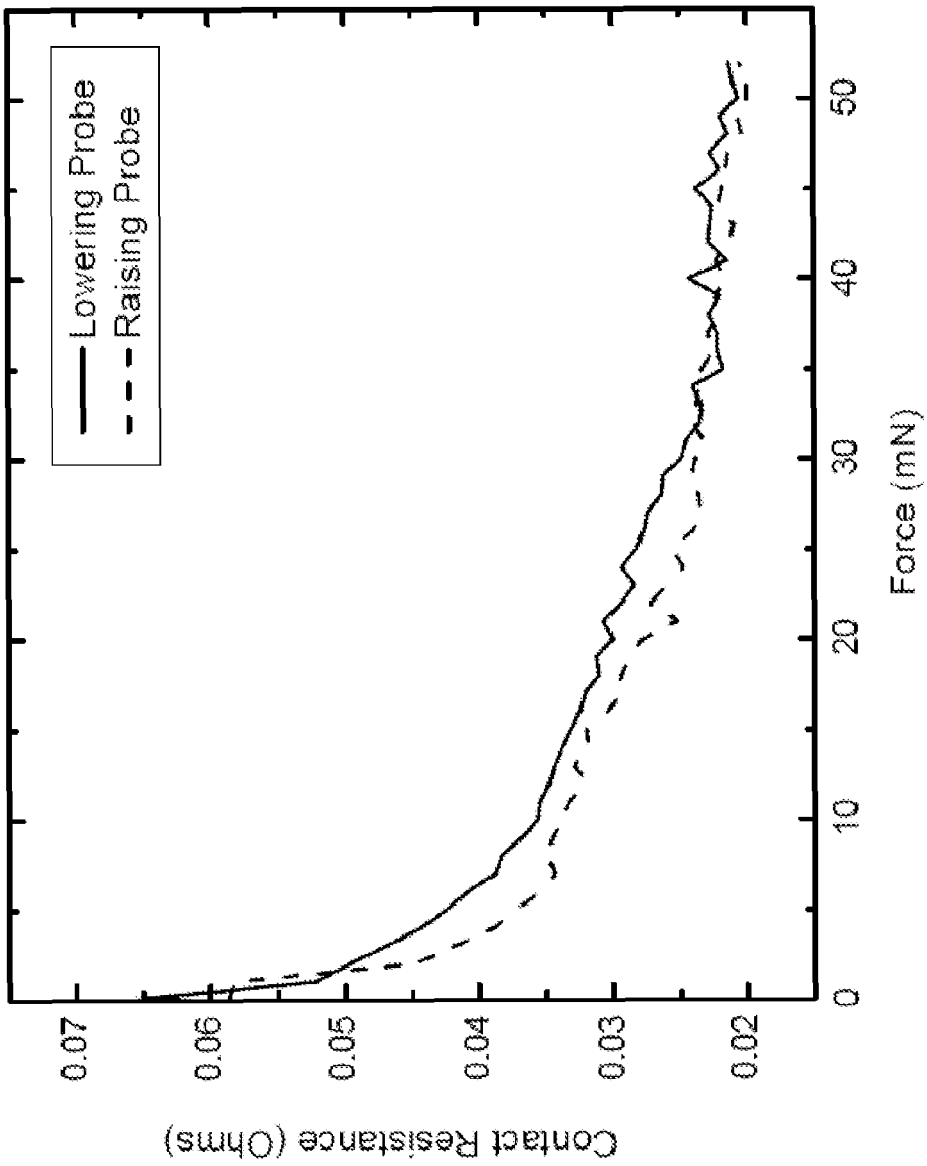

Lowering Probe
Raising Probe
Contact Resistance (Ohms)
0.07
0.06
0.05
0.04
0.03
0.02
0
10
20
30
40
50
Force (mN)

FIG. 16

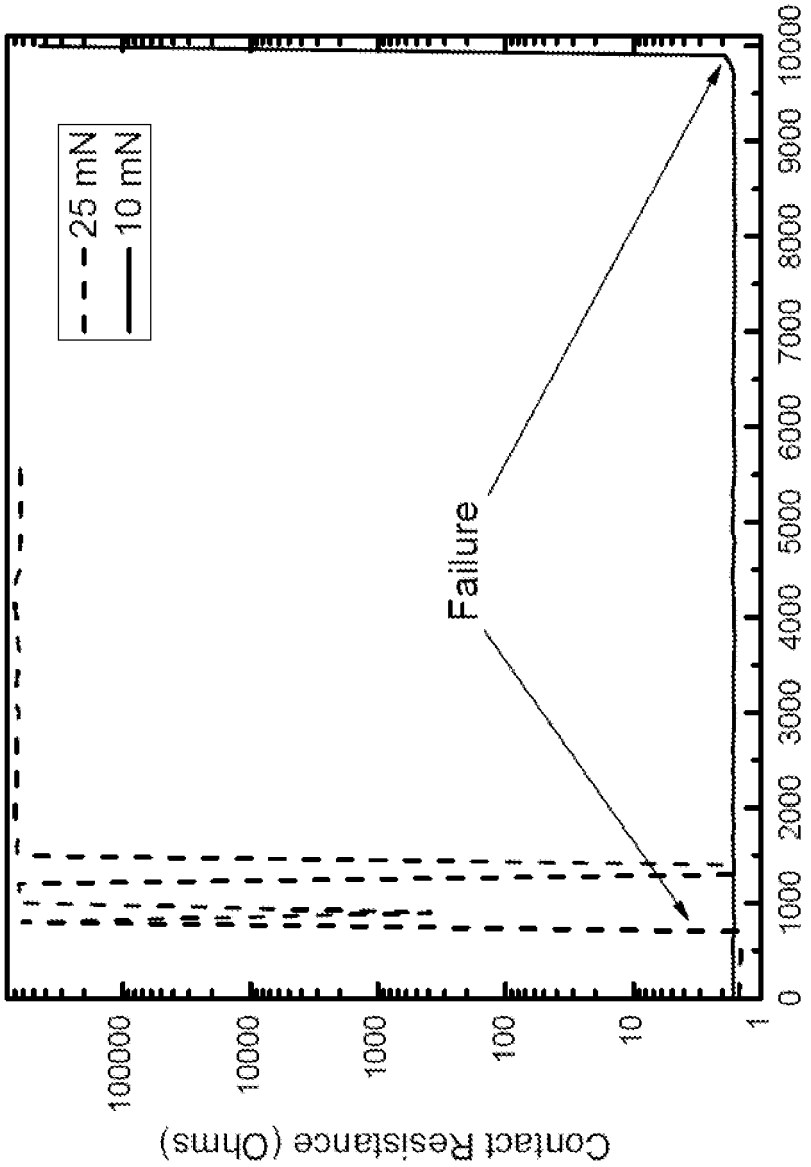

25 mN
10 mN
Failure
Contact Cycle
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
Contact Resistance (Ohms)
1
10
100
1000
10000
100000

FIG. 17

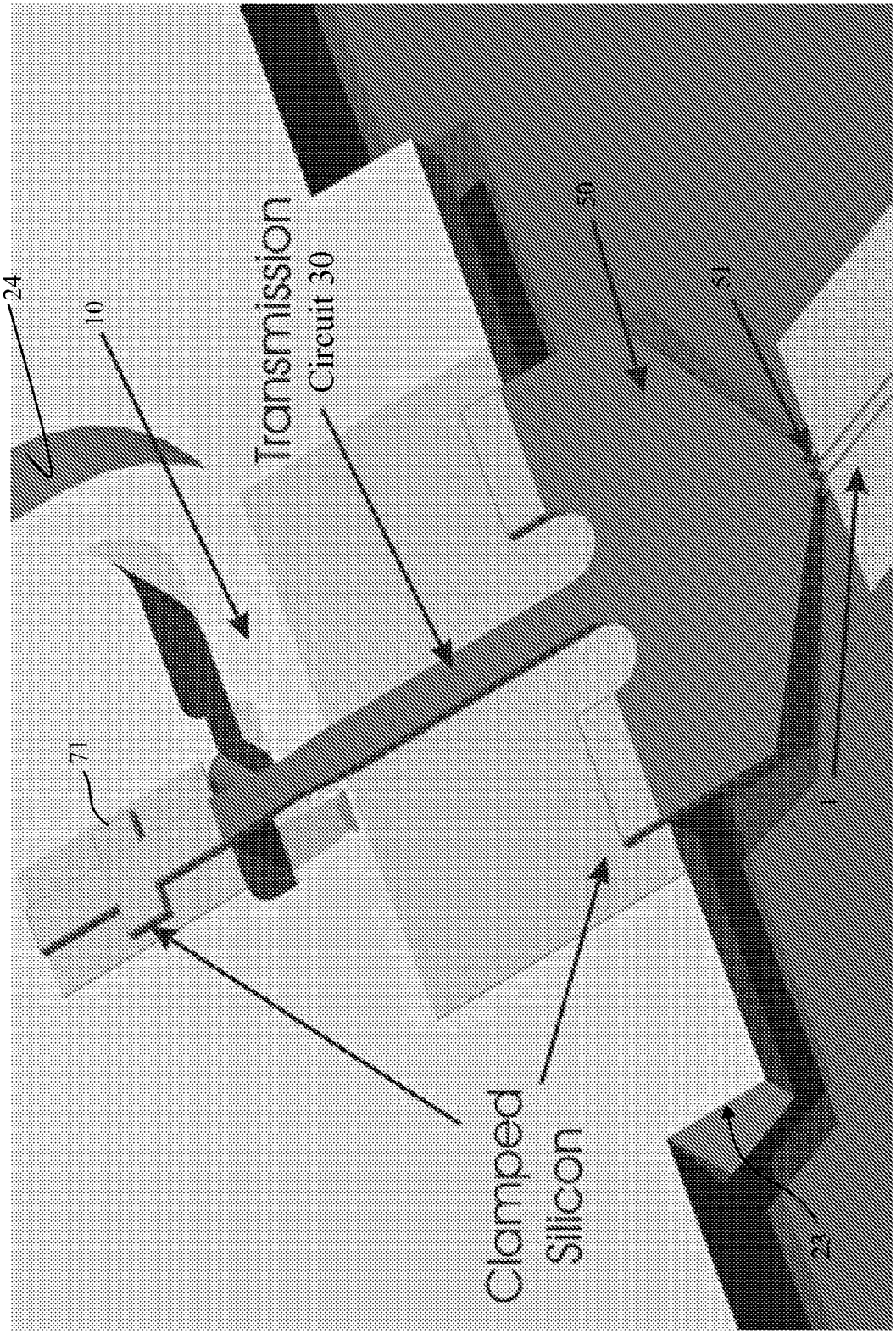


FIG. 18

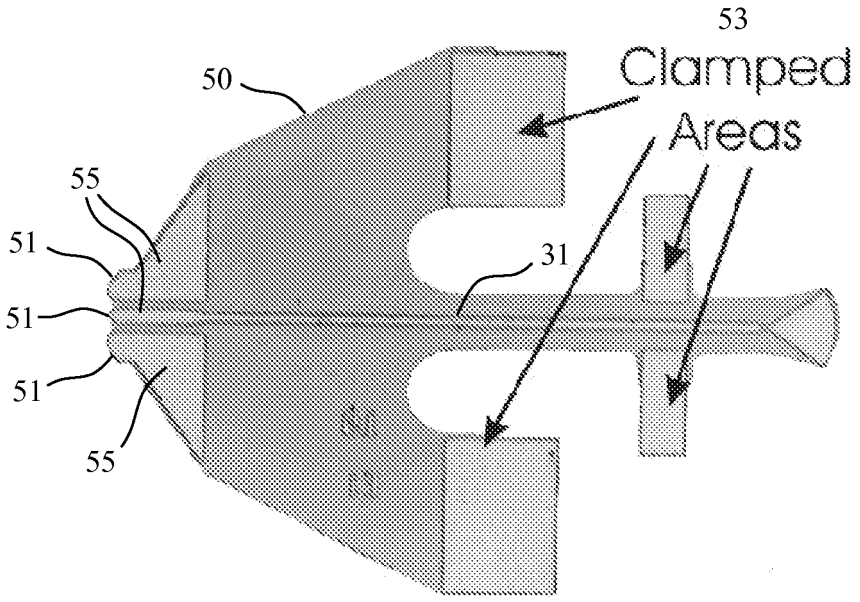


FIG. 19A

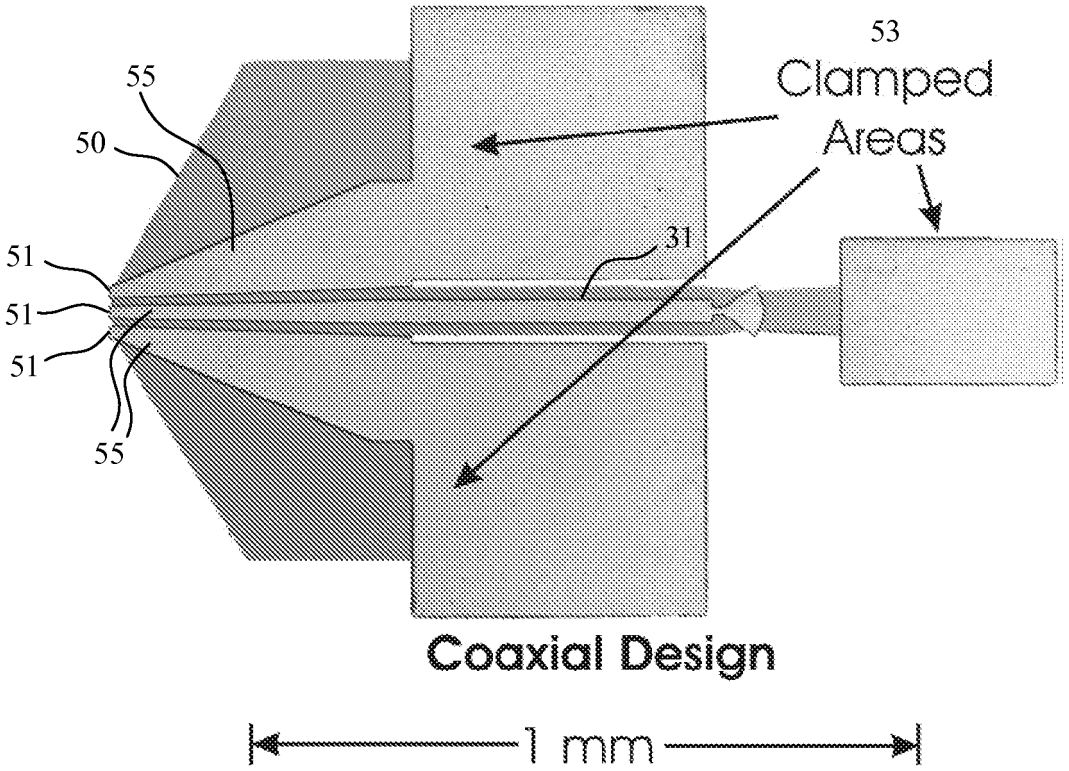


FIG. 19B

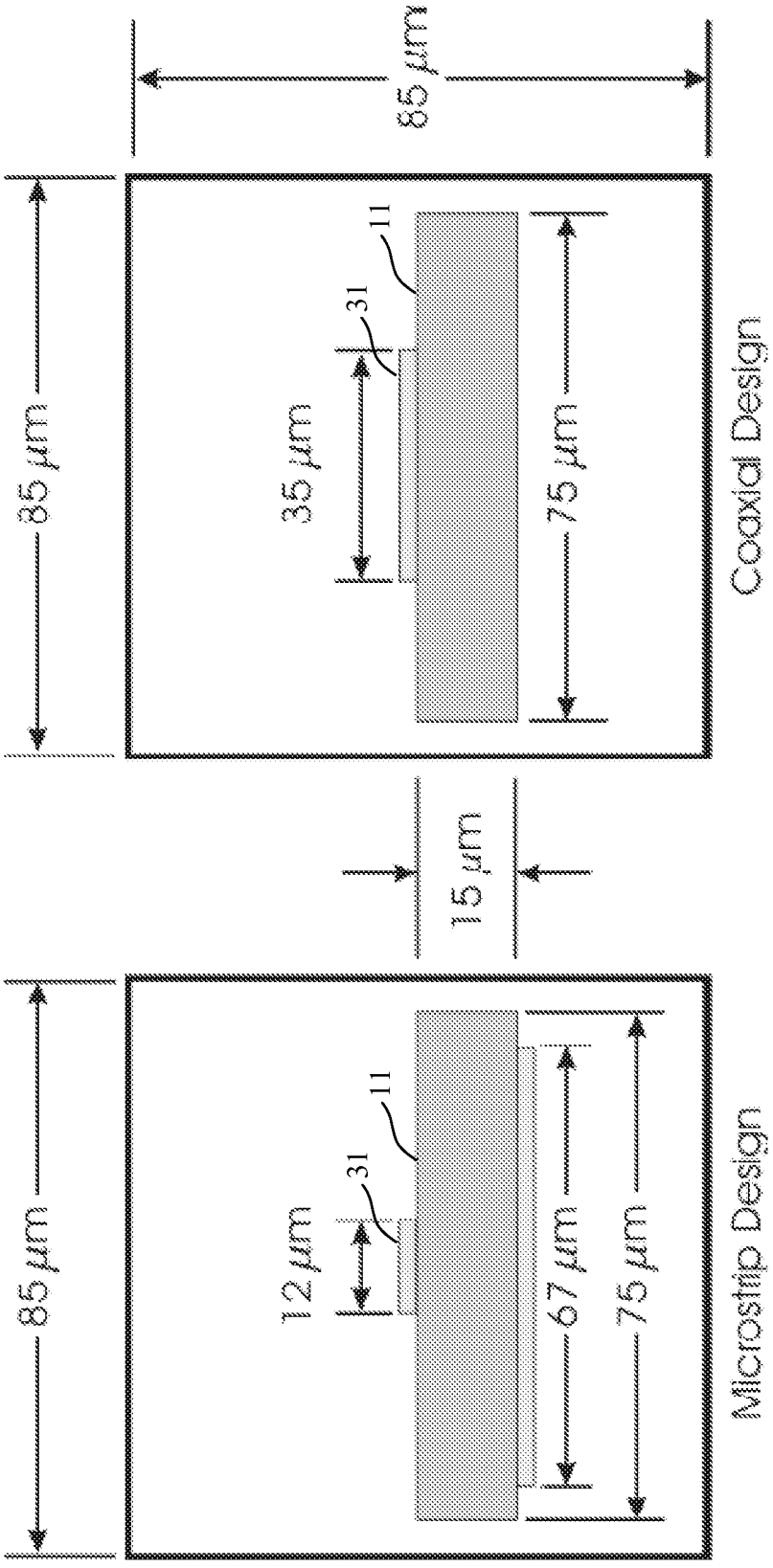
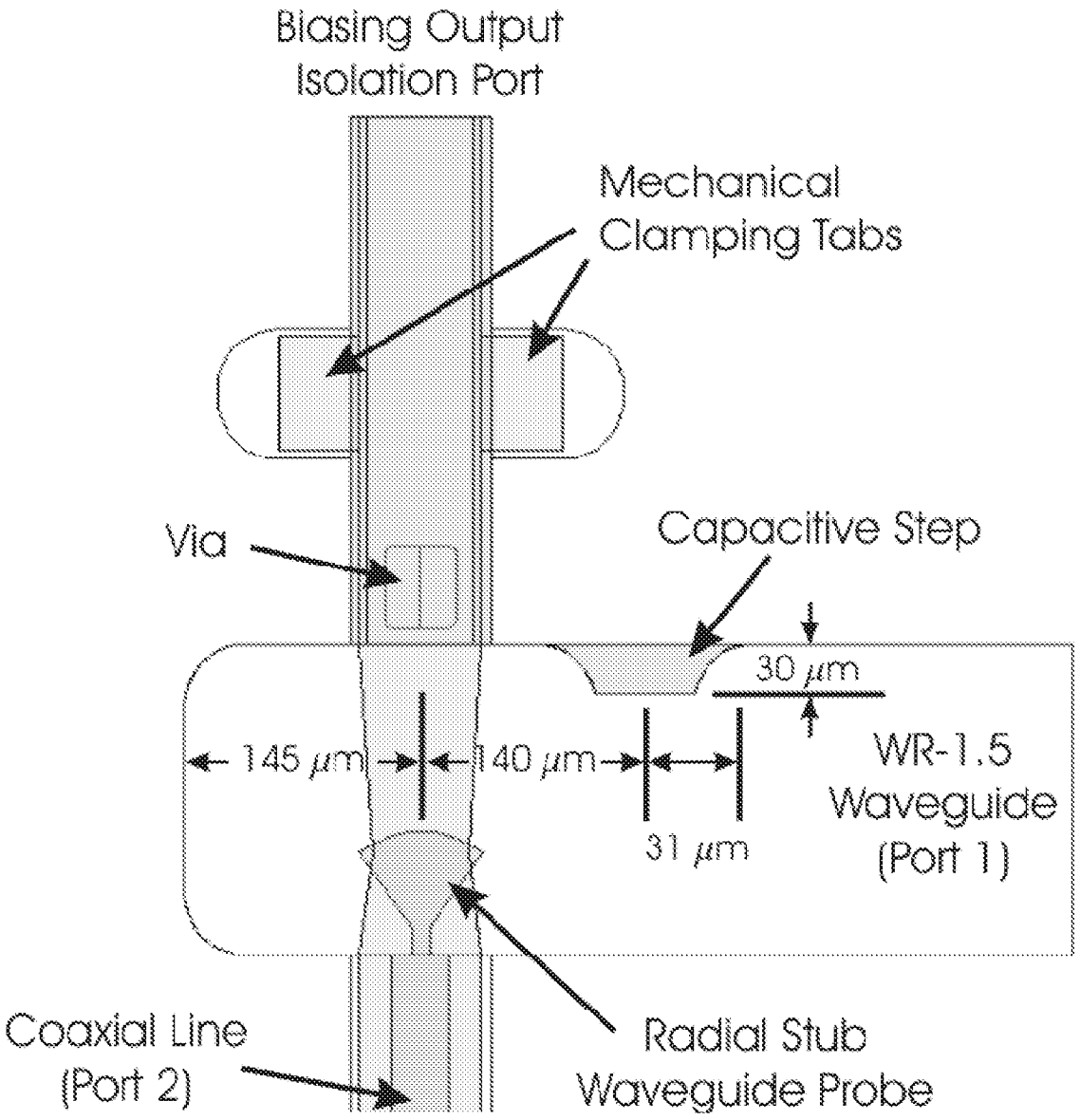


FIG. 20A

FIG. 20B


Biasing Output
Isolation Port
Mechanical
Clamping Tabs
Via
Capacitive Step
30 μm
145 μm
140 μm
31 μm
WR-1.5
Waveguide
(Port 1)
Coaxial Line
(Port 2)
Radial Stub
Waveguide Probe

31

FIG. 21A

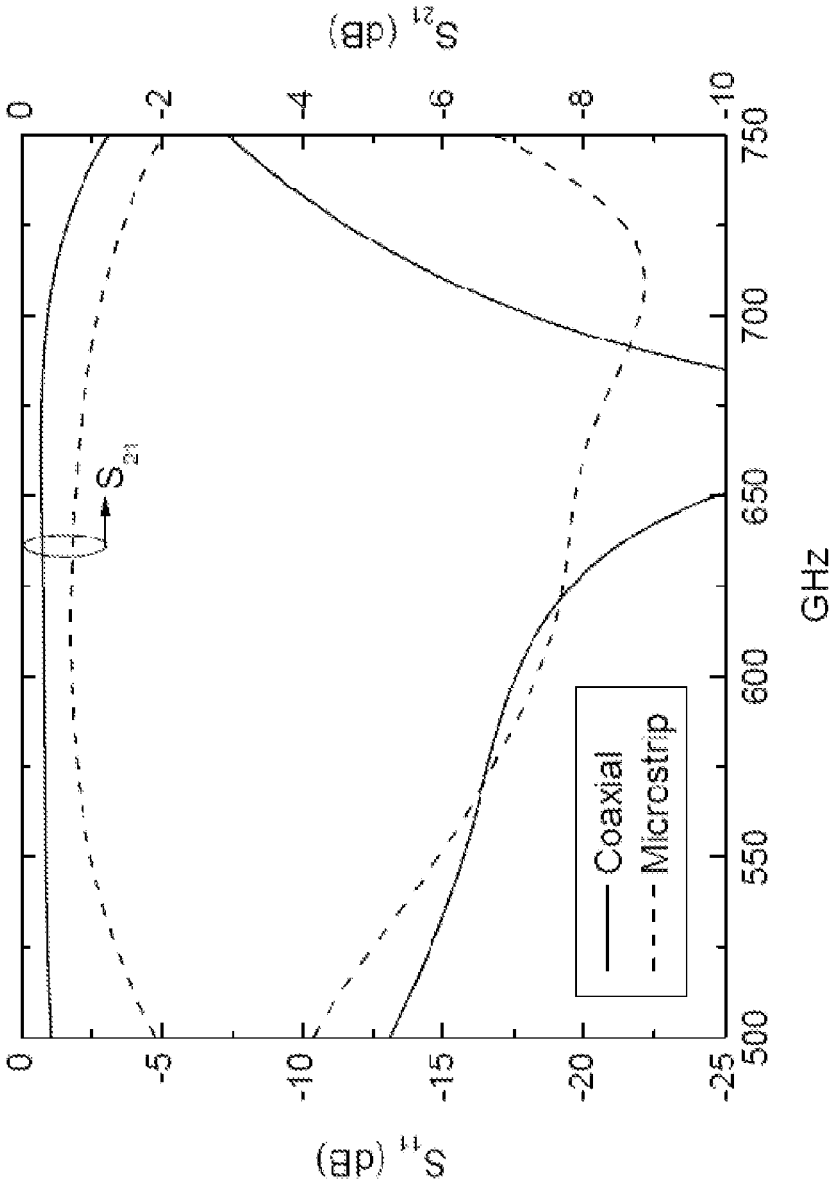

S21 (dB)
0
-2
-4
-6
-8
-10
750
700
650
600
550
500
GHz
S11 (dB)
0
-5
-10
-15
-20
-25
S21
Coaxial
Microstrip

FIG. 21B

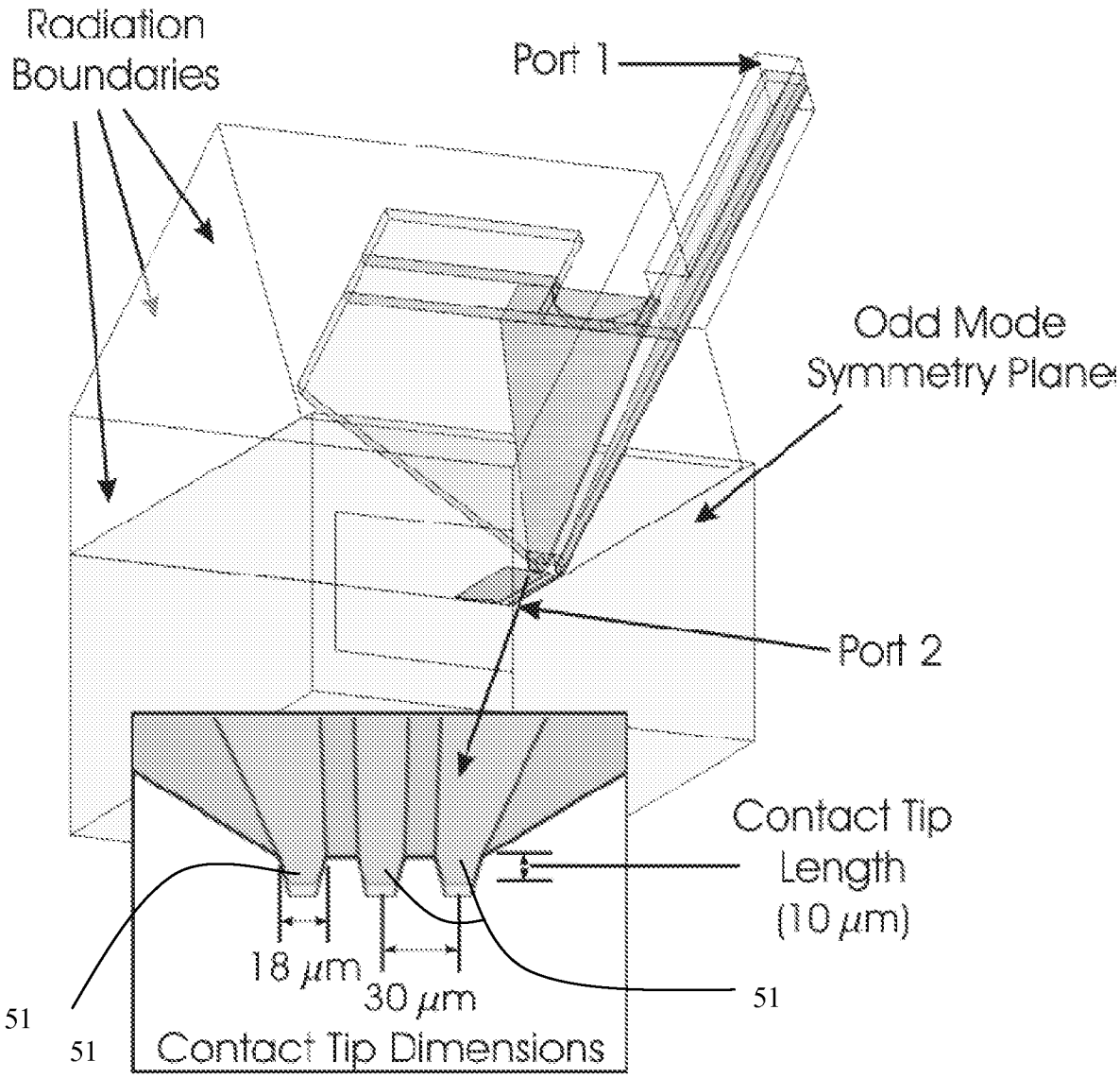

Radiation Boundaries
Port 1
Odd Mode Symmetry Plane
Port 2
Contact Tip Length (10 μm)
18 μm
30 μm
51
51
51
Contact Tip Dimensions

FIG. 22A

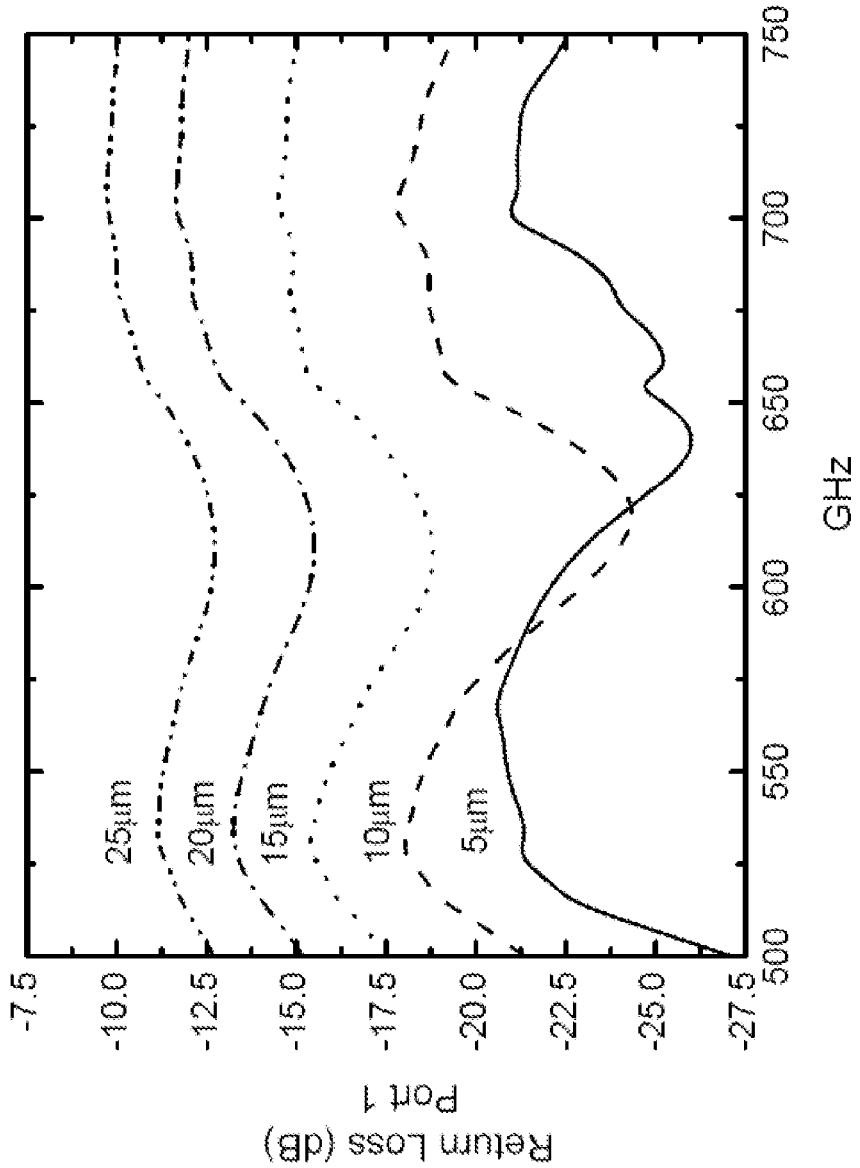

Return Loss (dB)
Port 1
-7.5
-10.0
-12.5
-15.0
-17.5
-20.0
-22.5
-25.0
-27.5
500
550
600
650
700
750
GHz
25μm
20μm
15μm
10μm
5μm

FIG. 22B

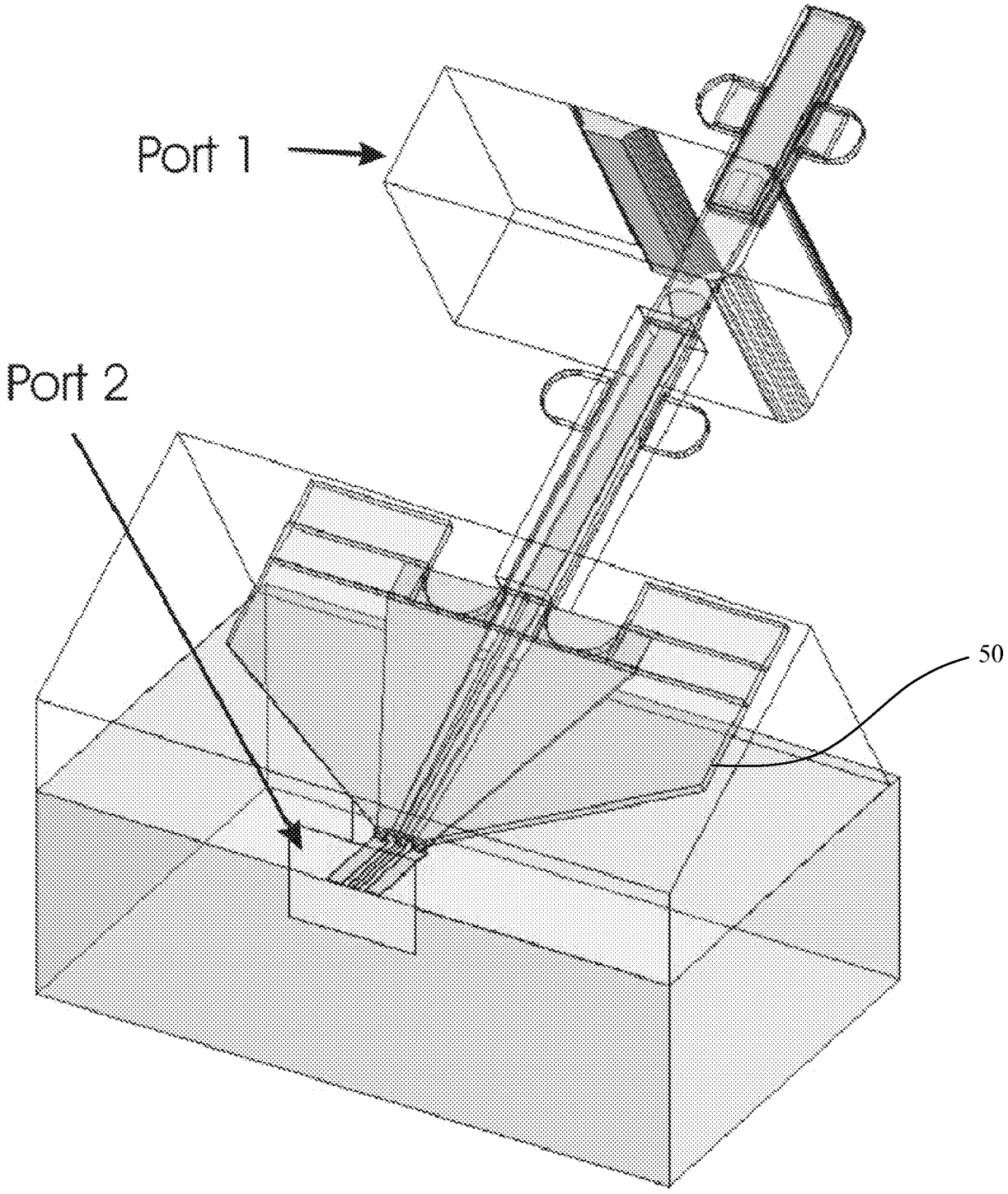


FIG. 23A

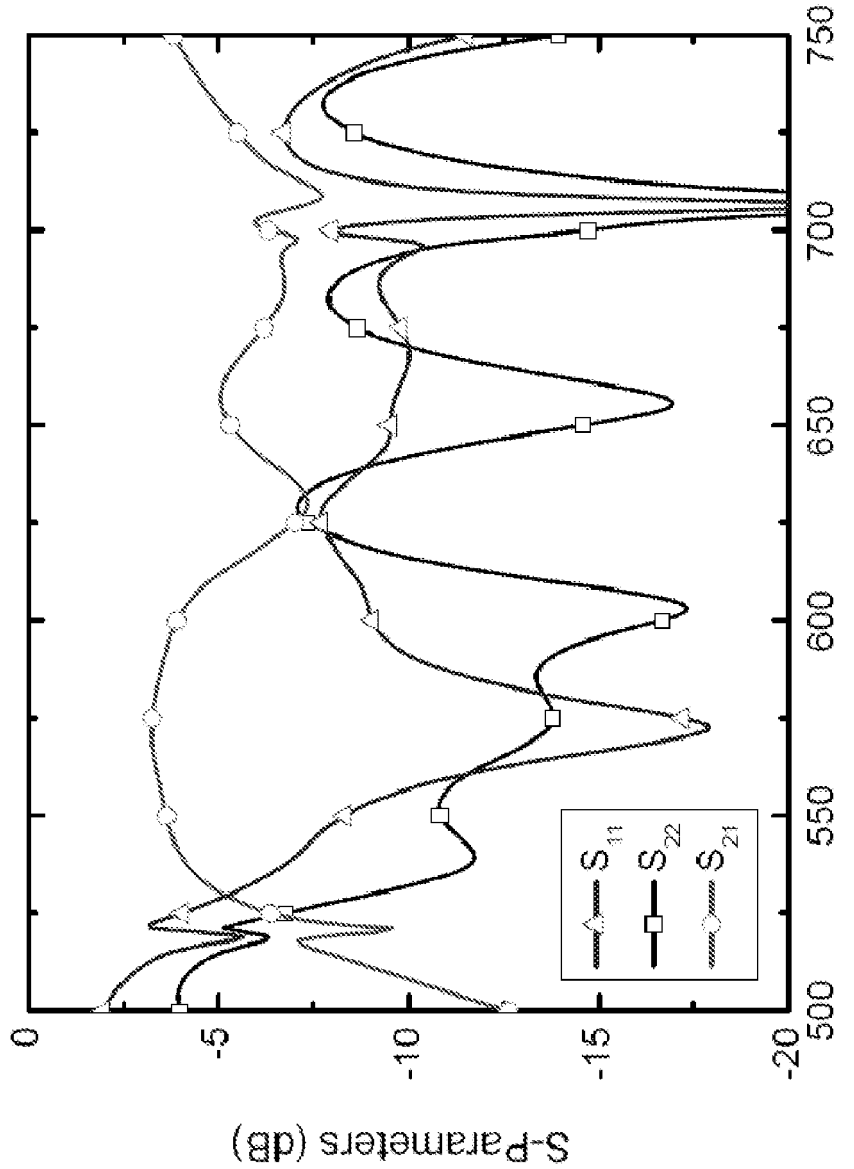

S-Parameters (dB)
0
-5
-10
-15
-20
500
550
600
650
700
750
GHz
S11
S22
S21

FIG. 23B

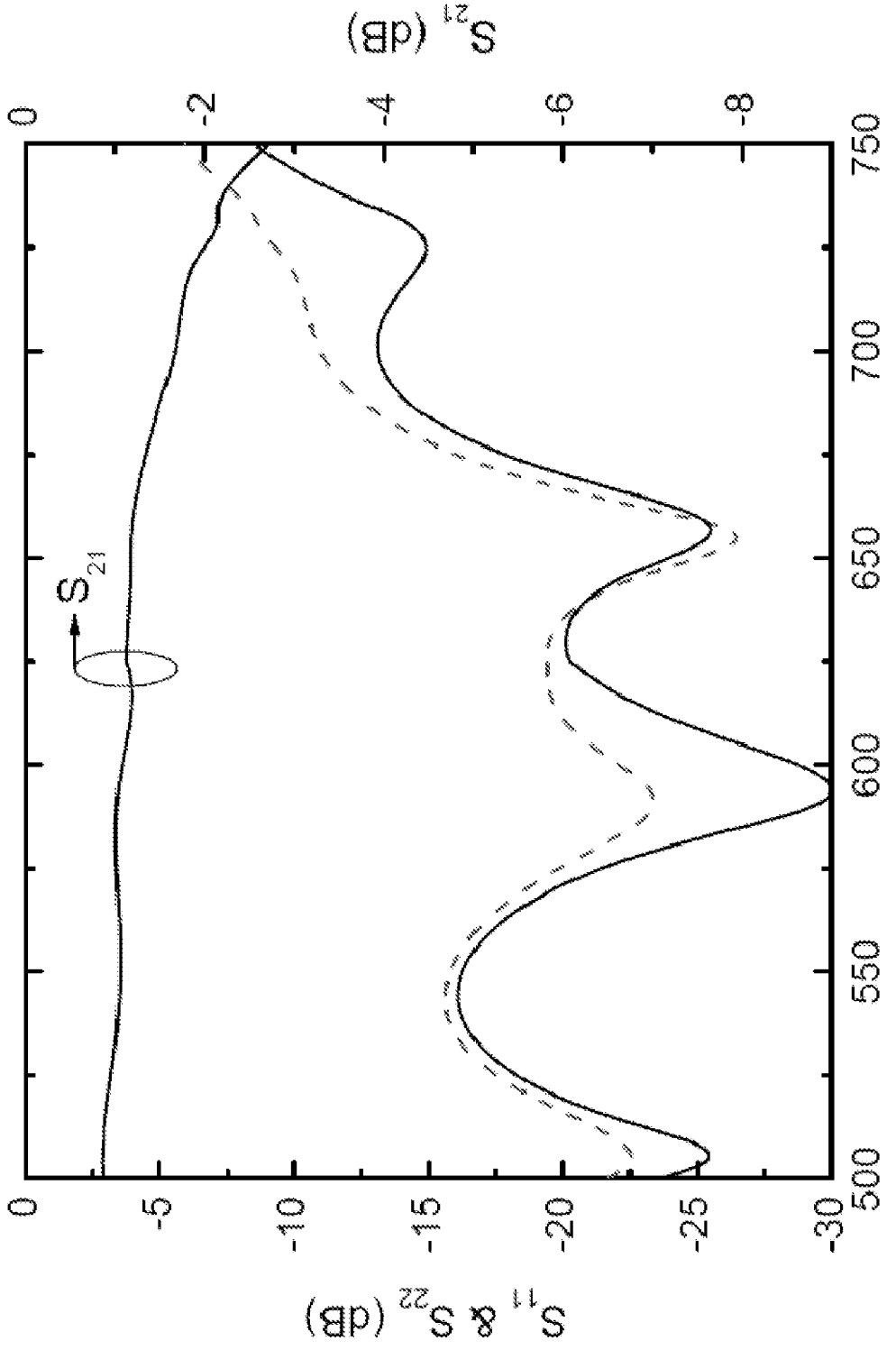

S11 & S22 (dB)
S21 (dB)
GHz
S21
0
-5
-10
-15
-20
-25
-30
500
550
600
650
700
750
-2
-4
-6
-8

FIG. 23C

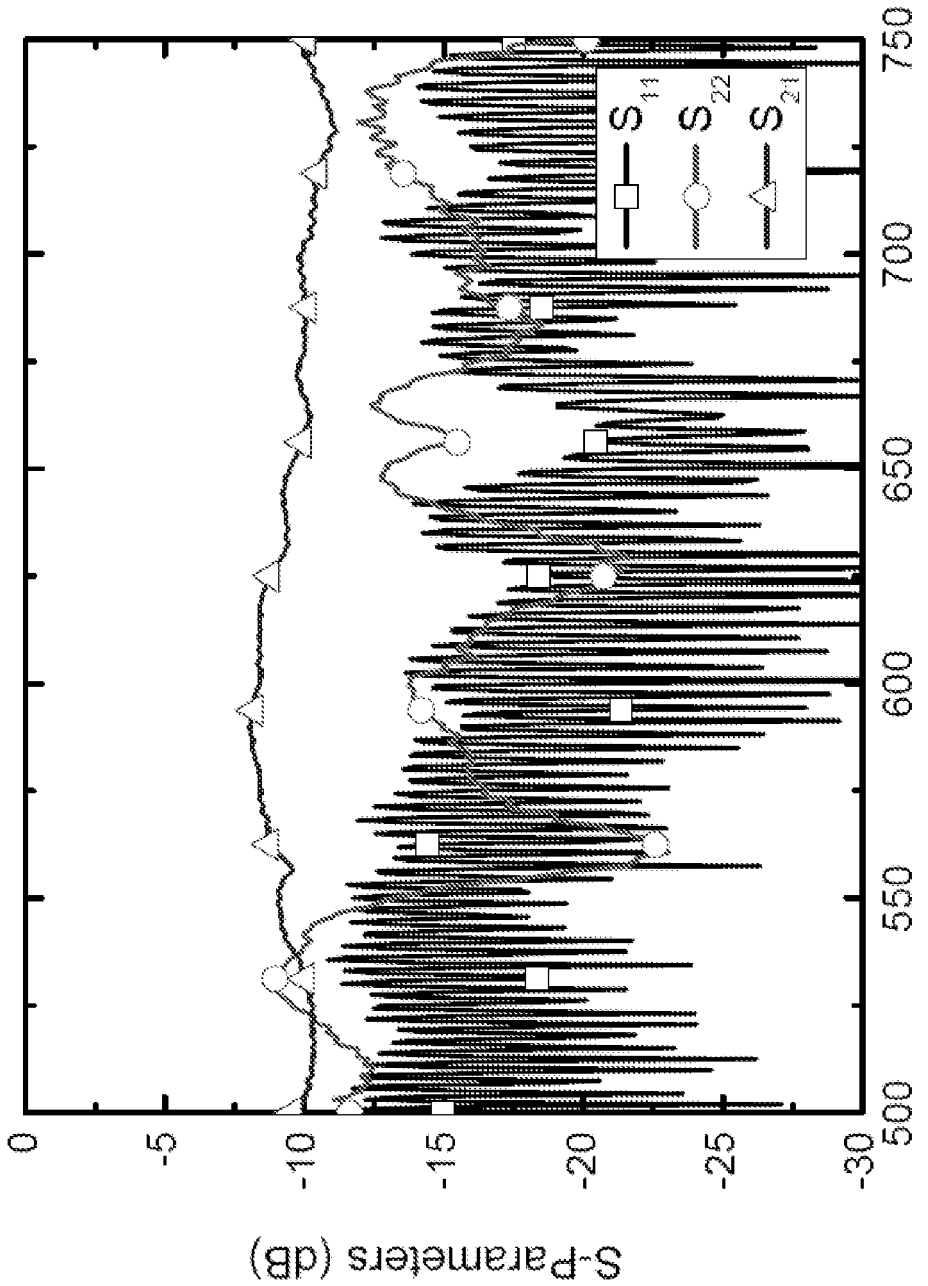

S-Parameters (dB)
0
-5
-10
-15
-20
-25
-30
500
550
600
650
700
750
GHz
S11
S22
S21

FIG. 24A

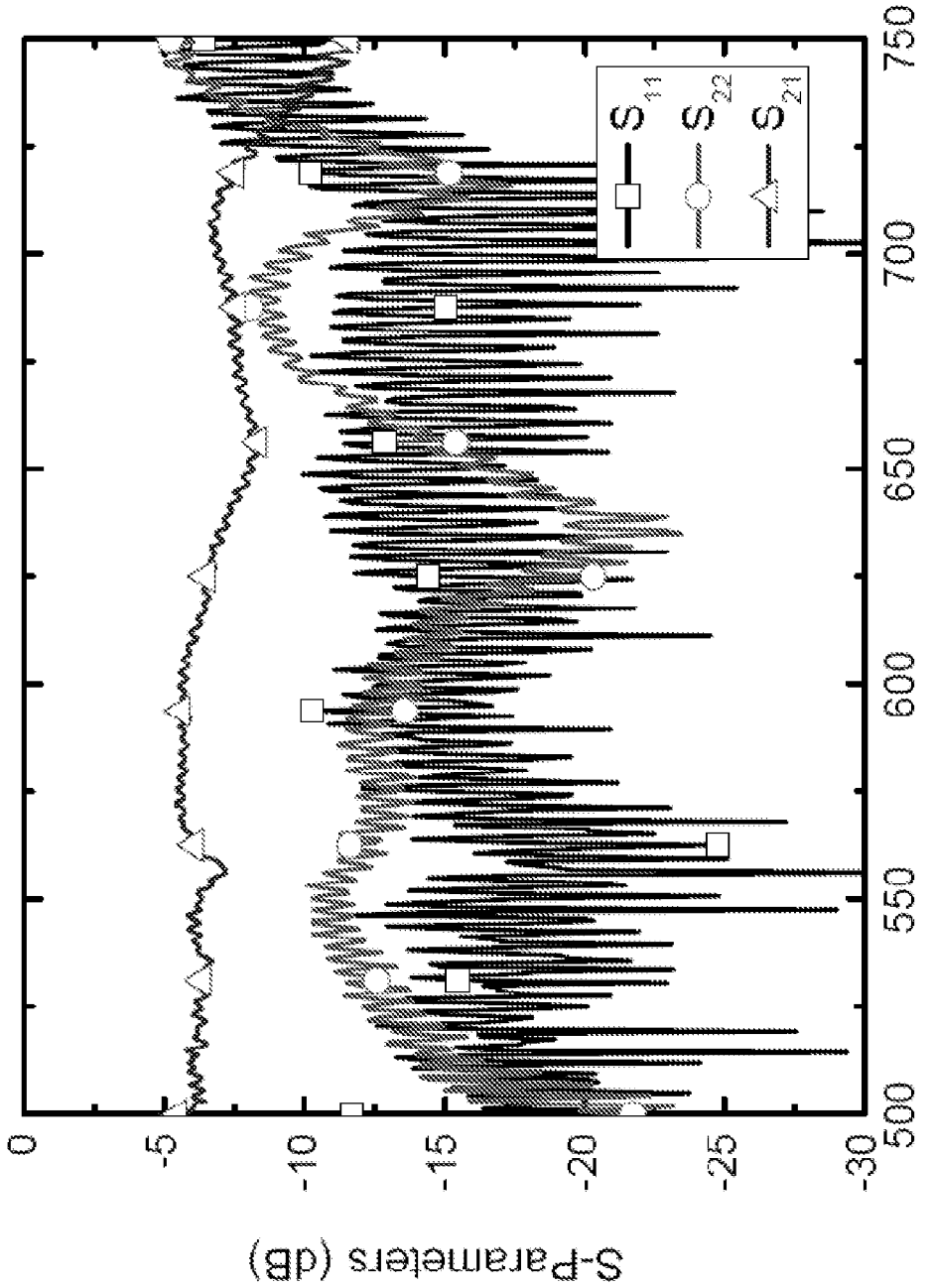

S-Parameters (dB)
0
-5
-10
-15
-20
-25
-30
500
550
600
650
700
750
GHz
S11
S22
S21

FIG. 24B

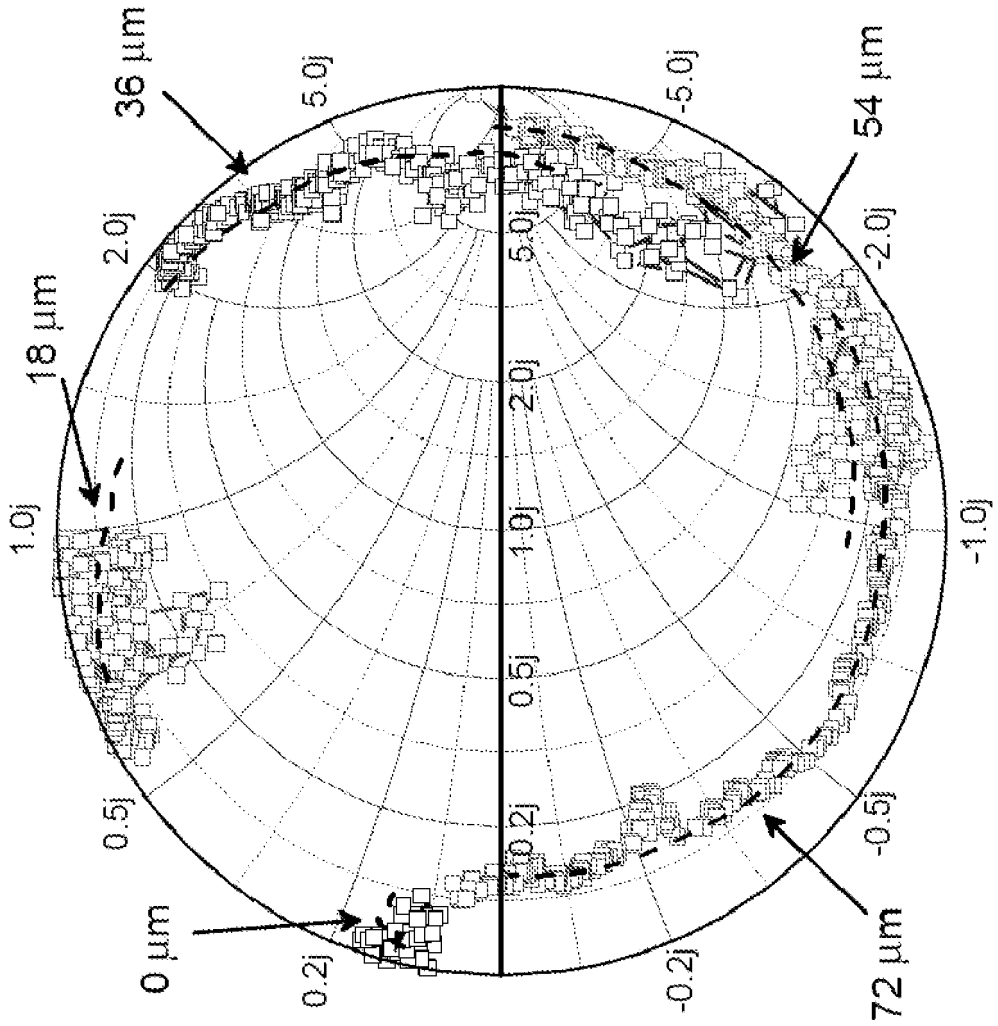


FIG. 25A

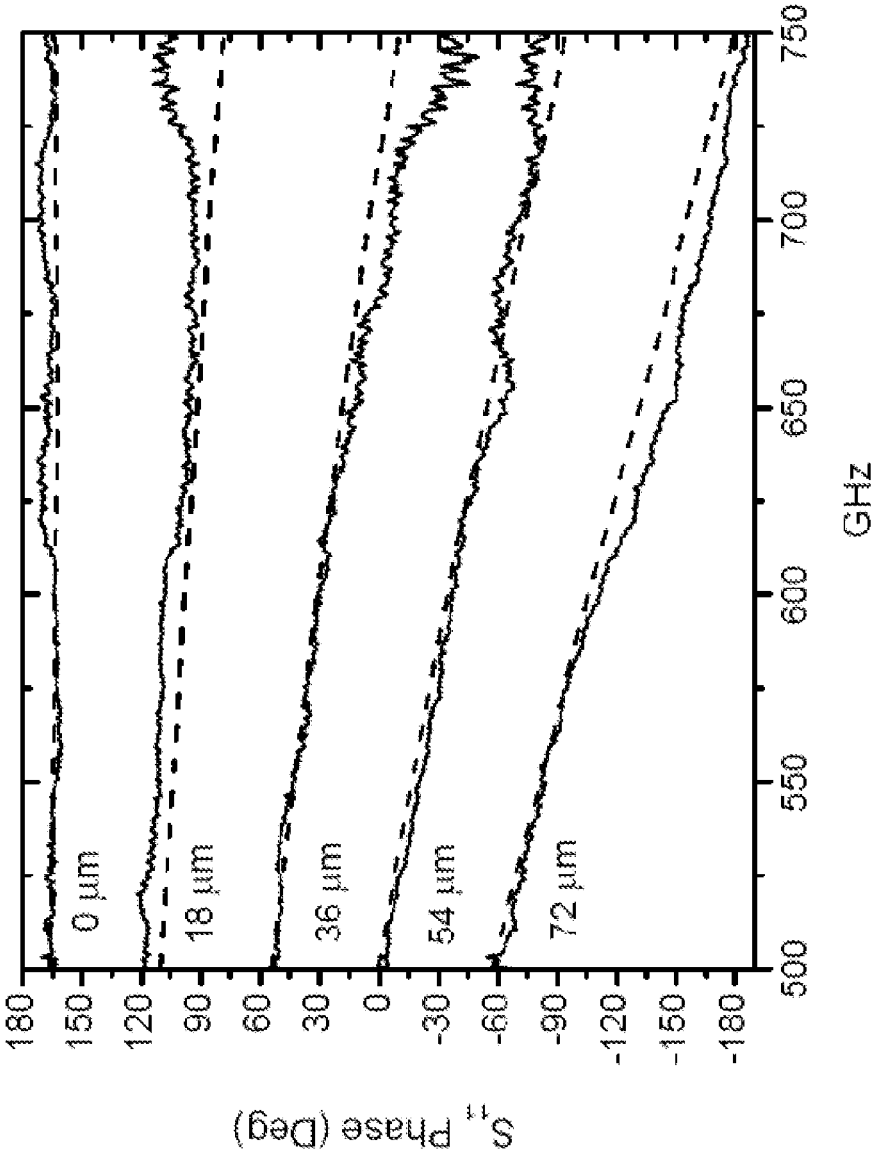

0 µm
18 µm
36 µm
54 µm
72 µm
180
150
120
90
60
30
0
-30
-60
-90
-120
-150
-180
500
550
600
650
700
750
GHz
S11 Phase (Deg)

FIG. 25B

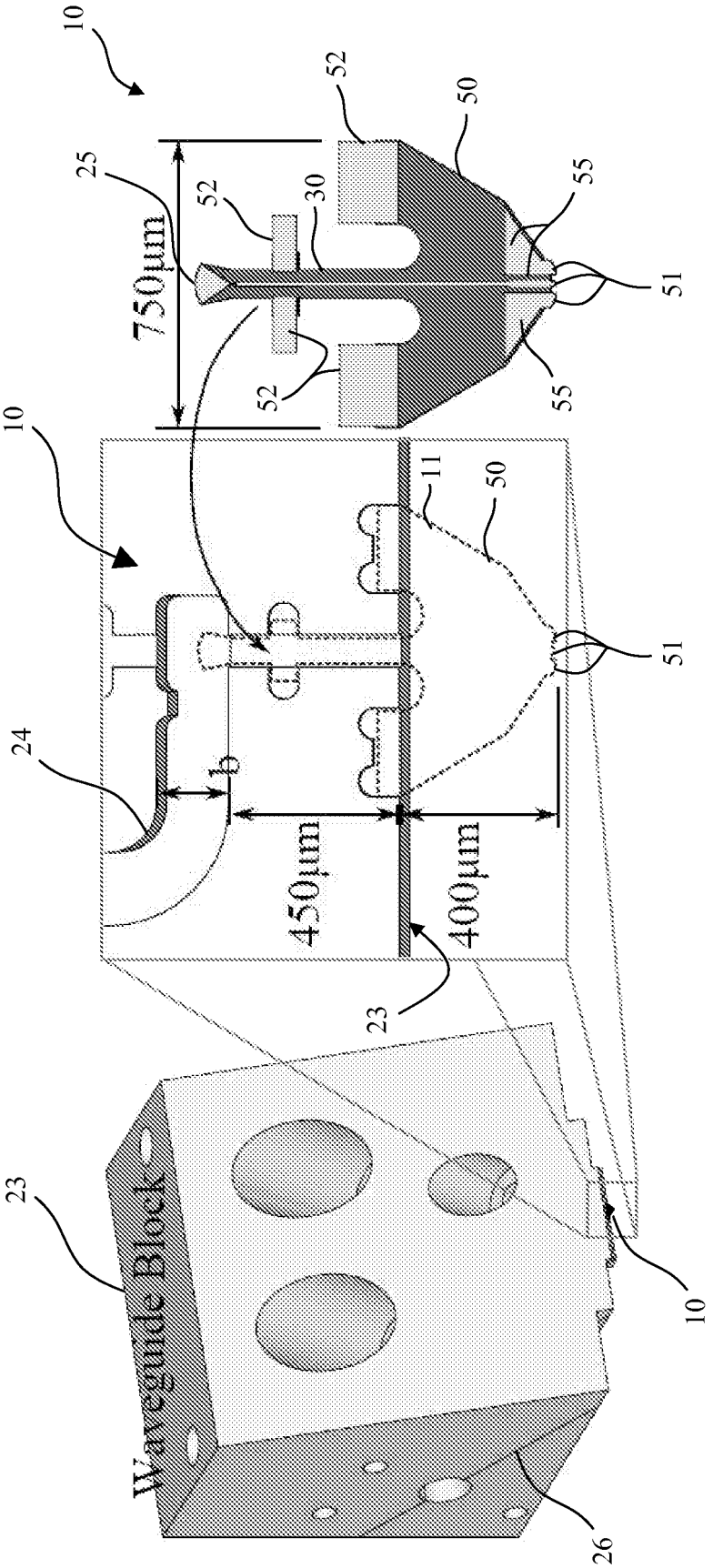


FIG. 26C

FIG. 26B

FIG. 26A

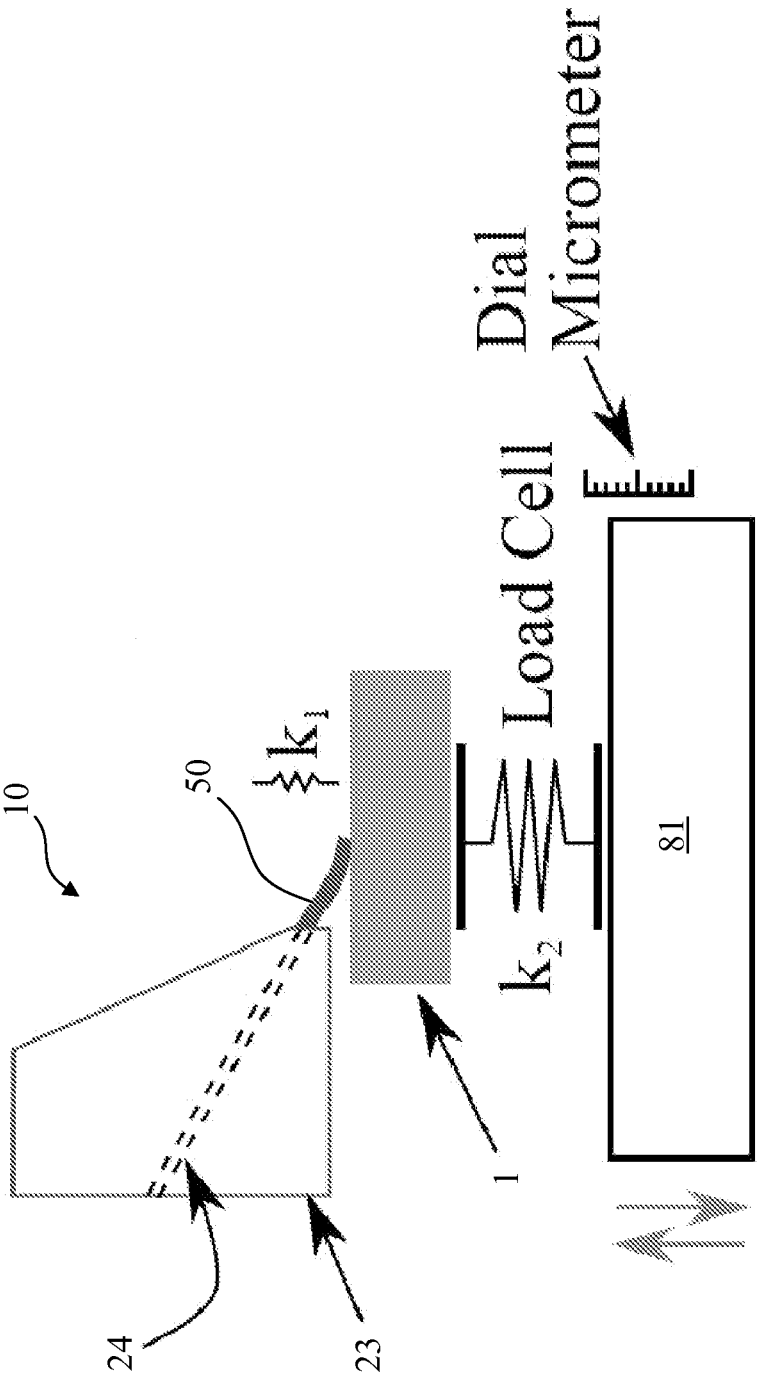


FIG. 27

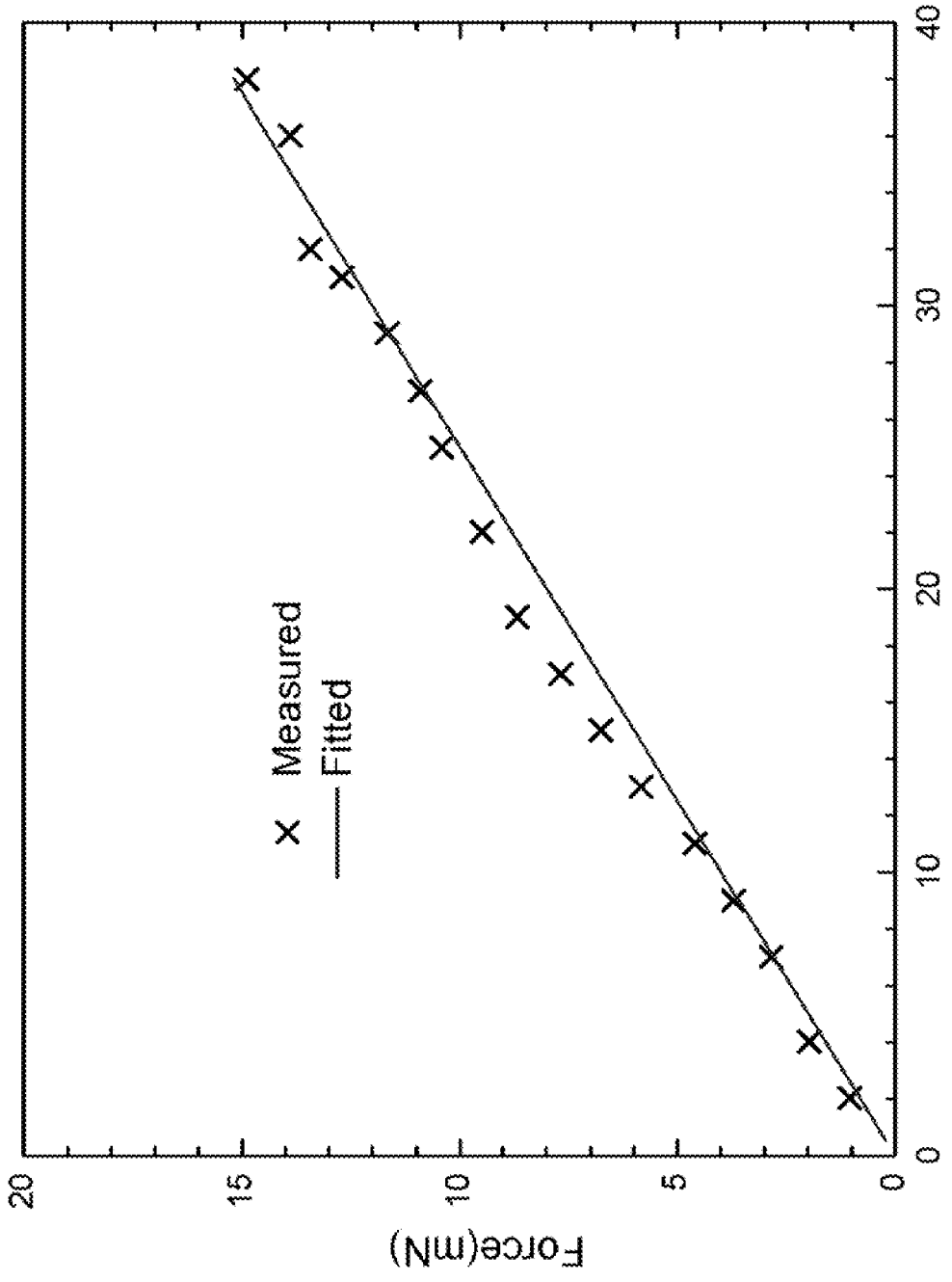

Force(mN)
Displacement(μm)
Measured
Fitted
0
5
10
15
20
0
10
20
30
40

FIG. 28

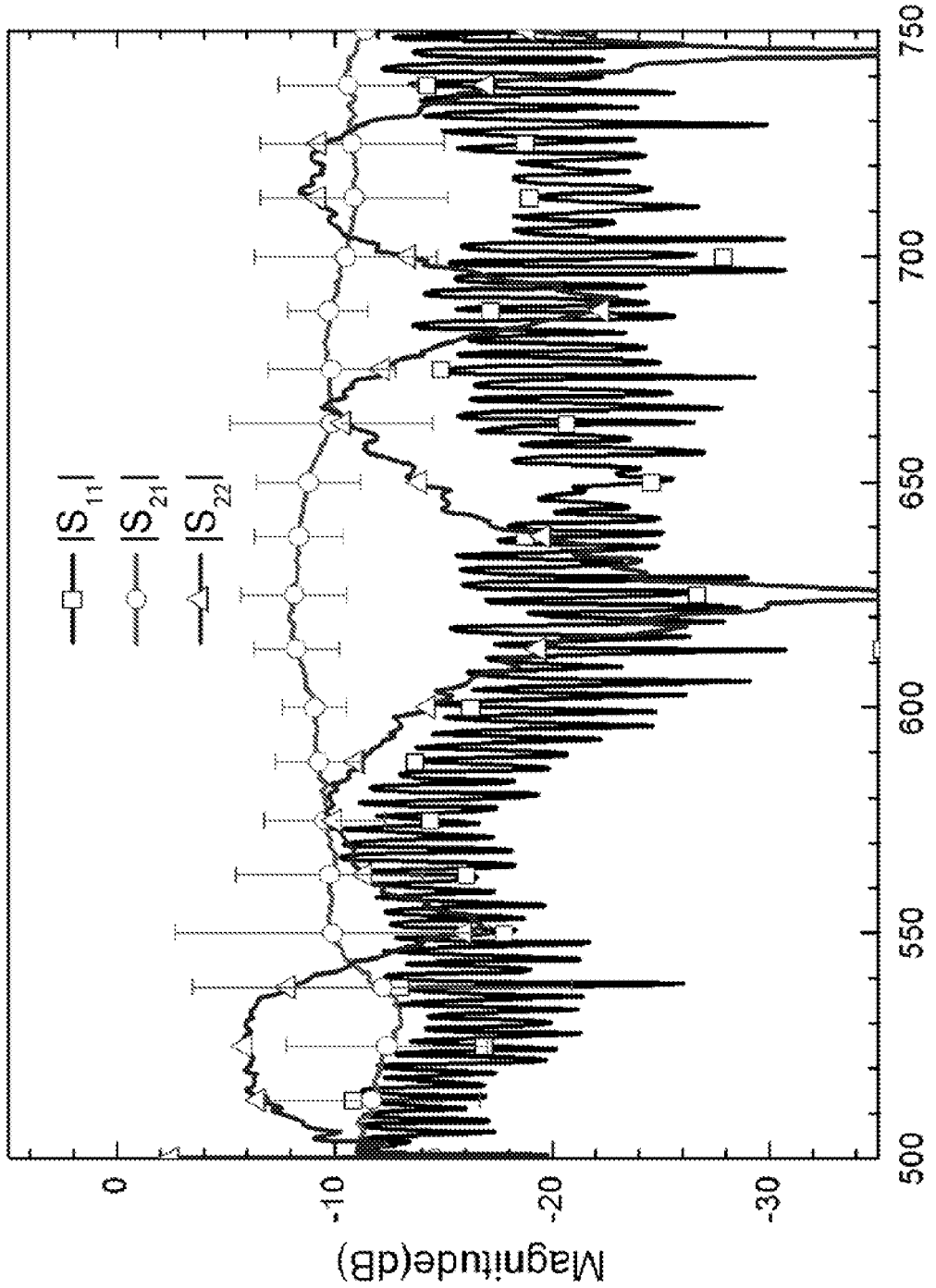

Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)
|S11|
|S21|
|S22|

FIG. 29

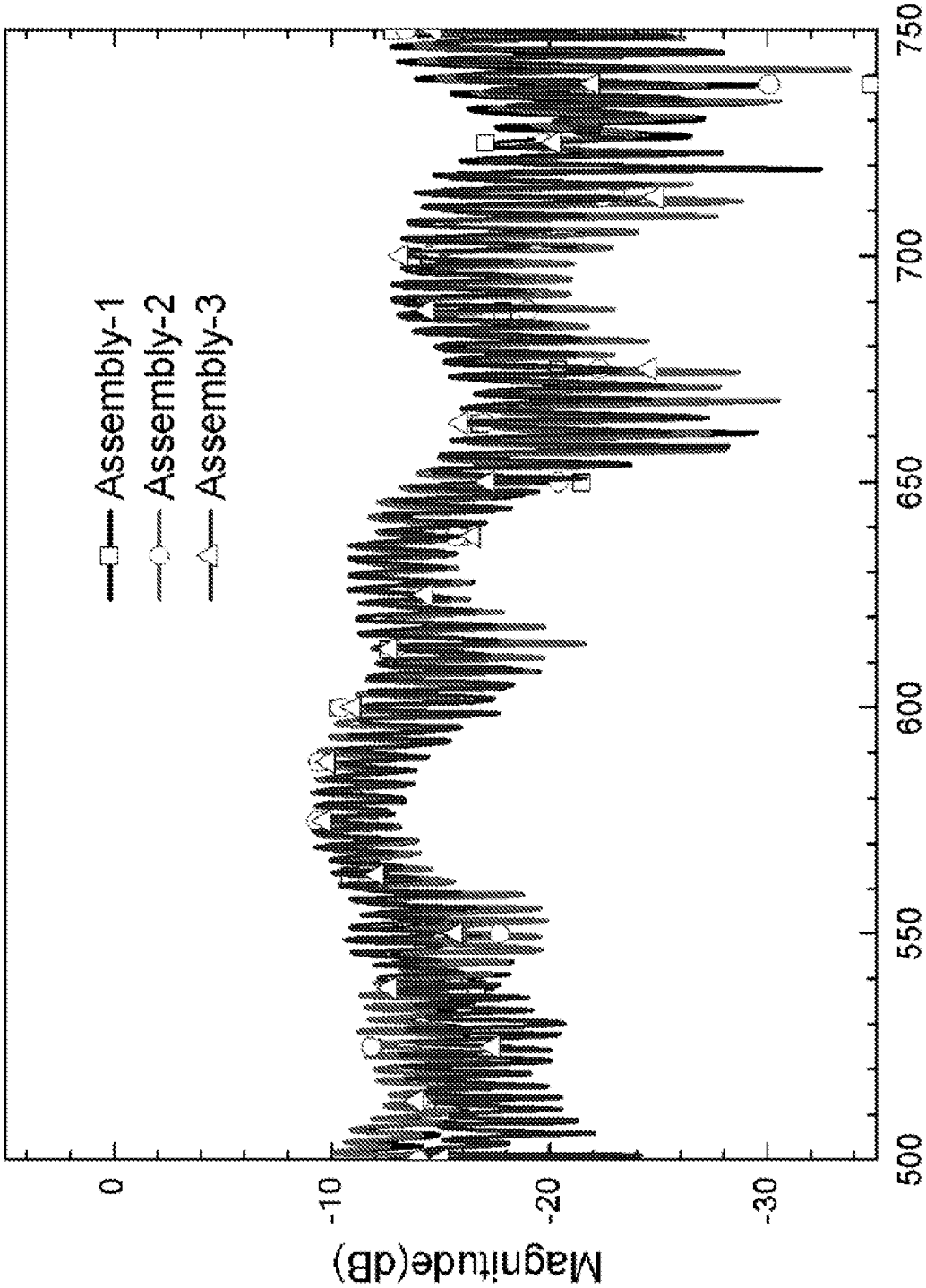

Assembly-1
Assembly-2
Assembly-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 30A

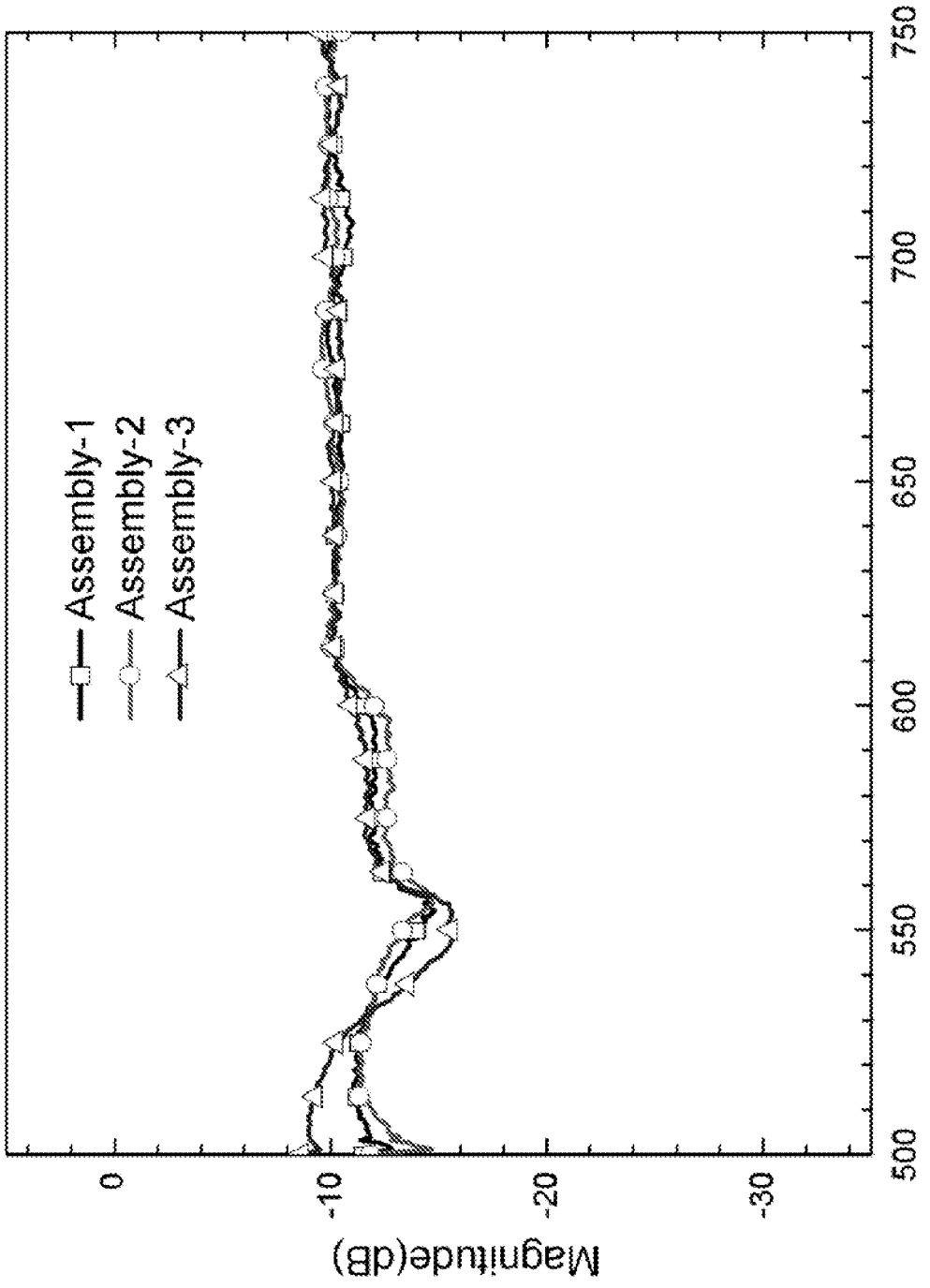

Assembly-1
Assembly-2
Assembly-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 30B

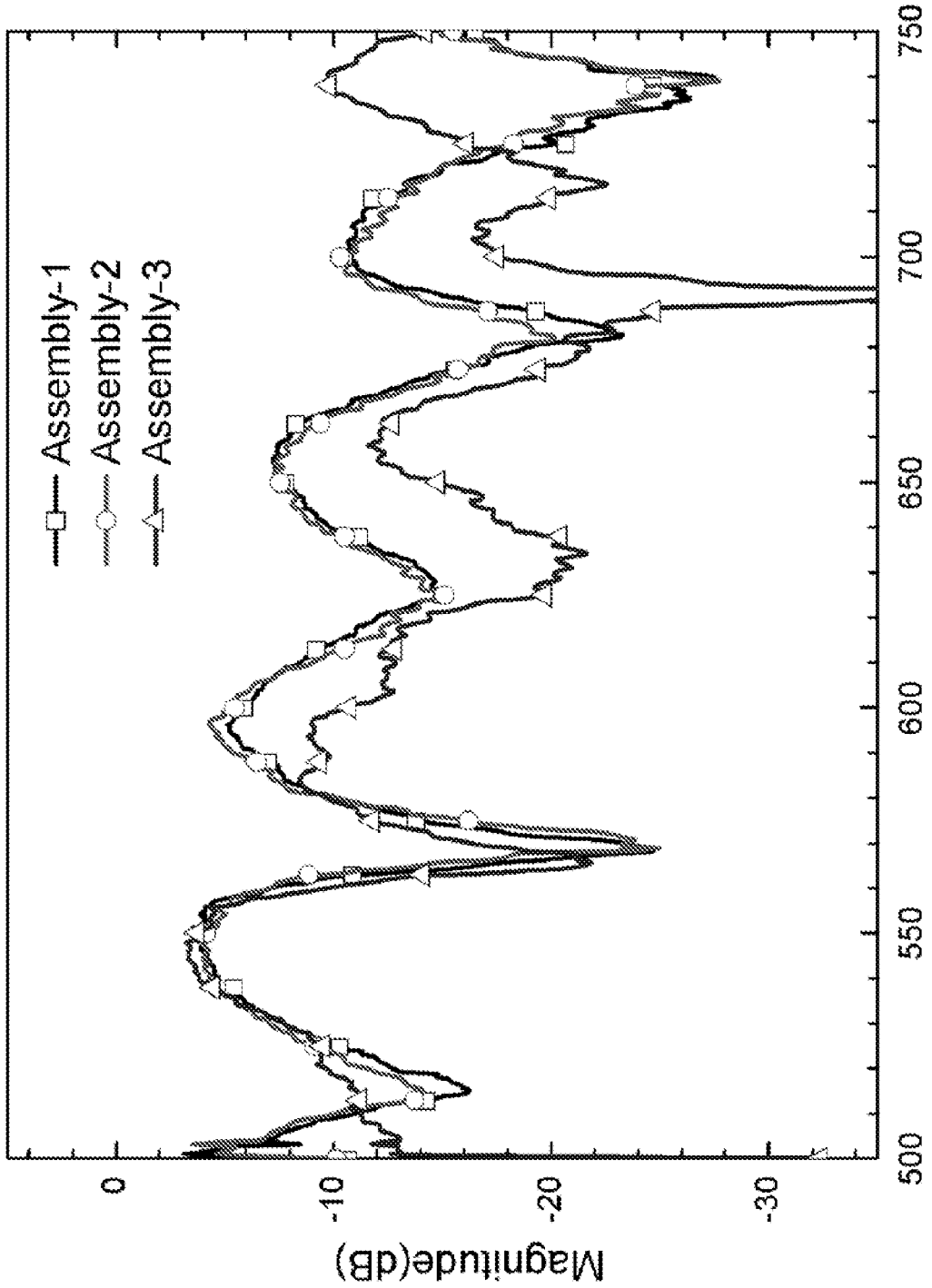

Assembly-1
Assembly-2
Assembly-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 30C

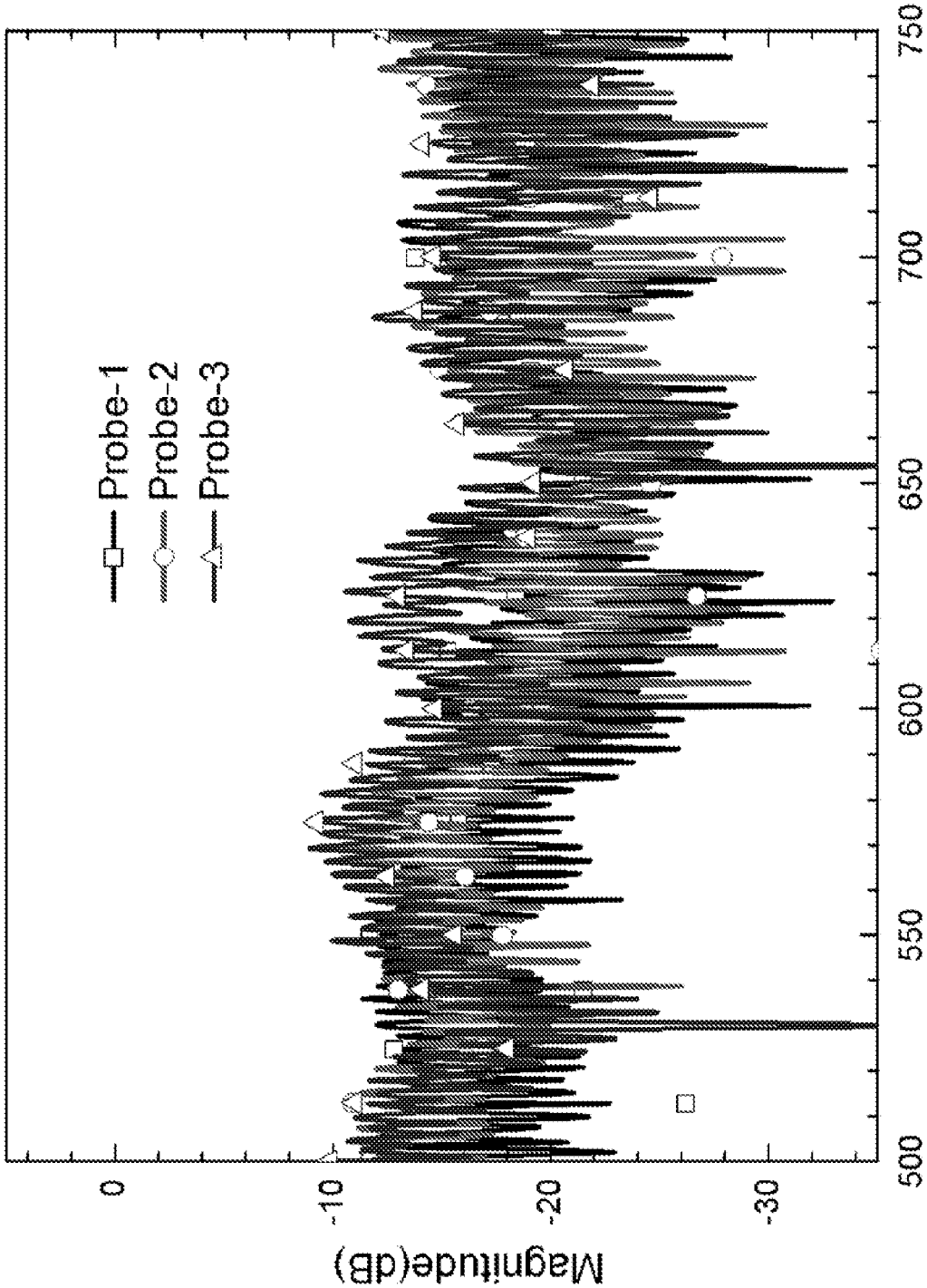

Probe-1
Probe-2
Probe-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 31A

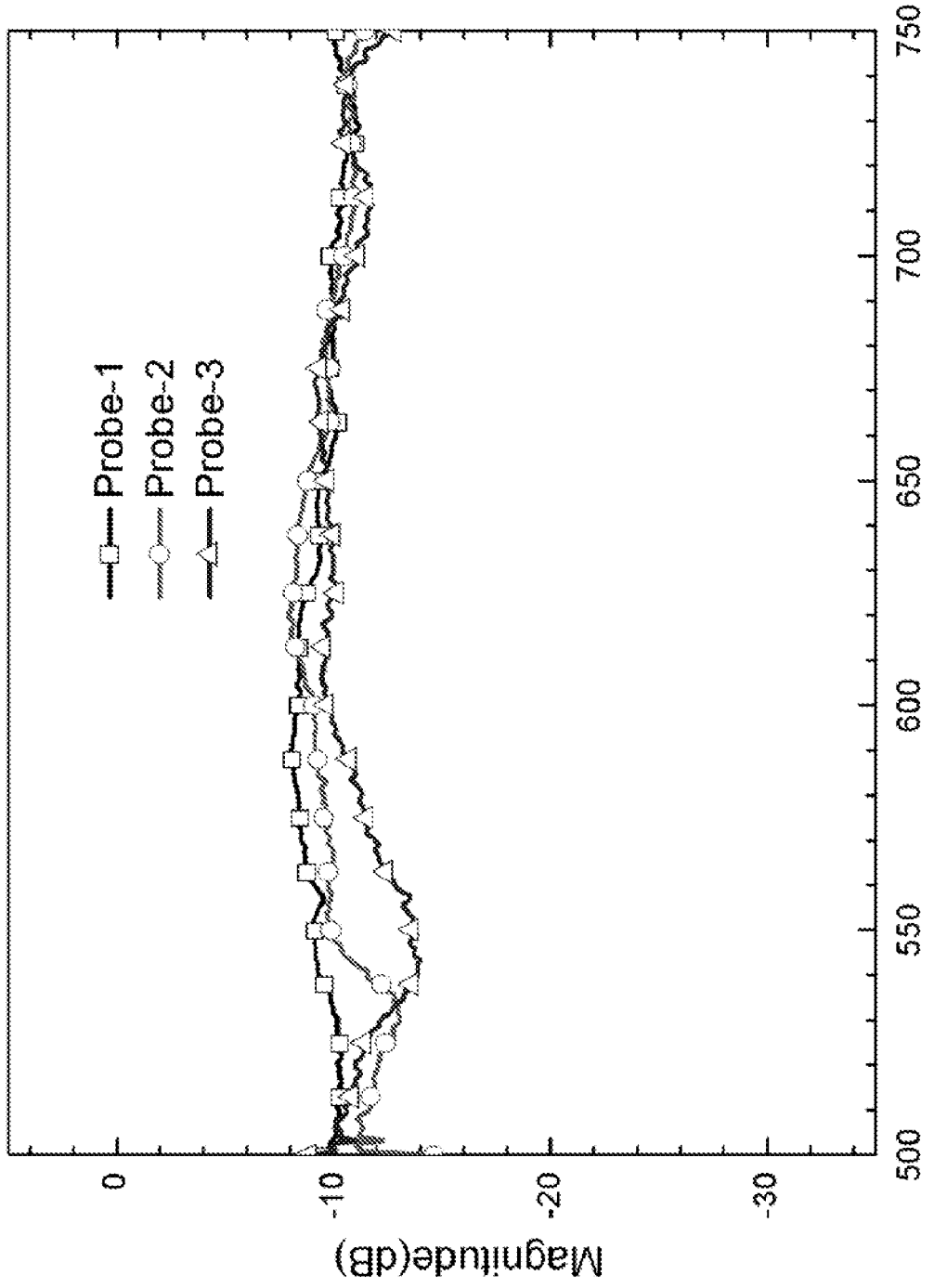

Probe-1
Probe-2
Probe-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 31B

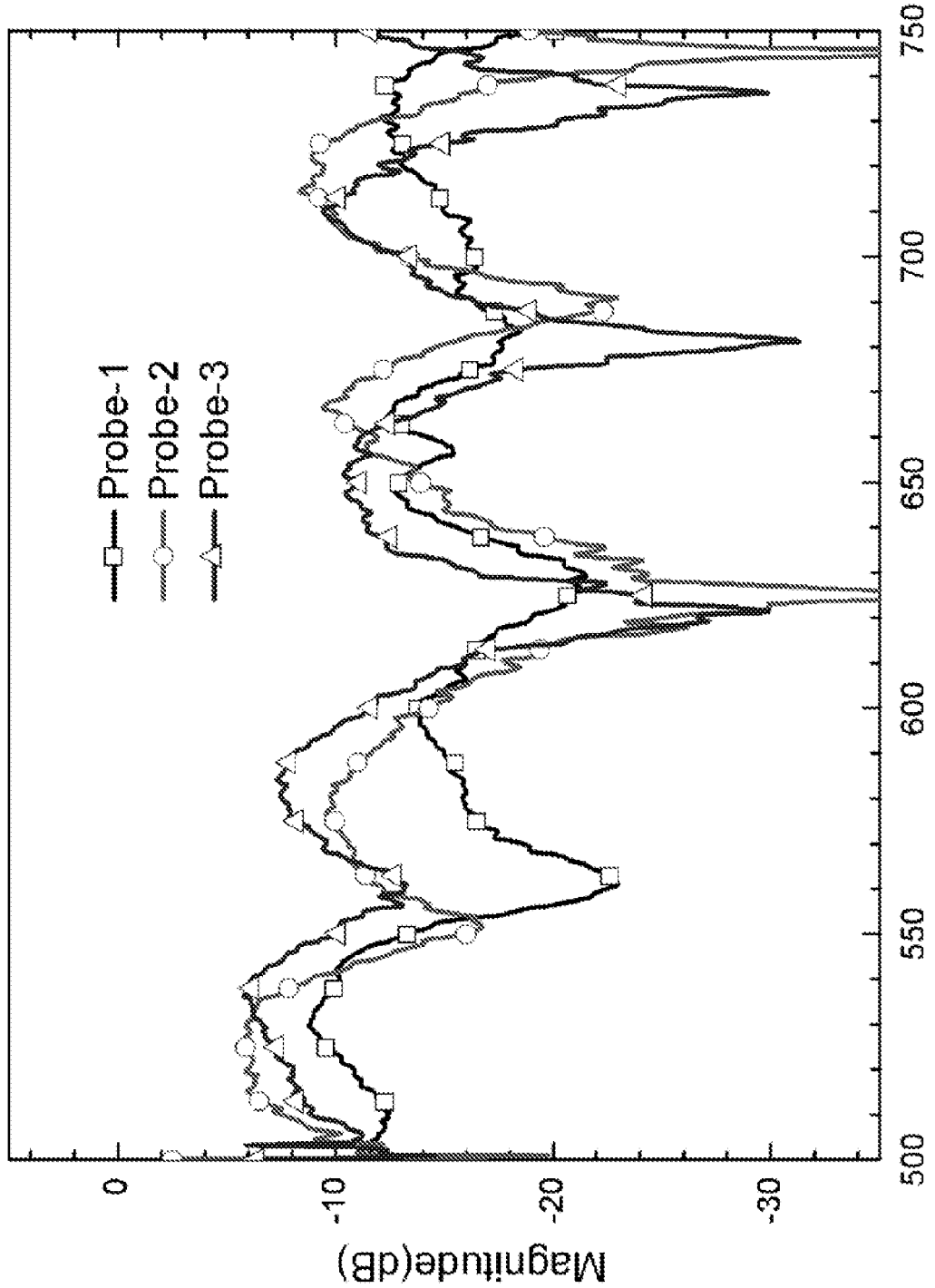

Probe-1
Probe-2
Probe-3
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 31C

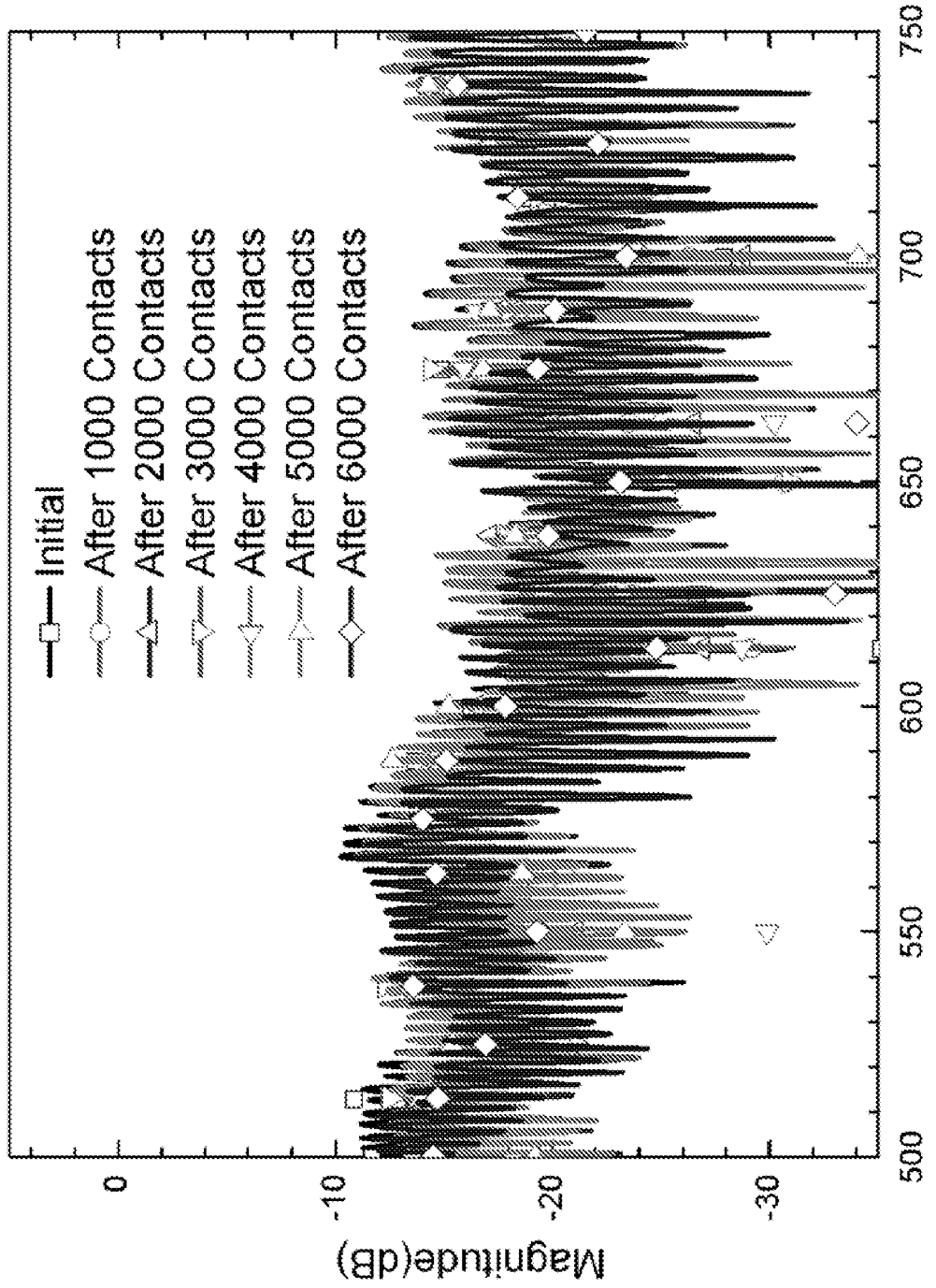

Initial
After 1000 Contacts
After 2000 Contacts
After 3000 Contacts
After 4000 Contacts
After 5000 Contacts
After 6000 Contacts
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 32A

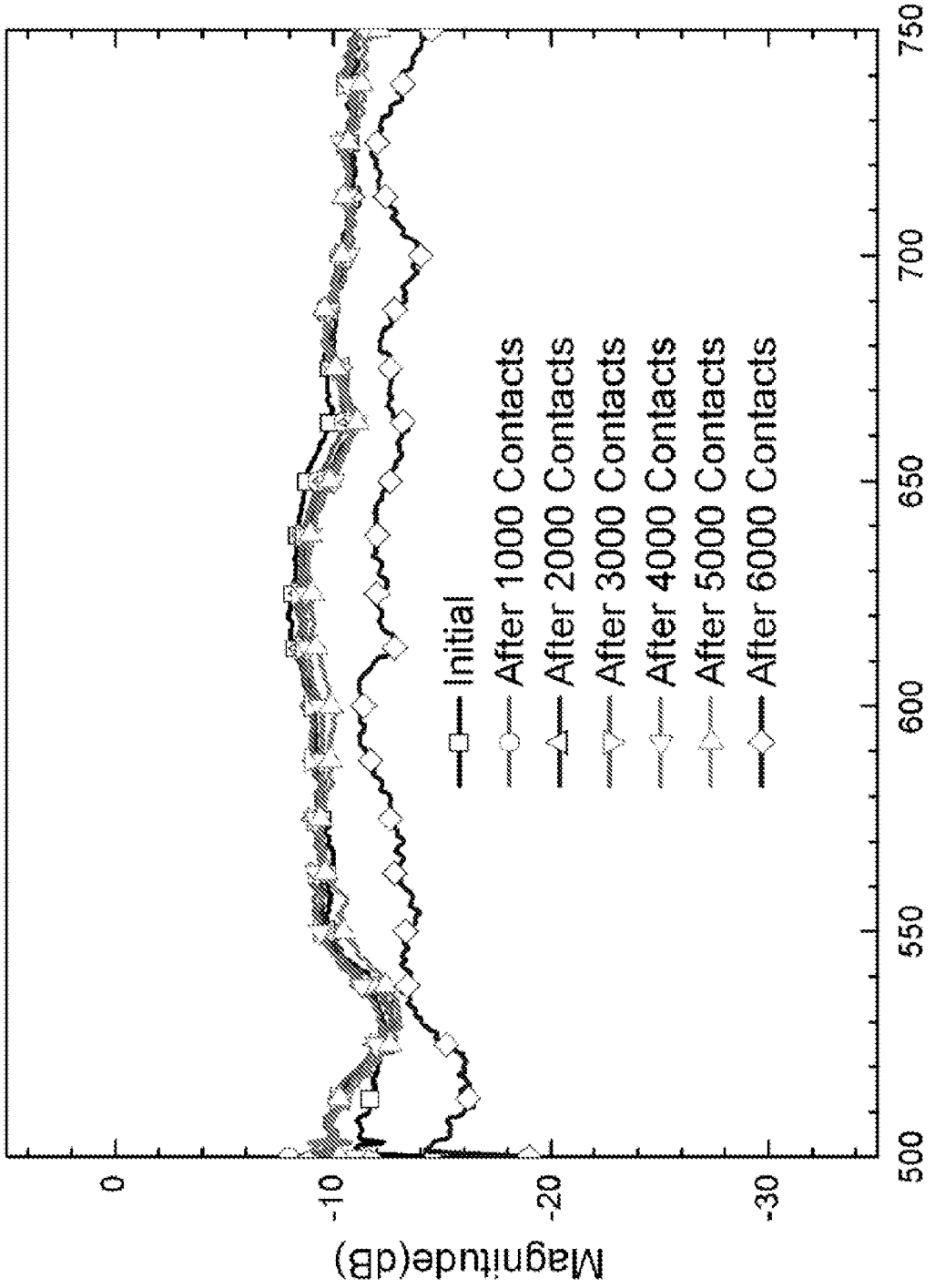

Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)
Initial
After 1000 Contacts
After 2000 Contacts
After 3000 Contacts
After 4000 Contacts
After 5000 Contacts
After 6000 Contacts

FIG. 32B

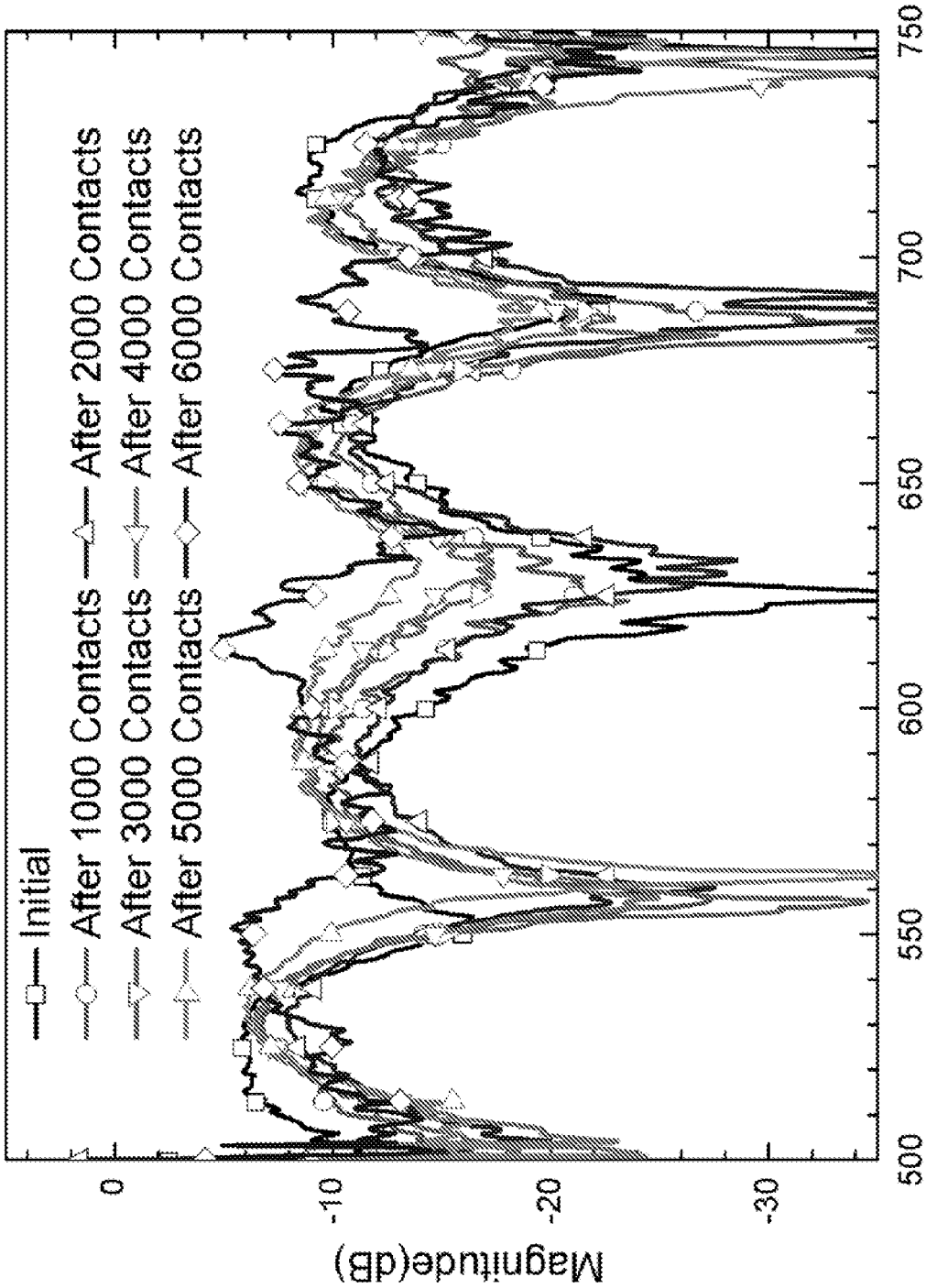

Initial
After 1000 Contacts
After 2000 Contacts
After 3000 Contacts
After 4000 Contacts
After 5000 Contacts
After 6000 Contacts
Magnitude(dB)
0
-10
-20
-30
500
550
600
650
700
750
Frequency(GHz)

FIG. 32C

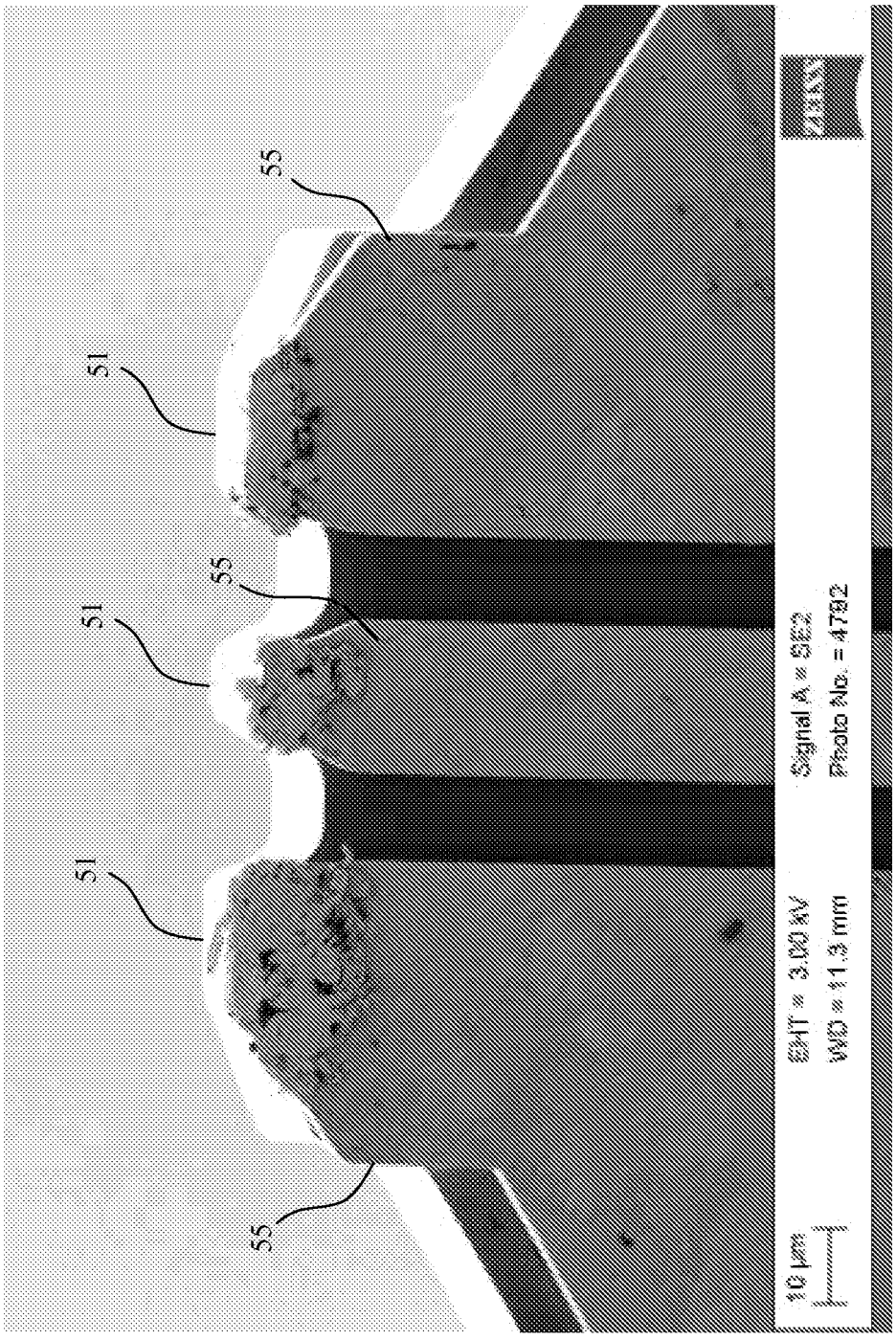

51
51
51
55
55
55
10 µm
EHT = 3.00 kV
WD = 11.3 mm
Signal A = SE2
Photo No. = 4792

FIG. 33A

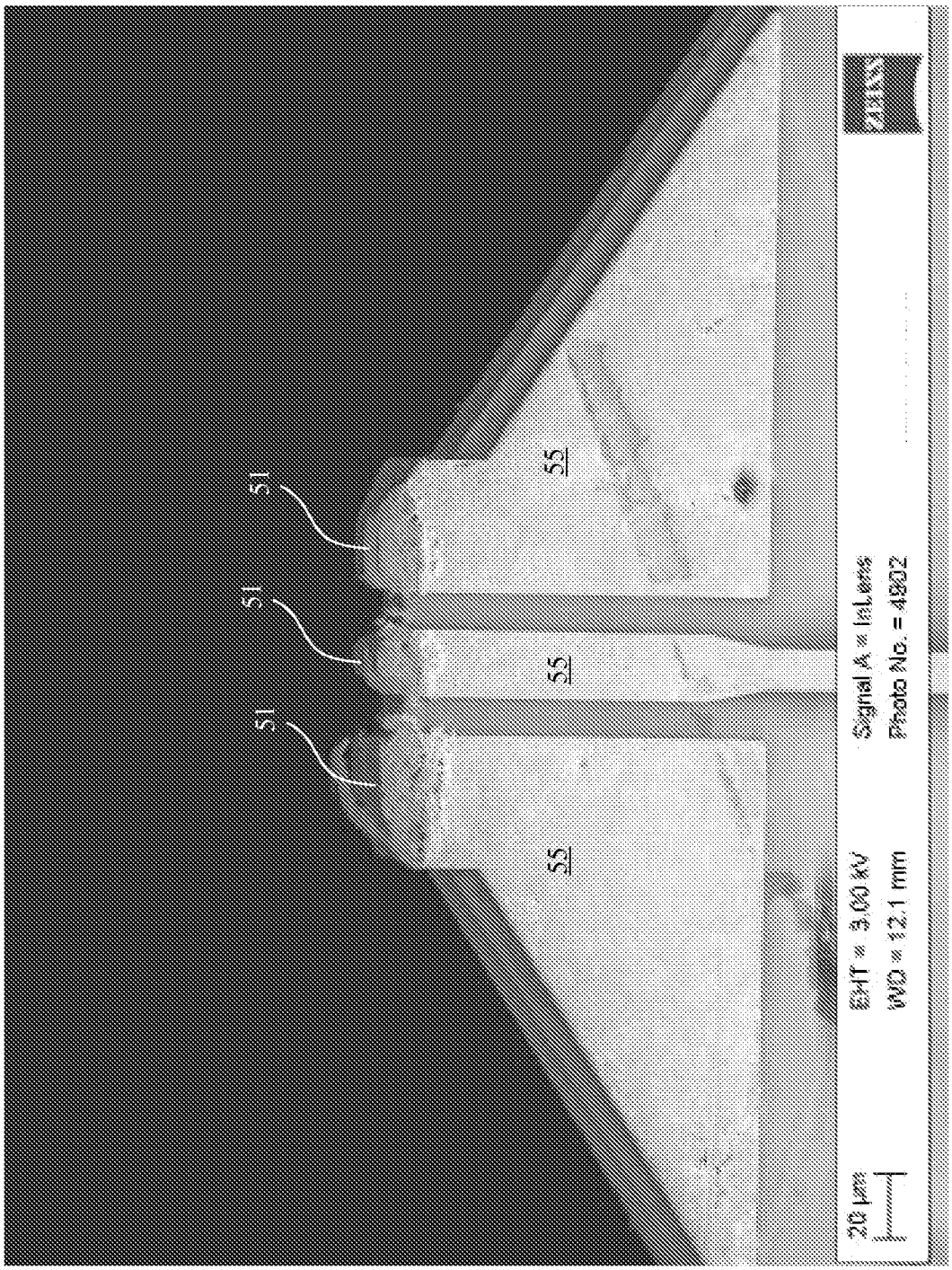

51
51
51
55
55
55
20 µm
EHT = 3.00 kV
WD = 12.1 mm
Signal A = InLens
Photo No. = 4802
ZEISS

FIG. 33B

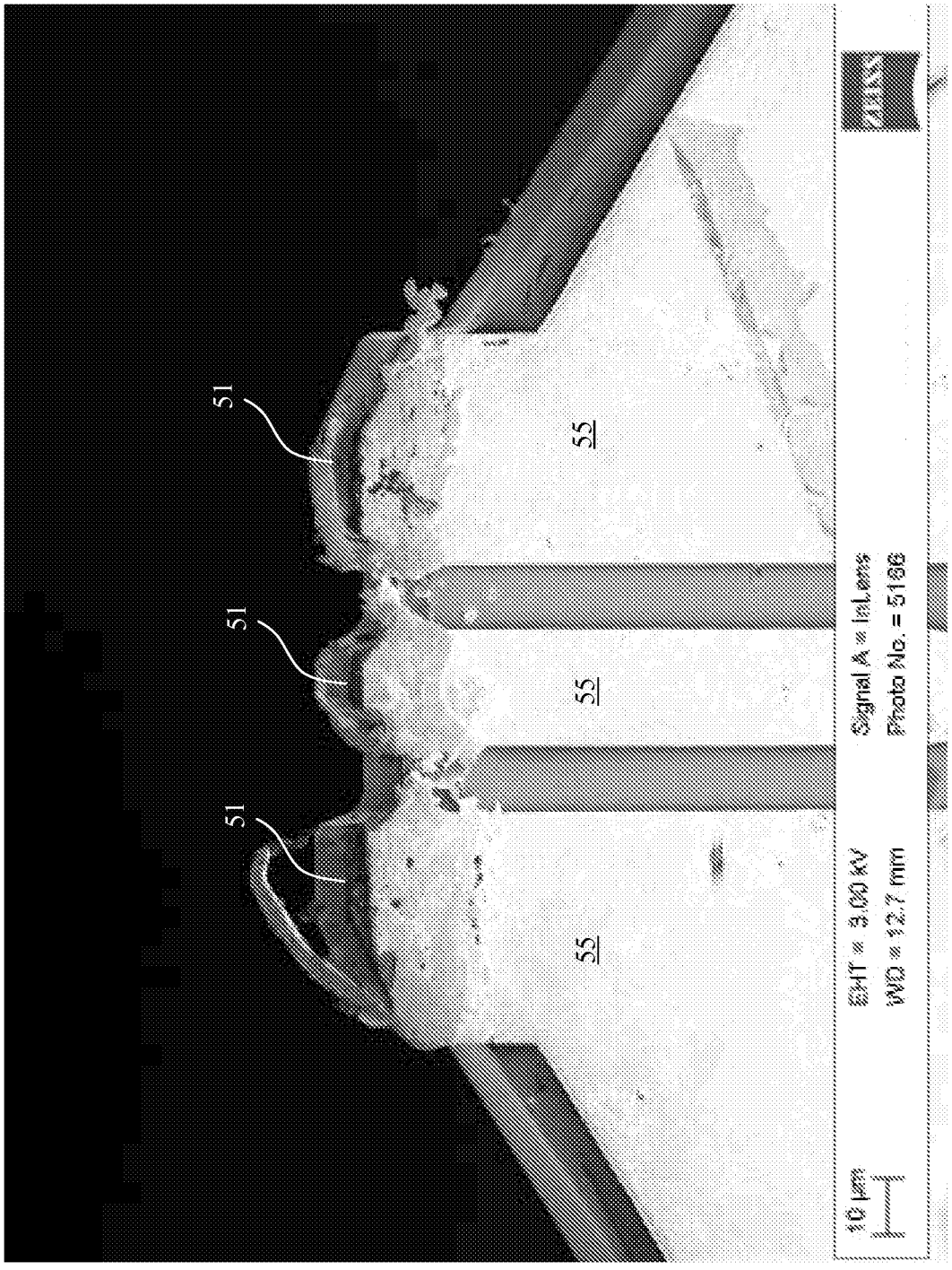

51
51
51
55
55
55
10 µm
EHT = 3.00 kV
WD = 12.7 mm
Signal A = InLens
Photo No. = 5136

FIG. 33C

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 2012131 A1 **[0007]**
- US 20090189623 A1 **[0008]**
- US 20080265919 A1 **[0009]**
- US 20080068034 A1 **[0010]**
- US 5408188 A **[0011]**
- US 4727319 A, Shahriary, I. **[0124]**
- US 5003253 A, Majidi-Ahy **[0124]**
- US 6759859 B2, Deng **[0124]**
- US 6930497 B2, Deng **[0124]**
- US 20030112024 A1, Deng **[0124]**
- US 20040189334 A1, Deng **[0124]**
- US 20050201683 A1, Ghiron **[0124]**
- US 7233160 B2, Hayden **[0124]**
- US 7456646 B2, Hayden **[0124]**
- US 7495461 B2, Hayden **[0124]**
- US 6242930 B1, Matsunaga **[0124]**
- US 4849689 A, Gleason **[0124]**
- US 7619419 B2, Campbell, R. **[0124]**
- US 4641140 A, Heckaman **[0124]**
- US 4894612 A, Drake **[0124]**
- US 7504842 B2, Schwindt, R. **[0124]**
- US 5477159 A, Hamling, D. **[0124]**
- US 5231349 A, Majidi-Ahy **[0124]**
- EP 0367542 A3, Gleason **[0124]**
- EP 89311203 **[0124]**
- EP 0367542 A2, Gleason **[0124]**
- US 7427868 B2, Strid **[0124]**
- US 7449899 B2, Campbell **[0124]**
- US 4827211 B2, Strid **[0124]**
- US 7304488 B2, Gleason **[0124]**
- US 7436194 B2, Gleason **[0124]**
- US 7501842 B2, Gleason **[0124]**
- US 20080042671 A1, Gleason **[0124]**
- US 97547107 **[0124]**
- WO 2004107401 A2, Gleason **[0124]**
- US 2004012806 W **[0124]**
- US 5565788 A, Burr **[0124]**
- US 7498829 B2, Gleason **[0124]**
- US 7394269 B2, Gleason **[0124]**
- US 7271603 B2, Gleason **[0124]**
- US 7057404 B2, Gleason **[0124]**
- US 7688097 B2, Hayden **[0124]**
- US 7898273 B2, Gleason **[0124]**

Non-patent literature cited in the description

- **J. HESLER ; A. KERR ; W. GRAMMER ; E. WOLLACK.** Recommendations for waveguide interfaces to 1 THZ. *18th International Symposium on Space Terahertz Technology,* 2007 **[0098] [0124]**
- **T. RECK ; L. CHEN ; C. ZHANG ; C. GROPPI ; H. XU ; A. ARSENOVIC ; S. BARKER ; A. LICHTENBERGER ; R. WEIKLE.** Calibration accuracy of a 625 GHz on-wafer probe. *76th ARFTG Microwave Measurement Conference Digest,* December 2010 **[0116]**
- **W. DEAL.** Solid-state amplifiers for terahertz electronics. *Proceedings of the IEEE MTT-S International Microwave Symposium,* 2010 **[0124]**
- **J. HACKER ; M. SEO ; A. YOUNG ; Z. GRIFFITH ; M. URTEAGA ; T. REED ; M. RODWELL.** THz MMICs based on InP HBT technology. *Proceedings of the IEEE MTT-S International Microwave Symposium,* 2010 **[0124]**
- **A. FUNG ; D. DAWSON ; L. SAMOSKA ; K. LEE ; T. GAIER ; P. KANGASLAHTI ; C. OLESON ; A. DENNING ; Y. LAU ; G. BOLL.** Two-port vector network analyzer measurements in the 218-344 and 356-500-GHz frequency bands. *Microwave Theory and Techniques, IEEE Transactions on,* December 2006, vol. 54 (12), 4507-4512 **[0124]**
- **S. LIU ; G. BOLL.** A new probe for w-band on-wafer measurements. *Microwave Symposium Digest, 1993., IEEE MTT-S International,* 1993, vol. 3, 1335-1338 **[0124]**
- **R. BASS ; A. LICHTENBERGER ; R. WEIKLE ; S. PAN ; E. BRYERTON ; J. KOOI ; C. WALKER.** Ultra-thin silicon chips for submillimeter-wave applications. *Proceedings of the Fifteenth International Symposium on Space THz Technology,* March 2004 **[0124]**

- **J. W. KOOI ; G. CHATTOPADHYAY ; S. WITHINGTON ; F. RICE ; J. ZMUIDZINAS ; C. WALKER ; G. YASSIN.** A full-height waveguide to thinfilm microstrip transition with exceptional RF bandwidth and coupling efficiency. *International Journal of Infrared and Millimeter Waves,* March 2003, vol. 24 (3), 261-284 **[0124]**
- **E. M. GODSHALK.** *Wafer probing at w-band,* September 1993, 848-850 **[0124]**
- The infinity probe for on-wafer device characterization and modeling to 110 GHZ. *Cascade Microtech, Tech. Rep.,* 2004 **[0124]**
- Infinity probe: high-frequency performance with low, stable contact resistance. Tech. Rep. Cascade Microtech, Inc, 2008 **[0124]**
- **J. SCHIMKAT.** Contact measurements providing basic design data for microrelay actuators. *Sensors and Actuators A: Physical,* 1999, vol. 73 (1-2), 138-143, http://www.sciencedirect.com/science/article/B6THG-3WWKPDW-1F/2/27c17f2b6bd61b893f706210565ca324 **[0124]**
- **I. CHASIOTIS ; C. BATESON ; K. TIMPANO ; A. MCCARTY ; N. BARKER ; J. STANEC.** Strain rate effects on the mechanical behavior of nanocrystalline Au films. *Thin Solid Films,* 2007, vol. 515 (6), 3183-3189 **[0124]**
- *Mechanical Behaviour of Thin Films and Small Structures - TMS,* 2005, http://www.sciencedirect.com/science/article/B6TW0-4JCBN4F-5/2/0d8c70a8e8b0fc0b3ac34377f55b75bb **[0124]**
- **D. SON ; J.-J. KIM ; T. W. LIM ; D. KWON.** Evaluation of fatigue strength of LIGA nickel film by microtensile tests. *Scripta Materialia,* May 2004, vol. 50, 1265-1269 **[0124]**
- Fused silica. *Del Mar Ventures, Tech. Rep.,* 2007, http://www.sciner.com/Opticsland/FS.htm. **[0124]**
- **K. HJORT ; J. SODERKVIST ; J. A. SCHWEITZ.** Gallium arsenide as a mechanical material. *Journal of Micromechanics and Microengineering,* 1994, vol. 4 (1), 1, http://stacks.iop.org/0960-1317/4/i=1/a=001 **[0124]**
- **H. BELSINGER et al.** A fracture criterion for gallium arsenide wafers. *Engineering Fracture Mechanics,* May 1994, vol. 48 (2), 199-205 **[0124]**
- Aluminum oxide. *Accuratus, Tech. Rep.,* 2002, http://www.accuratus.com/alumox.html. **[0124]**
- Silicon nitride. *Accuratus, Tech. Rep.,* 2002, http://www.accuratus.com/silinit.html. **[0124]**
- Kapton polyimide film. *Du Pont, Tech. Rep.,* 2010, http://www2.dupont.com/Kapton/. **[0124]**
- **J. S. DANEL ; G. DELAPIERRE.** Quartz: a material for microdevices. *Journal of Micromechanics and Microengineering,* 1991, vol. 1 (4), 187, http://stacks.iop.org/0960-1317/1/i=4/a=001 **[0124]**
- **X. LI ; T. KASAI ; S. NAKAO ; H. TANAKA ; T. ANDO ; M. SHIKIDA ; K. SATO.** Measurement for fracture toughness of single crystal silicon film with tensile test. *Sensors and Actuators A: Physical,* 2005, vol. 119 (1), 229-235, http://www.sciencedirect.com/science/article/B6THG-4CY0GYV-1/2/390b1252940707c4776e9761c6cc3a5b **[0124]**
- **M. AFSAR ; H. CHI ; X. LI.** Millimeter wave complex refractive index, complex dielectric permittivity and loss tangent of high purity and compensated silicon. *Precision Electromagnetic Measurements, 1990. CPEM '90 Digest., Conference on,* 1990, vol. 11-14, 238-239 **[0124]**
- **F. P. BEER ; J. E. RUSSELL JOHNSTON ; J. T. DEWOLF.** Mechanics of Materials. McGraw-Hill, 2002 **[0124]**
- **M. RIAZIAT ; R. MAJIDI-AHY ; I.-J. FENG.** Propagation modes and dispersion characteristics of coplanar waveguides. *Microwave Theory and Techniques, IEEE Transactions on,* March 1990, vol. 38 (3), 245-251 **[0124]**
- **L. CHEN ; C. ZHANG ; T. J. RECK ; C. GROPPIL ; A. ARSENOVIC ; A. LICHTENBERGER ; R. M. WEIKLE ; N. S. BARKER.** Terahertz micromachined onwafer probes: Repeatability and robustness. *International Microwave Symposium,* 2011 **[0124]**
- **E. RABINOWICZ.** Friction and Wear of Materials. John Wiley & Sons, Inc, 1995 **[0124]**
- **A. BROUE ; J. DHENNIN ; F. COURTADE ; P.-L. CHARVET ; P. PONS ; X. LAFONTAN ; R. PLANA.** *Thermal and topological characterization of Au, Ru and Au/Ru based MEMS contacts using nanoindenter,* 2010, 544-547 **[0124]**
- **Z. ZHOU ; K. MELDE.** Development of a broadband coplanar waveguide-to-microstrip transition with vias. *Advanced Packaging, IEEE Transactions on,* November 2008, vol. 31 (4), 861-872 **[0124]**
- **T. RECK ; L. CHEN ; C. ZHANG ; C. GROPPI ; H. XU ; A. ARSENOVIC ; S. BARKER ; A. LICHTENBERGER ; R. WEIKLE.** Micromachined on-wafer probes. *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International,* May 2010, 65-68 **[0124]**
- **C. RISACHER ; V. VASSILEV ; A. PAVOLOTSKY ; V. BELITSKY.** Waveguideto-microstrip transition with integrated bias-T. *IEEE Microwave and Wireless Components Letters,* July 2003, vol. 13 (7), 262-264 **[0124]**
- **D. KASILINGAM ; D. RUTLEDGE.** Surface-wave losses of coplanar tranmission lines. *Microwave Symposium Digenst, MTT-S International,* May 1983, vol. 83 (1), 113-116 **[0124]**
- **J. OU ; M. CAGGIANO.** *Determine two-port s-parameters from oneport measurements using calibration substrate standards,* May 2005, vol. 2, 1765-1768 **[0124]**

- **K. WONG.** Uncertainty analysis of the weighted least squares VNA calibration. *ARFTG Microwave Measurements Conference, Fall 2004. 64th,* December 2004, 23-31 **[0124]**
- Virginia Diodes Inc. waveguide band designations. Tech. Rep. Virginia Diodes Inc, 2009 **[0124]**
- **T. RECK ; L. CHEN ; C. ZHANG ; C. GROPPI ; H. XU ; A. ARSENOVIC ; S. BARKER ; A. LICHTENBERGER ; R. WEIKLE.** Calibration accuracy of a 625 GHZ on-wafer probe. *76th ARFTG Microwave Measurement Conference Digest,* December 2010 **[0124]**
- **P. SIEGEL.** Terahertz technology. *Microwave Theory and Techniques, IEEE Transactions on,* March 2002, vol. 50, 910-928 **[0124]**
- **R. LAI ; X. MEI ; W. DEAL ; W. YOSHIDA ; Y. KIM ; P. LIU ; J. LEE ; J. UYEDA ; V. RADISIC ; M. LANGE et al.** Sub 50 nm InP HEMT Device with fmax Greater than 1 THz. *IEEE International Electron Devices Meeting, 2007. IEDM 2007,* 2007, 606-611 **[0124]**
- **L. SAMOSKA ; W. DEAL ; G. CHATTOPADHYAY ; D. PUKALA ; A. FUNG ; T. GAIER ; M. SORIA ; V. RADISIC ; X. MEI ; R. LAI.** A Submillimeter-Wave HEMT Amplifier Module With Integrated Waveguide Transitions Operating Above 300 GHz. *Microwave Theory and Techniques, IEEE Transactions on,* June 2008, vol. 56, 1380-1388 **[0124]**
- On-wafer vector network analyzer measurements in the 220-325 GHz frequency band. **A. FUNG ; D. DAWSON ; L. SAMOSKA ; K. LEE ; C. OLESON ; G. BOLL.** Microwave Symposium Digest, 2006. IEEE MTT-S International. IEEE, 2007, 1931-1934 **[0124]**
- **T. J. RECK ; L. CHEN ; C. ZHANG ; C. GROPPI ; H. XU ; A. ARSENOVIC ; N. S. BARKER ; A. LICHTENBERGER ; R. M. WEIKLE.** Micromachined on wafer probes. *Microwave Symposium Digest, 2010., IEEE MTT-S International,* June 2010 **[0124]**