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(54) **Method and apparatus for management of power supplied from a phase-cut ac supply**

(57) Disclosed is a method of managing the supply of power to a load from a phase-cut AC supply over a plurality of AC supply half-cycle periods, the method comprising: drawing energy from the phase-cut AC supply during at least one part of a first interval, the first interval being at least part of at least one AC supply half-cycle;

storing some of the energy; and supplying the some of the energy to the load during a second interval being at least one subsequent AC supply half-cycle; wherein the first and second interval total to the plurality of AC supply half-cycle periods. A corresponding controller, a load control circuit such as a lighting control circuit, and a lighting circuit, are also disclosed.

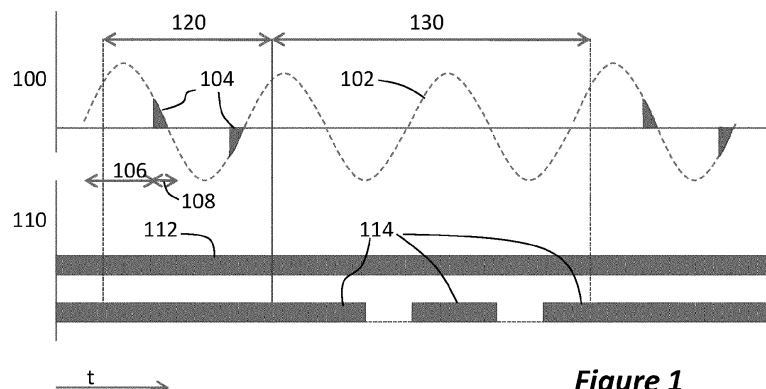


Figure 1

Description

Field of the Invention

[0001] This invention relates to method of controlling loads under mains-dimmers, and to power convertors configured to operate according to such methods.

Background of the Invention

[0002] Mains-dimmers are widely used for lighting applications. The most common type of mains dimmer is the phase-cut dimmer, which relies on the generally sinusoidal cyclic characteristic of the mains voltage signal, and disables the supply during a part of the mains phase.

[0003] Apart from minor problems of flickering at very high dimming levels (that is to say, low output levels, at which the power is significantly reduced) phase-cut dimmers operate effectively for incandescent lighting. However other forms of lighting, such as CFL (compact fluorescent lighting) or LED (light emitting diode) lighting generally require relatively complex control and driver circuitry since they generally are high impedance loads, in contrast to the low impedance characteristic of incandescent lighting. They are thus typically not compatible with phase-cut dimmers.

[0004] Phase-cut dimmers are either "leading-edge" or "trailing edge", depending on which part of the mains half-cycle is cut. Leading-edge dimmers are typically implemented using a triac as the switching device, and trailing edge dimmers using a transistor such as a MOS transistor. In the case of a leading edge dimmer, a firing network inside the dimmer senses the mains voltage and fires at the appropriate phase angle of the mains voltage. At the firing moment, the switching device is triggered. Provided that sufficient current remains flowing in the triac (in the case of a leading edge dimmer) after it is fired and it starts conducting, it stays in a conducting mode until the next zero-crossing of the mains current. Such leading-edge dimmers therefore need a minimum current to be drawn in order to prevent them turning off too early. This current may be referred to as the holding current

[0005] Since high efficiency forms of lighting, such as CFL and LED require less power than equivalent incandescent lighting, at deep dimming levels, the current drawn by the lighting application may become so low that it is not able to keep the dimmer conducting once the triac has fired. In known CFL and SSL systems, the load is configured to draw an additional current, which may be 10 - 50 mA for a typical domestic wall-mounted dimmer, by means of a bleed resistor in order to keep the dimmer conducting. This current is not useful for providing luminosity and thus significantly decreases the system's efficiency especially at low lighting levels.

[0006] A further problem arises for CFL and LED lighting applications, in that the firing network requires a voltage across the dimmer in order to generate the proper firing pulse. If the load is too small or completely absent,

the voltage across the dimmer becomes insufficient to trigger the firing correctly, which results in either firing at an increased angle or not firing at all. A minimum current is therefore required to be drawn by the load in order to supply the firing network - this current, of the order of a few milliamps, is normally provided by a second bleeder resistor, which acts to further reduce the operational efficiency.

[0007] The effects of the bleeder resistors are accentuated at very deep dimming levels where only very low currents are drawn; they are even more significant for smart lighting applications when in standby mode, at which times it is important to keep the power drawn to a minimum in order to preserve the time for which the device can remain in standby.

Summary of the invention

[0008] According to a first aspect of the invention there is provided a method of managing the supply of power to a load from a phase-cut AC supply over a plurality of AC supply half-cycle periods, the method comprising: drawing energy from the phase-cut AC supply during at least one part of a first interval, the first interval being at least part of at least one AC supply half-cycle; storing some of the energy, and supplying the some of the energy to the load during a second interval being at least one subsequent AC supply half-cycle; wherein the first and second intervals total to the plurality of AC supply half-cycle periods. The power drawn from the AC supply, during the at least one part of a first interval may thus be higher than it would be absent the second interval during which power is not drawn. The load may be disconnected from the supply during the second interval. Without restricting the inventing thereto, it is noted that in applications with high impedance loads, such as CFL or LED lighting application, it may be possible to reduce or even eliminate the losses associated with bleeders thereby. The term 'plurality' includes a whole number, that is to say 'a plurality' includes 'an integral plurality'; however, it also includes a non-integral number, that is to say, plurality includes for instance two-and-a-half. In the case that the first and second intervals total to the plurality of AC supply half-cycle periods, which plurality is non-integral (for instance, two-and-a-third half-cycles) there may be a delay between the end of the second interval and start of the next subsequent first interval, such that that first interval starts at a zero-crossing of the AC supply. In embodiments, the method further comprises setting a duration of at least one of the first interval and the second interval such that the power drawn during the at least part of the first interval is sufficient to enable triggering of the AC phase-cutting device. The AC phase-cutting device is the device which cuts the phase of the AC supply, and may, for instance, be a triac or a transistor, and may cut the leading edge or the trailing edge of the AC-phase. In the case of a leading-edge phase-cut AC supply, the supply is switched on or triggered at the leading

edge; in the case of a trailing edge phase-cut supply, the supply is triggered or switched on at the start of the phase. It may be possible to reduce or even eliminate the need for a bleeder, which might otherwise be required to ensure correct triggering and/or operation of the phase-cutting switch.

[0009] In embodiments the first interval is an AC supply half-cycle and the at least part of a first interval comprises a single window.

[0010] In other embodiments the first interval is a plurality of AC supply half-cycles, and the at least part of a first interval comprises a single window in each of the plurality of AC supply half-cycles. In embodiments, the method may further comprise detecting a phase of the AC supply, and synchronising the or each window to the phase of the AC supply.

[0011] In embodiments, detecting a phase of the AC supply comprises detecting a zero-crossing of the mains, and the method further comprises predicting a further zero-crossing based on the detected zero-crossing.

[0012] In embodiments, the first and second intervals total to an odd-number of AC supply half-cycles. Generation of harmonics of the mains frequency are generally undesirable, and in some environments may be limited by regulations. In particular, even harmonics (with a frequency twice, four times, six times, etc. the fundamental) are often undesirable. By requiring the total of the first and second interval to be an odd number of half-cycles, that is to say, by requiring the sub-cycling to be over an odd number of half-cycles, even-order harmonics may be reduced or even eliminated. It will be appreciated that elimination of harmonics may not be necessary, or may be necessary only to a lesser extent, particularly in cases such as standby modes for smart lighting,

[0013] In embodiments, the at least one part of a first interval is one part of a first interval and is shorter than a conduction angle of the phase-cut AC supply. Such embodiments may reduce or avoid the requirement for or the size of, a bleeder circuit, even when the energy which is required to be drawn from the AC supply is very low.

[0014] According to another aspect there is provided a controller for supplying power to a load from a phase-cut AC supply over an integral plurality of AC supply half-cycle periods, the controller being connectable to an energy store, the controller being configured to: draw energy from the phase-cut AC supply during at least one part of a first interval, the first interval being at least part of at least one AC supply half-cycle, store some of the energy in the energy store and supply the some of the energy to the load during a second interval being at least one subsequent AC supply half-cycle, wherein the first and second interval total to the integral plurality of AC supply half-cycle periods.

[0015] In embodiments the energy store is a capacitor.

[0016] In embodiments, the controller further comprises a zero-crossing detection unit. It may further comprise a zero-crossing prediction unit.

[0017] According another aspect, there is provided a lighting control circuit comprising a switched mode power converter and a controller as just described, and according to yet another aspect there is provided a lighting system comprising a lighting unit, the lighting system further comprising a lighting control circuit or a controller as just described.

[0018] These and other aspects of the invention will be apparent from, and elucidated with reference to, the embodiments described hereinafter.

Brief description of Drawings

[0019] Embodiments of the invention will be described, by way of example only, with reference to the drawings, in which

Figure 1 illustrates methods according embodiments of the invention;

Figure 2 shows the dimmer current according to embodiments of the invention;

Figure 3 is a block diagram of a power management system which illustrates embodiments of the invention

Figure 4 is a block diagram of a control block for use in embodiments of the invention;

Figure 5 illustrates waveforms and a timing diagram associated with a controller operable in according with a leading edge phase-cut AC supply;

Figure 6 illustrates waveforms and a timing diagram associated with a controller operable in according with a trailing edge phase-cut AC supply;

Figure 7 is a schematic circuit diagram of a conventional circuit for a leading edge dimmer;

Figure 8 is a schematic circuit diagram of a circuit for a leading edge dimmer in which the load can be disconnected from the dimmer;

Figure 9 shows simulated waveforms of a dimmer circuit according to embodiments in which the first interval is synchronised with a mains zero-crossing; Figure 10 shows simulated waveforms of a dimmer circuit according to embodiments in which the first interval is not synchronised with a mains zero-crossing;

Figure 11 shows simulated waveforms of a dimmer circuit according to embodiments in which the first interval is well synchronised with a mains zero-crossing, but in which a proper firing mode is restored, and Figure 12 shows a block diagram of a controller configured to restore a proper firing mode.

[0020] It should be noted that the Figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar feature in modified and different embodiments

Detailed description of embodiments

[0021] Embodiments of the invention are illustrated in figure 1: figure 1 shows, plotted against time t , at 100, energy drawn from a generally sinusoidal mains power supply, which is input into a phase-cut dimmer. In figure 1 the phase-cut dimmer is a leading-edge dimmer. The dimmer is set to be heavily dimmed, that is to say, the dimmer switches on only towards the end of each mains half-cycle. For the first part 106 of the mains half-cycle, the dimmer is switched off, and does not supply any energy and so no energy is transferred; during the last part 108 of the mains half-cycle, the dimmer is switched on and can transfer energy to a load.

[0022] This figure also shows, at 110, the energy which is delivered to a load. As can be seen from plot 112, energy is continuously supplied to the load, in this example; however, in other embodiments, such as that shown schematically at 114, energy need not be supplied continuously: it may only be required intermittently.

[0023] If the power required by the load is very low, then the energy required by the load over the mains half-cycle is also very low: thus, unless the conversion means itself consumes significant energy, the energy required to be supplied from the mains during the dimmer-on part 108 is also low, and thus the power during the dimmer-on part 108 may also be low.

[0024] As has already been discussed, if the power demanded from the dimmer is too low, this may result in incorrect operation of the dimmer and in particular the dimmer may fail to trigger. This problem is overcome, according to embodiments of the invention, as shown in figure 1 by requiring the energy supplied during the dimmer-on the part of the half-cycle, to be sufficient to power the load for one or more *additional* half-cycles, during which additional half-cycles, the dimmer does not provide energy for the load: in the illustration shown in figure 1, the dimmer is turned on during the dimmer-on parts 104 of two consecutive half-cycles shown in the first interval 120, and then is NOT turned on during the subsequent four half-cycles shown at 130. In this case, the quantum of energy drawn from the mains during each dimmer-on part 104 must be sufficient to supply energy to the load for three half-cycles (since 2 dimmer-on parts together supply the energy for both those two half-cycles and the following four half-cycles). The power drawn from the mains during each dimmer-on part 104 is thus three times as large as it would have been if the dimmer were made to trigger for every half-cycle. The relative lengths of the first interval 120 and the second interval 130 may be chosen so as to provide that the dimmer has to draw sufficient power during each dimmer-on part such that correct triggering operation occurs. This will in general depend on the particular application, and may or may not be known before the system is installed. It will, generally, depend on the characteristics of the specific type of dimmer used, and the level of dimming applied.

[0025] A simulated plot of dimmer output current over

several half-cycles, for another embodiment, is shown in figure 2. Figure 2 shows, at 210, a first set of three half-cycles 220 comprising a first interval, during which the dimmer operates in a conventional manner, followed by a set of four half-cycles at 230 comprising a second interval during which the dimmer remains off. At the end of the set of four half-cycles, a further set of three half-cycles, during which the dimmer operates, commences. The group 240 of 7 half-cycles forms a "sub-cycle", which term will be considered in more detail below.

[0026] As shown in figure 2, the conduction angle 250 of the dimmer may generally be less than the complete half-cycle 220. Thus the dimmer only conducts for a part of each of the first three half-cycles. In other words, power is only drawn from the mains over three parts of a first interval, which first interval comprises the first three mains half-cycles. It will be noted that in figure 2 the dimmer is dimmed less than in figure 1; in both cases a leading-edge dimmer is shown, although the invention is not limited thereto. Similarly to the embodiment shown in figure 1, although not shown in figure 2, the power is supplied to the load during at least one part of the second interval, which second interval is the set of four half-cycles 230.

[0027] Figure 3 shows a block diagram of a system configured to manage supply to a load, according to embodiments of the invention. The figure shows a dimmer 302 which is connected to a dimmer load 304. The dimmer load comprises a load 306 which consumes a certain power, for example a CFL (compact fluorescent lamp) driver stage. The dimmer load 304 further comprises a switchable converter 308. The switchable converter 308 draws energy from the dimmer and, neglecting for the moment the energy consumed by the switchable converter itself and other energy losses, delivers this energy to the load. The dimmer load 304 further comprises a control block 310 which controls the operation of the switchable converter 308. In particular the control block 310 only allows the switchable converter 308 to draw power from the dimmer part of the time, for instance during a specified time window of a sub-cycle (the term sub-cycle will be defined in more detail hereinbelow). Neglecting losses, the energy drawn by the switchable converter during the specified time window is equal to the energy required by the load during the complete sub-cycle. Since the window is shorter than the sub-cycle, the power drawn by the converter during this window is greater than the power of the load, which power is supplied over the whole sub-cycle.

[0028] The term "sub-cycle" is used herein to describe an integral number of mains half-cycles. Thus, for the sake of argument, the specified time window, corresponding to the first interval may be 2 mains half-cycles, and the sub-cycle may be 6 mains half-cycles if the first interval is followed by 4 half-cycles during which the dimmer does not conduct at all. Then, in the case that the dimmer is fully on (that is to say there is no phase-cutting at all and the mains supply is passed directly to the dim-

mer load), the switchable converter would draw energy from the mains for two half-cycles, but supply this energy over all 6 half-cycles: during the two half-cycles the switch mode converter draws three times the power from the dimmer than it would were it to be continuously drawing energy from the dimmer. The skilled person will appreciate, of course, that the invention will generally be used where the dimmer is not fully on, but is in a heavily dimmed state: the power drawn by the switchable converter during the dimmer-on interval will then be significantly higher than it would be were the dimmer always on; however, the increase in drawn power (by a factor of the sub-cycle time divided by the window time, neglecting losses) still holds, for this "window-controlled sub-cycle" operation. Although "sub-cycle" describes an integral number of mains half-cycles, the first and second intervals discussed hereunder need not total to an integral number of mains half-cycles, but may total to a non-integral number of mains half-cycles. In that case, there may be a delay between the end of a second interval and the start of a next subsequent first interval. Such a delay may be useful in order that the next subsequent first interval commences at a zero-crossing of the mains supply.

[0029] A non-limiting example of a switchable converter which may be used according to embodiments of the invention is a PFC (power factor converter). For applications which include a PFC stage, it is possible to switch the PFC on, that is to say switch it to an active switching state, during the specified time window, and switch it off, that is to say to an inactive state, outside of the window.

[0030] The skilled person would appreciate that, since the PFC stage is supplying energy only during part of the sub-cycle, whilst the load, such as a CFL lamp or a LED lamp, requires power to be supplied over the complete sub-cycle there needs to be some energy buffer such as an intermediate bus capacitor, inside the application. As shown in figure 3, the energy buffer may be inside the load 306 or the switchable converter 308 or may be a separate block within the connection between the load and the switchable converter and shown as arrow 312.

[0031] The inventors have also appreciated that the switchable converter 308 does not necessarily have to convert power during the complete conduction angle as set by the dimmer. For instance it may be provided that the switchable converter converts power only during part of a conduction angle, and then does not conduct for the whole of one or more subsequent conduction angles. This will be considered in more detail in relation to the non-limiting example of smart lighting on stand-by, below.

[0032] The dimmer itself may now be considered to be operating as a "slave" rather than as a "master": the possibility for more flexibility in the management of the control of the power arises. The function of the switchable converter is then twofold: firstly to deliver the proper average power (over time) in order to supply the requirements of the load; and secondly, to draw power from the dimmer, across the window, in such a way that the dimmer can

properly operate. In this context, proper operation means that the switching element in the dimmer, such as a triac, is loaded by a sufficiently high current to maintain it in and on-state once it has been fired. Moreover, it is not necessary that power is supplied continuously to the load; in some embodiments the load may only require intermittent power. Thus delivering the proper average power over time in order to supply the requirements of the load, may include supplying power at a variable level or even intermittently.

[0033] Figure 4 shows an example of a control block 310. Control block 310 includes a zero-crossing generation block 410, which enables the control to determine the start (or end) of the mains half-cycle, so as to ensure that the control remains in synchronisation with the mains. The zero-crossing generation block 410 includes dv/dt detection 412, zero-crossing detection 414 and a prediction block 416.

[0034] The zero-crossing generation block 410 takes as input the difference ($d1-d2$) between line voltage $d1$ and the dimmer output $d2$. Assuming that the capacitor across the dimmer output dominates, almost the complete amplitude of the mains is present at the inlets ($d1, d2$) when the dimmer is off. The signal $dVin/dt$ gives the steepness of the mains line voltage $d1$, and can be used to determine triggering event.

[0035] In the case that the dimmer does not fire (as will be discussed in more detail below) this will be detected. This is shown as "no firing" in figure 4. When the dimmer does not fire - that is to say, during the second interval, during which power is not drawn from the mains, but is still supplied to the load - the zero-crossing cannot (in general) be detected, so a zero-crossing prediction may have to be made, as shown by block 416.

[0036] Waveforms relevant to this control are shown at figure 5 for a leading edge dimmer, and at figure 6 for a trailing edge dimmer respectively. The figures show $d1-d2 = Vin$ (at 510 and 610 respectively), $dVin/dt$ at 520 and 620 respectively, detected zero-crossings at 530 and 630 respectively, and finally predicted zero-crossings (at 540 and 640). As is shown in the figures, the zero-crossings can be directly detected only around the first interval (that is to say, when the dimmer is conducting during at least a part of the half-cycle), or end of each active cycle, provided that the (bleeder) current is sufficient to prevent the triac from extinguishing before the mains voltage zero crossing.

[0037] During the second interval (that is to say, the half-cycles where the dimmer does not conduct at all), the zero-crossings cannot be directly detected, but are predicted by means of the prediction block 416. Thus the output of the prediction block is a continuous stream of zero-crossings, which continues even when no mains can be detected. The absence of a steep dV/dt pulse can be used as indication that the dimmer triac was not fired.

[0038] It will be immediately apparent to the skilled person, that there are several ways to implement the prediction mechanism. For example, and without limitation,

the prediction block may extrapolate zero-crossings based on one or more sensed zero-crossings and time information. If an accurate timing is present, such as a quartz crystal that is often a basic part of a microcontroller system, there are only two zero-crossings needed to predict the next ones. In cases in which the mains frequency is also known, a single zero-crossing may be sufficient to predict the later zero-crossings.

[0039] In some embodiments, ensuring synchronisation of the controller with the phase of the mains voltage may be necessary, in order to prevent a disturbance of the firing network of the dimmer.

[0040] Triac dimmers typically use a firing network, often including a diac and an RC network. A basic diagram of such a triac dimmer including a conventional firing network is shown in Figure 7. The circuit shows triac T1, connected in series with an EMI-suppressing coil L1, between input voltage V1 and ground in parallel with a smoothing capacitor C2. The gate of the triac is supplied through diac X1. A resistor R2 is generally provided, connected between gate of T1 and ground, in order to prevent unwanted switch-on of the triac T1. The input to diac X1 is connected between V1 and ground, through the RC network R1 and C1. R1 is either the dimmer potentiometer itself, or is adjustable by means of the dimmer switch. As long as the triac conducts, the firing network R1, C1 is supplied only to a minimal extent, due to the small voltage drop across the triac, which is effectively being zero. When the triac turns off, which normally occurs around the zero-crossing of the mains voltage, the triggering network starts charging C1, starting at a voltage approximately zero or relative close to zero. This means that the firing angle of the next cycle is almost completely determined by the mains voltage shape after the zero-crossing. It should be noted that, in practice, the firing angle is dependent on history to some extent, since some energy may remain in the capacitor C1 after firing the triac, depending on the properties of the trigger device X1.

[0041] Figure 8 shows schematic of a circuit that consumes zero, or almost zero, power, when the dimmer is not conducting. In this circuit, a triac dimmer is connected to an AC mains (V2) and loaded with a resistor R3 that can be switched off by, for instance, a voltage programmable resistor (X3). In other embodiments, a switch may be used, or a PFC (power factor control) stage may be switched on, in order to provide the loading. The resistor X3 is equal to the voltage between Rp and Rm. The load may thus be switched to a mode where it consumes almost no power from the mains during the off window. In this mode, the zero-crossings of the mains cannot always be detected because the voltage 510,610 depends on the actual capacitance present at both dimmer output (that is, the voltage across C2) and input of the load (represented by R3, X3 in fig 8). In the circuit of Figure 8, which results in the signals shown in figure 5, the ideal situation is drawn: no capacitance at all is present at input of the load, while the load is switched to the high ohmic

mode at the zero-crossing of the mains. C2 is then held at its last value of 0V (immediately after the dimmer turns off). This means that the full mains voltage remains present at the input of the load. However, in the case that a capacitor (with an undefined impedance) is present at the input of the load, or in the case that the load is switched to the high-ohmic mode at a moment other than at the zero-crossing of the mains, the phase relation between mains voltage and voltage at the input of the load, becomes uncertain, while the residual voltage at C2 disturbs the DC component at input of the load.

[0042] When the triac is conducting, the voltage across C1 (and thus across diac X1) remains at a low value until the zero-crossing of the mains, because the voltage across the conducting triac is low, keeping the firing network discharged. The connection between the dimmer and the load is interrupted at the zero-crossing of the mains. By switching the power off at the zero-crossing, the input of the firing network becomes high ohmic, preventing C1 from being charged provided that C2 is large compared to the input capacitance of the application (parallel to R3, not shown). When the connection between the dimmer and the load is re-established close to a zero-crossing, C1 is charged similar to the situation in which there was no power switch off; in other words, the firing angle during the interval where power is taken is not significantly changed compared with the situation where this power is continuously taken.

[0043] As already indicated it may be desirable to detect the mains zero-crossing, or to predict this when it cannot be directly detected. This will be illustrated having regard to figures 9 and 10, which show the effects of good, and poor, synchronisation respectively. Figures 9 and 10 show, against time on the x-axis or abscissa, plots of the current through R3 at 910 and 1010; the voltage across the input terminals of the programmable switch X3 at 920 and 1020; the input mains voltage at 930 and 1030; and the voltage Vdiac across the diac at 940 and 1040, in Figures 9 and 10, respectively for a controller in which the power-supplying first interval is, and is not, properly synchronized with the mains zero-crossing. In the example shown in figure 9, the start of the first interval is synchronized close to the zero-crossing of the mains (shown at about 12ms and 10ms respectively), whilst in figure 10 the first interval is started at 6ms, which is significantly different from the 10ms position of the zero-crossing. This latter situation results in charging of the firing network starting before the zero-crossing and therefore Vdiac starts with a pre-biasing voltage of the wrong sign, making it impossible to reach the trigger level of the diac before the next zero-crossing and therefore no firing at all and disturbance of the dimming process.

[0044] It would be necessary to increase the power level of the dimmer via adjusting the potentiometer R1 manually, to overcome this situation, unless preventative measures are taken. An example of such a preventative measure is illustrated in figure 11, which shows plots against time of the same currents and voltages, as well

as a plot of the voltage at the dimmer terminal, that is, the voltage V_{T2} at terminal T2 of X3 in figure 8, at 1350. As in figure 10, between $t=6\text{ms}$ and $t=20\text{ms}$, the firing network operates in the wrong mode. At $t=20\text{ms}$, being a zero-crossing of the mains voltage, the load is disconnected. The result is that the voltage at the dimmer terminal V_{T2} remains 0 and in this way C1 is prevented from being charged to the opposite polarity. If the load is now connected at the next zero-crossing, the polarity of the voltage at C1 has the proper sign to be charged to the firing level. In this way the system can be forced to the proper mode of operation of the firing network again. Therefore the sequence of (a) disconnecting the load close to a zero-crossing of the mains voltage when no firing angle is detected followed by; (b) connecting the load to the mains at the next zero-crossing of the mains (or the Nth zero-crossing as an alternative, N being an odd number) may ensure proper operation of the device.

[0045] As the mains voltage cannot be sensed while the triac is off and a load is connected to the dimmer, it may be possible to use this method only if the zero-crossings can be determined in another way. If the load is disconnected it is again possible to sense the shape of the mains voltage and to lock the zero-crossing generation block such that it predicts the zero-crossings, as discussed above. Generally, then, the zero-crossing generation including predicting future zero-crossings is carried out before the load is disconnected.

[0046] Figure 12 shows a block diagram of a control block according to an embodiment implementing the above features: in this embodiment, the control block 310 include zero-crossing generation block 410, together with logic 1210. A signal 'enable window' defines the desired length of the window, during which the dimmer is able to supply power, that is to say, it defines the first interval. Without limitation, the first interval may be a single half-cycle, or may be multiple half-cycles. In other embodiments, the first interval may be shorter than a single half-cycle. In particular in such other embodiments, the first interval may be shorter than the conduction angle of the dimmer, such that, in order to transfer the same energy as would be the case were the dimmer to be conducting over the whole of its conduction window, it has to operated at a higher power for the shorter first interval.

[0047] The logic block 1210 synchronizes the enable window with the zero-crossings of the mains voltage in order to maintain proper operation of the firing network of the dimmer. In some embodiments this block may also, when no firing is detected, disconnect the load close to a zero-crossing of the mains voltage and reconnect the load to the dimmer at the next, or a subsequent zero-crossing of the mains. The triac should then fire according to the correct operation. In some embodiments, in case that no zero-crossing signal is available, logic 1210 can be set to disconnect the load from the dimmer for a few mains cycles in order to sense the zero-crossings and lock the zero-crossing generation block, as discussed

above.

[0048] Some embodiments of the invention may be used for instance to supply stand-by power to a controller such as a smart lighting controller. In such an application, the controller may only require a minimal level of power, sufficient only to ensure that the controller "wakes up" when required. Such power may generally be supplied by a battery or capacitor. However, when the charge in the battery or capacitor falls below a certain level, it will require recharging. The recharging may be through the lighting dimmer and may require only a small amount of energy. If the dimmer were to provide this energy spread across the whole of one conduction angle, it may be that the power level would be too low to trigger the dimming device (either a triac or transistor), particular if the dimmer is set so as not to heavily dim - that is so the conduction angle is a large part - or even all, of the half-cycle. In such a case, according to embodiments of the invention, the first interval may be only a part of the conduction angle of the dimmer. Since the energy is then drawn during only a shorter interval than the conduction angle, the power level is thus higher than would be the case were the energy transfer to occur over the complete conduction angle.

[0049] Other embodiments of the invention may also be used in applications such as smart lighting as just discussed. The difference between the average power required by the application, and the power required in order to correctly operate a dimmer, whether triac-based, or transistor-based, may be even more pronounced: the light may be heavily dimmed - for instance in response to a signal such as from a wireless remote control - even when the dimmer is set for a high light level, and so would be expected to be conducting during almost the complete mains cycle. In this situation the losses associated with bleeder dissipation absent a method such as is disclosed in embodiments above, might be even more than in a standard lighting application.

[0050] Although embodiments described above have been directed mainly to leading edge phase cut mains supplies, the skilled person will appreciate that the invention is not limited thereto; in particular, controllers for trailing edge phase cut AC supplies may fall within the scope of the invention. Generally, the power level during conduction of the dimmer switch - which typically in this case is a MOS transistor, should be maintained at a sufficiently high level that the switch does not turn-off prematurely, before the end of the conduction-angle (or, in the case of a window or first interval which is smaller than the conduction angle, before the end of the window). Further, for trailing edge dimmers, synchronisation with the mains zero crossing may be less critical, provided only that the timing is sufficiently nearly synchronised that the window does not completely miss the conduction angle (which could possibly be the case under very heavily dimmed operation).

[0051] Further, the skilled person will appreciate that although the example embodiments above have been

described in relation at a phase-cut mains supply, the invention may also extend to other AC supplies, such as, without limitation, a marine or aircraft-based AC-supply, or an inverter-based supply.

[0052] From reading the present disclosure, other variations and modifications will be apparent to the skilled person. Such variations and modifications may involve equivalent and other features which are already known in the art of phase-cut dimmers, and which may be used instead of, or in addition to, features already described herein.

[0053] Although embodiments above have been described in relation to phase-cut dimmers such as are commonly used in lighting circuit, the skilled person will appreciate that the invention is not limited thereto, but extend to other leading edge or trailing edge phase-cut AC supplies designed for applications other than lighting, such as power control for an electric fan by phase cut control.

[0054] It will be appreciated that, in order to provide a clear understanding of the invention, in the above discussion a simplifying assumption has been made that the load current through the triac is pure resistive, or at least completely in phase with the mains voltage. The skilled person will be aware that in practice, some phase shift may occur, and can readily derive the circuit behaviour of such non-resistive output loads. For clarity, however, these effects are not discussed herein, since they are not of relevance for the invention.

[0055] Although the appended claims are directed to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

[0056] Features which are described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features which are, for brevity, described in the context of a single embodiment, may also be provided separately or in any suitable sub-combination.

[0057] The applicant hereby gives notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

[0058] For the sake of completeness it is also stated that the term "comprising" does not exclude other elements or steps, the term "a" or "an" does not exclude a plurality, a single processor or other unit may fulfil the functions of several means recited in the claims and reference signs in the claims shall not be construed as limiting the scope of the claims.

Claims

1. A method of managing the supply of power to a load from a phase-cut AC supply over a plurality of AC supply half-cycle periods, the method comprising:
 - drawing energy from the phase-cut AC supply during at least one part of a first interval, the first interval being at least part of at least one AC supply half-cycle,
 - storing some of the energy and
 - supplying the some of the energy to the load during a second interval being at least one subsequent AC supply half-cycle,
 - wherein the first and second intervals total to the plurality of AC supply half-cycle periods.
2. The method of any preceding claim further comprising:
 - setting a duration of at least one of the first interval and the second interval such that the power drawn during the at least part of the first interval is sufficient to enable triggering of the AC phase-cutting device.
3. The method of claim 1 or 2 wherein the first interval is an AC supply half-cycle and the at least part of a first interval comprises a single window.
4. The method of claim 1 or 2 wherein the first interval is a plurality of AC supply half-cycles, and the at least part of a first interval comprises a single window in each of the plurality of AC supply half-cycles.
5. The method of claim 3 or 4 further comprising
 - detecting a phase of the AC supply, and
 - synchronising the or each window to the phase of the AC supply.
6. The method of claim 5 wherein
 - detecting a phase of the AC supply comprises detecting a zero-crossing of the mains,
 - the method further comprising predicting a further zero-crossing based on the detected zero-crossing.
7. The method of any of claims 3 to 6, wherein the first and second interval total to an odd-number of AC supply half-cycles.
8. The method of claim 1 or 2, wherein the at least one part of a first interval is one part of a first interval and is shorter than a conduction angle of the phase-cut AC supply.

9. A controller for supplying power to a load from a phase-cut AC supply over a plurality of AC supply half-cycle periods, the controller being connectable to an energy store, the controller being configured to:
- draw energy from the phase-cut AC supply during at least one part of a first interval, the first interval being at least part of at least one AC supply half-cycle,
 - store some of the energy in the energy store and
 - supply the some of the energy to the load during a second interval being at least one subsequent AC supply half-cycle,
 - wherein the first and second interval total to the plurality of AC supply half-cycle periods.
10. A controller according to claim 9, wherein the energy store is a capacitor.
11. A controller according to claim 9 or 10, further comprising a zero-crossing detection unit.
12. A controller according to any of claims 9 to 11, further comprising a zero-crossing prediction unit.
13. A load control circuit comprising a switched mode power converter and a controller according to any of claims 9-12.
14. A load system comprising a load, the load system further comprising a load control circuit as claimed in claim 13 or a controller as claimed in any of claims 9-12.
15. A lighting system comprising a lighting unit, the lighting system further comprising a load control circuit as claimed in claim 13 or a controller as claimed in any of claims 9-12.

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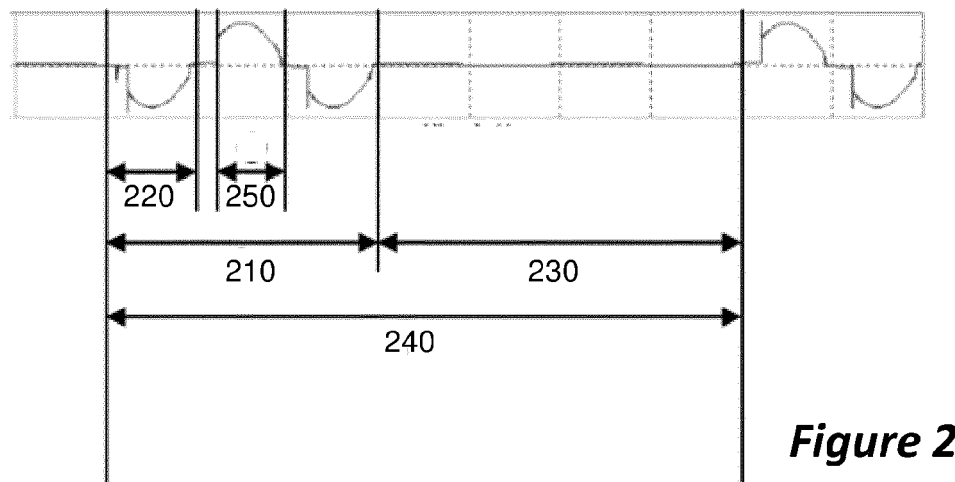
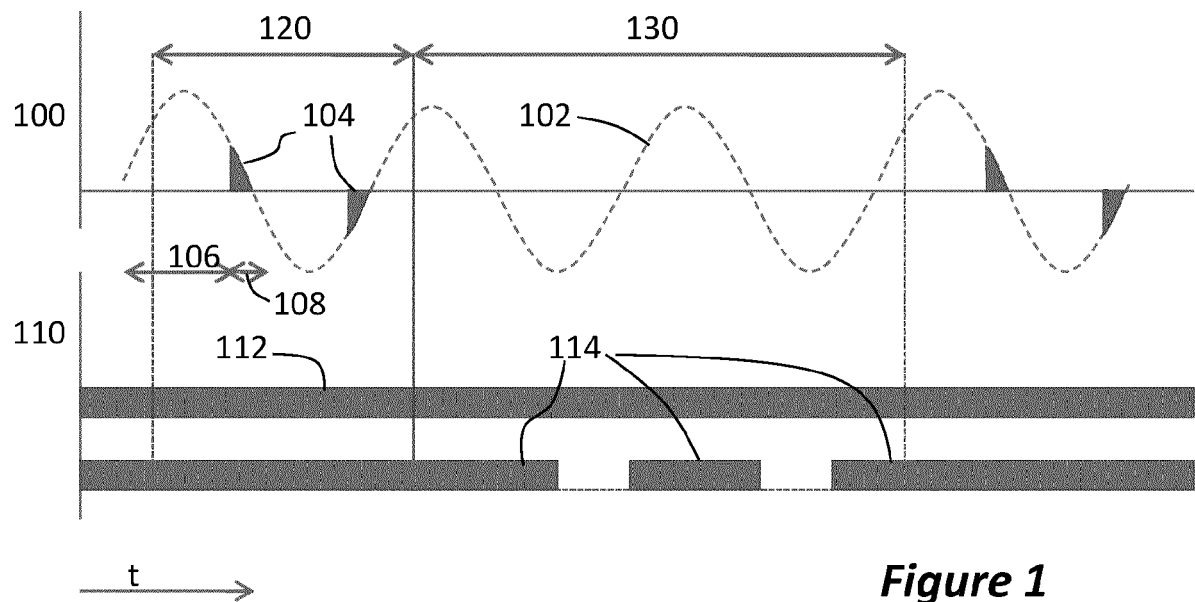
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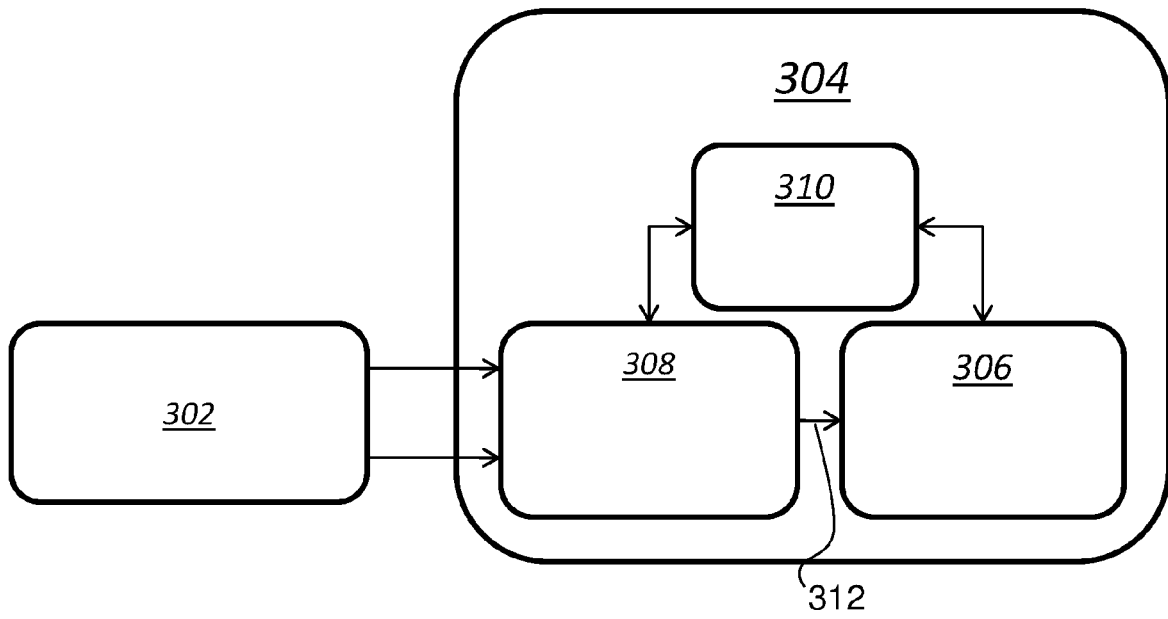


Figure 3

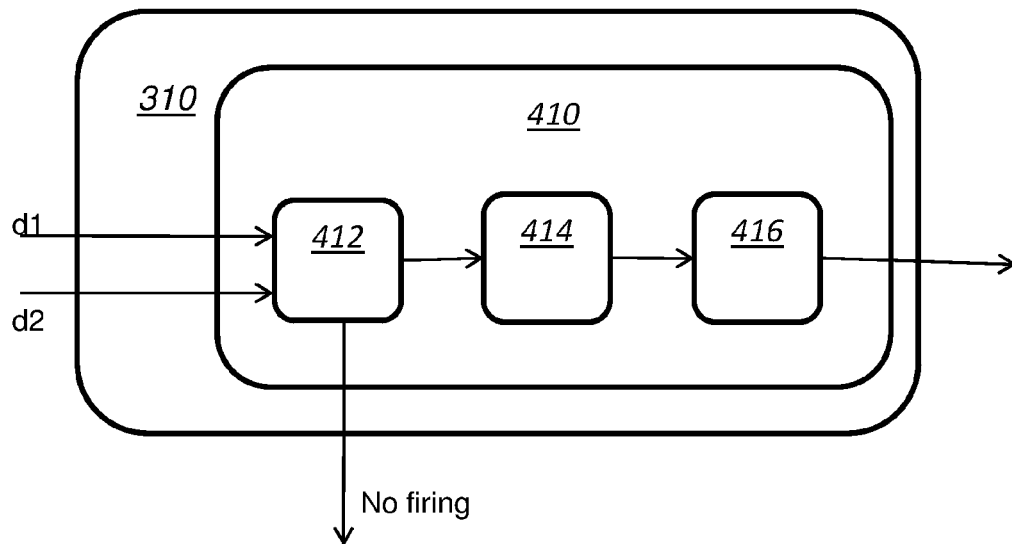


Figure 4

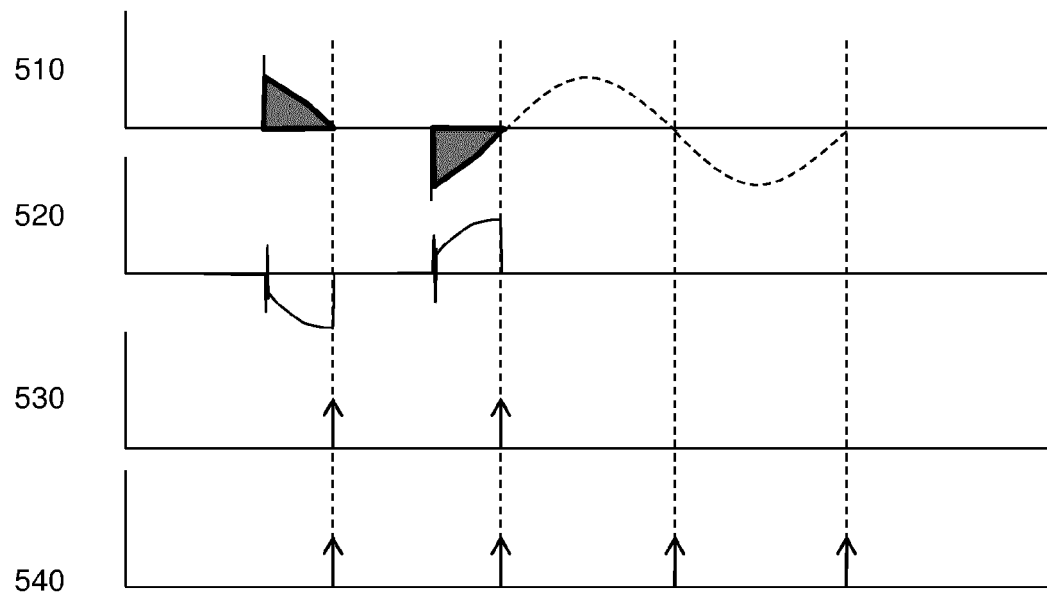


Figure 5

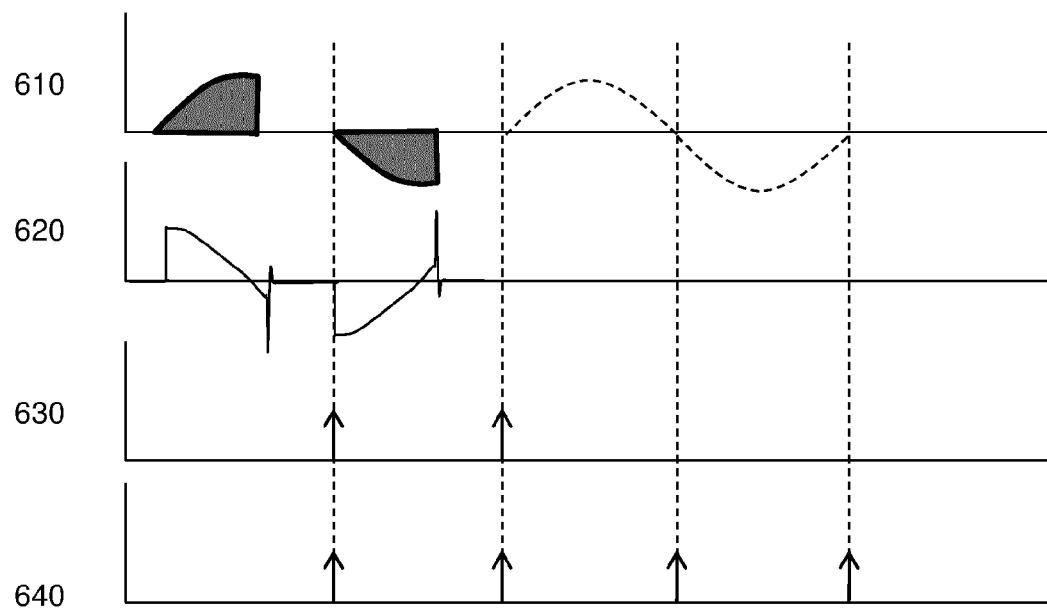


Figure 6

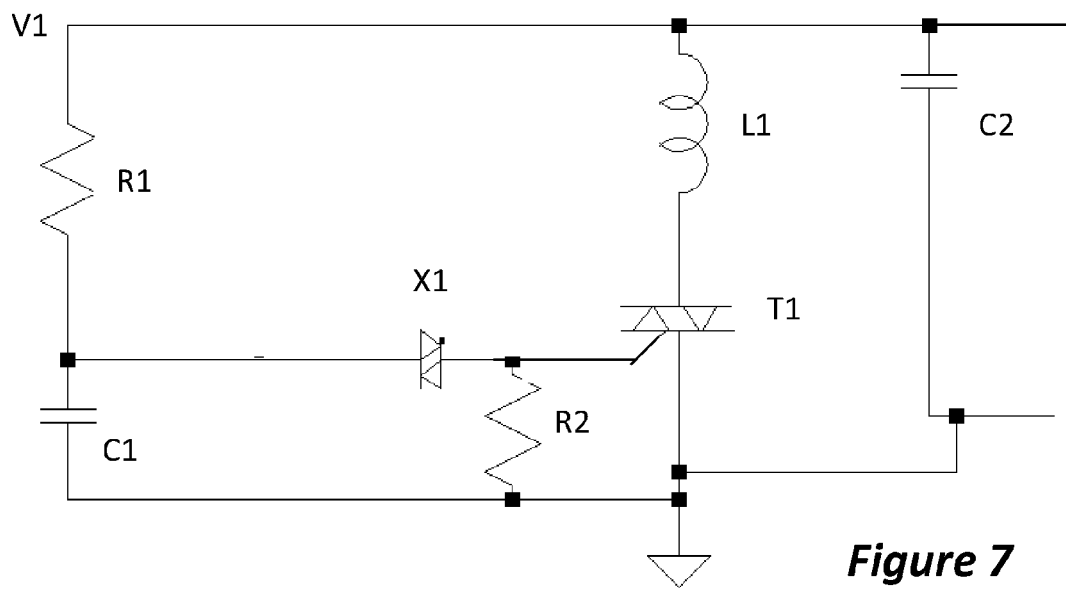


Figure 7

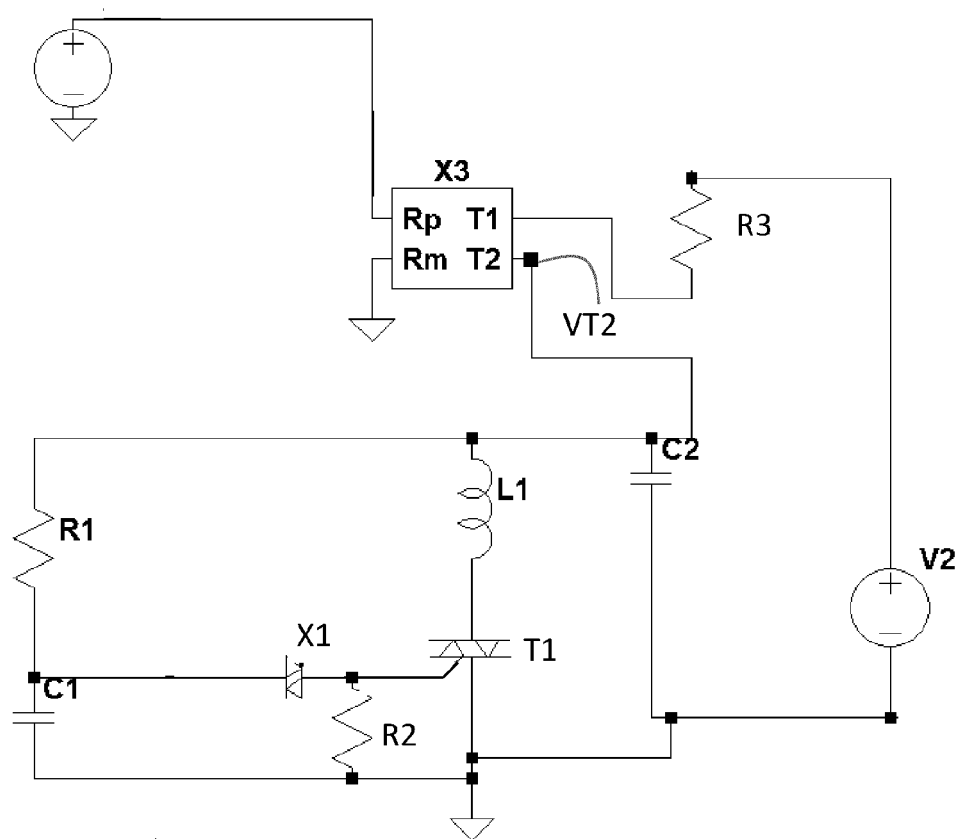


Figure 8

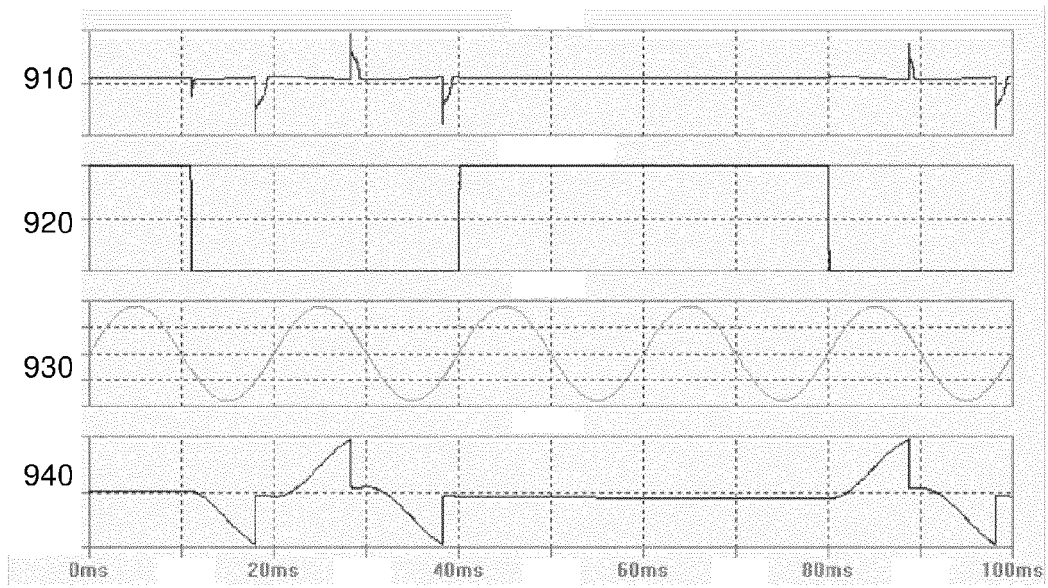


Figure 9

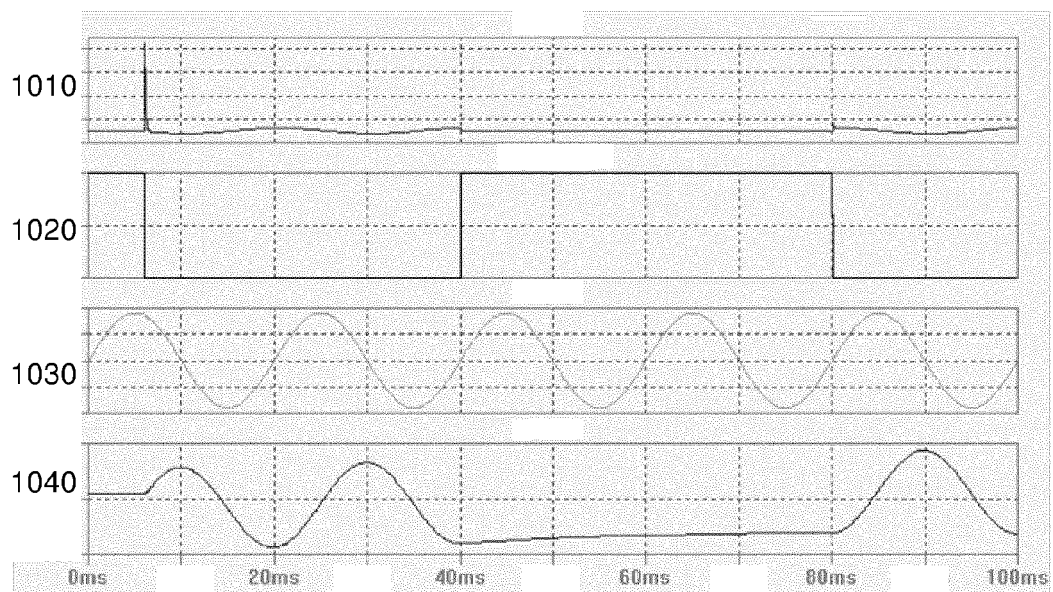


Figure 10

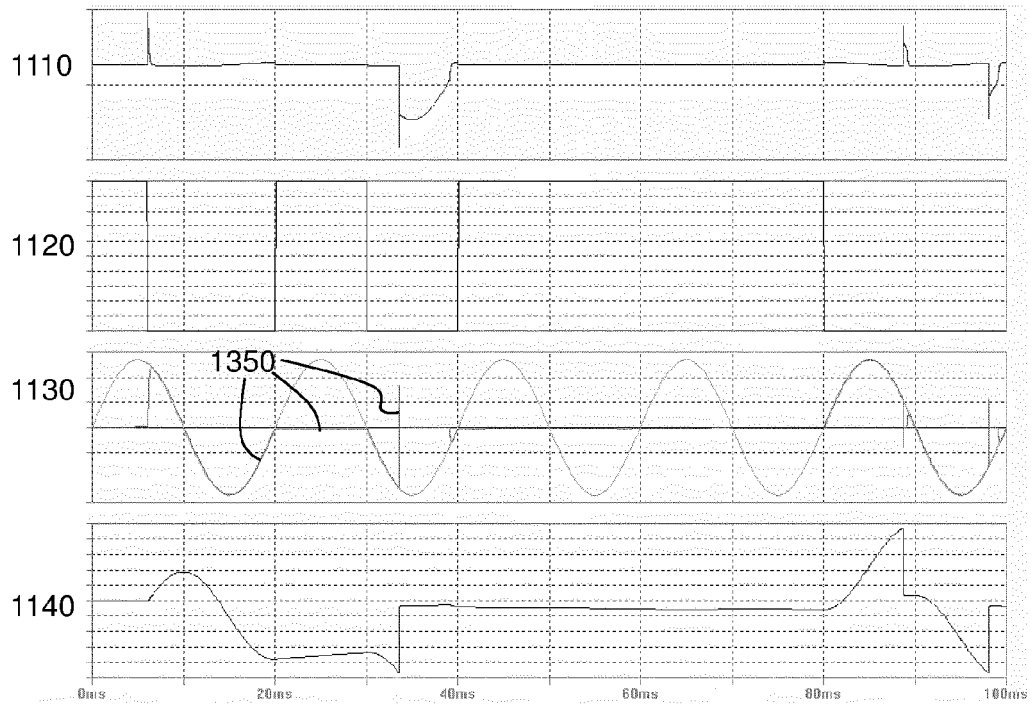


Figure 11

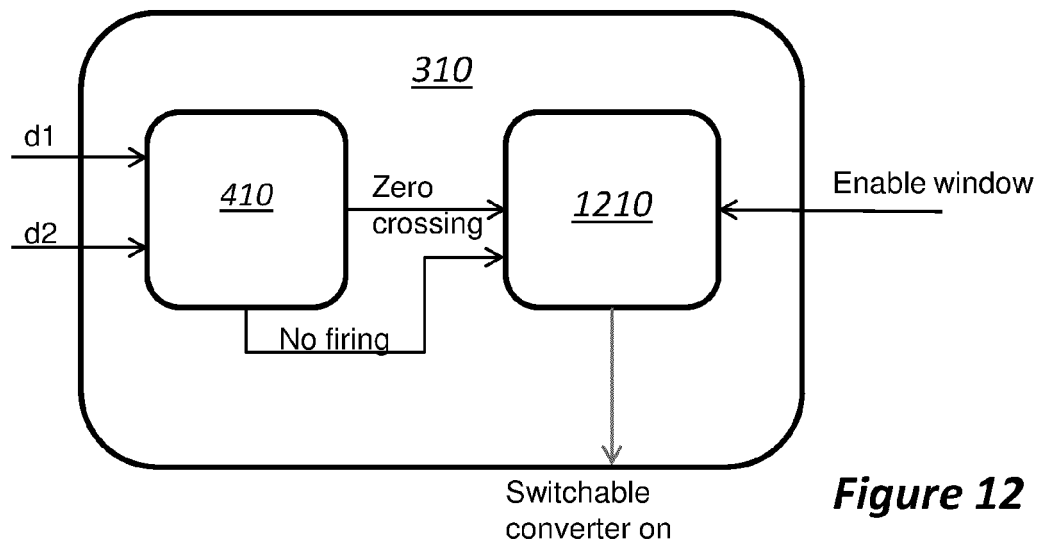


Figure 12



EUROPEAN SEARCH REPORT

Application Number
EP 11 19 4264

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2010/320840 A1 (FRIDBERG MIKHAIL [US]) 23 December 2010 (2010-12-23) * figures 8-13 * * paragraphs [0003] - [0017] * * paragraphs [0038] - [0087] * -----	1-15	INV. H05B33/08
X	WO 2011/056068 A2 (ELDOLAB HOLDING B V [NL]; SAES MARC [NL]; WELTEN PETRUS JOHANNES MARIA) 12 May 2011 (2011-05-12) * the whole document * -----	1-15	
X	WO 2011/045057 A1 (TRIDONIC UK LTD [GB]; WILSON IAN [GB]; FRANKLAND JAMES [GB]) 21 April 2011 (2011-04-21) * the whole document * -----	1-15	
A	WO 2010/027254 A1 (ELDOLAB HOLDING B V [NL]; WELTEN PETRUS JOHANNES MARIA [NL]) 11 March 2010 (2010-03-11) * the whole document * -----	1-15	
A	US 2008/054728 A1 (WATSON TOM [US]) 6 March 2008 (2008-03-06) * the whole document * -----	1-15	TECHNICAL FIELDS SEARCHED (IPC) H05B
A	US 2006/273775 A1 (DOBBINS AARON [US] ET AL) 7 December 2006 (2006-12-07) * the whole document * -----	1-15	
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 10 May 2012	Examiner João Carlos Silva
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 11 19 4264

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The members are as contained in the European Patent Office EDP file on
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10-05-2012

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010320840 A1	23-12-2010	NONE	
WO 2011056068 A2	12-05-2011	NONE	
WO 2011045057 A1	21-04-2011	NONE	
WO 2010027254 A1	11-03-2010	CN 102239742 A	09-11-2011
		EP 2322017 A1	18-05-2011
		TW 201018303 A	01-05-2010
		US 2011248640 A1	13-10-2011
		WO 2010027254 A1	11-03-2010
US 2008054728 A1	06-03-2008	NONE	
US 2006273775 A1	07-12-2006	US 2006273775 A1	07-12-2006
		US 2008246451 A1	09-10-2008

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82