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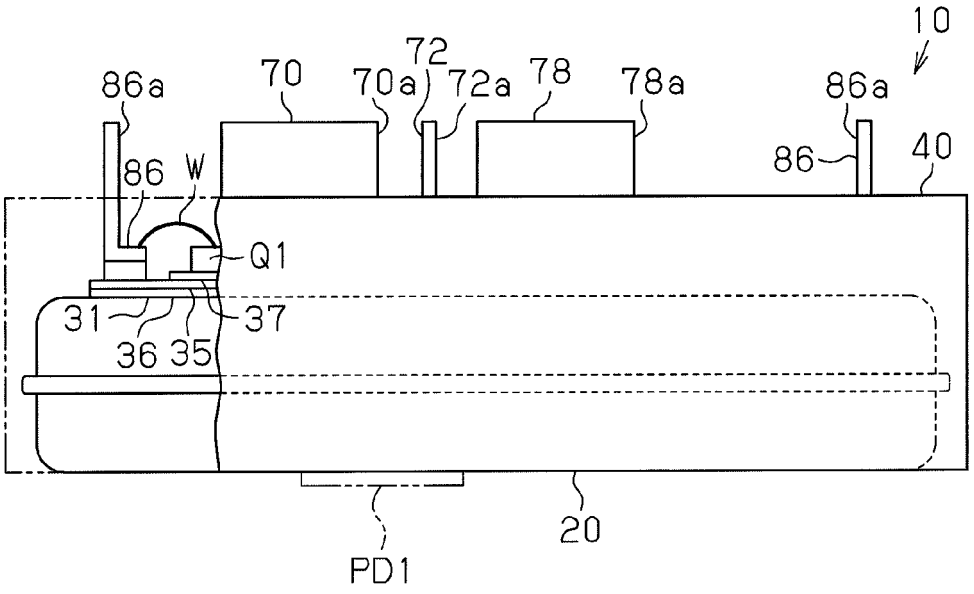
(54) Semiconductor device and method for manufacturing semiconductor device

(57) A semiconductor device includes a cooling device, an insulating substrate, a semiconductor element, an external connection terminal, and a resin portion. The insulating substrate is brazed to an outer surface of the cooling device. The semiconductor element is brazed to the insulating substrate. The external connection terminal includes a first end, which is electrically connected to the semiconductor element, and an opposite second end. The resin portion is molded to the insulating substrate, the semiconductor element, the first end of the external connection terminal, and at least part of the cooling device.

Fig.1A



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device.

[0002] Japanese Laid-Open Patent Publication No. 2008-263210 discloses a power semiconductor device provided with a first lead, which includes a first die pad, a power chip, which is arranged on an upper surface of the first die pad, and an insulating seat, which is applied to a lower surface of the first die pad. The power semiconductor device is also provided with a second lead, which includes a second die pad, a control chip, which is arranged on the second die pad, a wire, which connects the power chip and the control chip and of which the main component is gold, and a molded resin portion. The control chip and the power chip are embedded in the resin portion so that an end of the first lead and an end of the second lead project from the resin portion. The insulating seat has a higher heat conductivity than the resin portion.

[0003] Referring to Fig. 9, a power semiconductor element may be mounted on a substrate and a resin portion may be molded on the substrate to form a semiconductor module 100. This increases the reliability of the element during a power cycle. To cool the power semiconductor element, which generates heat, by fixing the semiconductor module 100 to a heat dissipation member 101 (heat sink or the like), for example, a bracket 102 that applies urging force F is required to be fixed to the heat dissipation member 101. In this case, silicone grease 103 is filled in a gap formed between the heat dissipation member 101 and the semiconductor module 100 (e.g., gap formed by bending of the substrate). The silicone grease 103 has low heat conductivity and thus hinders cooling. Further, the use of the bracket 102 to fix the semiconductor module 100 enlarges the entire device.

SUMMARY OF THE INVENTION

[0004] It is an object of the present invention to provide a semiconductor device and a method for manufacturing a semiconductor device that increase the reliability of element portions joined by a molded resin portion, achieves a high cooling capability, and allows for reduction in size.

[0005] To achieve the above object, one aspect of the present invention is a semiconductor device provided with a cooling device including a coolant passage. An insulating substrate is brazed to an outer surface of the cooling device. A semiconductor element is soldered to the insulating substrate. An external connection terminal includes a first end, which is electrically connected to the semiconductor element, and an opposite second end. A resin portion is molded to the insulating substrate, the semiconductor element, the first end of the external connection terminal, and at least part of the cooling device.

[0006] A further aspect of the present invention is a method for manufacturing a semiconductor device. The method includes forming a cooling device by joining a first shell plate and a second shell plate. The first shell plate includes a peripheral portion and the second shell plate includes a peripheral portion, which is brazed together with the peripheral portion of the first shell plate. The method further includes brazing the first shell plate and an insulating substrate together to join the first shell plate and the insulating substrate; mounting a semiconductor element on the insulating substrate; soldering the semiconductor element and a first end of an external connection terminal together to join the semiconductor element and the external connection terminal; and molding a resin portion on the insulating substrate, the semiconductor element, the first end of the external connection terminal, and at least part of the first shell plate.

[0007] Other aspects and advantages of the present invention will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

Fig. 1A is a front view of an inverter module according to one embodiment of the present invention;
Fig. 1B is a plan view of the inverter module shown in Fig. 1A;
Fig. 2A is a front view of the inverter module shown in Fig. 1A in a state in which a resin portion is eliminated;
Fig. 2B is a plan view of the inverter module shown in Fig. 1A in a state in which the resin portion is eliminated;
Fig. 3 is a circuit diagram of the inverter module shown in Fig. 1A;
Fig. 4A is a front view showing insulating substrates of the cooling device of Fig. 1A;
Fig. 4B is a plan view showing the insulating substrates of the cooling device of Fig. 1A;
Fig. 5 is a cross-sectional view taken along V-V in Fig. 4B;
Fig. 6A is a front view illustrating a manufacturing process of the inverter module;
Fig. 6B is a plan view showing the inverter module of Fig. 6A;
Fig. 7 is a front view showing a modification of an inverter module;
Fig. 8 is a front view showing a modification of an inverter module; and
Fig. 9 is a cross-sectional view showing a structure

that fixes a heat dissipation member to a module.

DETAILED DESCRIPTION OF THE INVENTION

[0009] A vehicle inverter according to one embodiment of the present invention will now be described with reference to the drawings.

[0010] Referring to Figs. 1A and 1B, an inverter module 10 includes a cooling device. The inverter module 10 is resin-molded and includes substrates on which semiconductor elements (chips) are mounted. As shown in Figs. 1A to 2B, the inverter module 10 includes a water-cooling type cooling device 20, four insulating substrates 31, 32, 33 and 34, six transistors (chips) Q1, Q2, Q3, Q4, Q5, and Q6, six diodes (chips) D1, D2, D3, D4, D5, and D6, and a molded resin portion 40. The resin portion 40 may be formed from, for example, epoxy resin.

[0011] Fig. 3 shows the circuit configuration of the inverter module 10. The inverter module 10 includes an inverter 50, which converts DC power supplied from an external device, to AC power. Then, the inverter 50 supplies the AC power to a travel motor 60. This drives the motor 60, which produces rotation.

[0012] In detail, the inverter 50 includes a plurality of arms, namely, a U-phase arm, a V-phase arm, and a W-phase arm arranged in parallel between a power supply line and a ground line. The arms include two series-connected transistors (IGBT) Q1 and Q2, Q3 and Q4, and Q5 and Q6, respectively. Diodes D1, D2, D3, D4, D5, and D6 are arranged between the collector and emitter of the transistors Q1, Q2, Q3, Q4, Q5, and Q6, respectively. Each diode allows for current to pass from the emitter to the collector of the corresponding transistor.

[0013] As shown in Figs. 1A to 2B, the insulating substrates 31, 32, 33, and 34 are formed by direct brazed aluminum (DBA) substrates. Each DBA substrate includes a ceramic substrate 35, an aluminum layer 36, which is formed on a first surface of the ceramic substrate 35, and an aluminum layer 37, which is formed on a second surface of the ceramic substrate 35. The aluminum layer 36 is patterned on the first surface of the ceramic substrate 35. In the same manner, the aluminum layer 37 is patterned on the second surface of the ceramic substrate 35.

[0014] The cooling device 20 has the shape of a tetragonal box having a low profile and is formed from aluminum. As shown in Fig. 5, the cooling device 20 includes an upper plate 24, which functions as a first shell plate, a lower plate 25, which functions as a second shell plate, and inner fins 26, which are undulated. A peripheral portion of the upper plate 24 and a peripheral portion of the lower plate 25 are swaged together. In this state, the peripheral portions of the upper plate 24 and the lower plate 25 are brazed to each other. This brazes the upper plate 24 and the lower plate 25 at their peripheral portions in the cooling device 20. A coolant passage P1 is formed between the upper plate 24 and the lower plate 25. The inner fins 26 are also brazed to and between the upper plate 24 and lower plate 25.

[0015] In this manner, the cooling device 20 includes a coolant passage P1 (refer to Fig. 5). Coolant is supplied to the cooling device 20 through a pipe (not shown) and discharged from the cooling device 20 through a pipe (not shown).

[0016] The four insulating substrates 31, 32, 33, and 34 are brazed to the upper surface (outer surface) of the cooling device 20. In detail, the aluminum layer 36 under the ceramic substrate 35 in each of the four insulating substrates 31, 32, 33, and 34 is brazed and joined with the upper surface of the cooling device 20.

[0017] The aluminum layer 37 on the ceramic substrate 35 in the insulating substrate 31 is a wiring material. The transistor (chip) Q1 and the diode (chip) D1 are soldered and joined with the upper surface of the aluminum layer 37. The aluminum layer 37 on the ceramic substrate 35 in the insulating substrate 32 is a wiring material. The transistor (chip) Q3 and the diode (chip) D3 are soldered and joined with the upper surface of the aluminum layer 37. The aluminum layer 37 on the ceramic substrate 35 in the insulating substrate 33 is a wiring material. The transistor (chip) Q5 and the diode (chip) D5 are soldered and joined with the upper surface of the aluminum layer 37. The aluminum layer 37 on the ceramic substrate 35 in the insulating substrate 34 is a wiring material. The transistors (chips) Q2, Q4, and Q6 and the diodes (chips) D2, D4, and D6 are soldered and joined with the upper surface of the aluminum layer 37.

[0018] The collector terminals on the upper surfaces of the transistors Q1, Q3, and Q5 and the cathode terminals on the upper surfaces of the diodes D1, D3, and D5 are joined with a conductive plate 70, which functions as an external connection terminal, by solder 71. The collector terminal on the upper surface of the transistor Q2, the cathode terminal on the upper surface of the diode D2, and the aluminum layer 37 in the insulating substrate 31 (the emitter of the transistor Q1 and the anode of the diode D1) are joined with a conductive plate 72, which functions as an external connection terminal, by solder 73. Further, the collector terminal on the upper surface of the transistor Q4, the cathode terminal on the upper surface of the diode D4, and the aluminum layer 37 in the insulating substrate 32 (i.e., the emitter of the transistor Q3 and the anode of the diode D3) are joined with a conductive plate 74, which functions as an external connection terminal, by solder 75. The collector terminal on the upper surface of the transistor Q6, the cathode terminal on the upper surface of the diode D6, and the aluminum layer 37 in the insulating substrate 33 (i.e., the emitter of the transistor Q5 and the anode of the diode D5) are joined with a conductive plate 76, which functions as an external connection terminal, by solder 77. A conductive plate 78, which functions as an external connection terminal, is soldered to the aluminum layer 37 on the ceramic substrate 35 in the insulating substrate 34. The conductive plates 70, 72, 74, 76, and 78 are made of copper. The conductive plates 70, 72, 74, 76, and 78

each include a first end a second end. The first ends of the conductive plates 70, 72, 74, 76, and 78 are electrically connected to the corresponding transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the corresponding diodes D1, D2, D3, D4, D5, and D6.

[0019] The second end of the conductive plate 70 is bent upward. In the same manner, the second end of the conductive plate 72 is bent upward. The second end of the conductive plate 74 is bent upward. The second end of the conductive plate 76 is bent upward. The second end of the conductive plate 78 is bent upward.

[0020] Six connection pin seats 80, 81, 82, 83, 84, and 85 are fixed to the upper surface the cooling device 20. Three connection pins 86, which function as external connection terminals, are fixed to each of the connection pin seats 80, 81, 82, 83, 84, and 85. The connection pins 86 are made of copper. One of the three connection pins 86 forms a gate voltage application line, and the two remaining connection pins 86 forming an emitter voltage detection line and an emitter temperature detection line. The three connection pins 86 include first terminals electrically connected by wires W formed by a wiring material, or wire-bonded, to the transistors (chips) Q1, Q2, Q3, Q4, Q5, and Q6.

[0021] The three connection pins 86 include the first terminals, which are electrically connected to the corresponding transistors Q1, Q2, Q3, Q4, Q5, and Q6, and second terminals, which are bent upward.

[0022] The resin portion 40 covers the components arranged on the upper surface of the cooling device 20 (i.e., the insulating substrates 31, 32, 33, and 34, the transistors Q1, Q2, Q3, Q4, Q5, and Q6, the diodes D1, D2, D3, D4, D5, and D6, the conductive plates 70, 72, 74, 76, and 78, the connection pins 86, and the wire W). The conductive plates 70, 72, 74, 76, and 78 include upright portions 70a, 72a, 74a, 76a, and 78a with upper ends exposed from the resin portion 40. In the same manner, the three connection pins 86, which are connected to each of the transistors Q1, Q2, Q3, Q4, Q5, and Q6, include upright portions 86a with upper ends exposed from the resin portion 40. The resin is molded onto a brazed part B (refer to Fig. 5) at the peripheral portions of the upper plate 24 and lower plate 25 in the cooling device 20.

[0023] The cooling device 20 includes an exposed lower surface. An electronic component PD1 (refer to Fig. 1A) is arranged on the lower surface of the cooling device 20. The electronic component PD1 generates heat that is transferred to the cooling device 20. In this manner, metal (aluminum) exposed from the lower surface of the cooling device 20 allows for cooling of the electronic component PD1, which is a heat generating body.

[0024] The operation of the inverter module 10 will now be described.

[0025] Coolant flows through the cooling device 20. The six transistors Q1, Q2, Q3, Q4, Q5, and Q6 of the inverter module 10 each generate heat when performing a switching operation. The six diodes D1, D2, D3, D4, D5, and D6 generate heat when activated. The heat generated by the transistors Q1, Q2, Q3, Q4, Q5, and Q6 is transferred to the cooling device 20 through the insulating substrates 31, 32, 33, and 34 (DBA substrates), which transfer heat to the coolant flowing through the cooling device 20. In the same manner, the heat generated by the six diodes D1, D2, D3, D4, D5, and D6 is transferred to the cooling device 20 through the insulating substrates 31, 32, 33, and 34 (DBA substrates), which transfer heat to the coolant flowing through the cooling device 20.

[0026] A method for manufacturing the inverter module 10 will now be described with reference to Figs. 1A to 2B and Figs. 4A to 6B.

[0027] Referring to Figs. 4A to 5, the insulating substrates 31, 32, 33, and 34 (DBA substrates) are prepared. The aluminum layer 36 is patterned on one surface of the ceramic substrate 35, and the aluminum layer 37 is patterned on the other surface of the ceramic substrate 35. The peripheral portions of the upper plate 24 and lower plate 25, which form the cooling device 20, are swaged and brazed together. Further, the undulated inner fins 26 are also brazed between the upper plate 24 and the lower plate 25. At the same time, the insulating substrates 31, 32, 33, and 34 (DBA substrates) are brazed to the upper surface of the cooling device 20. In detail, the aluminum layer 36 under the ceramic substrate 35 in each of the four insulating substrates 31, 32, 33, and 34 is brazed to the upper surface of the cooling device 20. The brazing is performed at about 600°C.

[0028] Subsequently, referring to Figs. 6A and 6B, each of the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and each of the diodes D1, D2, D3, D4, D5, and D6 are soldered to the upper surface of the aluminum layer 37 on the ceramic substrate 35 in the corresponding one of the insulating substrates 31, 32, 33, and 34.

[0029] At the same time, the conductive plates 70, 72, 74, 76, and 78 are soldered to the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the diodes D1, D2, D3, D4, D5, and D6. Further, the connection pin seats 80, 81, 82, 83, 84, and 85, on which the connection pins 86 are fixed, are fixed to the upper surface of the cooling device 20.

[0030] Further, the connection pins 86 are joined with the corresponding transistors (chips) Q1, Q2, Q3, Q4, Q5, and Q6 by the wire W.

[0031] As shown in Figs. 1A to 2B, the resin portion 40 is used to seal the components mounted on the cooling device 20. The components mounted on the cooling device 20 include the insulating substrates 31, 32, 33, and 34, the transistors Q1, Q2, Q3, Q4, Q5, and Q6, the diodes D1, D2, D3, D4, D5, and D6, the conductive plates 70, 72, 74, 76, and 78, and the wire W. The resin portion 40 is molded at about 120°C.

[0032] The above embodiment has the advantages described below.

(1) The inverter module 10, which serves as a semiconductor device, includes the cooling device 20, the insulating substrates 31, 32, 33, and 34, the tran-

sistors Q1, Q2, Q3, Q4, Q5, and Q6, the diodes D1, D2, D3, D4, D5, and D6, the conductive plates 70, 72, 74, 76, and 78, and the connection pins 86. The insulating substrates 31, 32, 33, and 34 are brazed to the outer surface of the cooling device 20. Further, in a state in which the second ends of the conductive plates 70, 72, 74, 76, and 78 and the second terminals of the connection pins 86 are exposed, the resin portion 40 is molded to the insulating substrates 31 to 34, the transistors Q1 to Q6, the diodes D1 to D6, the first ends of the conductive plates 70, 72, 74, 76, and 78, the first terminals of the connection pins 86, and at least part of the cooling device 20.

[0033] In this manner, the insulating substrates 31, 32, 33, and 34 are brazed (integrated with metal) to the cooling device 20. Further, the semiconductor elements (i.e., the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the diodes D1, D2, D3, D4, D5, and D6), the conductive plates 70, 72, 74, 76, and 78, and the connection pins 86 are embedded in the resin portion 40 of the cooling device 20. Moreover, the conductive plates 70, 72, 74, 76, and 78 and the connection pins 86 are exposed from the resin portion 40 and integrated by resin as a cooling device module.

[0034] The insulating substrates 31, 32, 33, and 34 are brazed to the outer surface of the cooling device 20. This increases the capability for cooling the semiconductor elements (i.e., the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the diodes D1, D2, D3, D4, D5, and D6). Further, the resin portion 40 is molded to the insulating substrates 31 to 34, the semiconductor elements (i.e., the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the diodes D1, D2, D3, D4, D5, and D6), the first ends of the conductive plates 70, 72, 74, 76, and 78, the first terminals of the connection pins 86, and at least part of the cooling device 20. This eliminates the need for a dedicated fixing member and allows for reduction in size.

[0035] In detail, the insulating substrates 31, 32, 33, and 34 are directly joined by metal (integrated by metal) with the cooling device 20. Further, the semiconductor elements (i.e., the transistors Q1, Q2, Q3, Q4, Q5, and Q6 and the diodes D1, D2, D3, D4, D5, and D6) are soldered to the insulating substrates 31, 32, 33, and 34. This allows for direct cooling of the semiconductor elements and increases the cooling capability. Further, the integration of the entire cooling device 20 with the resin portion 40 improves reliability. Moreover, the sealing of the entire cooling device 20 with the resin portion 40 eliminates the need for a fixing structure and allows for reduction in size. In this manner, the molding of resin onto members including the cooling device 20 allows for reduction in size, which would not be possible when using a fixing bracket 102 (pushing member) as shown in Fig. 9. Further, the silicone grease 103 of Fig. 9 becomes unnecessary.

[0036] In this manner, the resin portion 40 improves the reliability at joined portions of elements, increases the cooling capability, and allows for reduction in size.

(2) In the cooling device 20, the peripheral portions of the upper plate 24 and lower plate 25 are brazed together, and the coolant passage P1 is formed between the upper plate 24 and lower plate 25. Resin is molded to the brazed part B at the peripheral portions of the upper plate 24 and lower plate 25. This improves the seal of the upper plate 24 and lower plate 25.

[0037] In this manner, the resin portion 40 covers the side surfaces of the cooling device 20. This is preferable for increasing the seal (waterproof seal) of the cooling device.

(3) The semiconductor device manufacturing method includes a brazing step, a subsequent soldering step, and a subsequent molding step. Referring to Figs. 4 and 5, the brazing step joins the peripheral portions of the upper plate 24 (first shell plate) and lower plate 25 (second shell plate), which form the cooling device 20. The brazing step also joins the insulating substrates 31, 32, 33, and 34. Referring to Figs. 6A and 6B, the soldering step mounts the transistors Q1 to Q6 and diodes D1 to D6, which function as semiconductor elements, on the insulating substrates 31, 32, 33, and 34, and joins the transistors Q1 to Q6, which function as semiconductor elements, with the first ends of the conductive plates 70, 72, 74, 76, and 78, which function as external connection terminals. Referring to Figs. 1A to 2B, the molding step molds the resin portion 40 to the insulating substrates 31, 32, 33, and 34, the transistors Q1 to Q6, the diodes D1 to D6, the first ends of conductive plates 70, 72, 74, 76, and 78, and at least part of the upper plate 24, while exposing the second ends of the conductive plates 70, 72, 74, 76, and 78. The molding of the resin portion 40 improves the reliability of joined portions of elements and increases the cooling capability. Further, the inverter module 10 can be reduced in size.

[0038] It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Particularly, it should be understood that the present invention may be embodied in the following forms.

[0039] Referring to Fig. 7, instead of entirely sealing the side surfaces of the cooling device 20 with the resin portion 40, the side surfaces of the cooling device 20 may be partially sealed by the resin portion 40.

[0040] Referring to Fig. 8, instead of sealing the side surfaces of the cooling device 20 with the resin portion 40, the resin portion 40 may seal only the upper surface of the cooling device 20. This decreases the area of contact between the cooling device 20 and the resin portion

40 and lowers the force F1 applied to the cooling device 20 by the resin portion 40. Thus, deformation of the cooling device 20 caused by an external force is suppressed. Further, the amount of the resin can be decreased.

[0041] Although the insulating substrates 31, 32, 33, and 34 are DBA substrates, the insulating substrates may be direct brazed copper (DBC) substrates, each including a ceramic substrate 35 sandwiched by copper layers.

[0042] Although the present invention is applied to an inverter that functions as a power conversion device, the invention may be applied to other types of power conversion device, such as a converter.

[0043] The present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.

[0044] A semiconductor device includes a cooling device, an insulating substrate, a semiconductor element, an external connection terminal, and a resin portion. The insulating substrate is brazed to an outer surface of the cooling device. The semiconductor element is brazed to the insulating substrate. The external connection terminal includes a first end, which is electrically connected to the semiconductor element, and an opposite second end. The resin portion is molded to the insulating substrate, the semiconductor element, the first end of the external connection terminal, and at least part of the cooling device.

Claims

1. A semiconductor device **characterized by:**

   a cooling device (20) including a coolant passage (P1);
   an insulating substrate (31, 32, 33, 34) brazed to an outer surface of the cooling device (20);
   a semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6) soldered to the insulating substrate (31, 32, 33, 34);
   an external connection terminal (70, 72, 74, 76, 78) including a first end, which is electrically connected to the semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6), and an opposite second end; and
   a resin portion (40) molded to the insulating substrate (31, 32, 33, 34), the semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6), the first end of the external connection terminal (70, 72, 74, 76, 78), and at least part of the cooling device (20).

2. The semiconductor device according to claim 1, **characterized in that** the resin portion (40) is molded in a state in which the second end of the external connection terminal (70, 72, 74, 76, 78) is exposed from the resin portion (40).

3. The semiconductor device according to claim 1 or 2, **characterized in that**
   the cooling device (20) includes a first shell plate (24) and a second shell plate (25), each including a peripheral portion,
   the peripheral portions are brazed together to integrate the first shell plate (24) and the second shell plate (25), and
   the coolant passage (P1) is formed between the first shell plate (24) and the second shell plate (25).

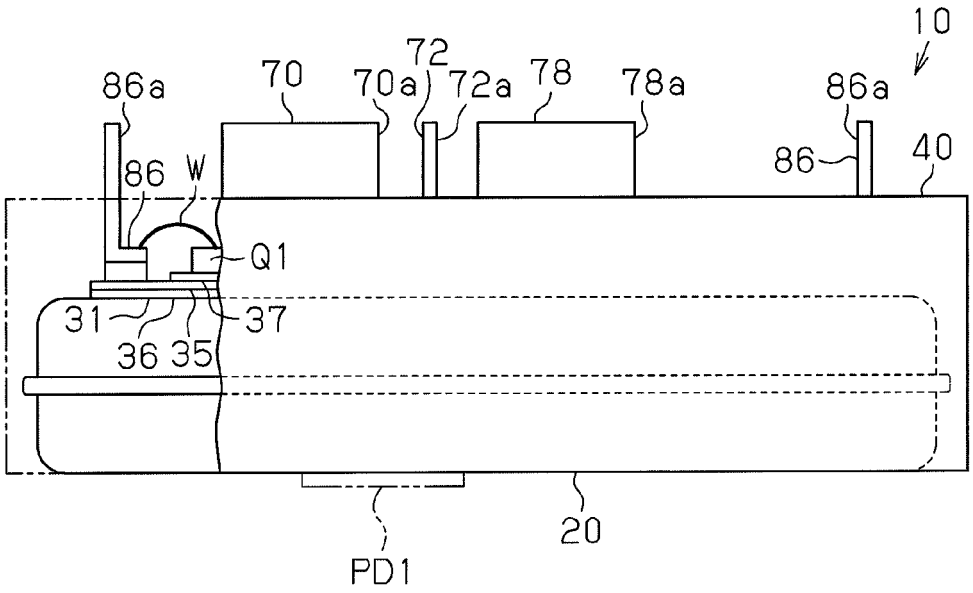
4. The semiconductor device according to claim 2, **characterized in that**
   the peripheral portion of the first shell plate (24) and the peripheral portion of the second shell plate (25) are brazed together to form a brazed portion (B), and the resin portion (40) is molded to the brazed portion (B).

5. A method for manufacturing a semiconductor device, the method **characterized by**:

   forming a cooling device (20) by joining a first shell plate (24) and a second shell plate (25), wherein the first shell plate (24) includes a peripheral portion and the second shell plate (25) includes a peripheral portion, which is brazed together with the peripheral portion of the first shell plate (24);
   brazing the first shell plate (24) and an insulating substrate (31, 32, 33, 34) together to join the first shell plate (24) and the insulating substrate (31, 32, 33, 34);
   mounting a semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6) on the insulating substrate (31, 32, 33, 34);
   soldering the semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6) and a first end of an external connection terminal (70, 72, 74, 76, 78) together to join the semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6) and the external connection terminal (70, 72, 74, 76, 78); and
   molding a resin portion (40) on the insulating substrate (31, 32, 33, 34), the semiconductor element (D1, D2, D3, D4, D5, D6, Q1, Q2, Q3, Q4, Q5, Q6), the first end of the external connection terminal (70, 72, 74, 76, 78), and at least part of the first shell plate (24).

6. The method for manufacturing a semiconductor device according to claim 5, **characterized in that** the resin portion (40) is molded in a state in which the second end of the external connection terminal (70, 72, 74, 76, 78) is exposed from the resin portion (40).

Fig.1A


10
72
86a
70
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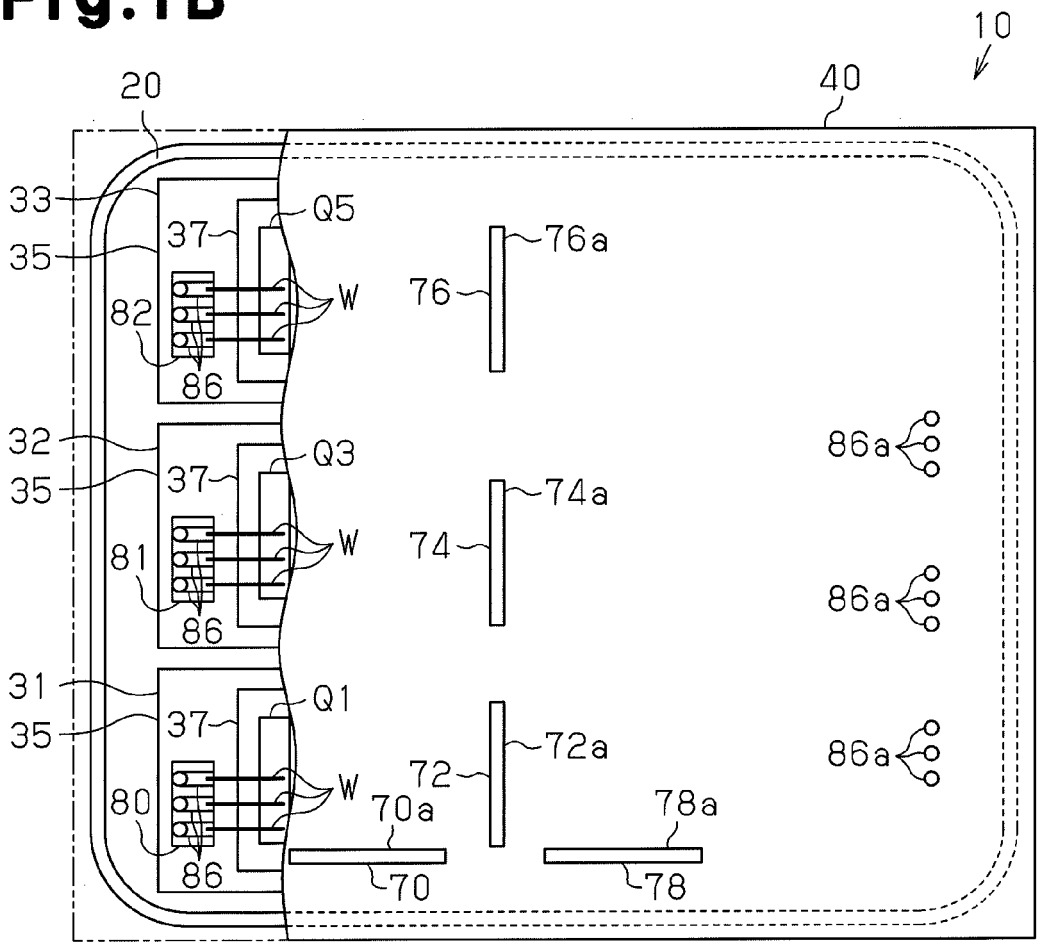
78
78a
86a
86
W
40
Q1
31
37
36
35
20
PD1

Fig.1B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86
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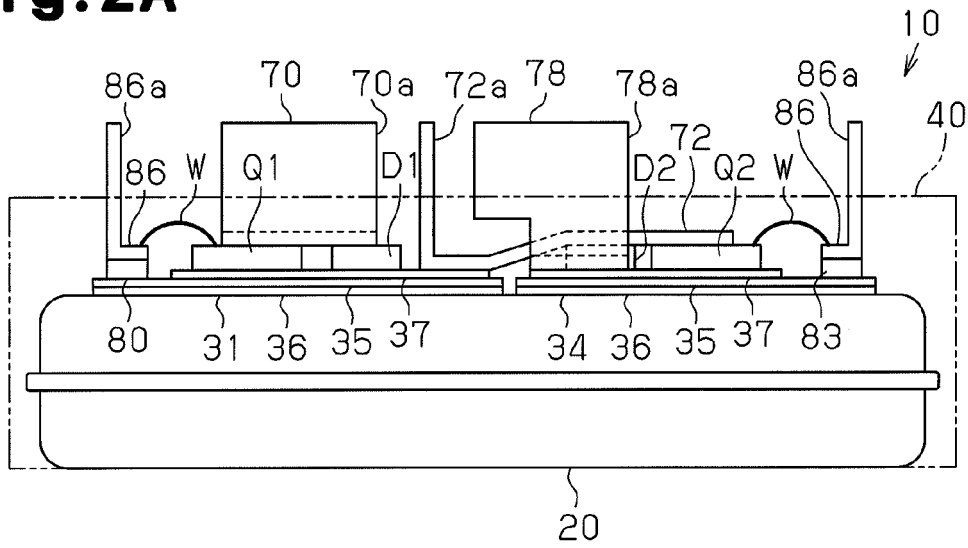
Fig.2A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D2
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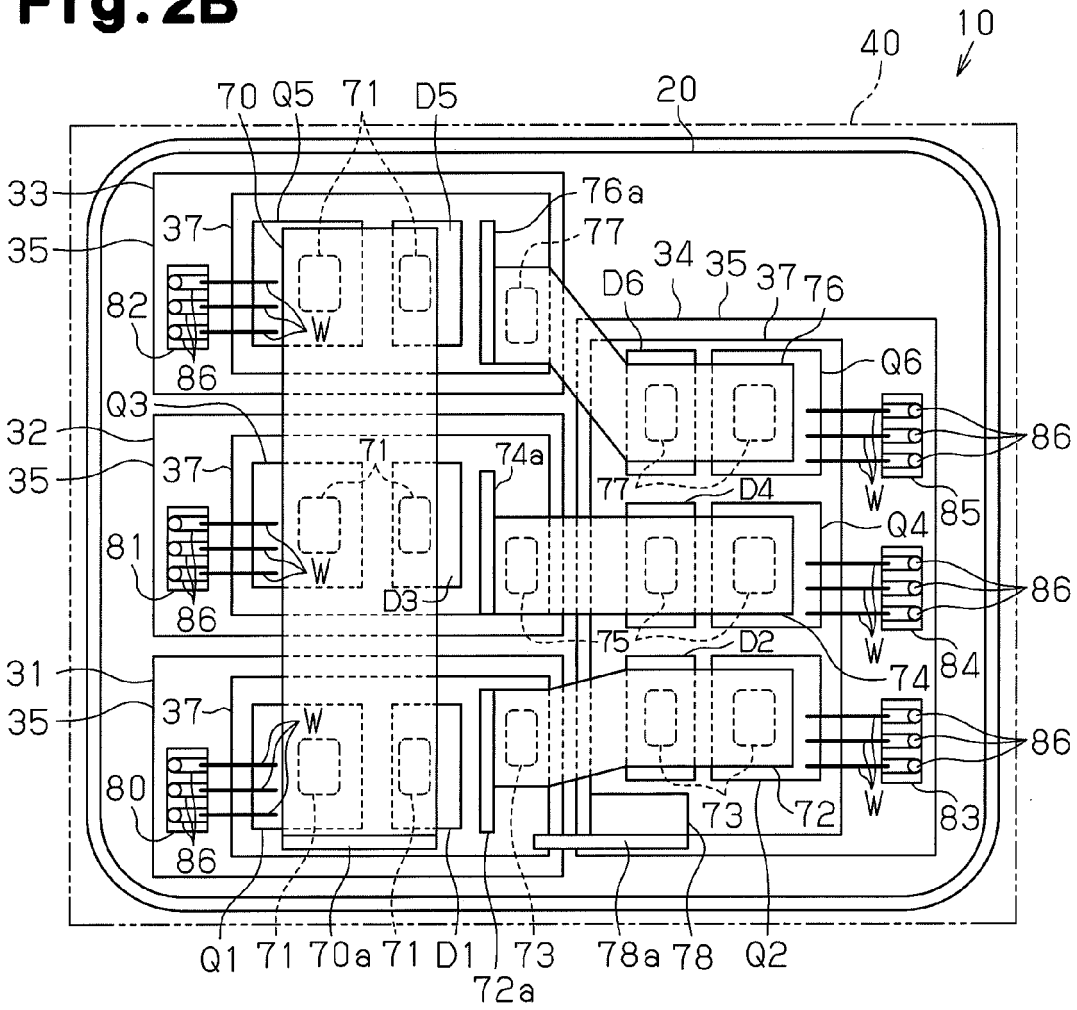
W
80
31
36
35
37
34
36
35
37
83
20

Fig.2B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Q5
71
D5
20
33
35
37
76a
77
34
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37
76
D6
82
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Q6
Q3
32
35
37
71
74a
77
D4
Q4
85
86
81
86
W
D3
75
D2
74
84
86
31
35
37
W
80
86
73
72
W
83
86
Q1
71
70a
71
D1
73
72a
78a
78
Q2

Fig.3

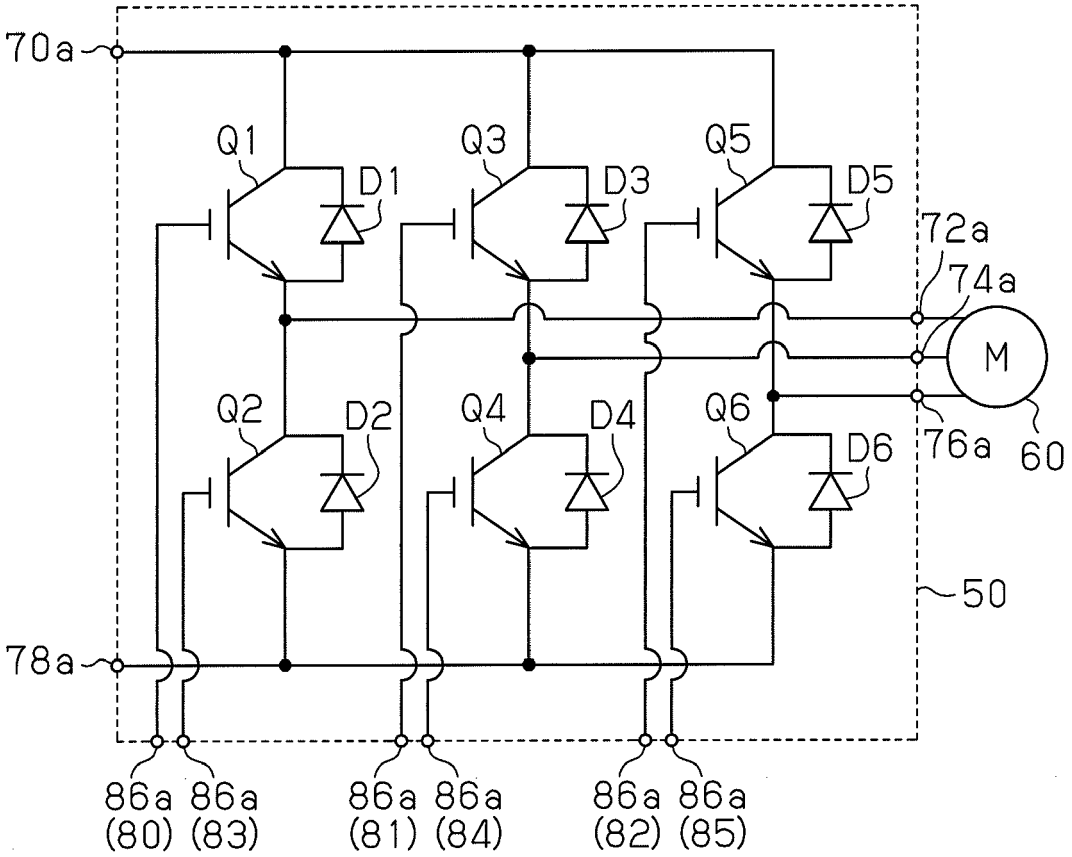

70a
Q1
D1
Q3
D3
Q5
D5
72a
74a
M
Q2
D2
Q4
D4
Q6
D6
76a
60
50
78a
86a (80)
86a (83)
86a (81)
86a (84)
86a (82)
86a (85)

Fig.4A

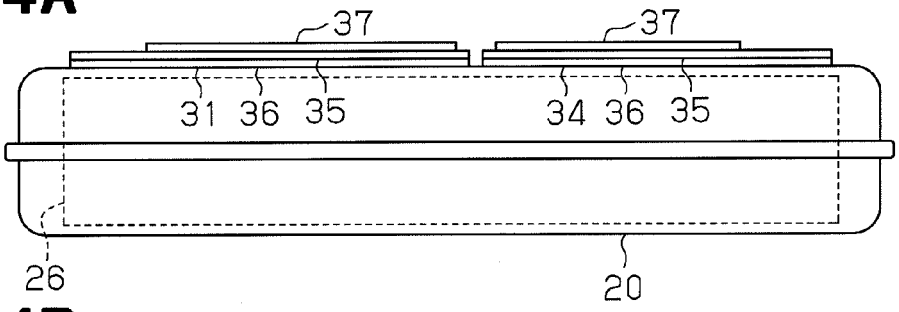


Fig.4B

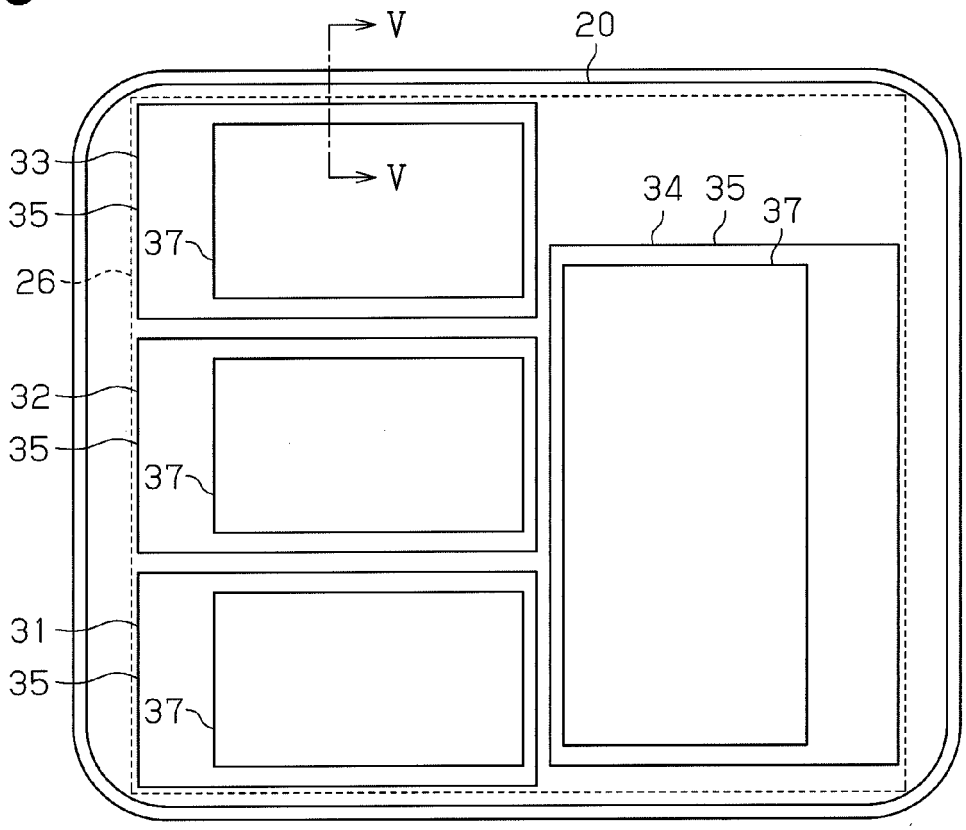


Fig.5

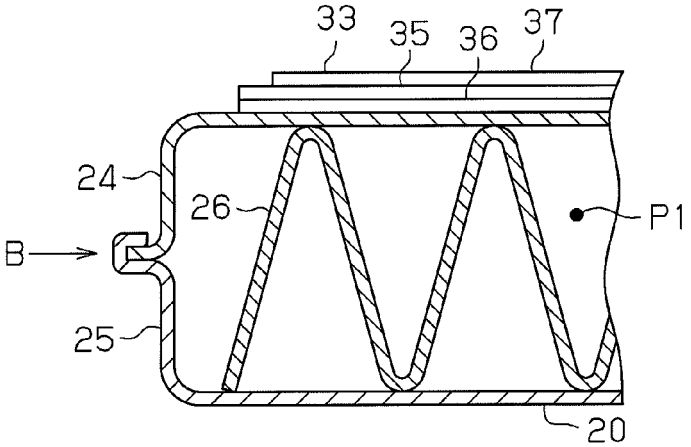
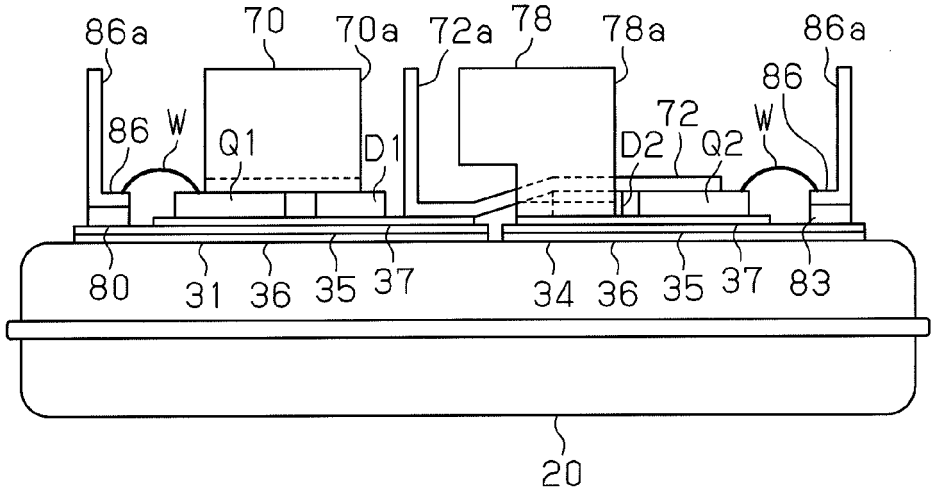


Fig.6A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D1
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D2
Q2
W
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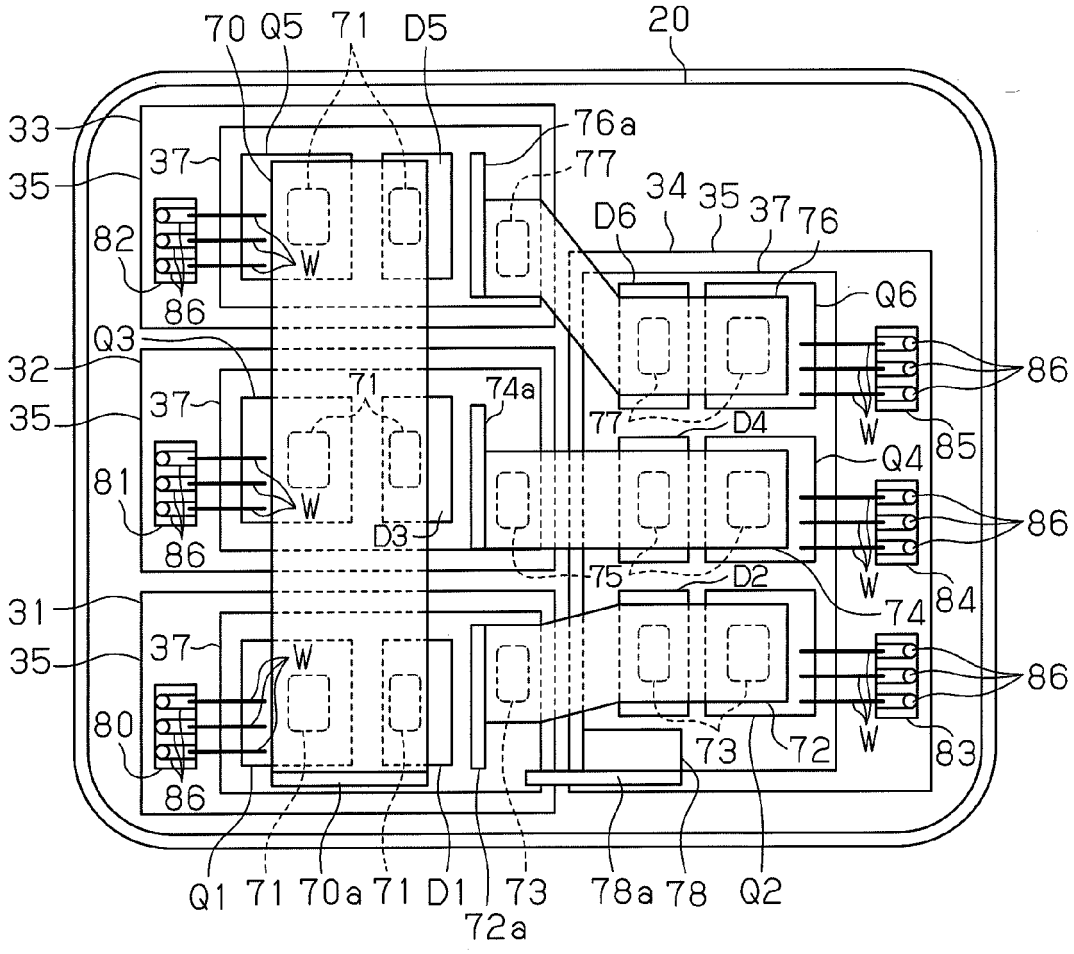
36
35
37
83
20

Fig.6B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Q4
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86
37
W
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D2
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83
86
Q1
71
70a
71
D1
73
72a
78a
78
Q2

Fig.7

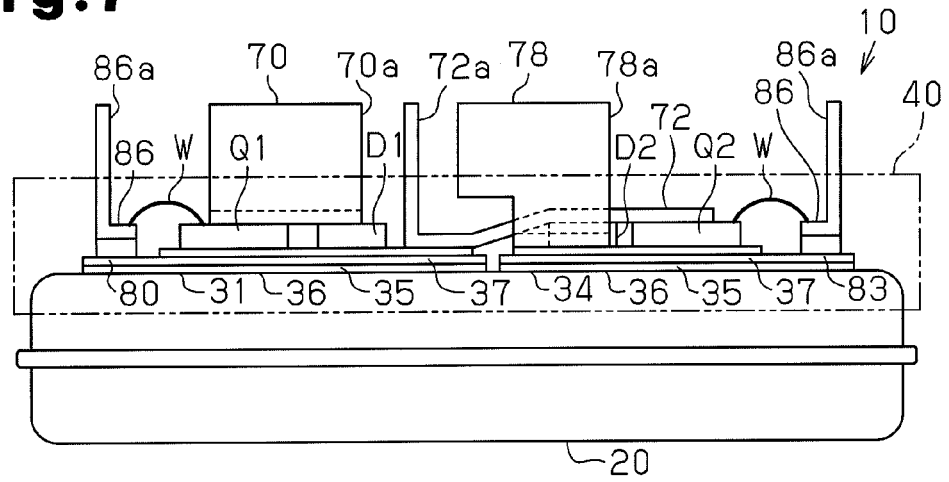


Fig.8

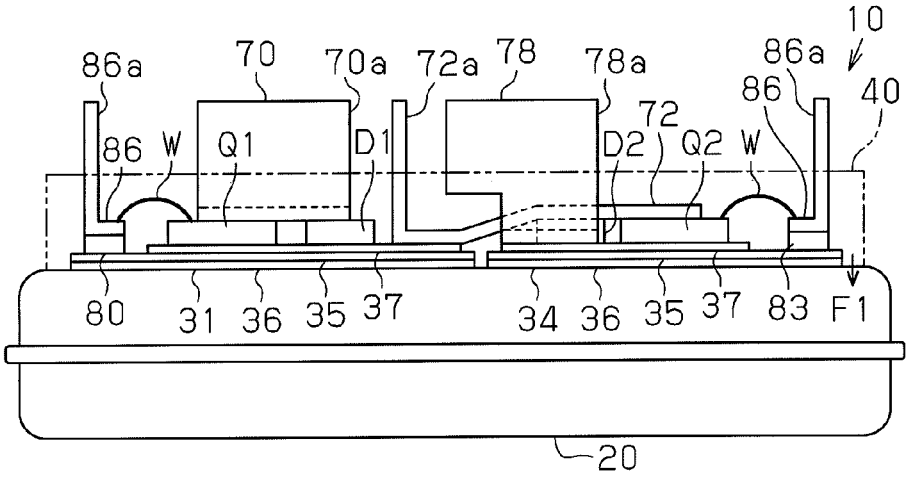
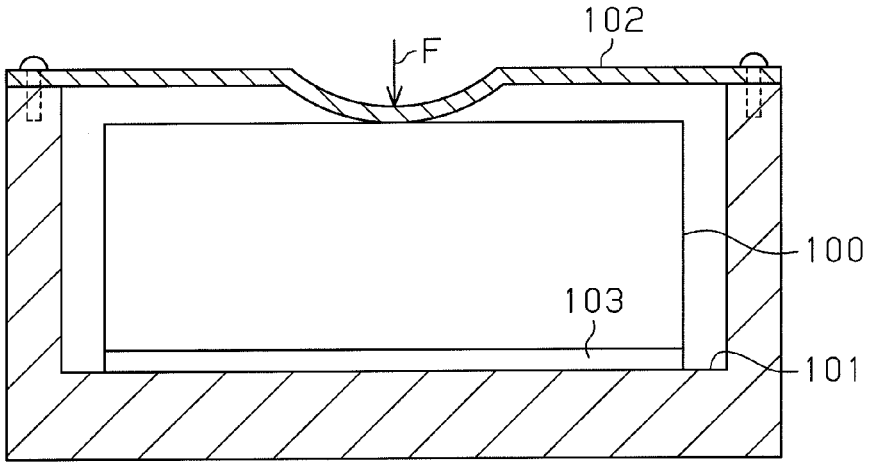


Fig.9



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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