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(54) **A fully differential amplifier topology to drive dynamic speakers in class AB mode**

Vollständig differenzielle Verstärkertopologie zur Ansteuerung dynamischer Lautsprecher in Klasse-AB-Modus

Topologie d'amplificateur entièrement différentiel pour entraîner des haut-parleurs dynamiques en mode de classe AB

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EP 2 645 565 B1

Description

Technical Field

[0001] This disclosure relates generally to the field of audio amplifier circuits and relates more specifically to a fully differential class AB amplifier topology.

Background

[0002] Power audio amplifiers are widely used to drive speakers in audio systems. Different classes of audio amplifiers are utilized to provide output signals. For example, class A amplifiers reproduce an entire input signal because an active element is constantly in active mode, hence having high power consumption.

[0003] To improve the full power efficiency of the previous Class A amplifier by reducing the wasted power in the form of heat, it is possible to design the power amplifier circuit with two transistors in its output stage producing what is commonly termed as a "push-pull" type amplifier configuration. Push-pull amplifiers use two "complementary" or matching transistors, one being an NPN-type and the other being a PNP-type with both power transistors receiving the same input signal together that is equal in magnitude, but in opposite phase to each other. This results in one transistor only amplifying one half or 180 degrees of the input waveform cycle while the other transistor amplifies the other half or remaining 180 degrees of the input waveform cycle with the resulting "two-halves" being put back together again at the output terminal. Then the conduction angle for this type of amplifier circuit is only 180 degrees or 50% of the input signal. These types of audio amplifier circuits are more generally known as the Class B Amplifier.

[0004] The Class AB Amplifier circuit is a compromise between the Class A and the Class B configurations. Both transistors slightly conduct even when no input signal is present.

[0005] In the class-D amplifier the input signal is converted to a sequence of higher voltage output pulses. The averaged-over-time power values of these pulses are directly proportional to the instantaneous amplitude of the input signal.

[0006] Class-G amplifiers use "rail switching" to decrease power consumption and increase efficiency. These amplifiers provide several power rails at different voltages and switch between them as the signal output approaches each level. Thus, the amplifier increases efficiency by reducing the wasted power at the output transistors.

[0007] The most common output driver modes are class AB and class D type; class AB uses the power stage devices in linear mode while class D uses the power devices in switched mode.

[0008] Current practice uses rail-to-rail intermediate stage to drive high/low side power devices. This approach has multiple disadvantages:

- In general, battery or output of a charge pump is used to supply the power stage, those same noisy supplies need to propagate to the intermediate stage, feeding noise and compromising PSR. One example of this mechanism is feed-forward through Miller compensation capacitors.
- When the supply is varying widely, like in class -G operation, its generally much more difficult to keep the intermediate stage biased in linear mode, requiring complex and larger design to arbitrate between adaptive (sometimes concurrent) controls inside the intermediate stage.
- When cascaded low voltage PMOS devices are used, it’s generally much more complicated in those topologies to protect their gates from seeing the full supply, especially at start-up.

[0009] It is a challenge for engineers to design an audio amplifier without the disadvantages cited above.

[0010] The object of the disclosure is achieved by the independent claims. Further embodiments are defined in the dependent claims.

[0011] WO 2009/063276 A1 discloses a fully differential amplifier operating in class AB mode.

[0012] LARSEN F ED - INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "A FULLY BALANCED, RAIL-TO RAIL, 3V, CLASS-AB OPERATIONAL AMPLIFIER", 1996 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS). CIRCUITS AND SYSTEMS CONNECTING THE WORLD. ATLANTA, MAY 12 - 15, 1996; [IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS (ISCAS)], NEW YORK, IEEE, US, 12 May 1996 (1996-85-12), pages 301-304, XP800825574, discloses a fully balanced, input/output rail-to-rail class AB amplifier.

[0013] THOUTAM S ET AL: "Power efficient fully differential low-voltage two stage class AB/AB op-amp architectures", PROCEEDINGS / 2004 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS: MAY 23 - 26, 2004, SHERATON VANCOUVER WALL CENTRE HOTEL, VANCOUVER, BRITISH COLUMBIA, CANADA, IEEE OPERATIONS CENTER, PISCATAWAY, NJ, 23 May 2004 (2004-05-23), pages 1-733, XP010719437, ISBN: 978-0-7803-8251-0 discloses a compact low-voltage two stage fully differential class AB/.AB op-amp architecture with high slew rate. The output stage does not require a quiescent current control circuit.

[0014] LOPEZ-MORILLO E ET AL: "A Very Low-Power Class AB/AB Op-amp based Sigma-Delta Modulator for Biomedical Applications", CIRCUITS AND SYSTEMS, 2006. MWSCAS '06.49TH IEEE INTERNATIONAL MIDWES T SYMPOSIUM ON, IEEE, PI, 1 August 2006 (2006-08-01), pages 458-462, XP031113639, ISBN: 978-1-4244-0172-7 discloses a Sigma-Delta modulator with 8 bits of resolution to be used for a cardiac pacemaker.

Summary of the invention

[0015] A principal object of the present disclosure is to achieve a fully differential amplifier topology.

[0016] A further object of the disclosure is to achieve a straightforward design of an intermediate stage of the amplifier.

[0017] A further object of the disclosure is allowing partial use of MOS capacitors (MOSCAPS) for frequency compensation, allowing further area savings.

[0018] A further object of the disclosure is to achieve a simpler design allowing large saving in area of the error amplifier.

[0019] A further object of the disclosure is to migrate more easily the design from one technology node to another.

[0020] A further object of the disclosure is to achieve a better immunity against supply ripple, reducing potential audio buzz (e.g. 217HZ).

[0021] A further object of the disclosure is to achieve a more suitable for ground-centered type of output.

[0022] A further object of the disclosure is to achieve an easy adaptation to class-G modulation.

[0023] As an exemplary embodiment not being part of the invention, a method to achieve a fully differential amplifier operating in class AB mode, comprising an arrangement for differential drive intermediate stage to control a differential loop, a common mode regulation and class AB regulation has been achieved. The method disclosed comprises, firstly, the following steps: (1) providing a fully differential amplifier operating in class AB mode comprising ports for differential input error signals Vip and Vim and for differential output signals Vop and Vom, wherein Vop is generated by a first output branch and Vom is generated by a second output branch wherein each output branch comprising high side and low side devices, wherein the amplifier comprises an output stage and an intermediate stage processing the input signals, and (2) enabling a main loop output common mode regulation by introducing dual differentiation of the input error signal to support common mode regulation by splitting driving signals for a first transistor of each of said output branch from a control path for a second transistor of each of said output branch. Furthermore the method comprises the steps of: (3) reducing a common mode error by decreasing both voltages Vop and Vom if a differential output common mode is higher than a common mode reference, and (4) regulating quiescent currents of both output branches inside the amplifier by sensing a current of a device of each output branch conducting the smallest current, comparing it with an internal reference current in order to regulate the minimum current.

[0024] As an exemplary embodiment not being part of the invention, a circuit of a fully differential amplifier operating in class AB mode has been achieved. The circuit disclosed firstly comprises: a differential output stage comprising a P and an M branch, wherein each branch comprises a high side device and a low side device and a differential intermediate stage. The differential intermediate stage comprises a first pair of PMOS transistors comprising a first and a second PMOS transistor, amplifying a differential input error signal wherein each transistor generates a driving signal for a correspondent said low side device and a control signal to a correspondent said high side device, wherein the sources of both transistors are connected, a first pair of NMOS transistors wherein a gate of each NMOS transistor is connected at a correspondent high impedance node to a drain of a correspondent transistor of the first pair of PMOS transistors and to a gate of said low side device and a drain of each NMOS transistor is connected to a drain and a gate of a correspondent NMOS transistor of a third pair of NMOS transistors, and said second pair of PMOS transistors, wherein each gate of the second pair of PMOS transistors is connected to a gate of a correspondent high side device forming a current mirror, wherein the each of the PMOS transistors of the second pair are scaled down in a same scale relative to the high side devices. Furthermore the intermediate stage comprises a loop control circuit, a common mode regulation loop circuit, and a class AB regulation loop.

Description of the drawings

[0025] In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 shows the basic elements of a class AB amplifier in differential mode.

Fig. 2 illustrates a simplified schematic of a class-AB amplifier using differential drive principle.

Fig. 3 illustrates a new arrangement of the intermediate stage to enable output common mode regulation.

Fig. 4a shows one way of sensing the differential output common mode.

Fig. 4b presents a simplified schematic of a common mode regulation circuit.

Fig. 5a illustrates how the output stage current sensing could be implemented (half bridge P).

Fig. 5b depicts a simplified schematic of class-AB feedback.

Fig. 6 shows a detailed schematic of the combined implementation of the four control loops.

Fig. 7 illustrates a small signal model of the amplifier disclosed.

Fig. 8 illustrates a flowchart of a method to achieve a fully differential amplifier operating in class AB mode, comprising an arrangement for differential drive intermediate stage to control a differential loop, a common mode regulation and class AB regulation.

Description of the preferred embodiments

[0026] Methods and circuits for a fully differential amplifier topology to drive dynamic speakers in class AB mode are disclosed.

[0027] **Fig. 1** shows the basic elements of a class AB amplifier in differential mode. **Fig. 1** depicts an amplifier **1,** receiving differential inputs **vip** and **vim** and providing differential outputs **vop** and **vom,** loudspeaker **2,** feedback resistors **3,** and input resistors **4.** Fig. 1 also shows input signals **5** and output signals **6.**

[0028] When a differential audio signal **vip** and **vim** is present at the input stage, the difference, or error, between the two inputs **vip** and **vim** is amplified to generate fully differential output signals **vop** and **vom.**

[0029] The bold lines of the input/output signals **5-6** indicate that each device operates the same way as in class B amplifiers over half the waveform, but also conducts a small amount on the other half. As a result, the region where both devices simultaneously are nearly off (the "dead zone") is reduced. The result is that when the waveforms from the two devices are combined, the crossover is greatly minimized or eliminated altogether.

[0030] The input/feedback resistors **3-4** are arranged in a switched network to achieve a programmable closed loop gain of the amplifier **1** (PGA). A speaker equivalent resistive load in portable applications is typically 32 Ohms but can be as low as 4 Ohms.

[0031] **Fig. 2** illustrates a simplified schematic of a class-AB amplifier using differential drive principle having two stages, an intermediate stage and an output stage. The output stage comprises two branches each generating respectively an output voltage **Vop** and **Vom.** A first output branch comprises high side device **M12** and low side device **M5,** the second branch comprises high side device **M11** and low side device **M6.** Furthermore the output stage comprises transistors **M7** and **M9** driving high side output transistor **M11** and transistors **M8** and **M10** driving high side output transistor **M12.**

[0032] Controlled current sources **20** and **21** are provided to supply the intermediate stage with current required. These current sources are controlled through the errors fed back from the class AB regulation loops as shown by **Fig 5a.**

[0033] The PMOS differential pair **M3/M4** of the intermediate stage amplifies an error **(vip-vim)** and generates on one hand a control signal of power PMOS transistors **M11/M12** using respectively **M7/M9** and **M8/M10.** Consequently a very simple differential pair can drive the power stage **M11/M12** with a neat splitting between the power supply via VDD rail of the output stage and the supply intermediate stage. This allows supplying the output stage e.g. with low voltage level (<1 V), while the intermediate stage could be still supplied from a higher core voltage.

[0034] The amplifier of **Fig. 2** shows how the differential amplification can be implemented using the differential drive principle, but it does not show how the common mode regulation and class-AB regulation could be implemented. Generally what happens is that any attempt to regulate the common mode by splitting the control of **M5/M6** from the control of M11/M12 conflicts with quiescent current regulation.

[0035] Therefore the object of the disclosure is to cover a new arrangement for differential drive intermediate stage to control the differential loop, the common mode regulation and the class-AB regulation.

<u>I Differential LOOP</u>

[0036] **Fig. 3** illustrates a new arrangement of the intermediate stage to enable output common mode regulation. The simplified schematic of **Fig. 3** introduces dual differentiation of the main loop error signal to support common mode regulation by splitting the intermediate stage into two simple differential stages, one controlling the low side devices and the other controlling the high side devices , i.e. splitting the diving signals from **M5/M6** from the control path of **M11/M12.**

[0037] The voltage error **vip-vim** is amplified through two separate paths:

1. differential pair M1/M2 to drive M5/M6, their gates are respectively node 1 and node 2.

2. differential pair M3/M4 to drive M11/M12, through respectively M7&M9 and M8&M10.

[0038] When voltage **vip** goes positive relative to voltage **vim,** nodes **1** and **3** are driven low to reduce drain currents of both transistors **M5** and **M11** while nodes **2** and **4** are driven high to increase the current of **M6** and **M12** simultaneously.. Therefore the differential output **(vop-vom)** increases.

II Output common mode regulation:

[0039] **Fig. 4a** shows one way of sensing the differential output common mode. The commode mode **CMFB** is sensed in the middle between two resistances **R** located between voltages **vop** and **vom.**

[0040] **Fig. 4b** presents a simplified schematic of a common mode regulation circuit **40.** The part of the circuit signified by **40** of the schematic of **Fig. 4b** show the common mode regulation circuit as part of the output driver. If the differential output common mode **(CMFB)** is higher than the common mode reference **(VREF)** then **M13** will draw more current reducing the tail current of differential pair **M3/M4** voltage of nodes **3** and **4** will tend to decrease, which makes **M9** and **M10** drain currents lower, therefore both **"vop"** and **"vom"** voltages will tend to decrease, reducing the common mode error.

[0041] Note that the high impedance nodes of the main loop are shared with the common mode regulation loop; therefore frequency compensation of both loops can be shared.

[0042] The new topology of **Fig. 4b** allows straightforward insertion of common mode regulation by imbalancing of the tail current of the intermediate stage differential pairs using M13/**M14.**

III Class -AB regulation

[0043] The main benefit of the class-AB regulation presented is the control of the cross-conducted current inside the amplifier with or without presence of audio signals. One additional benefit is to ensure the devices of both output stages remain in linear region to minimize crossover distortion.

[0044] The principle is to sense the current of the device conducting the smallest current, compare it to an internal reference current in order to regulate the minimum current by modulating - in opposite phase - the gate drives of **M12/M5** or **M6/M11.**

[0045] **Fig. 5a** illustrates how the output stage current sensing could be implemented (half bridge P) in order to generate a voltage **IQPFB** (respectively **IQMFB** for half bridge M), which are required to regulate the minimum current by using a differential amplifier **50.**

[0046] **Fig. 5b** depicts a simplified schematic of class-AB feedback (bold lines). It shows an example of quiescent current regulation feedback. The part of the circuit of **Fig. 5b** regulating the quiescent current is shown with bold lines.

[0047] If the minimum output current in the power stage **M5/M12** is higher than a predefined internal reference, the error between the two is scaling with feedback voltage **IQPFB** (respectively **IQMFB)** voltage and feeding back **IQPFB** to the active load connected to nodes **1** and **4** then node **1** and **4** voltages will decrease making currents in **M5, M8, M0**, and **M12** lower the quiescent current.

[0048] Regulation of the quiescent current of output stage **M6/M11** is implemented similarly by feeding feedback voltage **IQFMFB** to the active load connected to nodes **2** and **3.**

[0049] In summary the dual differential pair of the intermediate stage combines four different feedbacks and all share four high impedance nodes:

- Main loop regulation feedback (**Fig. 3**)
- Common mode regulation feedback (**Fig. 4b**)
- Output stage (P) quiescent current regulation (**Fig. 5b**)
- Output stage (M) quiescent current regulation **(Fig. 5b)**

[0050] **Fig. 6** shows a detailed schematic of the combined implementation of the four control loops. The part of the circuit of **Fig. 6** regulating the quiescent current is shown with bold lines. The part of the circuit of **Fig. 6** performing common mode regulation is shown using numeral 40.

[0051] This allows straightforward insertion of Class-AB regulation by use of feedback to the active load of the same intermediate stage differential pairs. **Fig. 6** shows as well how a straightforward Miller compensation of both output branches by capacitors **60-63** can be used to stabilize the four loops as they share the same high impedance nodes **1, 2, 3,** and **4.**

[0052] Alternatively MOSCAPS can be used for Miller compensation. In this case the MOSCAPS would have to be connected from nodes 1,2,3,4 to ground instead to the outputs as shown in Fig. 6 with capacitors 60-63.

[0053] As the high impedance nodes of the three regulation loops mentioned above are shared, compensation of the main loop improves also the stability of the common mode regulation loop and the class-AB regulation loop.

[0054] **Fig. 7** shows as well as how a straightforward Miller compensation can be used to stabilize the four loops as they share the same high impedance nodes **1, 2, 3,** and **4** as shown in **Fig. 6.,** wherein in **Fig.** 7 **vip/vim** signifies the differential input, **vc** signifies the common mode error, **vqp** signifies the quiescent current error (**P**), and **vqm** signifies the quiescent current error (**M**).

[0055] The table below shows how each feedback loop relates to transconductances of **Fig. 6:**

Transconductance	Regulation loop	Error signal
gm1=gm2=gm3=gm4	Differential	Vip-vim
gm13=gm14	Output common mode	vc
gmq (P side)	Quiescent current (P side)	vqp
gmq (M side)	Quiescent current (M side)	vqm

[0056] **Fig. 8** illustrates a flowchart of a method to achieve a fully differential amplifier operating in class AB mode, comprising an arrangement for differential drive intermediate stage to control a differential loop, a common mode regulation and class AB regulation. Step **80** of the method of **Fig. 8** illustrates the provision of a fully differential amplifier operating in class AB mode comprising ports for differential input error signals Vip and Vim and for differential output signals Vop and Vom and an output branch for Vop and an output branch for Vom. Step **81** depicts enabling output common mode regulation by introducing dual differentiation of the input error signal to support common mode regulation by splitting driving signals for a first transistor of each of said output branch from a control path for a second transistor of each of said output branch. Step **82** illustrates that if a differential output common mode is higher than a common mode reference, decreasing voltages of both Vop and Vom, thereby reducing a common mode error and, finally, step **83** illustrates regulating quiescent currents of both output branches inside the amplifier by sensing a current of a device of each output branch conducting the smallest current, comparing it with an internal reference current in order to regulate the minimum current.

[0057] In summary, main points of the disclosure are:

- New linear amplifier operating in class AB mode, comprising method of differential amplification, common mode regulation, and class AB regulation.
- Novel method of generating the output stage control signals by splitting the intermediate stage into two simple differential stages, one controlling the low side devices and the other controlling the high side devices.
- The new topology allows a neat splitting between the power supply of the output stage and the intermediate stage.
- The disclosure gives the possibility of supplying the output stage with low voltage level (<1 V), while the intermediate stage could be still supplied from a higher core voltage.
- The new topology allows straightforward insertion of common mode regulation by imbalancing of the tail current of the intermediate stage differential pairs.
- The disclosure prevents power supply feed-forward through compensation capacitors as the gate of the high side devices is no longer a high impedance node, hence improving PSR in the audio band.

[0058] The disclosed architecture allows straightforward insertion of Class-AB regulation by use of feedback to the active load of the same intermediate stage differential pairs.

- As the high impedance nodes of the three regulation loops mentioned above are shared, compensation of the main loop benefits also the stability of the common mode regulation loop and the class-AB regulation loop.
- Output stage PMOS devices are driven in current mirror configuration, hence the gate of the PMOS is naturally clamped and protected from breakdown in case low voltage power devices are used.

[0059] Furthermore it should be noted that an adaptation to Class G operation is straightforward with the current disclosure since the supply rail of the power stage is not shared with the supply rail of the control circuit of the main loop, common mode loop and Class AB regulation loop. Therefore switched supply can be easily connected to the power stage without any interaction with the core supply rails (generally low noise and well decoupled).

[0060] Moreover it should be noted that the disclosure could be applied not only to audio amplifiers but also to any other suitable amplifier application.

Claims

1. A method to achieve a fully differential amplifier operating in class AB mode, comprising an arrangement for a differential drive intermediate stage to control a differential loop, a common mode regulation and class AB regulation, comprising the following steps:

   (1) providing a fully differential amplifier operating in class AB mode comprising ports for differential input error signals Vip and Vim and for differential output signals Vop and Vom, wherein Vop is generated by a first output branch (M12, M5) of an output stage and Vom is generated by a second output branch (M11, M6) of the output stage wherein each output branch comprises high side (M11, M12) and low side transistors (M6, M5), wherein the amplifier comprises an intermediate stage processing the input signals;
   (2) splitting the intermediate stage into two simple differential stages, wherein a first (M1, M2) of these differential stages controls the low side transistors (M5, M6) and a second differential stage (M3, M4) controls the high side transistors (M11, M12) thus enabling differential output regulation by introducing dual differentiation of the input error signal to support common mode regulation by splitting driving signals of a first transistor of each of said output branch from a control path of a second transistor of each of said output branch;
   (3) reducing a common mode error by decreasing both voltages Vop and Vom if a differential output common mode (CMFB) is higher than a common mode reference (VREF), wherein a pair of NMOS transistors (M13/M14) compares the differential common mode (CMFB) with the common mode reference (VREF) and reduces the common mode error via said first and second differential stages; and
   (4) regulating quiescent currents of both output branches inside the amplifier by sensing a current of a transistor (M5/M12, M6/M11) of each output branch conducting the smallest current, comparing it with an internal reference current (IREF) in order to regulate the quiescent current, wherein said regulation of the quiescent current is performed by having each output branch being connected to a respective active load and feeding back a result of the comparison of the smallest current of each transistor (M5/M12, M6/M11) of each output branch with the internal reference current (IREF) to the respective active loads, thus decreasing voltages at corresponding nodes of each output branch and thus decreasing the quiescent currents.

2. The method of claim 1 wherein the amplifier is operating as an audio amplifier.

3. The method of claim 1 wherein the intermediate stage is split into two simple differential stages, one (M1, M2) controlling the low side transistors (M5, M6) and the other (M3, M4) controlling the high side transistors (M11, M12), thus performing said splitting driving signals.

4. The method of claim 1 wherein power supply voltage is split between a VDD rail of the output stage and a supply of the intermediate stage.

5. The method of claim 4 wherein the output stage is supplied with a voltage level lower than 1 V, while the intermediate stage could be still supplied from a higher core voltage.

6. The method of claim 1 wherein straightforward insertion of common mode regulation by imbalancing of tail current of differential pairs of the intermediate stage is enabled.

7. The method of claim 1 wherein PSR in the audio band is improved by preventing power supply feed-forward through compensation capacitors.

8. The method of claim 1 wherein a straightforward insertion of Class-AB regulation by use of feedback to an active load of intermediate stage differential pairs is enabled.

9. The method of claim 1 wherein compensation of a main regulation loop improves stability of a common mode regulation loop and of a class-AB regulation loop by having high impedance nodes (1, 2, 3, 4) of the regulation loop, the common regulation loop, and the class-AB regulation loop being shared.

10. The method of claim 1 wherein an adaptation to class-G operation can be performed by connecting a switched supply to a power stage.

11. A circuit of a fully differential amplifier operating in class AB mode, comprising:

- a differential (Vom, Vop) output stage comprising a P branch (M12, M5) and an M branch (M11, M6), wherein each of the P and M branches comprises a high side transistor (M11, M12) and a low side transistor (M6, M5);
- a differential intermediate stage comprising

  - a first pair of PMOS transistors (M3/M4) comprising a first (M3) and a second (M4) PMOS transistor, which is capable of amplifying a differential input error signal (vip/vim) wherein each transistor (M3/M4) is capable of generating a control signal to a correspondent said high side transistor (M11/M12), wherein the sources of both transistors of the first pair of PMOS transistors are connected, wherein controlled current sources (21) are deployed between each drain of the transistors of the first pair of PMOS transistors (M3/M4) and ground, wherein these controlled current sources (21) are configured to be controlled by errors fed back from class AB regulation loop circuits;
  - a first pair of NMOS transistors (M7/M8) wherein a gate of each NMOS transistor (M7/M8) is connected via a correspondent high impedance node (3, 4) to a drain of a correspondent transistor of the first pair of PMOS transistors (M3/M4) and a drain of each NMOS transistor (M7/M8) is connected to a drain and a gate of a correspondent PMOS transistor of a second pair of PMOS transistors (M9/M10);
  - said second pair of PMOS transistors (M9/M10), wherein each gate of the second pair of PMOS transistors (M9/M10) is connected to a gate of a correspondent said high side transistor (M11/M12) forming a current mirror,

wherein each of the PMOS transistors of the second pair (M9/M10) of PMOS transistors is scaled down in a same scale relative to the high side transistor;

  - a third pair of PMOS transistors (M1/M2) comprising a first (M1) and a second (M2) PMOS transistor, which is capable of amplifying the differential input error signal (vip/vim) wherein each transistor (M1/M2) is capable of generating a driving signal for a correspondent said low side transistor (M5/M6), wherein the sources of both transistors of the third pair of PMOS transistors (M1/M2) are connected, wherein controlled current sources (21) are deployed between each drain of the transistors of the third pair of PMOS transistors (M1/M2) and ground, wherein these controlled current sources (21) are configured to be controlled by errors fed back from the class AB regulation loop circuits;
  - a differential loop control circuit comprising a dual differentiation of the differential input error signal (vip/vim) by splitting the differential intermediate stage into two differential stages, wherein a first diffential stage thereof controls the low side transistors (M5, M6) by the third pair of PMOS transistors (M1/M2), wherein the gates of the transistors of the third pair of PMOS transistors (M1/M2) are respectively connected to input signals vip and vim of the differential input error signal (vip/vim) and wherein the gates of the low side transistors (M5,M6) are respectively connected to the drains of the transistors of the third pair of PMOS transistors (M1/M2) via a correspondent high impedance node (1,2) and wherein a second differential stage thereof controls the high side transistors (M11, M12) by the first pair of PMOS transistors (M3/M4), wherein the gates of the transistors of the first pair of PMOS transistors (M3/M4) are respectively connected to the input signals vip and vim of the differential input error signal (vip/vim) and wherein the gates of the high side transistors (M11, M12) are controlled via the high impedance nodes (3, 4) and a first NMOS transistor (M7) of the first pair of NMOS transistors (M7/M8) and a first PMOS transistor (M9) of the second pair of PMOS transistors (M9/M10) or respectively via a second NMOS transistor (M8) of the first pair of NMOS transistors (M7/M8) and a second PMOS transistor (M10) of the second pair of PMOS transistors (M9/M10);
  - a common mode regulation loop circuit comprising:

    - the third pair of PMOS transistors (M1/M2) in parallel to said first pair of PMOS transistors (M3/M4);, wherein each transistor of the third pair (M1/M2) of PMOS transistors is capable of controlling respectively one of said low side transistors (M5/M6) of the correspondent output branch (P/M branch) via the respective high impedance node (1,2) and each transistor of the first pair (M3/M4) of PMOS transistors is capable of controlling respectively one of said high side transistors of the correspondent output branch (P/M branch) (M11/M12) via the respective high impedance node (3, 4) wherein the sources of both transistors of the third PMOS pair (M1/M2) are connected; and
    - a second pair of NMOS transistors (M13/M14), wherein a drain of a first transistor (M13) of the second pair of NMOS transistors (M13/M14) is connected to the sources of the transistors of the first pair of PMOS transistors (M3/M4), a gate of the first transistor (M13) is connected to a common mode feedback (CMFB) sensed, a drain of a second transistor (M14) of the second pair of NMOS transistors (M13/M14) is connected to the sources of the transistors of the third pair of PMOS transistors (M1/M2), and a gate of the second transistor (M14) is connected to common mode reference voltage (VREF) ; wherein

frequency compensation of the differential loop control circuit and of the common mode regulation circuit is shared by sharing the high impedance nodes (1, 2, 3, 4) of the differential loop control circuit and of the common mode regulation circuit; and

- said class AB regulation loop circuits, wherein a first of said class AB regulation loop circuits is configured to provide a voltage (IQPFB) to the high impedance nodes (1, 4) configured to control the P branch (M12, M5), wherein the voltage (IQPFB) is configured to scale an quiescent current error of the P branch (M12, M5), wherein the quiescent current error of the P branch is the difference of the smallest current of the currents flowing respectively through the high side transistor (M12) or the low side transistor (M5) of the P branch compared with an internal reference current, in order to regulate the smallest current by modulating in opposite phase the gate drives of the high side transistor (M12) and the low side transistor (M5) of the P branch via said high impedance nodes (4, 1) configured to control the P branch and the second NMOS transistor (M8) of the first pair of NMOS transistors (M7/M8) and the second PMOS transistor (M10) of the second pair of PMOS transistors (M9/M10); and wherein a second of said class AB regulation loop circuits is configured to provide a voltage (IQMFB) to the high impedance nodes (2, 3) configured to control the M branch (M11, M6), wherein the voltage (IQMFB) is configured to scale an quiescent current error of the M branch (M12, M5), wherein the quiescent current error of the M branch is the difference of the smallest current of the currents flowing through the high side transistor (M11) or the low side transistor (M6) of the M branch compared with the internal reference current, in order to regulate the smallest current by modulating in opposite phase the gate drives of the high side transistor (M11) and the low side transistor (M6) of the M branch via said high impedance nodes (3, 2) configured to control the M branch and the first NMOS transistor (M7) of the first pair of NMOS transistors (M7/M8) and the first PMOS transistor (M9) of the second pair of PMOS transistors (M9/M10).

12. The circuit of claim 11 wherein the amplifier is operating as an audio amplifier.

13. The circuit of claim 11 wherein the output stage is configured to be supplied by a voltage lower than 1V.

14. The circuit of claim 13 wherein the intermediate stage is configured to be supplied by a voltage that is higher than a supply voltage of the output stage.

15. The circuit of claim 11 wherein the high impedance nodes (1, 2, 3, 4) are shared with the high impedance nodes of the common mode regulation loop enabling sharing of frequency compensation of both loops.

16. The circuit of claim 11 wherein in order to be capable of frequency compensation, a capacitor (60, 61) is connected between the M branch (M11, M6) and each of the high impedance nodes (2, 3) controlling the M branch and a capacitor (62, 69) is connected between the P branch (M5, M12) and each of the high impedance nodes (1, 4) capable of controlling the P branch (M5, M12).

17. The circuit of claim 11 wherein in order to be capable of frequency compensation, a MOS capacitor is connected between ground and each of the high impedance nodes (2, 3) capable of controlling the M branch (M11; M7) and a MOS capacitor is connected between ground and each of the high impedance nodes (1, 4) controlling the P branch (M5, M12).

18. The circuit of claim 11 wherein all regulation loops share the four high impedance nodes (1, 2, 3, 4).

19. The circuit of claim 11 wherein the circuit is capable of an insertion of common mode regulation by being configured for imbalancing of the tail current of the differential second pair of NMOS transistors (M13/M14) of the intermediate stage.

20. The circuit of claim 11 wherein the class AB regulation is configured to feed back the feedback voltage (IQPFB) to an active load connected to the related high impedance nodes (1, 4) wherein the voltages of the related high impedance nodes (1, 4) will decrease and hereby decrease quiescent currents in the high side transistor (M12) and the low side transitor (M5) of the P branch, in the second NMOS transistor (M8) of the first pair of NMOS transistors (M7/M8) and in the second PMOS transistor (M10) of the second pair of PMOS transistors (M9/M10); and is further configured to feed back the feedback voltage (IQFMB) to an active load connected to the related high impedance nodes (2, 3), wherein the voltages of the related high impedance nodes (2, 3) will decrease and hereby decrease quiescent currents in the high side transistor (M11) and the low side transitor (M6) of the M branch, in the first NMOS transistor (M7) of the first pair of NMOS transistors (M7/M8) and in the first PMOS transistor (M9) of the second pair of PMOS transistors (M9/M10).

21. The circuit of claim 11 wherein the circuit is capable of an adaptation to class-G operation by connecting a switched supply to a power stage.

Patentansprüche

1. Verfahren zum Erreichen eines Volldifferenzverstärkers, der im Class-AB-Modus arbeitet, umfassend eine Anordnung für eine Differentialtreiberzwischenstufe mit zum Steuern einer Differenzschleife, eine Gleichtaktregelung und eine Class-AB-Regelung, umfassend die folgenden Schritte:

(1) Bereitstellen eines voll differentiellen Verstärkers, der im Class-AB-Modus arbeitet und Anschlüsse für differentielle Eingangsfehlersignale Vip und Vim und für differentielle Ausgangssignale Vop und Vom umfasst, wobei Vop durch einen ersten Ausgangszweig (M12, M5) und Vom durch einen zweiten Ausgangszweig (M11, M6) erzeugt wird, wobei jeder Ausgangszweig eine Hochseiten- (M11, M12) und Niederseitenvorrichtungen (M6, M5) umfasst, wobei der Verstärker eine Ausgangsstufe und eine Zwischenstufe umfasst, welche die Eingangssignale verarbeitet;
dadurch gekennzeichnet, dass es die Schritte umfasst von:
(2) Aufteilen der Zwischenstufe in zwei einfache Differentialstufen, wobei eine erste (M1, M2) dieser Differentialstufen die Niederseitenvorrichtungen (M5, M6) und eine zweite Differentialstufe (M4, M3) die Hochseitenvorrichtungen (M11, M12) steuert und so eine Differentialausgangsregelung durch Einführung einer doppelten Differenzierung des Eingangsfehlersignals zur Unterstützung der Gleichtaktregelung ermöglicht, indem Steuersignale für einen ersten Transistor jedes der Ausgangszweige von einem Steuerweg für einen zweiten Transistor jedes der Ausgangszweige aufgeteilt werden;
(3) Reduzieren eines Gleichtaktfehlers durch Verringern der Spannungen Vop und Vom, wenn ein differentieller Gleichtakt (CMFB) höher ist als eine Gleichtaktreferenz (VREF), wobei ein Paar NMOS-Transistoren (M13/M14) den differentiellen Gleichtakt (CMFB) mit der Gleichtaktreferenz (VREF) vergleicht und den Gleichtaktfehler über die erste und zweite Differenzstufe reduziert; und
(4) Regeln von Ruheströmen beider Ausgangszweige innerhalb des Verstärkers durch Erfassen eines Stroms einer Vorrichtung (M5/M12, M6/M11) jedes Ausgangszweiges, der den kleinsten Strom führt, und Vergleichen mit einem internen Referenzstrom (IREF), um den Ruhestrom zu regeln, wobei die Regelung des Ruhestroms durch Rückführung eines Ergebnisses des Vergleichs des kleinsten Stroms jeder Vorrichtung (M5/M12, M6/M11) jedes Ausgangszweigs mit dem internen Referenzstrom (IREF) zu einer aktiven Last durchgeführt wird, die jeweils mit einem entsprechenden Ausgangszweig verbunden ist, wodurch Spannungen an entsprechenden Knoten jedes Ausgangszweigs verringert und somit die Ruhestromströme verringert werden.

2. Das Verfahren nach Anspruch 1, wobei der Verstärker als Audioverstärker arbeitet.

3. Das Verfahren nach Anspruch 1, wobei die Zwischenstufe in zwei einfache Differentialstufen aufgeteilt ist, wobei die eine (M1, M2) die Niederseitenvorrichtungen (M5, M6) und die andere (M3, M4) die Hochseitentransistoren (M11, M12) steuert, um so die Aufteilung der Steuersignale durchzuführen.

4. Das Verfahren nach Anspruch 1, wobei die Versorgungsspannung über eine VDD-Schiene der Endstufe und die Versorgung der Zwischenstufe aufgeteilt wird.

5. Das Verfahren nach Anspruch 4, wobei die Ausgangsstufe mit einem Spannungspegel von weniger als 1 V versorgt wird, während die Zwischenstufe noch von einer höheren Kernspannung versorgt werden kann.

6. Das Verfahren nach Anspruch 1, wobei das einfache Einfügen einer Gleichtaktregelung durch Ungleichgewicht des Deaktivierungsstromvon differentiellen Paaren der Zwischenstufe ermöglicht wird.

7. Das Verfahren nach Anspruch 1, wobei PSR im Audioband verbessert wird, indem die Rückführung der Stromversorgung durch Kompensationskondensatoren verhindert wird.

8. Das Verfahren nach Anspruch 1, wobei eine einfache Einführung der Class-AB-Regelung durch Verwendung von Rückkopplungen zu einer aktiven Last von Zwischenstufen-Differenzpaaren ermöglicht wird.

9. Das Verfahren nach Anspruch 1, wobei die Kompensation eines Hauptregelkreises die Stabilität eines Gleichtaktregelkreises und eines Klasse-AB-Regelkreises durch hochohmige Knoten (1, 2, 3, 4) des Regelkreises verbessert, wobei der gemeinsame Regelkreis und der Klasse-AB-Regelkreis gemeinsam genutzt werden.

10. Das Verfahren nach Anspruch 1, wobei eine Anpassung an den Klasse-G-Betrieb durch Anschließen einer geschalteten Stromversorgung an eine Leistungsstufe durchgeführt werden kann.

11. Eine Schaltung eines Volldifferenzverstärkers, der im Class AB-Modus arbeitet, umfassend:

- eine Differential-(Vom, Vop)-Ausgangsstufe, die einen P-Zweig (M12, M5) und einen M-Zweig (M1, M6) umfasst, wobei jeder Zweig einen Hochspannungstransistor (M1, M12) und einen Niederspannungstransistor (M6, M5) umfasst;
- eine differentielle Zwischenstufe, umfassend

  - ein erstes Paar PMOS-Transistoren (M4/M3), die einen ersten (M4) und einen zweiten (M3) PMOS-Transistor umfassen, in der Lage ist, ein differentielles Eingangsfehlersignal (vim/vip) zu verstärken, wobei jeder Transistor (M3/M4) in der Lage ist, ein Steuersignal für einen Korrespondenten des Hochspannungstransistors (M11/M12) zu erzeugen, wobei die Quellen beider Transistoren des ersten Paares von PMOS-Transistoren verbunden sind, wobei gesteuerte Stromquellen (21) zwischen jedem Drain des ersten Paares von PMOS-Transistoren (M4/M3) und Masse eingesetzt werden, wobei diese gesteuerten Stromquellen (21) konfiguriert sind, um durch Fehler gesteuert zu werden, die von Regelkreisen der Klasse AB zurückgeführt werden;
  - ein erstes Paar NMOS-Transistoren (M7/M8), wobei ein Gate jedes NMOS-Transistors (M7/M8) über einen entsprechenden hochohmigen Knoten (3, 4) mit einem Drain eines entsprechenden Transistors des ersten Paares von PMOS-Transistoren (M4/M3) und ein Drain jedes NMOS-Transistors (M7/M8) mit einem Drain und einem Gate eines entsprechenden PMOS-Transistors eines zweiten Paares von PMOS-Transistoren (M9/M10) verbunden ist;
  - wobei jedes Gate des zweiten Paares von PMOS-Transistoren (M9/M10) mit einem Gate einer entsprechenden Hochseiten-Vorrichtung (M11/M12) verbunden ist, die einen Stromspiegel bildet, wobei jeder der PMOS-Transistoren des zweiten Paares (M9/M10) von PMOS-Transistoren in einer gleichen Skala im Vergleich zum Hochseiten-Transistor verkleinert ist;

- ein drittes Paar PMOS-Transistoren (M1/M2), die einen ersten (M1) und einen zweiten (M2) PMOS-Transistor umfassen, die in der Lage ist, ein differentielles Eingangsfehlersignal (vim/vip) zu verstärken, wobei jeder Transistor (M1(M2) in der Lage ist, ein Treibersignal für einen entsprechenden Niederspannungstransistor (M5/M6) zu erzeugen, wobei die Quellen beider Transistoren des dritten Paares von PMOS-Transistoren (M1/M2) verbunden sind, wobei gesteuerte Stromquellen (21) zwischen jedem Drain des dritten Paares von PMOS-Transistoren (M1/M2) und der Masse eingesetzt werden, wobei diese gesteuerten Stromquellen (21) konfiguriert sind, um durch Fehler gesteuert zu werden, die von den Regelkreisen der Klasse AB zurückgeführt werden;
- eine Differentialschleifen-Steuerschaltung, die eine doppelte Differenzierung des Differentialspannungsfehlers (vip-vim) durch Aufteilen der Differentialzwischenstufe in zwei Differentialstufen umfasst, wobei eine erste Differentialstufe die Niedertransistoren (M5, M6) durch das dritte Paar PMOS-Transistoren steuert, wobei die Gates des dritten Paares von PMOS-Transistoren jeweils mit den Eingangssignalen vip oder vim verbunden sind und wobei die Gates der niederseitigen Transistoren (M5, M6) jeweils mit den Drains des dritten Paares von PMOS-Transistoren (M1/M2) der hochohmigen Knoten (1, 2) verbunden sind und wobei eine zweite Differenzstufe die hochseitigen Transistoren (M11, M12) durch das erste Paar PMOS-Transistoren (M4, M3) kontrolliert, wobei die Gates des ersten Paares PMOS-Transistoren (M4, M3) jeweils mit den Eingangssignalen vip oder vim verbunden sind, und wobei die Gates der Hochseiten-Transistoren (M11, M12) über die hochohmigen Knoten (3, 4) und einen ersten NMOS-Transistor (M7) des ersten Paares von NMOS-Transistoren (M7/M8) und einen ersten PMOS-Transistor (M9) des zweiten Paares von PMOS-Transistoren (M9/M10) oder jeweils über einen zweiten NMOS-Transistor (M8) des ersten Paares von NMOS-Transistoren (M7/M8) und einen zweiten PMOS-Transistor (M10) des zweiten Paares von PMOS-Transistoren (M9/M10) kontrolliert werden;

dadurch gekennzeichnet, dass es ferner umfasst:

  - eine Gleichtaktregelschleifenschaltung, umfassend:
  - das dritte Paar PMOS-Transistoren (M2/M1) parallel zu dem ersten Paar Transistoren (M4/M3), wobei jeder Transistor eines Paares des ersten (M4/M3) oder dritten Paares (M2/M1) von PMOS-Transistoren in

der Lage ist, jeweils einen Niederspannungstransistor (M5/M6) eines korrespondierenden Ausgangszweigs (P/M-Zweig) über einen jeweiligen hochohmigen Knoten (1,2) zu steuern, und jeder Transistor des anderen Paares des ersten (M4/M3) oder des dritten Paares (M2/M1) von PMOS-Transistoren in der Lage ist, jeweils eine Hochseiten-Vorrichtung (M11/M12) über den jeweiligen hochohmigen Knoten (3, 4) zu steuern, wobei die Quellen beider Transistoren des dritten PMOS-Paares (M1/M2) verbunden sind; und

- das zweite Paar NMOS-Transistoren (M13/M14), wobei ein Drain eines ersten Transistors (M13) des zweiten Paares von NMOS-Transistoren (M13/M14) mit den Quellen des ersten Paares von PMOS-Transistoren (M3/M4) verbunden ist, ein Gate des ersten Transistors (M13) mit einer erfassten Gleichtaktrückführung (CMFB) verbunden ist, eine Drain eines zweiten Transistors (M14) des zweiten Paares von NMOS-Transistoren (M13/M14) mit Quellen des dritten Paares von PMOS-Transistoren (M1/M2) verbunden ist, und ein Gate des zweiten Transistors (M14) mit einer Gleichtakt-Referenzspannung (VREF) verbunden ist; wobei die Frequenzkompensation der Differentialschleifen-Steuerschaltung und der Gleichtakt-Regelschaltung durch gemeinsame Nutzung der hochohmigen Knoten (1, 2, 3, 4) der Differentialschleifen-Steuerschaltung und der Gleichtakt-Regelschaltung erfolgt; und

- die Regelschleifenschaltungen der Klasse AB, wobei eine erste der Regelschleifenschaltungen der Klasse AB konfiguriert ist, um den hochohmigen Knoten (1, 4) eine Spannung (IQPFB) bereitzustellen, die zum Steuern des P-Zweigs (M12, M5) konfiguriert ist, wobei die Spannung (IQPFB) konfiguriert ist, um mit einem Ruhestromfehler des P-Zweigs (M12, M5) zu skalieren, wobei der Ruhestromfehler des P-Zweigs die Differenz des kleinsten Stroms der Ströme ist, die jeweils durch den

Hochspannungstransistor (M12) oder den Niederspannungstransistor (M5) des P-Zweigs fließen, verglichen mit einem internen Referenzstrom, um den kleinsten Strom zu regeln, indem die Gate-Treiber von M12/M5 über den hochohmigen Knoten 1 bzw. über den hochohmigen Knoten 4 und die Transistoren M8 und M10 in entgegengesetzter Phase moduliert werden, und wobei eine zweite der Regelschleifenschaltungen der Klasse AB konfiguriert ist, um eine Spannung (IQMFB) an die hochohmigen Knoten (2, 3) zu liefern, die konfiguriert sind, um den M-Zweig (M11, M6) zu steuern, wobei die Spannung (IQMFB) konfiguriert ist, um mit einem Ruhestromfehler des M-Zweigs (M12, M5) zu skalieren, wobei der Ruhestromfehler des M-Zweigs die Differenz des kleinsten Stroms der Ströme ist, die durch den Hochspannungstransistor (M11) oder den Niederspannungstransistor (M6) des M-Zweigs fließen, verglichen mit dem internen Referenzstrom, um den kleinsten Strom zu regeln, indem die Gate-Treiber von M11/M6 über den Hochimpedanzknoten 2 oder über den Hochimpedanzknoten 3 und die Transistoren M7 und M9 in entgegengesetzter Phase moduliert werden.

12. Die Schaltung nach Anspruch 11, wobei der Verstärker als Audioverstärker arbeitet.

13. Die Schaltung nach Anspruch 11, wobei die Ausgangsstufe konfiguriert ist, um mit einer Spannung von weniger als 1V versorgt zu werden.

14. Die Schaltung nach Anspruch 13, wobei die Zwischenstufe konfiguriert ist, um von einer Spannung versorgt zu werden, die höher ist als eine Versorgungsspannung der Endstufe.

15. Die Schaltung nach Anspruch 11, wobei die hochohmigen Knoten (1, 2, 3, 4) mit den hochohmigen Knoten der Gleichtaktregelschleife geteilt werden, was eine gemeinsame Frequenzkompensation beider Schleifen ermöglicht.

16. Die Schaltung nach Anspruch 11, wobei, um eine Frequenzkompensation zu ermöglichen, ein Kondensator (60, 61) zwischen dem M-Zweig (M11, M6) und jedem der hochohmigen Knoten (2, 3), die den M-Zweig steuern, und ein Kondensator (62, 69) zwischen dem P-Zweig (M5, M12) und jedem der hochohmigen Knoten (1, 4), der den P-Zweig (M5, M12) steuern kann, geschaltet ist.

17. Die Schaltung nach Anspruch 11, wobei, um eine Frequenzkompensation zu ermöglichen, ein MOS-Kondensator (60, 61) zwischen Masse und jedem der hochohmigen Knoten (2, 3), die den M-Zweig (M11; M7) steuern können, und ein Kondensator (62, 69) zwischen Masse und jedem der hochohmigen Knoten (1, 4), der den P-Zweig (M5, M12) steuert, geschaltet ist.

18. Die Schaltung nach Anspruch 11, wobei sich alle Regelkreise die vier hochohmigen Knoten (1, 2, 3, 4) teilen.

19. Die Schaltung nach Anspruch 11, wobei die Schaltung zum Einfügen einer Gleichtaktregelung durch Konfiguration zum Ungleichgewicht des Deaktivierungsstrom des differentiellen zweiten Paares von NMOS-Transistoren (M13/M14) der Zwischenstufe geeignet ist.

20. Die Schaltung nach Anspruch 11, wobei die Klasse AB-Regelung konfiguriert ist, um die Rückkopplungsspannung (IQPFB) an eine aktive Last zurückzuführen, die mit den zugehörigen hochohmigen Knoten (1, 4) verbunden ist, wobei die Spannungen der zugehörigen hochohmigen Knoten (1, 4) abnehmen und dadurch die Ruheströme in den Transistoren (M5 M8, M10 und M12) verringern,und ist ferner konfiguriert, um die Rückkopplungsspannung (IQFMB) auf eine aktive Last zurückzuführen, die mit den zugehörigen hochohmigen Knoten (2, 3) verbunden ist, wobei die Spannungen der zugehörigen hochohmigen Knoten (2, 3) abnehmen und dadurch die Ruheströme in den Transistoren (M6, M7, M9 und M11) abnehmen.

21. Die Schaltung nach Anspruch 11, wobei die Schaltung zu einer Anpassung an den Class-G-Betrieb durch Anschließen einer geschalteten Stromversorgung an eine Leistungsstufe fähig ist.

Revendications

1. Un procédé pour réaliser un amplificateur entièrement différentiel fonctionnant en mode de classe AB, comprenant une disposition pour un étage intermédiaire de commande différentielle pour commander une boucle différentielle, une régulation de mode commun et une régulation de classe AB, comprenant les étapes consistant à :

(1) fournir un amplificateur entièrement différentiel fonctionnant en classe AB comprenant des ports pour des signaux d'erreur d'entrée différentiels Vip et Vim et pour des signaux de sortie différentiels Vop et Vom, dans lequel Vop est généré par une première branche de sortie (M12, M5) d'un étage de sortie et Vom est généré par une seconde branche de sortie (M11, M6) de l'étage de sortie, dans lequel chacune des branches de sortie comporte des transistors de côté supérieur (M11, M12) et de côté inférieur (M6, M5), dans lequel l'amplificateur comporte un étage intermédiaire traitant les signaux d'entrée :
(2) séparer l'étage intermédiaire en deux étages différentiels simples, dans lequel un premier (M1, M2) de ces étages différentiels commande les transistors de côté inférieur (M5, M6) et un second étage différentiel (M3, M4) commande les transistors de côté supérieur (M11, M12), activant ainsi une régulation de sortie différentielle en introduisant une différentiation duale du signal d'erreur d'entrée pour supporter la régulation de mode commun en séparant les signaux de commande d'un premier transistor de chacune desdits branches de sortie à partir d'un chemin de commande d'un second transistor de chacune desdites branches de sortie ;
(3) réduire une erreur de mode commun en décroissant les deux tensions Vop et Vom si un mode commun de sortie différentielle (CMFB) est plus élevé qu'une référence de mode commun (VREF), dans lequel une paire de transistors NMOS (M13/M14) compare le mode commun différentiel (CMFB) avec la référence de mode commun (VREF) et réduit l'erreur de mode commun via lesdits premier et second étages différentiels ; et
(4) réguler les courants de repos des deux branches de sortie à l'intérieur de l'amplificateur en détectant un courant d'un transistor (M5/M12, M6/M11) de chaque branche de sortie conduisant le plus petit courant, comparant celui-ci avec un courant de référence interne (IREF) afin de réguler le courant de repos, dans lequel ladite régulation du courant de repos est effectuée par la connexion de chaque branche de sortie à une charge active respective et en ramenant un résultat de la comparaison du plus petit courant de chaque transistor (M5/M12, M6/M11) de chaque branche de sortie avec le courant de référence interne (IREF) vers les charges actives respectives, décroissant ainsi les tensions aux noeuds correspondant de chaque branche de sortie et décroissant ainsi les courants de repos.

2. Le procédé de la revendication 1 dans lequel l'amplificateur est un amplificateur audio.

3. Le procédé de la revendication 1 dans lequel l'étage intermédiaire est divisé en deux étages différentiels simples, l'un (M1, M2) commandant les transistors de côté inférieur (M5, M6) et l'autre (M3, M4) commandant les transistors de côté supérieur (M11, M12), réalisant ainsi ladite division des signaux de commande.

4. Le procédé de la revendication 1 dans lequel la tension d'alimentation est séparée entre un rail VDD de l'étage de sortie et une alimentation de l'étage intermédiaire.

5. Le procédé de la revendication 4 dans lequel l'étage de sortie est alimenté avec un niveau de tension inférieur à 1V, tandis que l'étage intermédiaire peut être encore alimenté à partir d'une tension supérieure.

6. Le procédé de la revendication 1 dans lequel est effectuée une insertion triviale d'une régulation de mode commun au moyen d'un déséquilibre du courant de rail des paires différentielles.

7. Le procédé de la revendication 1 dans lequel dans lequel PSR au sein de la bande audio est amélioré en empêchant une alimentation en avance au travers de capacités de compensation.

8. Le procédé de la revendication 1 dans lequel est effectuée une insertion triviale d'une régulation de classe AB au moyen d'une utilisation d'une rétroaction vers une charge active de paires différentielles d'un étage intermédiaire.

9. Le procédé de la revendication 1 dans lequel une compension de la boucle de régulation principale augmente la stabilité d'une boucle de régulation en mode commun et d'une boucle de régulation en classe AB au moyen de noeuds de haute impédance (1, 2, 3, 4) de la boucle de régulation, la boucle de régulation commune, et la boucle de régulation de classe AB étant partagées.

10. Le procédé de la revendication 1 dans lequel une adaptation vers un fonctionnement en classe G peut être réalisé en connecté une alimentation commutée à un étage de puissance.

11. Un circuit d'un amplificateur entièrement différentiel fonctionnant en classe AB, comprenant :

- un étage de sortie différentiel (Vom, Vop) comprenant une branche P (M12, M5) et une branche M (M11, M6), dans lequel chacune des branches P et M comporte un transistor de côté supérieur (M11, M12) et un transistor de côté inférieur (M6, M5);
- un étage intermédiaire différentiel comprenant

  - une première paire de transistors PMOS (M3/M4) comprenant un premier (M3) et un second (M4) transistor PMOS, qui est capable d'amplifier un signal d'erreur d'entrée différentiel (vip/vim), dans lequel chaque transistor (M3/M4) est capable de générer un signal de commande pour un transistor correspondant parmi lesdits transistors de côté supérieur (M11/M12), dans lequel les sources des deux transistors de la première paire de transistor PMOS sont connectées, dans lequel des sources de courant commandées (21) sont déployées entre chaque drain des transistors de la première paire de transistors PMOS (M3/M4) et la terre, dans lequel ces sources de courant commandées (21) sont configurées pour être commandées par des erreurs rapportées par des circuits de la boucle de régulation AB ;
  - une première paire de transistors NMOS (M7/M8) dans laquelle une grille de chaque transistors NMOS (M7/M8) est connectée via un noeud de haute impédance correspondant (3, 4) vers un drain d'un transistor correspondant de la première paire de transistors PMOS (M3/M4) et un drain de chaque transistor NMOS (M7/M8) est connecté à un drain et une grille d'un transistor PMOS correspondant d'une seconde paire de transistors PMOS (M9/M10);
  - ladite seconde paire de transistors PMOS (M9/M10), dans laquelle chaque grille de la seconde paire de transistors PMOS (M9/M10) est connectée à une grille d'un transistor de côté supérieur correspondant (M11/M12) formant un miroir de courant,
  dans lequel chaque transistors PMOS de la seconde paire (M9/M10) de transistors PMOS est réduite suivant une même échelle relative du transistor de côté supérieur ;
  - une troisième paire de transistors PMOS (M1/M2) comprenant un premier (M1) et un second (M2) transistor PMOS, qui est capable d'amplifier le signal d'erreur d'entrée différentiel (vip/vim) dans lequel chaque transistor (M1 :M2) est capable de générer un signal de commande pour un desdits transistors de côté inférieur correspondant (M5/M6), dans lequel les sources des deux transistors de la troisième paire de transistors PMOS (M1/M2) sont connectées, dans lequel des sources de courant commandées (21) sont déployées entre chaque drain des transistors de la troisième paire de transistors PMOS (M1/M2) et la terre,
  dans lequel ces sources de courant commandées (21) sont configurées pour être commandées par des erreurs ramenées par rétroaction des circuits de la boucle de régulation de classe AB ;
  - un circuit de commande de boucle différentielle comprenant une différentiation duale du signal d'erreur d'entrée différentiel (vip/vim) en séparant l'étage intermédiaire différentiel en deux étages différentiels, dans lequel un premier étage différentiel commande les transistors de côté inférieur (M5, M6) au moyen de la troisième paire de transistors PMOS (M1/M2), dans lequel les grilles des transistors de la troisième paire de transistors PMOS (M1/M2) sont respectivement connectées aux signaux d'entrée vip et vim du signal d'erreur d'entrée différentiel (vip/vim) et dans lequel les grilles des transistors de côté inférieur (M5, M6) sont respectivement connectées aux drains des transistors de la troisième paire de transistors PMOS (M1/M2) via un noeud à haute impédance correspondant (1, 2) et dans lequel un second étage différentiel commande les transistors de côté supérieur (M11 /M12) au moyen de la première paire de transistors PMOS (M3/M4), dans lequel les grilles des transistors de la première paire de transistors PMOS (M3/M4) sont respectivement connectées aux signaux d'entrée vip et vim du signal d'erreur d'entrée différentiel

(vip/vim) et dans lequel les grilles des transistors de côté supérieur (M11/M12) sont commandées via les noeuds à haute impédance (3, 4) et un premier transistor NMOS (M7) de la première paire de transistors NMOS (M7/M8) et un premier transistor PMOS (M9) de la seconde paire de transistors NMOS (M9/M10) ou respectivement via un second transistor NMOS (M8) de la première paire de transistors NMOS (M7/M8) et un second transistor PMOS (M10) de la seconde paire de transistors PMOS (M9/M10) ;

- un circuit de boucle de régulation de mode commun comprenant :
- la troisième paire de transistors PMOS (M1/M2) en parallèle à ladite première paire de transistors PMOS (M3/M4), dans lequel chaque transistor de la troisième paire (M1/M2) de transistors PMOS est capable de commander respectivement l'un desdits transistors de côté inférieur (M5/M6) de la branche de sortie correspondante (branche P/M) via le noeud à haute impédance respectif (1, 2) et chaque transistor de la première paire (M3/M4) de transistors PMOS est capable de commander respectivement une desdits transistors de côté supérieur de la branche de sortie correspondante (branche P/M) (M11/M12) via le noeud à haute impédance respectif (3, 4) dans lequel les sources des deux transistors de la troisième paire de transistors PMOS (M1/M2) sont connectées, et
- une seconde paire de transistors NMOS (M13/M14), dans laquelle un drain d'un premier transistor (M13) de la seconde paire de transistors NMOS (M13/M14) est connecté aux sources des transistors de la première paire de transistors PMOS (M3/M4), une grille du premier transistor (M13) est connectée à un retour en mode commun (CMFB) détecté, un drain d'un second transistor (M14) de la seconde paire de transistors NMOS (M13/M14) est connecté aux sources des transistors de la troisième paire de transistors PMOS (M1/M2), et une grille du second transistor (M14) est connectée au potentiel de référence de mode commun (VREF) ;

dans lequel une compensation de fréquence du circuit de commande de boucle différentielle et du circuit de régulation du mode commun est partagé au moyen d'un partage des noeuds à haute impédance (1, 2, 3, 4) du circuit de commande de boucle différentielle et du circuit de régulation de mode commun ; et

- lesdits circuits de boucle de régulation de classe AB, dans lequel un premier circuit parmi lesdits circuits de boucle de régulation de classe AB est configuré pour fournir une tension (IQPFB) aux noeuds à haute impédance (1, 4) configurés pour commander la branche P (M12, M5), dans lequel la tension (IQPFB) est configurée pour ramener à l'échelle une erreur de courant de repos de la branche P (M12, M5), dans lequel l'erreur de courant de repos de la branche P est la différent du plus petit courant parmi les courants s'écoulant respectivement au travers le transistor de côté supérieur (M12) ou le transistor de côté inférieur (M5) de la branche P en comparaison avec un courant de référence interne,

afin de réguler le plus petit courant au moyen d'une modulation en opposition de phase, la grille commande le transistor de côté supérieur (M12) et le transistor de côté inférieur (M5) de la branche P via lesdits noeuds à haute impédance (4, 1) configurés pour commander la branche P et le second transistor NMOS (M8) de la première paire de transistors NMOS (M7/M8) et le second transistor PMOS (M10) de la seconde paire de transistor PMOS (M9/M10) ; et dans lequel un circuit parmi lesdits circuits de boucle de régulation de classe AB est configuré pour fournir une tension (IQMFB) aux noeuds à haute impédance (2, 3) configurés pour commander la branche M (M11, M6), dans lequel la tension (IQMFB) est configurée pour ramener à l'échelle une erreur de courant de repos de la branche M (M12, M5), dans lequel l'erreur de courant de repos de la branche M est la différence du plus petit courant parmi les courants s'écoulant via le transistor de côté supérieur (M11) ou le transistor de côté inférieur (M6) de la branche M en comparaison avec le courant de référence interne,

afin de réguler le plus petit courant par une modulation en opposition de phase, la grille commande le transistor de côté supérieur (M11) et le transistor de côté inférieur (M6) de la branche M via lesdits noeuds à haute impédance (3, 2) configurés pour commander la branche M et le premier transistor NMOS (M7) de la première paire de transistors NMOS (M7/M8) et le premier transistor PMOS (M9) de la seconde paire de transistors PMOS (M9 /M10).

12. Le circuit de la revendication 11 dans lequel l'amplificateur fonctionne en tant qu'amplificateur audio.

13. Le circuit de la revendication 11 dans lequel l'étage de sortie est configuré pour être alimenté par une tension inférieure à 1 volt.

14. Le circuit de la revendication 11 dans lequel l'étage intermédiaire est configuré pour être alimenté par une tension qui est supérieure à une tension d'alimentation de l'étage de sortie.

15. Le circuit de la revendication 11 dans lequel les noeuds à haute impédance (1, 2, 3, 4) sont partagés avec les noeuds à haute impédance de la boucle de régulation en mode commun permettant le partage de la compensation de fréquence des deux boucles.

16. Le circuit de la revendication 11 dans lequel, afin de permettre la compensation de fréquence, une capacité (60, 61) est connectée entre la branche M (M11, M6) et chacun des noeuds à haute impédance (2, 3) commandant la branche M et une capacité (62, 69) est connectée entre la branche P (M5, M12) et chacun des noeuds à haute impédance (1, 4) capable de commander la branche P (M5, M12).

17. Le circuit de la revendication 11 dans lequel, afin de permettre la compensation de fréquence, une capacité MOS est connectée entre la terre et chaque noeuds à haute impédance (2, 3) capable de commander la branche M (M11 ; M7) et une capacité MOS est connectée entre la terre et chacun des noeuds à haute impédance (1, 4) commandant la branche P (M5, M12).

18. Le circuit de la revendication 11 dans lequel toutes les boucles de régulation partagent les quatres noeuds à haute impédance (1, 2, 3, 4).

19. Le circuit de la revendication 11 dans lequel le circuit est capable d'une insertion d'une régulation en mode commun en étant configuré pour un déséquilibre du courant de queue de la seconde paire différentielle de transistors NMOS (M13/M14) de l'étage intermédiaire.

20. Le circuit de la revendication 11 dans lequel dans lequel la régulation de classe AB est configurée pour ramener la tension de retour (IQPFB) à une charge active connectée aux noeuds à haute impédance relatifs (1, 4), dans lequel les tensions des noeuds à haute impédance relatifs (1, 4) décroissent et réduisent en conséquence les courants de repos du transistor de côté supérieur (M12) et du transistor de côté inférieur (M8) de la première paire de transistors NMOS (M7/M8) et dans le second transistor PMOS (M10) de la seconde paire de transistors PMOS (M9/M10) ;
et est en outre configuré pour ramener en retour le potentiel de retour (IQFMB) à une charge active connectée aux noeuds à haute impédance relatifs (2, 3), dans lequel les tensions des noeuds à haute impédance relatifs (2, 3) décroissent et ainsi réduisent les courants de repos dans le transistor de côté supérieur (M11) et le transistor de côté inférieur (M6) de la branche M, dans le premier transistor NMOS (M7) de la première paire de transistors NMOS (M7/M8) et dans le premier transistor PMOS (M9) de la seconde paire de transistors PMOS (M9/M10).

21. Le circuit de la revendication 11 dans lequel le circuit est capable d'adaptation à un fonctionnement en classe G via une connexion de l'étage de puissance à une alimentation commutée.

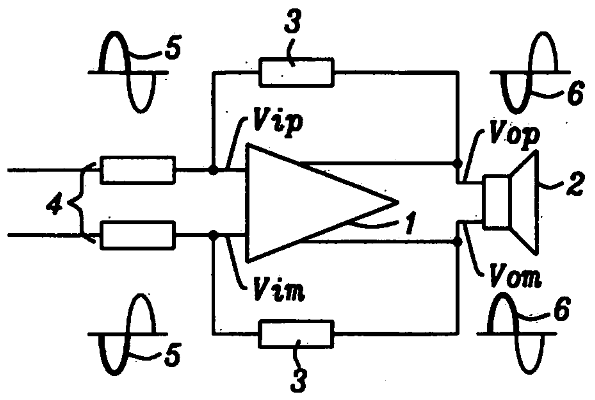
3
5
6
Vip
Vop
4
2
1
Vim
Vom
5
6
3

FIG. 1

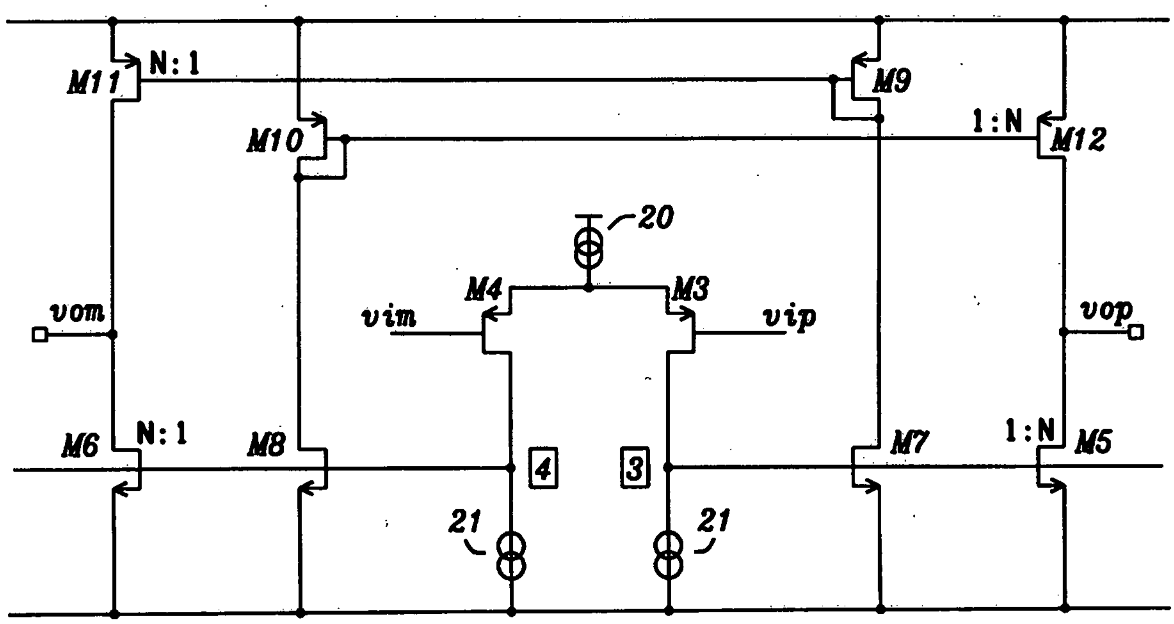
N:1
M11
M9
M10
1:N
M12
20
M4
M3
vim
vip
vom
vop
M6
N:1
M8
M7
1:N
M5
4
3
21
21

FIG. 2

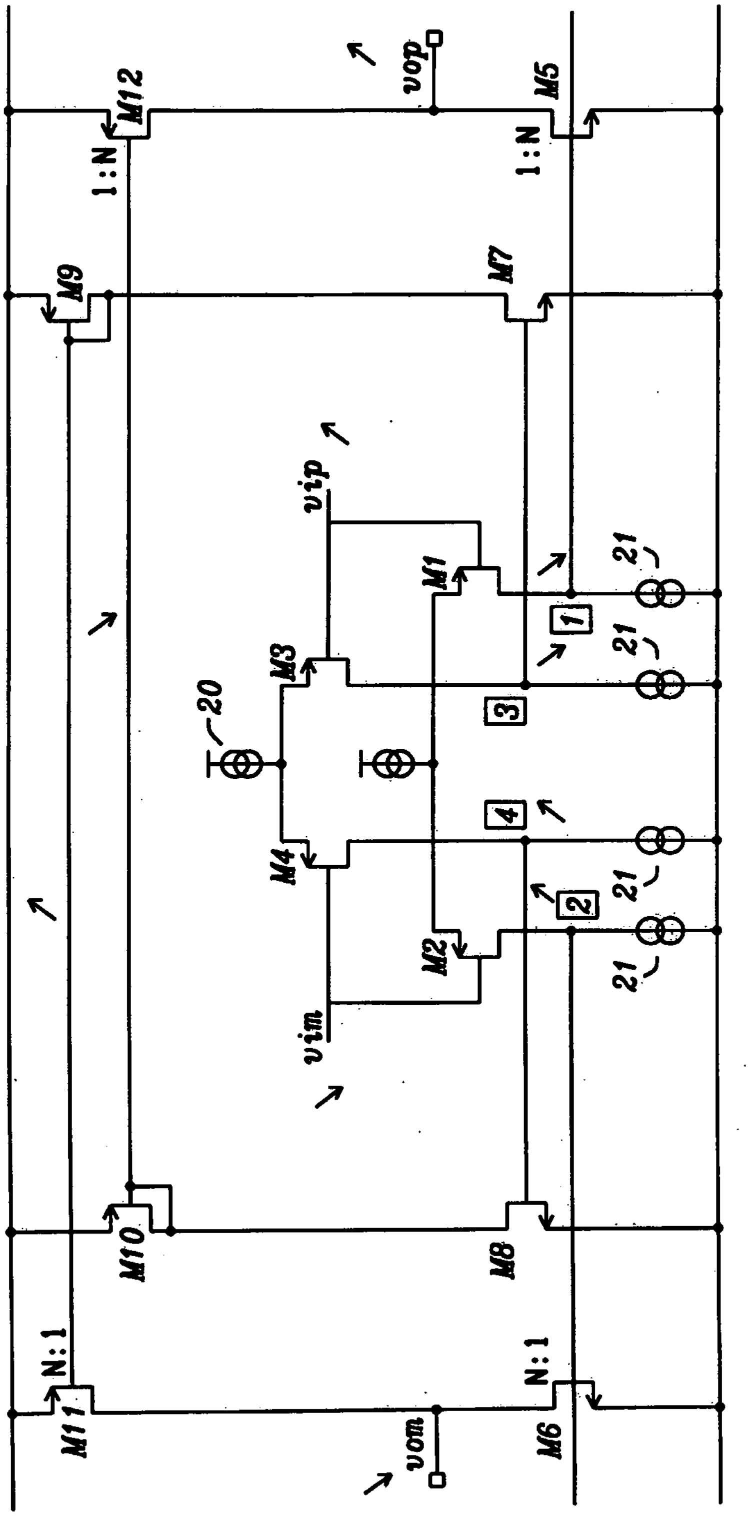
M12
1:N
M9
M7
M5
1:N
vop
vip
M1
M3
20
M4
M2
vim
21
21
21
21
1
3
4
2
M10
M8
N:1
M11
N:1
M6
vom

FIG. 3

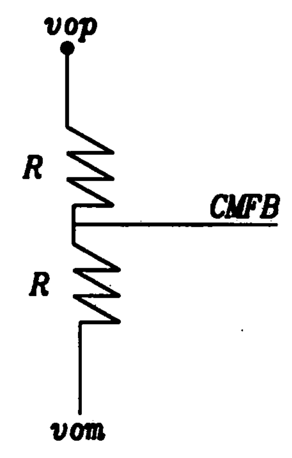
vop
R
CMFB
R
vom

FIG. 4a

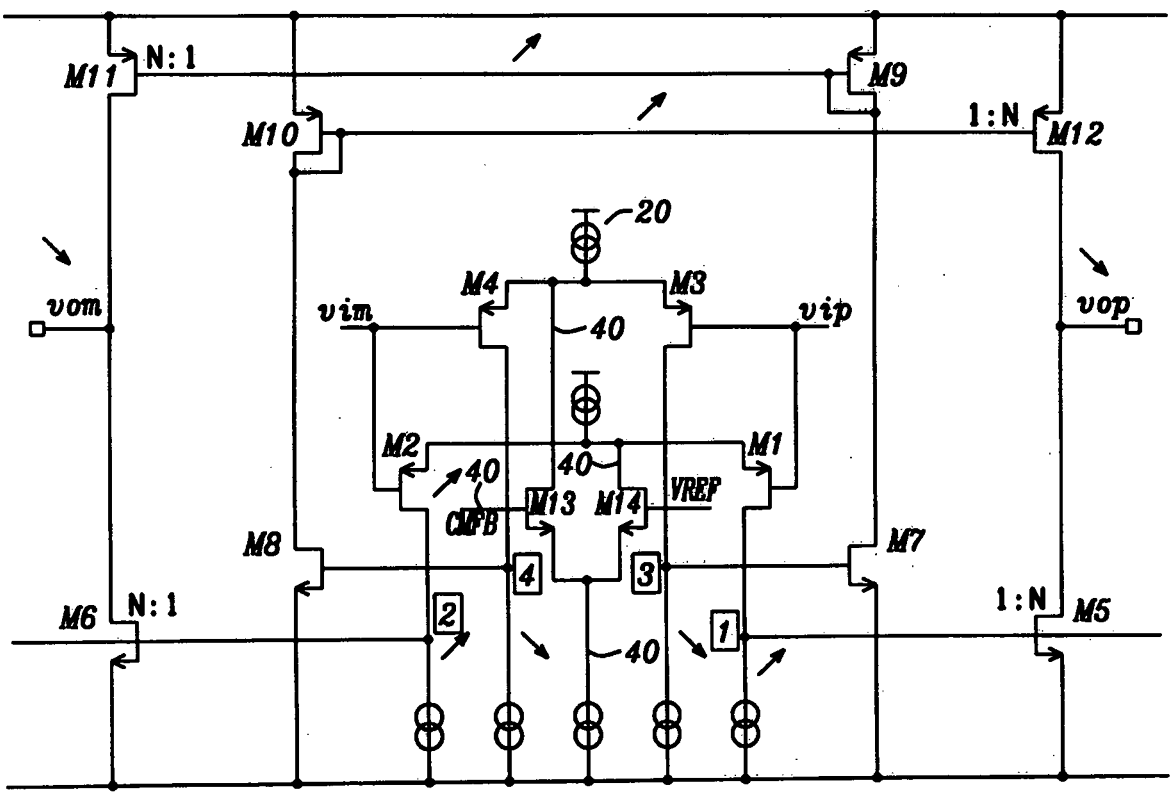
M11
N:1
M9
M10
1:N
M12
20
M4
M3
vim
40
vip
vom
vop
M2
M1
40
40
M13
M14
VREF
CMFB
M8
M7
4
3
M6
N:1
2
1
1:N
M5
40

FIG. 4b

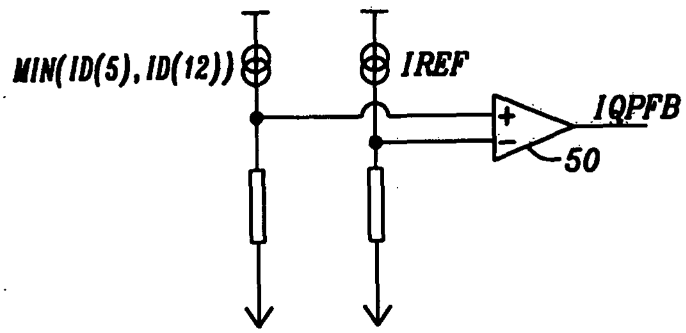
MIN(ID(5),ID(12))
IREF
IQPFB
50

FIG. 5a

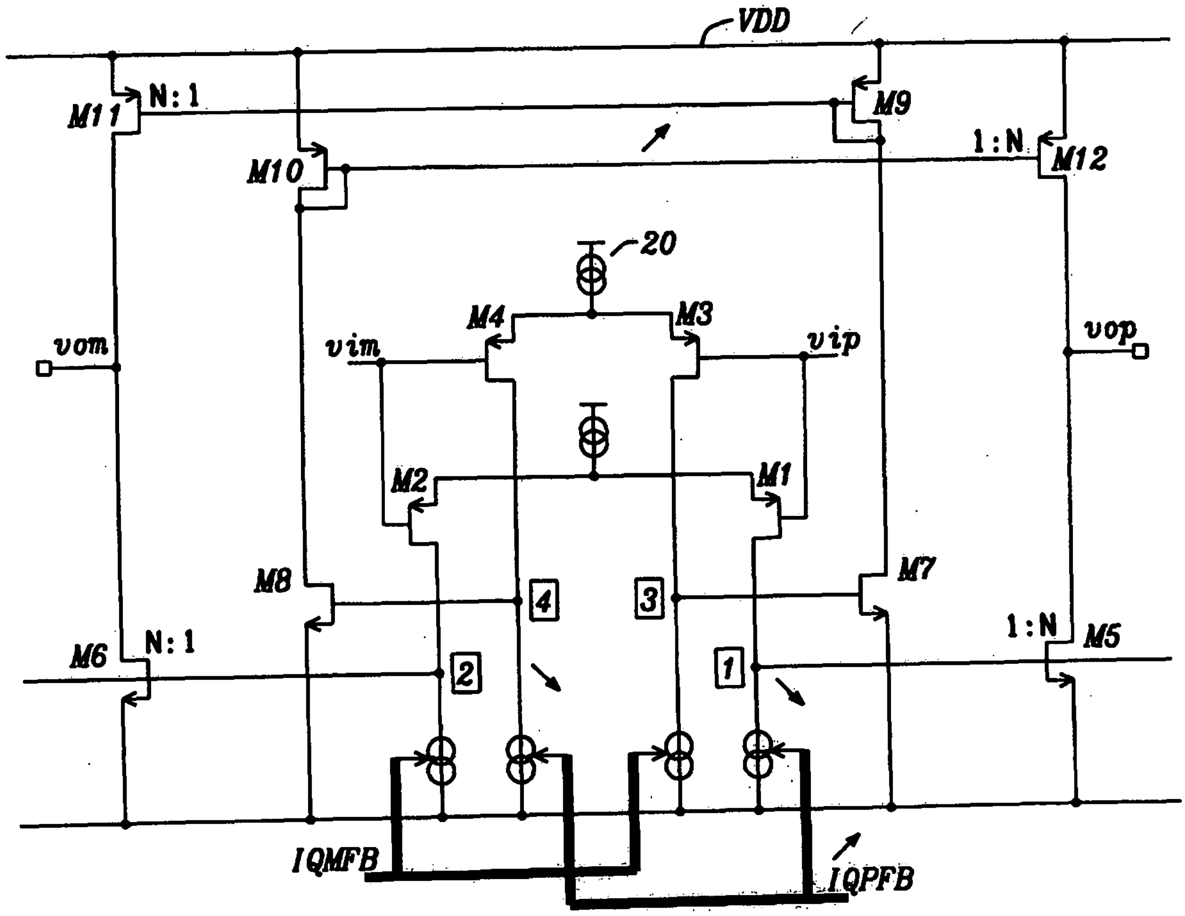
VDD
M11
N:1
M9
M10
1:N
M12
20
M4
M3
vom
vim
vip
vop
M2
M1
M8
M7
4
3
M6
N:1
1:N
M5
2
1
IQMFB
IQPFB

FIG. 5b

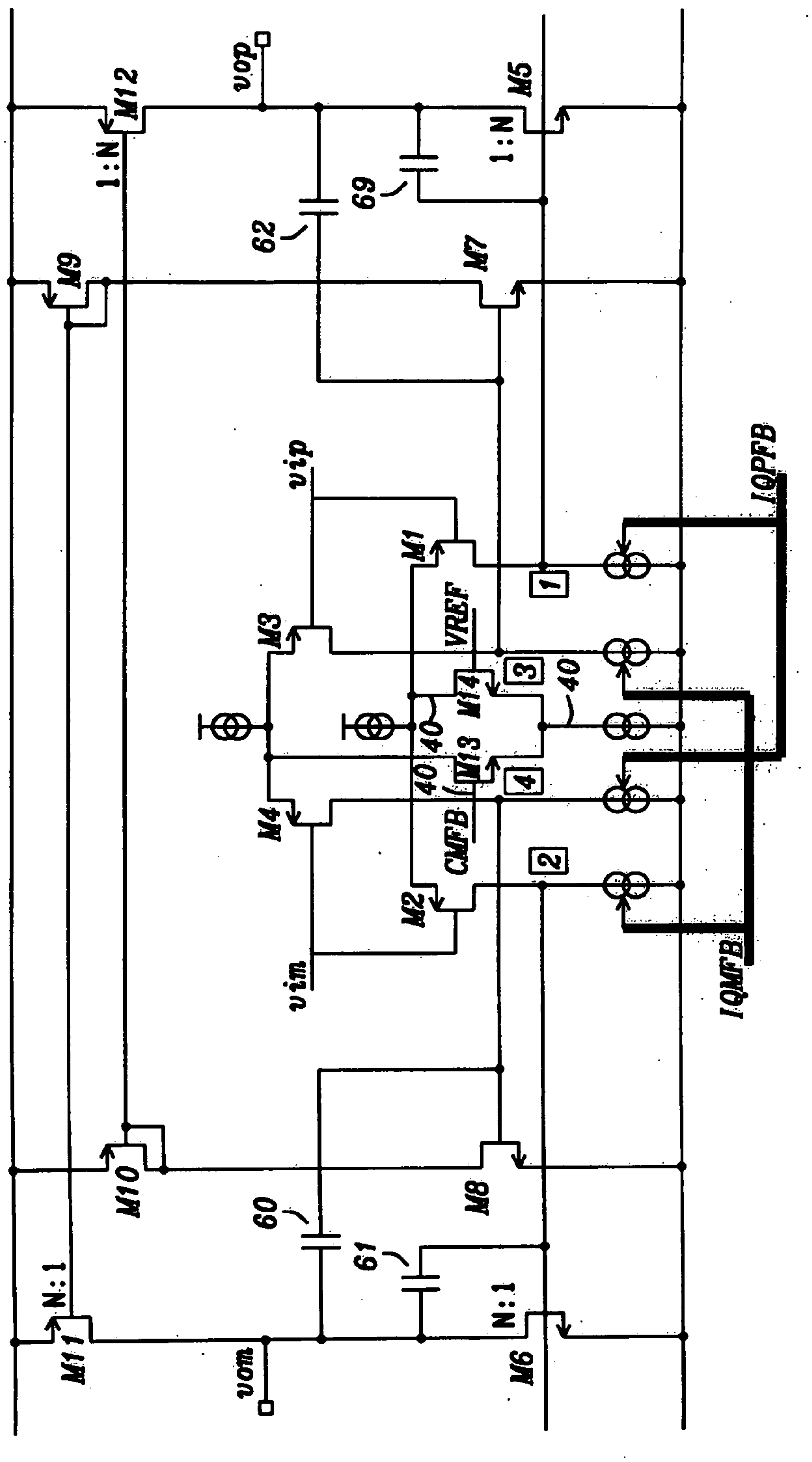
vop
M12
1:N
M5
1:N
69
62
M9
M7
vip
IQPFB
M1
M3
VREF
1
3
40
M14
40
M13
40
4
M4
CMFB
2
M2
vim
IQMFB
M10
M8
60
61
N:1
M11
N:1
M6
vom

FIG. 6

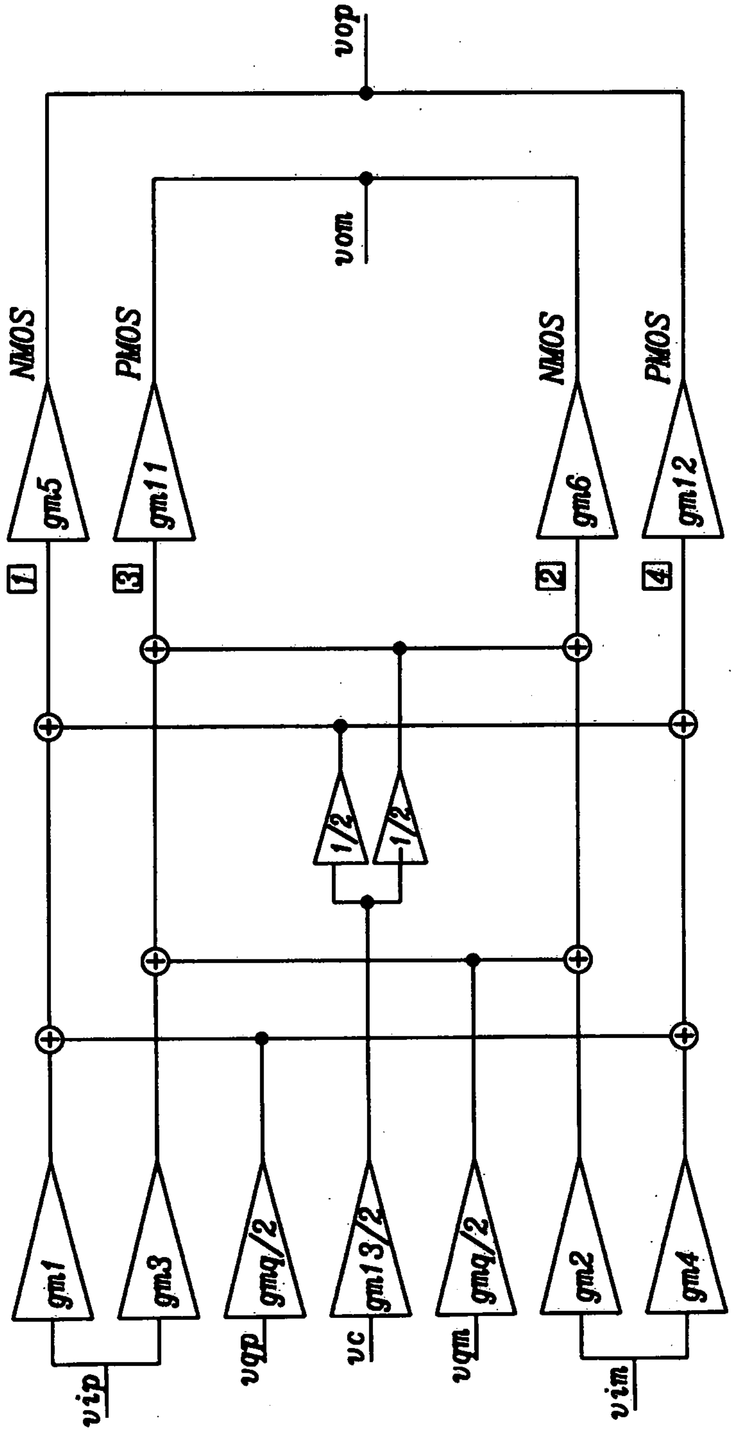
vop
vom
NMOS
PMOS
NMOS
PMOS
gm5
gm11
gm6
gm12
1
3
2
4
1/2
1/2
gm1
gm3
gmq/2
gm13/2
gmq/2
gm2
gm4
vip
vqp
vc
vqm
vim

FIG. 7

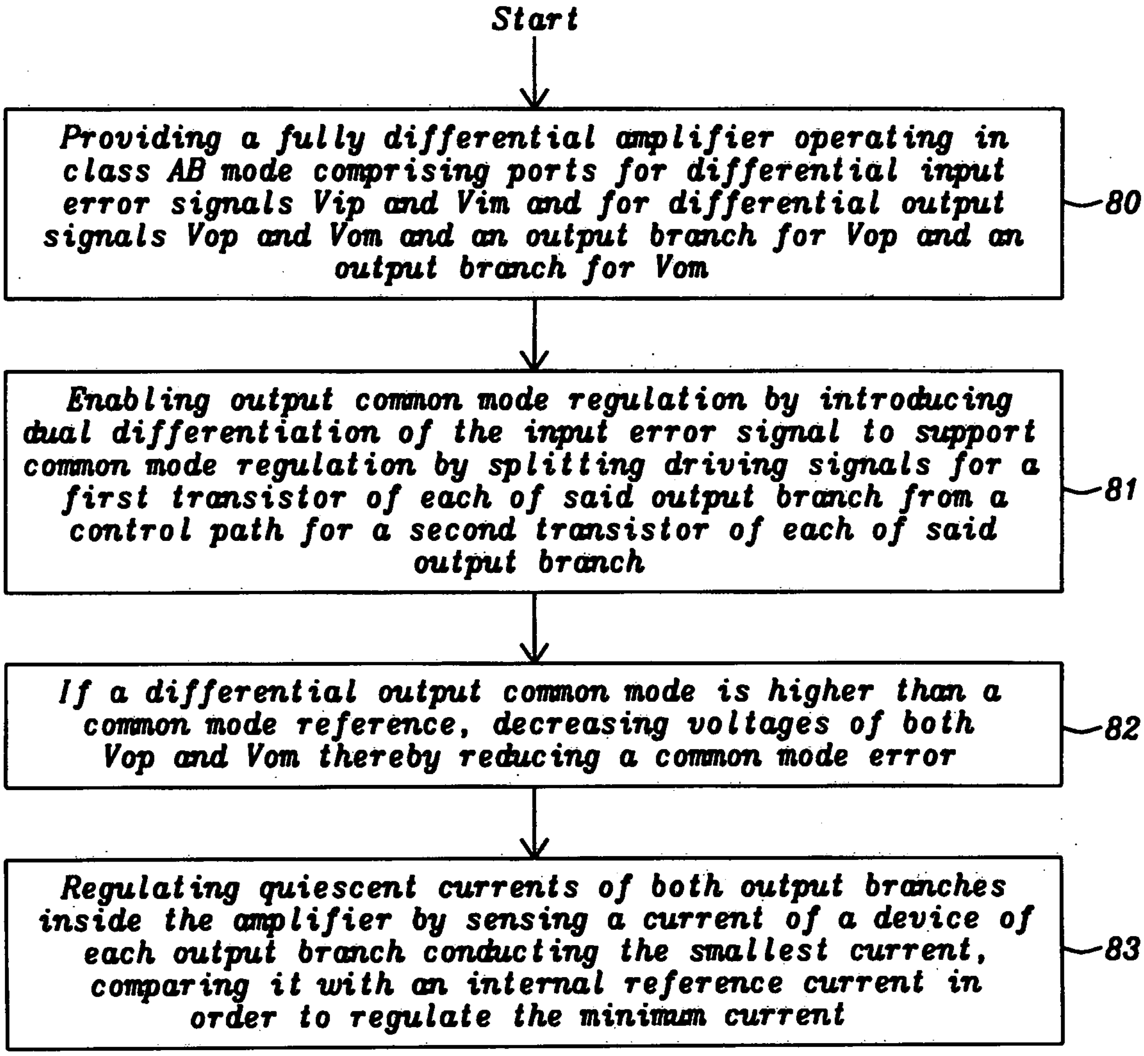
Start
Providing a fully differential amplifier operating in class AB mode comprising ports for differential input error signals Vip and Vim and for differential output signals Vop and Vom and an output branch for Vop and an output branch for Vom
80
Enabling output common mode regulation by introducing dual differentiation of the input error signal to support common mode regulation by splitting driving signals for a first transistor of each of said output branch from a control path for a second transistor of each of said output branch
81
If a differential output common mode is higher than a common mode reference, decreasing voltages of both Vop and Vom thereby reducing a common mode error
82
Regulating quiescent currents of both output branches inside the amplifier by sensing a current of a device of each output branch conducting the smallest current, comparing it with an internal reference current in order to regulate the minimum current
83

FIG. 8

REFERENCES CITED IN THE DESCRIPTION

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- WO 2009063276 A1 **[0011]**

Non-patent literature cited in the description

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- Power efficient fully differential low-voltage two stage class AB/AB op-amp architectures. **THOUTAM S et al.** PROCEEDINGS / 2004 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS: MAY 23 - 26, 2004, SHERATON VANCOUVER WALL CENTRE HOTEL. IEEE OPERATIONS CENTER, 23 May 2004, 1-733 **[0013]**
- A Very Low-Power Class AB/AB Op-amp based Sigma-Delta Modulator for Biomedical Applications. **LOPEZ-MORILLO E et al.** CIRCUITS AND SYSTEMS, 2006. MWSCAS '06.49TH IEEE INTERNATIONAL MIDWES T SYMPOSIUM ON. IEEE, 01 August 2006, 458-462 **[0014]**