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(54) **BATTERY PACK SYSTEM**

BATTERIEPACKSYSTEM

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## Description

### TECHNICAL FIELD

**[0001]** This disclosure relates to the field of battery pack systems. In some embodiments, it relates to electric vehicle (EV) battery pack systems and also EV power train systems.

### BACKGROUND

**[0002]** An EV battery pack typically includes several battery modules, each comprised out of several batteries (e.g., several single cell batteries), that are packed into a hardened package. The specification of the battery pack is determined by the car manufacturer and takes into consideration the extreme needs of the engine and the expected environmental conditions. Thus the specification usually calls for extra battery modules and/or for extra material, such as electrolyte, to be added to the cells to compensate for production faults and degradation of the batteries over time. Additionally, EV battery packs have a fixed current and voltage output.

**[0003]** Because electric engines need high current in order to produce high torque and high voltage to produce high speed, the engine's demands from the battery pack change over time as the car goes from a state of high acceleration to a high speed state.

**[0004]** US 2010/261048 describes a reconfigurable framework for a large-scale battery system having a battery cell array.

### SUMMARY

**[0005]** Described herein is an improved battery pack system. In one aspect, the improved battery pack system includes battery pack that includes a switching grid coupled to a main controller. In some embodiments, the switching grid includes a plurality of battery modules and a wiring structure that enables the controller to change the configuration of the batteries (e.g., cells) within the battery module and/or battery pack. This switching grid is used to change the output of the battery pack to fit the engine's current needs. The improved battery pack may be configured to take into consideration the concurrent state of each battery in the battery pack and environmental condition as well as the battery history information and the manufacturer recommendations.

**[0006]** In one particular aspect, a battery pack comprising: a main controller, and a plurality of switcher chips for use in interconnecting a set plurality of cells is provided. In some embodiments, each switcher chip comprises a switching control logic; and a communication circuit; the communication circuit comprising: a transmitter, and a receiver, wherein the receiver is communicatively connected in use to either the main controller or a transmitter of an adjacent switcher chip such that the receiver is operable to receive switching commands transmitted from

either the main controller or the transmitter of the adjacent switcher chip, and wherein the transmitter is for transmitting switching commands to another adjacent switcher chip.

**[0007]** The battery pack further comprising: a main negative terminal of a first switcher chip connected to a main positive terminal of a second switcher chip; a negative terminal of the first switcher chip; a main positive terminal of the first switcher chip connected to a main positive terminal of a third switcher chip; a positive terminal of a first switcher chip connected to a negative terminal of a fourth switcher chip; a plurality of cell terminals; and a plurality of switches.

**[0008]** The first switcher chip is configured such that: when a set of cells are connected to the first switcher chip via the plurality of cell terminals and a first set of the plurality of switches are closed and the remainder of the switches are open, the set of cells are connected in parallel with each other and current is able to flow through the set of cells and out of the main positive terminal but is not able to flow out of the positive terminal, when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a second set of the plurality of switches are closed and the remainder of the switches are open, the set of cells are connected in series with each other and current is able to flow through the set of cells and out of the main positive terminal but is not able to flow out the positive terminal, when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a third set of the plurality of switches are closed and the remainder of the switches are open, at least two of the cells in the set of cells are connected in series with each other and current is able to flow through the set of cells and out of the positive terminal but is not able to flow out the main positive terminal, when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a fourth set of the plurality of switches are closed and the remainder of the switches are open, a subset of the set of cells are connected in parallel with each other, at least one cell is electrically disconnected from each of the other cells, and current is able to flow through the set of cells and out of the main positive terminal but is not able to flow out the positive terminal, and when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a fifth set of the plurality of switches are closed and the remainder of the switches are open, a subset of the set of cells are connected in series with each other and at least one cell from the set is electrically disconnected from each of the other cells of the set.

**[0009]** In some embodiments, the switcher chips further comprise a command decoder configured to error check commands received by the communication circuit from the main controller or from another switcher chip and configured to block erroneous commands.

**[0010]** In some embodiments, the switcher chips further comprise the switching control logic connected to the command decoder and configured to convert com-

mands received by the communication circuit from the main controller into switch on-off commands for switching elements within the battery pack.

**[0011]** In some embodiments, the switcher chips further comprise a safety switching sequencer configured to receive the on-off commands from the switching control logic and configured to turn on or off at exact sequence and time one or more of the switches based on the received on-off commands.

**[0012]** In some embodiments, the switcher chips further comprise a slave input terminal; a master output terminal; the receiver being a slave communication module block; the transmitter being a master communication module block; a command decoder block; and a safety switching sequencer block.

**[0013]** In some embodiments, the plurality of switches comprises a plurality of power metal-oxide semiconductor field effect transistors (MOSFETs).

**[0014]** In another aspect, a battery apparatus is provided. In some embodiments, the battery apparatus comprises: a first switcher chip, a second switcher chip, a third switcher chip, and a fourth switcher chip; and each switcher chip comprising: a switching control logic, and a communication circuit, wherein the communication circuit comprises: a transmitter, and a receiver, wherein each receiver is communicatively connected in use to either a main controller or a transmitter of an adjacent switcher chip such that the receiver is operable to receive switching commands transmitted from either the main controller or the transmitter of the adjacent switcher chip, and wherein the transmitter is for transmitting switching commands to another adjacent switcher chip. The first switcher chip further comprising: a first plurality of switches, a first main positive terminal, a first main negative terminal, a first cascading positive terminal and a first cascading negative terminal; and a set of cells, the set of cells comprising: (i) a first cell having a positive terminal and a negative terminal, the positive terminal being connected to a first cell terminal of the first switcher chip and the negative terminal being connected to a second cell terminal of the first switcher chip, and (ii) a second cell having a positive terminal and a negative terminal, the positive terminal is connected to a third cell terminal of the first switcher chip and the negative terminal is connected to a fourth cell terminal of the first switcher chip, the second switcher chip further comprising: a second plurality of switches, a second main positive terminal and a second main negative terminal, the second main positive terminal of the second switcher chip being connected to the first main negative terminal of the first switcher chip; the third switcher chip (301a) comprising: a third plurality of switches, a third main positive terminal, a third main negative terminal, and a second negative terminal (581), the second negative terminal (581) of the third switcher chip (301a), being connected to the first positive terminal (582) of the first switcher chip (301b); and the fourth switcher chip (301) comprising: a fourth plurality of switches, a fourth main positive terminal and a fourth

main negative terminal, the fourth main positive terminal of the fourth switcher chip being connected to the first main positive terminal of the first switcher chip, wherein the first switcher chip is operable to: (i) configure the first plurality of switches such that (a) the cells are connected in series, (b) current is able to flow out of the first switcher chip via the first main positive terminal but is not able to flow out the first switcher chip via the first cascading positive terminal, and (c) current is able to flow into the first switcher chip via the first main negative terminal, (ii) configure the first plurality of switches such that (a) the cells are connected in series, (b) current is able to flow out of the first switcher chip via the first cascading positive terminal but is not able to flow out the first switcher chip via the first main positive terminal, and (c) current is able to flow into the first switcher chip via the first cascading negative terminal, and (iii) configure the switches such that (a) the cells are connected in parallel, (b) current is able to flow out of the first switcher chip via the first main positive terminal but is not able to flow out the first switcher chip via the first cascading positive terminal, and (c) current is able to flow into the first switcher chip via the first main negative terminal.

**[0015]** In some embodiments, each of the first, second, third, and fourth switcher chips further comprise: a command decoder configured to error check commands received by the communication circuit from the controller or from another switcher chip and configured to block erroneous commands. In some embodiments, each of the first, second, third, and fourth switcher chips further comprise: the switching control logic connected to the command decoder and configured to convert commands received by the communication circuit from the controller into switch on-off commands for switching elements within the battery module. In some embodiments, each of the first, second, third, and fourth switcher chips further comprise: a safety switching sequencer configured to receive the on-off commands from the switching control logic and configured to turn on or off at exact sequence and time one or more of the switches based on the received on-off commands.

**[0016]** In some embodiments, the first cell is a micro-cell and the second cell is a micro-cell. In some embodiments, the switcher chip controls less than seventeen single cell batteries but more than three single cell batteries. In some embodiments, each of the first, second, third, and fourth switcher chips control more than 7 single cell batteries and less than 13 single cell batteries.

**[0017]** In some embodiments, the battery apparatus comprises a battery pack that comprises: a first cluster of battery modules comprising a first column of battery modules and a second column of battery modules; a first circuit for connecting the first column of battery modules in parallel with the second column of battery modules; a second circuit for connecting the first column of battery modules in series with the second column of battery modules; a second cluster of battery modules comprising a third column of battery modules and a fourth column of

battery modules; a third circuit for connecting the third column of battery modules in parallel with the fourth column of battery modules; a fourth circuit for connecting the third column of battery modules in series with the fourth column of battery modules, wherein at least one of the battery modules in the first column has (i) a switch for connecting and disconnecting a main output of the battery module to the first circuit and (ii) a switch for connecting and disconnecting a cascading output of the battery module to the second circuit, at least one of the battery modules in the second column has (i) a switch for connecting and disconnecting a main output of the battery module to the first circuit and (ii) a switch for connecting and disconnecting a cascading output of the battery module to the second circuit, at least one of the battery modules in the third column has (i) a switch for connecting and disconnecting a main output of the battery module to the third circuit and (ii) a switch for connecting and disconnecting a cascading output of the battery module to the fourth circuit, and at least one of the battery modules in the fourth column has (i) a switch for connecting and disconnecting a main output of the battery module to the third circuit and (ii) a switch for connecting and disconnecting a cascading output of the battery module to the fourth circuit.

**[0018]** The controller may be operable to: (a) place the battery pack in a first mode of operation in which the battery pack produces a voltage  $V_1$ ; and (b) place the battery pack in second mode of operation in which the battery pack produces a voltage  $V_2$ , where  $V_2 > V_1$ .  $V_2$  may be greater than or equal to  $(n)(3.6)V_1$ , where  $n$  is greater than or equal to 1. In some embodiments, at least one of the battery modules comprises: a switcher chip comprising: a plurality of switches, a main positive terminal, a main negative terminal, a cascading positive terminal and a cascading negative terminal; and a set of cells comprising (i) a first cell having a positive terminal and a negative terminal, the positive terminal being connected to a first cell terminal of the switcher chip and the negative terminal being connected to a second cell terminal of the switcher chip, and (ii) a second cell having a positive terminal and a negative terminal, the positive terminal is connected to a third cell terminal of the switcher chip and the negative terminal is connected to a fourth cell terminal of the switcher chip.

**[0019]** In some embodiments, the controller is operable to: (i) cause the battery module to configure the switches such that (a) the cells are connected in series, (b) current is able to flow out of the switcher chip via the main positive terminal but is not able to flow out the switcher chip via the cascading positive terminal, and (c) current is able to flow into the switcher chip via the main negative terminal but is not able to flow into the switcher chip via the cascading negative terminal, (ii) cause the battery module to configure the switches such that (a) the cells are connected in series, (b) current is able to flow out of the switcher chip via the cascading positive terminal but is not able to flow out the switcher chip via

the main positive terminal, and (c) current is able to flow into the switcher chip via the cascading negative terminal but is not able to flow into the switcher chip via the main negative terminal, and (iii) cause the battery module to configure the switches such that (a) the cells are connected in parallel, (b) current is able to flow out of the switcher chip via the main positive terminal but is not able to flow out the switcher chip via the cascading positive terminal, and (c) current is able to flow into the switcher chip via the main negative terminal but is not able to flow into the switcher chip via the cascading negative terminal.

**[0020]** Other features are described below.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0021]**

FIG. 1 illustrates an example battery pack system according to some embodiments.

FIG. 2 illustrates further illustrates an example battery pack system and shows it being used in an vehicle having an electronic motor.

FIG. 3 illustrates an example battery pack according to some embodiments.

FIGs. 4-8 illustrate an example battery module according to some embodiments.

FIG. 9 illustrates another example battery pack according to some embodiments.

FIG. 10 illustrates another example battery module, according to some embodiments, that is based on a special dedicated chip.

FIG. 11 is a functional block diagram of a main controller according to some embodiments.

FIG. 12 illustrates an environment in which a battery pack system according to some embodiments may be used.

FIG. 13 illustrates a battery module according to another embodiment.

FIG. 14 illustrate a battery module according to still another embodiment.

## DETAILED DESCRIPTION OF EMBODIMENTS

**[0022]** Conventional battery pack systems comprise a moderate numbers of batteries and a number of controllers, each of which monitors a group of the batteries (e.g., 10 of the batteries) for safety reasons mostly. Such a controller senses the voltage, temperature, and current of each battery in the group and, during the regular operation of the battery pack, levels the amount of charge in each battery by discharging batteries that are overcharged. In the case of an emergency (e.g., when the temperature or voltage of a certain cell reaches a predefined value), the controller sends a signals to an aggregator controller that than shuts off a main power switch to disconnect the battery pack from the electric engine. This mechanism is fine for the sake of safety but does not apply to the other parameters needed from the battery

pack.

**[0023]** It is well known in the industry that the nominal voltage of a cell is determined by the cell chemistry which is the electrochemical parameters of the chemicals used for the production. But when used, the actual voltage on the cell terminals changes over time and depends of various parameters that affect the internal impedance of the cells, like the ambient temperature, the state of charge of the cells, the age of the cell, as well as the actual load current.

**[0024]** In the case of EV batteries packs, the use of Li-ion is the most common and the nominal voltage value of each cell is 3.6V. Electric engines are commonly used in many transportation vehicles like trains and submarines, these engines are very efficient and produce gradable power depending on the voltage and current provided to them. The voltage and current range is in the order of hundreds, the voltage affects the rotation speed of the motor while the current determines the Torque. The power of the motor in horse power is positive proportional to the multiplication of the rotation speed by the Torque.

**[0025]** In order to reach the range of hundreds of volts, tens of cells are connected in series and then tens of chains are connected in parallel to support the peak current provisioning. Since the cells are manufactured in a relatively large capacity, if a certain cell is malfunctioning the effect on the whole battery pack performance is significant. Moreover, because the battery pack structure is fixed and predefined, this malfunctioning cell cannot be electrically excluded from the battery pack structure even though its impact on the power performance of the battery can be negative.

**[0026]** This adds to the fact that the battery parameters are changing over time and with regards to the environmental and use conditions and since the structure is predetermined and fixed in the production process it needs to be compensated by additional material in the cells that are connected in a non optimal fixed configuration. In practice, this fact leads the EV battery manufacturers to assign more than 60% more capacity in the battery pack design and manufacturing to overcome the discussed problems

**[0027]** Referring now to FIG. 1, FIG. 1 is a diagram illustrating a battery pack system 100, according to some embodiments, which overcomes at least some of the deficiencies of conventional battery pack systems.

**[0028]** As shown in FIG. 1, battery pack system 100 includes a battery pack 104, which includes (i) several batteries 101 (e.g., several single cell batteries - which we shall refer to as a "cell") and (ii) a battery switching grid 102 (a.k.a., "3D Battery Switching Grid™"302) that enables the connection of the cells 101 in various different modes. In some embodiments, the 3D Battery Switching Grid includes a plurality of low cost chips (a.k.a., "switcher chips"), each of which is responsible for configuring a particular subset of the cells of the battery pack and each of which contains a set of switches con-

nected to the particular subset of cells and circuit logic for controlling the switches. Battery pack system 100 may further include a main controller 106 (a.k.a., EV Processor™) that monitors the state of each cell by its sensing the cell's specific parameters (e.g., state of charge, voltage, current, temperature, pressure etc.) and controls the switching grid based on, at least in part, the current needs of the engine and the sensed parameters. The controller may also take into account the usage history of the cells, the manufacturer motor behavior diagrams, and driver history and desires. Accordingly, battery pack system 100 enables more efficient power utilization of the cells, increases safety, and provides the best suited power source for different motors and for the current needs of that motor based on the driver's behavior and directions and the driving environment. In some embodiments, the EV Processor incorporated within battery pack 104.

**[0029]** In some embodiments, as shown in FIG. 1, the battery pack system 100 includes a number of cells that are each monitored separately and can be electrically interconnected in various modes (e.g., parallel, serial or any other structure) during the usage by the car engine and during the charge time. This way in which the cells are electrically interconnected may be changed periodically by the EV Processor to best match the actual needs of the car (e.g., if high torque is needed the battery system can be configured to provide a maximum amount of current. The specific configuration of each cell is determined by its current status, its history and the current task being performed as well as environmental conditions.

**[0030]** For example, if the battery pack system 100 needs to perform in low temperature conditions more cells can be connected in series to compensate for the degraded voltage contribution of each cell. This method is also applicable for compensating of degradation in time. As another example, if a certain cell is malfunctioning, the malfunctioning cell may be electrically excluded from the battery pack structure and the negative effect of its fault will be prevented.

**[0031]** In some embodiments, the cells may be relatively small (e.g., the cells may have a relatively small capacity - such as 2Ah v. 20Ah, for example), in which case they may be referred to as micro-cells. With the use of micro-cells management tasks can be done at adequate granularity and the battery manufacturer can design the battery in a much more optimal manner and can then reach higher power capacity and better performance over time for the same weight and volume. Another advantage of using micro-cells is that because they are smaller they can be used more cycles and the heat dissipation from them is better.

**[0032]** An EV battery pack is a fairly large object that consumes significant car space and weight. There is a tradeoff in the design of a battery pack between energy capacity, space and weight - for the sake of more energy you would want to enlarge the battery pack, but this cost a lot in expensive material, space consumed in the car

and additional car weight. Conventional battery packs are designed for providing the maximum voltage and current needed for the electric engine used and the energy capacity needed between charges and for the sake of the battery lifetime.

**[0033]** Since most EV battery packs today are made using Li-ion battery cells the cells need to be monitored for overheating and over charging or else a cell might explode. A battery cell that reaches 4.2v or a designated temperature given by the manufacturer is considered dangerous and provokes shut down of the main battery switch immediately causing the car to stand aside. This mode of operation is essential to the ability of using Li-ion in cars.

**[0034]** An improvement on conventional battery pack design is to add a switching grid (a.k.a., 3D Battery Switching Grid™) that will be comprised of multiple instantiations of a single low cost chip that enables controller 106 to manage each cell in the battery pack separately. Referring now to FIG. 2, FIG. 2 illustrates the 3D Switching Grid concept. As illustrated in FIG. 2, battery pack 104 includes not only a collection of cells 101, but also a collection of switches 202. As further illustrated in the embodiment shown in FIG. 2, at least two switches are present for each cell 101. In the example shown, switch 202a and switch 202b are used to either (1) connect cell 101a in series with other cells or (2) electrically disconnect cell 101a from all the other cells. Thus, each cell in battery pack 104 can be electrically included in the battery pack or electrically excluded from the battery pack.

**[0035]** The switching grid enables creating a structure that provides higher voltage, higher peak current or different cell order. It enables to charge the cells in different order and to use part or all of the cells in different utilization cases and by that optimizing the wear-out of the battery over the years. It will also enable to employ a safer use method because of the ability to temporarily or permanently electrically exclude malfunctioning cells from the pack 104 in an early stage of a problematic situation without the need to switch off the whole battery and stop the car.

**[0036]** Referring now to FIG. 3, FIG. 3 illustrates an example structure of battery pack 104 according to some embodiments. As shown in FIG. 3, the example battery pack 104 includes two clusters of battery modules 301. The first cluster (cluster 1) is made of two sets (or "columns") of M battery modules (col. 1a and col. 1b) and a cascade wire 585 that is used to connect col. 1a and col. 1b in series. Likewise, the second cluster (cluster 2) is made of two sets (or "columns") of M battery modules (col. 2a and col. 2b) and a cascade wire that is used to connect col. 2a and col. 2b in series. In the example shown in FIG. 3, M=3. In some embodiments, battery module 301 includes a set of cells (e.g., 4 cells, 8 cells, or some other number of cells) and a component of the switching grid 102 (e.g., one of the switcher chips mentioned above that contain a set of switches).

**[0037]** Depending on how switches within battery mod-

ules 301a and 301b are configured, col. 1a will either be in parallel with col. 1b or they will be in series. Likewise, depending on how switches within battery modules 301c and 301d are configured, col. 2a will either be in parallel with col. 2b or they will be in series. Thus, for each cluster, the columns of the cluster may be connected in parallel or in series. However, in the embodiment shown, no column of cluster 1 can be connected in series with a column of cluster 2. Accordingly, battery pack 104 may have at least two modes of operation: in one mode the columns in each cluster are connected in parallel and in another the columns in each cluster are connected in series. It is not required, however, that all columns in a cluster be connected in series or parallel. For example, with a cluster having four columns, the cluster may be configured such that columns 1 and 2 are in series thereby forming a first meta-column and columns 3 and 4 are in series thereby forming a second meta-column and the first meta-column is in parallel with the second meta-column. As described further herein, there may be yet additional modes of operation because each battery module 301 can be configured such that it produces  $V_a$  volts or  $V_b$  volts depending on whether the cells of the battery module are connected in series or parallel. If each battery module produces  $V_i$  volts (e.g.,  $V_a$  or  $V_b$ ) and the all the columns of each cluster are connected in parallel, then the battery pack 104 produces  $M \times V_i$  volts. However, if each battery module produces  $V_i$  volts and the columns within each cluster are connected in series, then the battery pack 104 produces  $B \times M \times V_a$  volts, where B is the number of columns in the cluster. As described herein, a main controller may configured battery pack 104 based on, for example, data regarding the needs of the engine and/or the environment. Thus, if the engine requires a high voltage, the main controller could send one or more commands to the battery pack that cause the battery pack to connect the columns within each cluster in series and/or the cells within each battery module in series. Likewise, if the engine requires a high peak current, the main controller could send one or more commands to the battery pack that cause the battery pack to connect the columns within each cluster in parallel and/or the cells within each battery module in parallel.

**[0038]** In the above structure, if one or several battery modules within the column are malfunctioning, then the influence of these battery modules on the whole pack can be trimmed by using switches within the battery module to bypass the battery modules temporarily or permanently. Another advantage of the above structure is that the energy capacity redundancy designed by the manufacturer can be spread wisely within the pack and can be utilized to provide more current or more voltage according to the actual needs of the engine in any given time.

**[0039]** Referring now to FIGs. 4-8, FIGs. 4-8 illustrate an example battery module 301, which includes four batteries c1, c2, c3, c4 (e.g., four micro-cells), a set of switches (s0 through s14), a main positive terminal 402, a main negative terminal 404, a cascading positive terminal 582,

and a cascading negative terminal 581. For simplicity, we shall refer to the batteries c1-c4 as cells with the understanding that the batteries are not limited to single-cell devices.

**[0040]** Switches s1-s4, s6-s8 and s10-s13 are used for interconnecting cells c1-c4, while switches s0, s5, s9 and s14 are used for cascading columns in a cluster. That is, switches s0, s5, s9 and s14 enable the battery module to connect in series with another battery module in a neighboring column of the same cluster. For instance, terminals 581 and 582 are each connected to a respective cascade wire. The other end of the cascade wire is connected to a corresponding cascade terminal in a battery module that is positioned in an adjacent column. For instance, as shown in FIG. 3, terminal 581 of module 301a is connected to wire 585 and the other end of the wire is connected to terminal 582 of module 301b. To connect col. 1a in series with col. 1b, then (A) module 301a is configured such that the following switches are closed s4-s8 and the others are open and (B) module 301b is configured such that the following switches are closed s6-s10 and the others are open

**[0041]** As illustrated in FIGs. 4-8, a battery module (components of which may be formed on a single chip) according to various embodiments of the invention is capable of switching C cells that can be connected in serial, parallel or excluded from the grid. For example, a battery module is capable of electrically connecting C cells in parallel or in series. As another example, for each one of the C cells, the battery module can electrically disconnect the cell from all of the other cells in the battery module. Accordingly, a battery module has responsibility for C cells of the battery pack.

**[0042]** Thus, if one or several cells within the module are malfunctioning, then the influence of these cells on the whole pack can be trimmed by using the switches within the battery module to bypass the cells temporarily or permanently. Another advantage of the above structure is that the energy capacity redundancy designed by the manufacturer can be spread wisely within the pack and can be utilized to provide more current or more voltage according to the actual needs of the engine in any given time.

**[0043]** As mentioned above, components of battery module 301 may be implemented as an integrated circuit or "microchip" ("chip" for short). That is, in some embodiments, battery module 301 comprises a chip and a set of cells connected to the chip. The chip is responsible for configuring the set of cells. For example, the chip is responsible for connecting the cells either in series with each other or in parallel with each other. The chip may include digital, analog and communication components. The chip may make use of a noise-resilient communication module that decreases possible control errors to the automotive levels needed as well as prevents unauthorized designers to make use of the module. In some embodiments, the chip uses Power FET technology for the switching elements enabling very low Rds-on that leads

to low self power dissipation needed for energy efficiency. The chip may also include a safety switching sequencer that manages the exact switching sequence and time of an individual cell to prevent hazardous situations. In some embodiments, the chip may include a small CPU and software code that in addition to taking actions in response to commands received from a controller can also act like a controller for certain tasks and react to specific localized situations and take autonomic specific actions such as, for instance, immediately switching-out a certain cell, or several cells, that the chip senses is malfunctioning.

**[0044]** The switching elements need to support switching time that relates to the application using the battery. In the case of an EV car, the switching time needed is relatively slow and do not pose significant needs from the switching elements, for instance the Power MOSFET mentioned

**[0045]** The constellations in which the switching elements are arranged within the battery module determines the level of flexibility when building the battery switching grid. It is preferable to keep the number of switching elements per battery module as low as possible in order to be able to design a cost effective solution. Moreover, it is also preferable that each of the switching elements need to bear only 1xI and thus can be relatively small. The connection that aggregate the currents from several cells is done outside the chip of the battery module and utilize several terminals of the chip.

**[0046]** FIG. 5 shows the battery module being configured such that all of the cells of the module are connected in parallel with each other. That is, c1 is parallel with c2, which is parallel with c3, which is parallel with c4. This is accomplished by closing switches s1-s4 and s10-s13 and keeping the others open. FIG. 6 shows the battery module being configured so that cell c1 is excluded from the parallel circuit. This is accomplished by closing switches s2-s4 and s11-s13 and keeping the other switches open.

**[0047]** FIG. 7 shows the battery module being configured such that all of the cells of the module are connected in in series. That is, c1 is in series with c2, which is in series with c3, which is in series with c4. This is accomplished by closing switches s4, s6-s8, s10 and keeping the others open. In this configuration, current (i.e., conventional current) is able to flow out of main positive terminal 402 and current is able to flow into main negative terminal 404. If cascading is desired, then switches s5 and s9 are closed and switches s4 and s10 are opened. In this cascading configuration, a current is able to flow into cascading negative terminal 581 and then through cells c1-c4 and then out cascading positive terminal 582. FIG. 8 shows the battery module being configured so that cell c1 is excluded from the series circuit. This is accomplished by closing switches s4, s7, s8, s11 and keeping the others open.

**[0048]** As is illustrated in FIGs. 6 and 8, the switches are connected in a way that enables to still make use of most of the other cell's while the problematic one is fully

excluded from the module. Preferably, the switches (e.g., Power FETs) have a very high switch-off impedance thus enable to safely exclude cells that are malfunctioning without the need to activate a main switch 1210 (see FIG. 2 or FIG. 12) and causing the car to stop.

**[0049]** Since electric engines need high current in order to produce high torque and high voltage to produce high speed, the needs from the battery are changing from the start of movement of the car that needs high current to the state when the car needs to increase the speed and the engine need high voltage. The common range of the voltage needed is 48 to 800 volts and the current changes between several to 300 Amperes. This configuration enables a dynamic power range of  $1:C$ , where  $C$  is the number of cells handled by each battery module, meaning it can drive  $C$  times the basic current or  $C$  times the basic voltage or any in between.

**[0050]** As described above, in the example battery module 301 shown in FIG. 4, which module is responsible for four cells (cl-c4), switches are connected in a way that enables the battery module to connect the cells in parallel or series connection. Moreover, as discussed above, other switches enable the cascading of columns within structure to support much higher battery voltages. This structure benefits a high level of flexibility while still maintaining relatively low number of switches and simple routing structure. The above configuration is unique also because the aggregation of the current from each of the branches is done in the wiring outside of the battery module, enabling each Power FET to be designed to transfer only  $1 \times I$  current, keeping the area of the chip as small as possible and enables the lowest cost.

**[0051]** Referring now to FIG. 13, FIG. 13 illustrates a configuration of battery module 301 according to another embodiment. In this example, three cells are shown for the sake of simplicity. In this embodiment, switches s1-s8 and s10-s12 are used for interconnecting cells cl-c4, while switches s9 and s13 are used for cascading columns in a cluster. In this embodiment, each cell can individually be disconnected from the other cells when the module is in the series arrangement. For example, if the cells are connected in series and then it is determined that cell c2 is bad, c2 can be disconnected by opening switch s8 and closing switch s11.

**[0052]** Referring now to FIGs. 14a, 14b, and 14c, these figures show an embodiment of battery module 301 that is similar to the embodiment shown in FIG. 3. One difference is that there are no middle cells and the cells that are used have higher current capacity than the cells used in the embodiment shown in FIG. 3. This embodiment illustrates that the same chip used in the battery module shown in FIG. 3 can be re-used to implement other configurations.

**[0053]** Referring back to FIG. 3, while FIG. 3 shows that the example battery pack includes only two clusters, a battery pack according to other embodiments may have more clusters. Likewise, while FIG. 3 shows that the example battery pack includes only two columns per cluster

and three battery modules 301 per column, other embodiments may have other configurations.

**[0054]** For example, FIG. 9 shows an embodiment of battery pack 104 that includes  $N$  clusters of battery modules, where each cluster includes  $B$  columns of battery modules, where each column includes  $M$  battery modules, for a total of  $N \times B \times M$  battery modules. Each battery pack can be designed with different parameters of  $C$ ,  $M$ ,  $B$  and  $N$ , thus best matching the need of the specific car or manufacturing line. In one arrangement, each cluster is connected in parallel with each other cluster. For each cluster, the columns of the cluster may be connected in parallel or in series. For each column, the battery modules of the column are capable of being connected in series.

**[0055]** An advantage of this structure is the ability to limit the current that is passing through each Power FET within the battery module to  $1 \times I$ , where  $I$  is the maximum current supported in the specific design. This means that in any configuration of the switching controls of the battery module the aggregation of the current is done by the special wiring structure outside of the battery module itself, enabling a cost effective solution. Currently we found out that a cost-effective constellation is built out of switches with  $C=4$  to 16. More preferably, in some applications,  $C$  ranges between 8 and 12.

**[0056]** The implementation of many parallel structures enables the use of relatively small Power FET that can be designated to small current and voltage with lower Rds-on resistance, thus dissipates a smaller amount of power and become energy efficient.

**[0057]** Specifically, this structure enable the connection of  $C \times B \times N$  cells in parallel providing maximum current of  $I \times (C \times B \times N)$  to be drawn out of all the cells and with the change of controls it enables the connection of  $C \times M \times B$  cells in series, reaching  $V \times (C \times M \times B)$  volts. The cascading of the columns within each cluster is enabled by the arrangement of switches that are used to interconnect the battery modules (see FIG. 3). This ability to draw high current and reach very high voltage enables the manufacturer of the car to reach better care performance without the limitations of fixed battery structure and is the outcome of the constellation of the switching elements within the battery module together with the specific routing design of the 3D Battery Switching Grid™ outside the battery module.

**[0058]** FIG. 10 is a block diagram of an example battery module 301 according to some embodiments. In this embodiment, the battery module 301 includes (a) a chip 1002 containing switches and control circuitry and (b) a module of cells 1004 (in this example the module of cells includes four cells, other configurations are possible, such as 8 cells, which has been found to be a cost effective number of cells). The example chip 1002 shown in FIG. 10 is comprised of an analog and a digital part. The analog part is built out of Power MOSFETs that are arranged in the special constellation as described above. On one embodiment the number of switches (e.g., Power



MOSFETs) is  $3+3*8=27$ .

**[0059]** These analog switches are controlled by the digital part of chip 1002 that is comprised of several blocks: a communication module that is capable of receiving switching commands from the EVProcessor™ in an error-resilient fashion to meet the car safety standards. This module is built out of a master (e.g., transmitter) and a slave (e.g., receiver) to enable a serial transfer of commands between one battery module to the other and by that minimize the number of wires transferring the switching commands within the battery pack. In some embodiments, the slave communication unit of a switcher chip 1002 (i) receives switching information from the master communication unit of an upstream switcher chip 1002, (ii) selects the switching information that is addressed to it, and (iii) transfers to the next chip in the communication chain through the master communication unit the remainder of the switching information that it received from the upstream chip. In this manner we save on the number of wires that runs in the battery for transferring the switching commands. That is, for example, the battery modules may be configured in a daisy chain arrangement where one of the battery modules is configured to receive switching information from an outside controller and then pass some, none or all of that switching information to the next battery module in the communication chain, which module then does the same thing for the next battery module in the chain, etc.

**[0060]** A command decoder checks the received command to eliminate possible functional errors that might create improper switching situation within the battery module or on a larger scale in the module or pack and translates the command for the switching control logic.

**[0061]** The switching control logic breaks the switching orders into actual on-off orders for each of the switching elements within the battery module.

**[0062]** The safety switching sequencer receives the on-off commands for each of the switches and determines the exact sequence and timing in which each of the Power FETs needs to be switched. It takes into consideration the speed of the switching element, energy consumption during the switching sequence and of course safety reasons - not to short any of the cells or create even momentarily an imbalance structure within the module or pack.

The EVProcessor™ 106 - Sophisticated Powerful Controller

**[0063]** The idea of using many small battery cells is incorporated with the use of a special powerful chip that can handle efficiently the implementation of the switching scheme according to the currently needed task and usage method.

**[0064]** FIG. 11 is a functional block diagram of such proposed EVProcessor™ 106.

**[0065]** The EVProcessor™ is based on a processing device that can run sophisticated algorithms and make

use of various different accelerators that optimally match the computational tasks needed in order to utilize the EV battery efficiently by the electric engine and to enable more longevity and safety.

**[0066]** The EVProcessor™ implements control and "wear-out" algorithms enabling to manage each of the cells within the battery modules. This innovative way of managing the battery cells will increase the energy efficiency of the battery enabling longer car distance drive and decrease the cost of the battery. The solution will also increase the safety usage of the battery by disconnecting malfunctioning individual cells from the pack without the need to stop the car and will decrease the type-2 errors of "faulty state of charge" from the same reason.

**[0067]** The EVProcessor™ runs two separate SW models: SmartLoad™ is an element which manages individual cells at all conditions and significantly improves battery pack performance and DynamicPower™ is a vehicle-system fed component that is designed to deliver voltage and current conditions matching the current specific engine needs in optimum fashion to the EV's inverter 1202 (see FIG 12).

**[0068]** While SmartLoad™ is a standalone battery system booster that outsmarts existing EV batteries by handling cells individually, rather than the battery pack as a whole, DynamicPower™ requires integration with car-makers and presents, beyond energy savings, an increased driving performance with simplified and cheaper inverter 1202.

**[0069]** The EVProcessor™ can sense the battery cells by means of analog or digital inputs, it can manage the cells switching grid (i.e., the switches within pack 104) using the digital outputs, it can connect to additional devices through the scalability port, it can make use of its internal memory and Flash to hold the battery history and statistics for each cell and can extend this DB to an external memory. It can also connect to external engines through its specific bus and can communicate with the car main controller or other devices by means of wired or wireless connections to manage battery storage for instance.

**[0070]** The ability to change the structure of the battery on-the-fly and in a dynamic manner that best matches the environmental and engine changing needs and that can compensate different time degradation effects and malfunctions of part of the cells redefines the battery specification and largely affect the ability to use it in different scenarios with changing parameters and environments especially cover for temperature changes.

**[0071]** FIG. 12 illustrates an example EV power train system 1200 that includes an embodiment of battery pack system 100 described herein. As shown, system 1200 includes a motor 1204 connected to an inverter 1202 that is electrically connected to the output terminals of battery pack 104, thereby receiving current output from battery pack 104. System 1200 also includes a main controller 1206 and a bus 1208 that allows the components to communicate. For example, EVProcessor™ can use

bus to obtain data from main controller and to provide commands to battery modules 301 within battery pack 104. The EVProcessor™ can also reside inside the battery pack 104 or as part of the main controller 1206 in the form of control-software and algorithms.

## EXAMPLES

### 1. A Cell Is Producing Lower Voltage than the Rated Voltage

**[0072]** Because of the chemical structure a certain cell within the battery pack can become defected, let's say because of production fault and produces less than the rated voltage. In the current structure of the battery pack this cell will continue to appear in the serial structure of the chain and the outcome will be that the voltage that is produced out of the battery is constantly reduced by that amount. Over time, more and more cells are producing less voltage and the battery output voltage is dropped significantly.

**[0073]** To overcome this problem the manufacturer is using additional spare cells in series that leads to higher voltage than the actual needed and is then dropped within the system.

**[0074]** With the systems described herein, for a certain interval of time, the EVProcessor™ reads the current engine speed, determines the best appropriate voltage for that speed, and calculates the number of series cells needed to supply the best appropriate voltage. This can be done by utilizing the engine manufacturing information that specifies the best appropriate voltage per each speed. It then reads a cell history database and reviews the amount of usage cycles of each cell. The processor also reads the current voltage of each cell and decides for the coming period of time which of the cells will be used and how many cells will be connected in serial and in parallel.

**[0075]** In some embodiments, the use of many micro-cells instead of large cells enables the processor to control the battery voltage in fine granularity and if a certain cell is malfunctioning and kept aside the overall effect on the battery capacity is negligible.

**[0076]** The outcome of this periodically continues process is that the voltage that the battery produces can be kept constant over time and overcome the hurdle of loss of voltage because of wear-out of certain battery cells within the chain.

**[0077]** The battery manufacturer can then specify less redundant cells within the battery structure because it can use less serial constantly connected cells and this additional cells can support the parallel structure instead to provide for the needed peak current.

### 2. Voltage Drop Because Of Environmental Temperature

**[0078]** It is well known that batteries are producing less voltage if the ambient temperature drops significantly. To

overcome this problem the manufacturers are specifying additional series cells that in regular ambient temperature are then producing excessive voltage than needed and is then dropped within the system.

**[0079]** With the systems described herein, for a certain interval of time, the EVProcessor™ reads the current engine speed and calculates the amount of series cells needed to supply the best appropriate voltage. It then reads the cell history database and reviews the amount of usage cycles of each cell. The processor also reads the actual voltage of each cell that is with respect to the current ambient temperature and decides for the coming period of time which of the cells will be used and how many cells will be connected in serial and in parallel.

### 3. Efficient Battery Charging

**[0080]** In the case of such large batteries that are comprised of many cells, that need to perform well over a long period of time, say 5 years in Li-ion car batteries, the charging task is becoming critical for the lifetime of the battery and the safety of the user. The current constant structure of the battery poses a process of charge that involves all the battery cells at once. This process of charging can be harmful if a certain cell is overcharged and for that there is a safety leveling mechanism that discharges the cells to a certain voltage, keeping all the cells in a predefined voltage range.

**[0081]** With the systems described herein, for a certain charge interval of time, the EVProcessor™ reads the actual voltage of each cell and the cell history database to review the amount of charge cycles the cell have already passed. It then decides for the coming period of charge time which of the cells will be charged and how many cells will be connected in serial and in parallel in order to create the best charge current flow. Cells that reach the maximum voltage allowed are kept aside while other cells charge continues. This enables charge of all of the cells to their maximum capacity. In this manner the full capacity of the battery can be used.

**[0082]** The outcome of this charge process is that cells that don't need to be charged are kept out of the charging chain and are not worn-out by unnecessary charges. These cells are also less exposed to over-charge situation thus the battery usage is much safer. The overall charge time can be reduced in the factor of N because of charging more cells in parallel and even utilize charge in lower charge current per cell, extending the life cycle of the battery. The battery manufacturer can then specify less cells within the battery structure because it can use less serial constantly connected cells that overcome the wear-out problem and this additional cells can support the parallel structure instead to provide for the needed peak current.

### 4. Efficient Battery Discharging

**[0083]** In the case of such large batteries that are com-

prised of many cells, that need to perform well over a long period of time, say 5 years in Li-ion car batteries, the discharging task is becoming critical for the lifetime of the battery. The Li-ion chemistry limits the charging of the cells to 2.5V minimum. Discharging the battery to lower rate will create irreversible damage to the cell and will disable the use of the whole pack. The current constant structure of the battery poses a process of discharge that involves all the battery cells at once. This process of discharging can be harmful if a certain cell is over discharged and for that reason there is a mechanism that stops the discharge of the entire pack if even only one of the cells reaches 2.5V. This mechanism disables the utilization of the full capacity of each of the cells and limits it by the weakest cell in the pack. It is well known that after only 200 cycles the battery pack will have significant cell to cell variations and this creates inefficient utilization of the battery capacity.

**[0084]** With the systems described herein, for a certain charge interval of time, the EVProcessor™ reads the actual voltage of each cell. It then decides for the coming period of charge time which of the cells will be discharged and how many cells will be connected in serial and in parallel in order to create the best discharge current flow. Cells that reach the minimum voltage of 2.5V allowed are kept aside (i.e., electrically disconnected as described above) while other cells discharge continues. This enables the discharge of all of the cells to their minimum capacity. In this manner the full capacity of the battery can be used.

**[0085]** The outcome of this discharge process is that cells that finished the discharge cycle are kept out of the discharge chain and are not limiting the ability to continue the discharge of the rest of the cells. These cells are also less exposed to over-discharge situation thus the battery usage is much gentle, extending the life cycle of the battery. The battery manufacturer can then specify fewer cells within the battery structure because it can use less constantly connected cells that overcome the wear-out problem reducing the overall cost of the battery.

## 5. Optimized EV Motor performance

**[0086]** In the case of such large battery packs that are comprised of many cells, that need to perform well over a long period of time, providing the best values of current/voltage according to the constantly changing needs of the motor is a challenging task. The current constant structure of the battery poses the manufacturer to assemble the battery pack in a structure that will have enough cells in parallel connection to support the highest current needed for needed torque performance and in the same time to assemble enough cell in serial to support that highest voltage needed to support the horse power needs. This design process is limited by the weight and cost of the battery pack and forces the manufacturer to compromise on the car performance values.

**[0087]** With the systems described herein, for a certain

interval of time, the EVProcessor™ reads the car manufacturer engine graph that is stored in the database and the actual voltage of each cell and as well as the cell history database to review the amount of charge cycles the cell have already passed. It then decides for the coming period of time which of the cells will be used and how many cells will be connected in serial and in parallel in order to create the best structure to support the needed motor voltage and current. This way of using the cells in a flexible structure gives the manufacturer a new degree of freedom in the design of the battery structure and supports better motor values of torque and horse power providing a better car to the customer for the same battery cost.

**[0088]** The battery manufacturer can also specify fewer cells within the battery structure because it can use different cell structure to support the extreme current or voltage needs in different period of time.

**[0089]** This advance use of the battery power is saving a lot of energy, complexity and cost invested today into the structure of the inverter that needs to support the demanding AC needs of the motor from a fixed DC battery power. The EVProcessor™ can replace most of the functionality of the Inverter by creating the desired AC power by constantly changing the amount of serial cells connected together to create the momentarily voltage.

## Other Battery Uses

**[0090]** Even though the primary goal of this invention is to better utilize Electric Vehicles Battery packs, battery pack system 100 can be used for different battery applications like mobile phones or laptop computers. Of course, the economy of each use-case is different but the basic practice in which we divide the battery to cells, connect them with the 3D Battery Switching Grid™ battery switching grid and employ sophisticated micro-management and control methods can be matched to every case.

## Claims

1. A battery pack comprising: a main controller, and a plurality of switcher chips each for interconnecting a plurality of battery cells, each switcher chip of the plurality of switcher chips comprising:

a switching control logic; and  
a communication circuit;  
the communication circuit comprising:

a transmitter, and  
a receiver,  
wherein the receiver is communicatively connected in use to either the main controller or a transmitter of an adjacent switcher

chip such that the receiver is operable to receive switching commands transmitted from either the main controller or the transmitter of the adjacent switcher chip, and wherein the transmitter is for transmitting switching commands to another adjacent switcher chip;

the battery pack further comprising:

a main negative terminal (404) of a first switcher chip (301b) connected to a main positive terminal of a second switcher chip;  
 a negative terminal (581) of the first switcher chip (301b);  
 a main positive terminal (402) of the first switcher chip (301b) connected to a main positive terminal of a third switcher chip (301);  
 a positive terminal (582) of the first switcher chip connected to a negative terminal (581) of a fourth switcher chip (301a);  
 a plurality of cell terminals; and  
 a plurality of switches, wherein the first switcher chip is configured such that:

when a set of cells are connected to the first switcher chip via the plurality of cell terminals and a first set of the plurality of switches are closed and the remainder of the plurality of switches are open, the set of cells are connected in parallel with each other and current is able to flow through the set of cells and out of the main positive terminal (402) but is not able to flow out of the positive terminal (582),

when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a second set of the plurality of switches are closed and the remainder of the plurality of switches are open, the set of cells are connected in series with each other and current is able to flow through the set of cells and out of the main positive terminal (402) but is not able to flow out the positive terminal (582),

when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a third set of the plurality of switches are closed and the remainder of the plurality of switches are open, at least two of the cells in the set of cells are connected in series with each other and current is able to flow through the set of cells and out of the positive terminal (582) but is not able to flow out the main positive terminal (402),

when the set of cells are connected to the first switcher chip via the plurality of cell ter-

minals and a fourth set of the plurality of switches are closed and the remainder of the plurality of switches are open, a subset of the set of cells are connected in parallel with each other, at least one cell is electrically disconnected from each of the other cells in the set of cells, and current is able to flow through the set of cells and out of the main positive terminal (402) but is not able to flow out the positive terminal (582), and

when the set of cells are connected to the first switcher chip via the plurality of cell terminals and a fifth set of the plurality of switches are closed and the remainder of the plurality of switches are open, another subset of the set of cells are connected in series with each other and at least one cell from the set of cells is electrically disconnected from each of the other cells of the set.

2. The battery pack of claim 1, the switcher chips further comprising:

a command decoder configured to error check commands received by the communication circuit from the main controller or from another switcher chip and configured to block erroneous commands.

3. The battery pack of claim 2, the switcher chips further comprising:

the switching control logic connected to the command decoder and configured to convert commands received by the communication circuit from the main controller into switch on-off commands for switching elements within the battery pack.

4. The battery pack of claim 3, the switcher chips further comprising:

a safety switching sequencer configured to receive the on-off commands from the switching control logic and configured to turn on or off at exact sequence and time one or more of the switches based on the received on-off commands.

5. The battery pack of claim 1, the switcher chips further comprising:

a slave input terminal;  
 a master output terminal;  
 the receiver being a slave communication module block;  
 the transmitter being a master communication module block;  
 a command decoder block;  
 a safety switching sequencer block.

6. The battery pack of claim 1, wherein the plurality of switches comprises a plurality of power metal-oxide

semiconductor field effect transistors (MOSFETs).

7. A battery apparatus, comprising:

a first switcher chip (301b), a second switcher chip, a third switcher chip, and a fourth switcher chip, each for interconnecting a plurality of battery cells; and  
 each switcher chip of the first switcher chip (301b), the second switcher chip, the third switcher chip, and the fourth switcher chip comprising: a switching control logic, and a communication circuit, wherein the communication circuit comprises:  
 a transmitter, and a receiver,

wherein each receiver is communicatively connected in use to either a main controller or a transmitter of an adjacent switcher chip such that the receiver is operable to receive switching commands transmitted from either the main controller or the transmitter of the adjacent switcher chip, and wherein the transmitter is for transmitting switching commands to another adjacent switcher chip;

the first switcher chip (301b) further comprising a first plurality of switches, a first main positive terminal (402), a first main negative terminal (404), a first positive terminal (582) and a first negative terminal (581); and

a set of cells, the set of cells comprising:

(i) a first cell having a positive terminal and a negative terminal, the positive terminal of the first cell being connected to a first cell terminal of the first switcher chip and the negative terminal of the first cell being connected to a second cell terminal of the first switcher chip, and  
 (ii) a second cell having a positive terminal and a negative terminal, the positive terminal of the second cell is connected to a third cell terminal of the first switcher chip and the negative terminal of the second cell is connected to a fourth cell terminal of the first switcher chip,

the second switcher chip further comprising: a second plurality of switches, a second main positive terminal and a second main negative terminal, the second main positive terminal of the second switcher chip being connected to the first main negative terminal of the first switcher chip;

the third switcher chip (301a) comprising: a third plurality of switches, a third main positive terminal, a third main negative terminal, and a second negative terminal (581), the second negative terminal (581) of the third switcher chip (301a), being connected to the first positive terminal (582) of the first switcher chip (301b); and

the fourth switcher chip (301) comprising: a fourth

plurality of switches, a fourth main positive terminal and a fourth main negative terminal, the fourth main positive terminal of the fourth switcher chip being connected to the first main positive terminal of the first switcher chip, wherein the first switcher chip is operable to:

(i) configure the first plurality of switches such that (a) the cells of the set of cells are connected in series, (b) current is able to flow out of the first switcher chip via the first main positive terminal (402) but is not able to flow out the first switcher chip via the first positive terminal, and (c) current is able to flow into the first switcher chip via the first main negative terminal,

(ii) configure the first plurality of switches such that (a) the cells of the sets of cells are connected in series, (b) current is able to flow out of the first switcher chip via the first positive terminal but is not able to flow out the first switcher chip via the first main positive terminal, and (c) current is able to flow into the first switcher chip via the first negative terminal, and

(iii) configure the first plurality of switches such that (a) the cells of the set of cells are connected in parallel, (b) current is able to flow out of the first switcher chip via the first main positive terminal (402) but is not able to flow out the first switcher chip via the first positive terminal, and (c) current is able to flow into the first switcher chip via the first main negative terminal.

8. The battery apparatus of claim 7, wherein each of the first, second, third and fourth switcher chips further comprise:

a command decoder configured to error check commands received by the communication circuit from the main controller or from another switcher chip and configured to block erroneous commands.

9. The battery apparatus of claim 8, wherein each of the first, second, third and fourth switcher chips further comprise:

the switching control logic connected to the command decoder and configured to convert commands received by the communication circuit from the main controller into switch on-off commands for switching elements within the battery apparatus.

10. The battery apparatus of claim 9, wherein each of the first, second, third and fourth switcher chips further comprise:

a safety switching sequencer configured to receive the on-off commands from the switching control logic and configured to turn on or off at exact sequence and time one or more of the switches based on the received on-off commands.

11. The battery apparatus of claim 7, wherein the first cell is a micro-cell and the second cell is a micro-cell.

12. The battery apparatus of claim 7 comprising a battery pack, the battery pack comprising:

a first cluster of battery modules comprising a first column of battery modules and a second column of battery modules;

a first circuit for connecting the first column of battery modules in parallel with the second column of battery modules;

a second circuit for connecting the first column of battery modules in series with the second column of battery modules;

a second cluster of battery modules comprising a third column of battery modules and a fourth column of battery modules;

a third circuit for connecting the third column of battery modules in parallel with the fourth column of battery modules;

a fourth circuit for connecting the third column of battery modules in series with the fourth column of battery modules, wherein

at least one of the battery modules in the first column of battery modules has (i) a switch for connecting and disconnecting a main output of the battery module to the first circuit and (ii) a switch for connecting and disconnecting an output of the battery module to the second circuit,

at least one of the battery modules in the second column of battery modules has (i) a switch for connecting and disconnecting a main output of the battery module to the first circuit and (ii) a switch for connecting and disconnecting an output of the battery module to the second circuit,

at least one of the battery modules in the third column of battery modules has (i) a switch for connecting and disconnecting a main output of the battery module to the third circuit and (ii) a switch for connecting and disconnecting an output of the battery module to the fourth circuit, and

at least one of the battery modules in the fourth column of battery modules has (i) a switch for connecting and disconnecting a main output of the battery module to the third circuit and (ii) a switch for connecting and disconnecting an output of the battery module to the fourth circuit.

13. The battery apparatus of claim 12, wherein the main controller is operable to:

(a) place the battery pack in a first mode of operation in which the battery pack produces a voltage V1; and

(b) place the battery pack in second mode of operation in which the battery pack produces a voltage V2, where  $V2 > V1$ .

14. The battery apparatus of claim 13, wherein at least one of the battery modules comprises:

a switcher chip comprising: a plurality of switches, a main positive terminal, a main negative terminal, a positive terminal and a negative terminal; and

a set of cells comprising (i) a first cell having a positive terminal and a negative terminal, the positive terminal being connected to a first cell terminal of the switcher chip and the negative terminal being connected to a second cell terminal of the switcher chip, and (ii) a second cell having a positive terminal and a negative terminal, the positive terminal is connected to a third cell terminal of the switcher chip and the negative terminal is connected to a fourth cell terminal of the switcher chip.

15. The battery apparatus of claim 14, wherein the main controller is operable to:

(i) cause the at least one of the battery modules to configure the switches of the plurality of switches such that (a) the cells of the set of cells are connected in series, (b) current is able to flow out of the switcher chip via the main positive terminal (402) but is not able to flow out the switcher chip via the positive terminal, and (c) current is able to flow into the switcher chip via the main negative terminal but is not able to flow into the switcher chip via the negative terminal,

(ii) cause the at least one of the battery modules to configure the switches of the plurality of switches such that (a) the cells of the set of cells are connected in series, (b) current is able to flow out of the switcher chip via the positive terminal but is not able to flow out the switcher chip via the main positive terminal, and (c) current is able to flow into the switcher chip via the negative terminal but is not able to flow into the switcher chip via the main negative terminal, and

(iii) cause the at least one of the battery modules to configure the switches of the plurality of switches such that (a) the cells of the set of cells are connected in parallel, (b) current is able to flow out of the switcher chip via the main positive terminal (402) but is not able to flow out the switcher chip via the positive terminal, and (c) current is able to flow into the switcher chip via the main negative terminal but is not able to flow into the switcher chip via the negative terminal.

#### Patentansprüche

1. Batteriepack, umfassend: Einen Haupt-Controller und eine Vielzahl von Schalter-Chips jeder zum Verschalten einer Vielzahl von Batteriezellen, Jeder Schalter-Chip der Vielzahl von Schalter-Chips umfassend:

Eine Schaltsteuerlogik; und  
eine Kommunikationsschaltung;  
wobei die Kommunikationsschaltung umfasst:

Einen Sender, und  
einen Empfänger,  
wobei der Empfänger kommunikativ im Ein-  
satz mit entweder dem Haupt-Controller  
oder einem Sender eines benachbarten  
Schalter-Chips derartig verbunden ist, dass  
der Empfänger betriebsfähig ist, Schaltbe-  
fehle zu empfangen, die entweder vom  
Haupt-Controller oder dem Sender des be-  
nachbarten Schalter-Chips gesendet wur-  
den, und wobei der Sender zum Senden  
von Schaltbefehlen zu einem weiteren be-  
nachbarten Schalter-Chip ist;

den Batteriepack, der weiter umfasst:

Einen negativen Hauptpol (404) eines ersten  
Schalter-Chips (301b) der mit einem positiven  
Hauptpol eines zweiten Schalter-Chips verbun-  
den ist;  
einen negativen Pol (581) des ersten Schalter-  
Chips (301b);  
einen positiven Hauptpol (402) des ersten  
Schalter-Chips (301b), der mit einem positiven  
Hauptpol eines dritten Schalter-Chips (301) ver-  
bunden ist;  
einen positiven Pol (582) des ersten Schalter-  
Chips, der mit einem negativen Pol (581) eines  
vierten Schalter-Chips (301a) verbunden ist;  
eine Vielzahl von Zellenklemmen; und  
eine Vielzahl von Schaltern, wobei  
der erste Schalter-Chip derartig konfiguriert ist,  
dass:

Wenn ein Satz von Zellen über die Vielzahl  
von Zellenklemmen mit dem ersten Schal-  
ter-Chip verbunden ist und ein erster Satz  
der Vielzahl von Schaltern geschlossen ist  
und der Rest der Vielzahl von Schaltern of-  
fen ist, ist der Satz von Zellen parallel mit-  
einander verbunden und Strom ist fähig  
durch den Satz von Zellen und aus dem po-  
sitiven Hauptpol (402) zu fließen, aber ist  
unfähig aus dem positiven Pol (582) zu flie-  
ßen,  
wenn der Satz von Zellen über die Vielzahl  
von Zellenklemmen mit dem ersten Schal-  
ter-Chip verbunden ist und ein erster Satz  
der Vielzahl von Schaltern geschlossen ist  
und der Rest der Vielzahl von Schaltern of-  
fen ist, ist der Satz von Zellen in Reihe mit-  
einander verbunden und Strom ist fähig  
durch den Satz von Zellen und aus dem po-  
sitiven Hauptpol (402) zu fließen, aber ist

unfähig aus dem positiven Pol (582) zu flie-  
ßen,

wenn der Satz von Zellen über die Vielzahl  
von Zellenklemmen mit dem ersten Schal-  
ter-Chip verbunden ist und ein dritter Satz  
der Vielzahl von Schaltern geschlossen ist  
und der Rest der Vielzahl von Schaltern of-  
fen ist, sind zumindest zwei der Zellen im  
Satz von Zellen in Reihe miteinander ver-  
bunden und Strom ist fähig durch den Satz  
von Zellen und aus dem positiven Pol (582)  
zu fließen, aber ist unfähig aus dem positi-  
ven Hauptpol (402) zu fließen,  
wenn der Satz von Zellen über die Vielzahl  
von Zellenklemmen mit dem ersten Schal-  
ter-Chip verbunden ist und ein vierter Satz  
der Vielzahl von Schaltern geschlossen ist  
und der Rest der Vielzahl von Schaltern of-  
fen ist, ist ein Teilsatz des Satzes von Zellen  
parallel miteinander verbunden, wobei zu-  
mindest eine Zelle von jeder der anderen  
Zellen im Satz von Zellen elektrisch ge-  
trennt ist, und Strom ist fähig durch den Satz  
von Zellen und aus dem positiven Hauptpol  
(402) zu fließen, aber ist unfähig aus dem  
positiven Pol (582) zu fließen, und  
wenn der Satz von Zellen über die Vielzahl  
von Zellenklemmen mit dem ersten Schal-  
ter-Chip verbunden ist und ein fünfter Satz  
von Schaltern geschlossen ist und der Rest  
der Vielzahl von Schaltern offen ist, ist ein  
weiterer Teilsatz des Satzes von Zellen in  
Reihe miteinander verbunden und zumin-  
dest eine Zelle des Satzes von Zellen ist  
von jeder der anderen Zellen des Satzes  
elektrisch getrennt.

2. Batteriepack nach Anspruch 1, wobei die Schalter-  
Chips ferner umfassen:

Einen Befehlsdecoder, der konfiguriert ist, Befehle  
auf Fehler zu prüfen, die durch die Kommunika-  
tionsschaltung ab dem Haupt-Controller oder von einem  
anderen Schalter-Chip empfangen wurden und kon-  
figuriert ist, fehlerhafte Befehle zu blockieren.

3. Batteriepack nach Anspruch 2, wobei die Schalter-  
Chips ferner umfassen:

Die Schaltsteuerlogik, die mit dem Befehlsdecoder  
verbunden und konfiguriert ist, durch die Kommuni-  
kationsschaltung ab dem Haupt-Controller empfan-  
gene Befehle in Ein-/Ausschaltbefehle für Schalte-  
lemente innerhalb des Batteriepacks umzuwandeln.

4. Batteriepack nach Anspruch 3, wobei die Schalter-  
Chips ferner umfassen:

Einen Sicherheits-Schaltsequenzer, der konfiguriert  
ist, die Ein/Aus-Befehle von der Schaltsteuerlogik zu  
empfangen und konfiguriert ist, zur exakten Se-

quenz und Zeit einen oder mehrere der Schalter auf Basis der empfangenen Ein/Aus-Befehle ein- oder auszuschalten.

5. Batteriepack nach Anspruch 1, wobei die Schalter-Chips ferner umfassen:

Eine Slave-Eingangsklemme;  
eine Master-Ausgangsklemme;  
den Empfänger, der ein Slave-Kommunikationsmodulblock ist;  
den Sender, der ein Master-Kommunikationsmodulblock ist;  
einen Befehls-Decoderblock;  
einen Sicherheits-Schaltsequenzerblock.

6. Batteriepack nach Anspruch 1, wobei die Vielzahl von Schaltern eine Vielzahl von Leistungs-Metall-oxidhalbleiter-Feldeffekttransistoren (MOSFETs) umfasst.

7. Batterievorrichtung, umfassend:

Einen ersten Schalter-Chip (301b), einen zweiten Schalter-Chip, einen dritten Schalter-Chip und einen vierten Schalter-Chip, jeder zum Verschalten einer Vielzahl von Batteriezellen; und jeder Schalter-Chip des ersten Schalter-Chips (301b), des zweiten Schalter-Chips, des dritten Schalter-Chips und des vierten Schalter-Chips umfassend: Eine Schaltsteuerlogik und eine Kommunikationsschaltung, wobei die Kommunikationsschaltung umfasst:  
Einen Sender und einen Empfänger,

wobei jeder Empfänger kommunikativ im Einsatz mit entweder einem Haupt-Controller oder einem Sender eines benachbarten Schalter-Chips derartig verbunden ist, dass der Empfänger betriebsfähig ist, Schaltbefehle zu empfangen, die entweder vom Haupt-Controller oder dem Sender des benachbarten Schalter-Chips gesendet wurden, und wobei der Sender zum Senden von Schaltbefehlen zu einem weiteren benachbarten Schalter-Chip ist; wobei der erste Schalter-Chip (301b) ferner eine erste Vielzahl von Schaltern, einen ersten positiven Hauptpol (402), einen ersten negativen Hauptpol (404), einen ersten positiven Pol (582) und einen ersten negativen Pol (581) umfasst; und einen Satz von Zellen, wobei der Satz von Zellen umfasst:

(i) eine erste Zelle mit einem positiven Pol und einem negativen Pol, wobei der positive Pol der ersten Zelle mit einer ersten Zellenklemme des ersten Schalter-Chips verbunden ist und der negative Pol der ersten Zelle mit einer zweiten Zellenklemme des ersten Schalter-Chips verbun-

den ist, und

(ii) eine zweite Zelle mit einem positiven Pol und einem negativen Pol, wobei der positive Pol der zweiten Zelle mit einer dritten Zellenklemme des ersten Schalter-Chips verbunden ist und der negative Pol der zweiten Zelle mit einer vierten Zellenklemme des ersten Schalter-Chips verbunden ist,

den zweiten Schalter-Chip ferner umfassend: Eine zweite Vielzahl von Schaltern, einen zweiten positiven Hauptpol und einen zweiten negativen Hauptpol, wobei der zweite positive Hauptpol des zweiten Schalter-Chips mit dem ersten negativen Hauptpol des ersten Schalter-Chips verbunden ist; den dritten Schalter-Chip (301a) umfassend: Eine dritte Vielzahl von Schaltern, einen dritten positiven Hauptpol, einen dritten negativen Hauptpol und einen zweiten negativen Pol (581), wobei der zweite negative Pol (581) des dritten Schalter-Chips (301a) mit dem ersten positiven Pol (582) des ersten Schalter-Chips (301b) verbunden ist; und den vierten Schalter-Chip (301), umfassend: Eine vierte Vielzahl von Schaltern, einen vierten positiven Hauptpol und einen vierten negativen Hauptpol, wobei der vierte positive Hauptpol des vierten Schalter-Chips mit dem ersten positiven Hauptpol des ersten Schalter-Chips verbunden ist, wobei der erste Schalter-Chip betriebsfähig ist, Folgendes zu tun:

(i) Konfigurieren der ersten Vielzahl von Schaltern derartig, dass (a) die Zellen des Satzes von Zellen in Reihe verbunden sind, (b) Strom fähig ist, über den ersten positiven Hauptpol (402) aus dem ersten Schalter-Chip zu fließen, aber unfähig ist, über den ersten positiven Pol aus dem ersten Schalter-Chip zu fließen, und (c) Strom fähig ist, über den ersten negativen Hauptpol in den ersten Schalter-Chip zu fließen,

(ii) Konfigurieren der ersten Vielzahl von Schaltern derartig, dass (a) die Zellen der Sätze von Zellen in Reihe verbunden sind, (b) Strom fähig ist, über den ersten positiven Pol aus dem ersten Schalter-Chip zu fließen, aber unfähig ist, über den ersten positiven Hauptpol aus dem ersten Schalter-Chip zu fließen, und (c) Strom fähig ist, über den ersten negativen Pol in den ersten Schalter-Chip zu fließen, und

(iii) Konfigurieren der ersten Vielzahl von Schaltern derartig, dass (a) die Zellen des Satzes von Zellen parallel verbunden sind, (b) Strom fähig ist, über den ersten positiven Hauptpol (402) aus dem ersten Schalter-Chip zu fließen, aber unfähig ist, über den ersten positiven Pol aus dem ersten Schalter-Chip zu fließen, und (c) Strom fähig ist, über den ersten negativen Hauptpol in den ersten Schalter-Chip zu fließen.



8. Batterievorrichtung nach Anspruch 7, wobei jeder der ersten, zweiten, dritten und vierten Schalter-Chips ferner umfasst:  
 Einen Befehlsdecoder, der konfiguriert ist, Befehle auf Fehler zu prüfen, die durch die Kommunikationsschaltung ab dem Haupt-Controller oder von einem anderen Schalter-Chip empfangen wurden und konfiguriert ist, fehlerhafte Befehle zu blockieren. 5
9. Batterievorrichtung nach Anspruch 8, wobei jeder der ersten, zweiten, dritten und vierten Schalter-Chips ferner umfasst:  
 Die Schaltsteuerlogik, die mit dem Befehlsdecoder verbunden und konfiguriert ist, durch die Kommunikationsschaltung ab dem Haupt-Controller empfangene Befehle in Ein-/Ausschaltbefehle für Schaltelemente innerhalb der Batterievorrichtung umzuwandeln. 10 15
10. Batterievorrichtung nach Anspruch 9, wobei jeder der ersten, zweiten, dritten und vierten Schalter-Chips ferner umfasst:  
 Einen Sicherheits-Schaltsequenzer, der konfiguriert ist, die Ein/Aus-Befehle von der Schaltsteuerlogik zu empfangen und konfiguriert ist, zur exakten Sequenz und Zeit einen oder mehrere der Schalter auf Basis der empfangenen Ein/Aus-Befehle ein- oder auszuschalten. 20 25
11. Batterievorrichtung nach Anspruch 7, wobei die erste Zelle eine Mikrozele ist und die zweite Zelle eine Mikrozele ist. 30
12. Batterievorrichtung nach Anspruch 7, die einen Batteriepack umfasst, wobei der Batteriepack umfasst:  
 Einen ersten Verbund von Batteriemodulen, der eine erste Säule von Batteriemodulen und eine zweite Säule von Batteriemodulen umfasst;  
 einen ersten Stromkreis zum Verbinden der ersten Säule von Batteriemodulen parallel mit der zweiten Säule von Batteriemodulen;  
 einen zweiten Stromkreis zum Verbinden der ersten Säule von Batteriemodulen in Reihe mit der zweiten Säule von Batteriemodulen;  
 einen zweiten Verbund von Batteriemodulen, der eine dritte Säule von Batteriemodulen und eine vierte Säule von Batteriemodulen umfasst;  
 einen dritten Stromkreis zum Verbinden der dritten Säule von Batteriemodulen parallel mit der vierten Säule von Batteriemodulen;  
 einen vierten Stromkreis zum Verbinden der dritten Säule von Batteriemodulen in Reihe mit der vierten Säule von Batteriemodulen, wobei zumindest eins der Batteriemodule in der ersten Säule von Batteriemodulen (i) einen Schalter zum Verbinden und Trennen eines Hauptausgangs des Batteriemoduls mit/vom ersten Stromkreis und (ii) einen Schalter zum Verbinden und Trennen eines Ausgangs des Batteriemoduls mit/vom zweiten Stromkreis aufweist, zumindest eins der Batteriemodule in der dritten Säule von Batteriemodulen (i) einen Schalter zum Verbinden und Trennen eines Hauptausgangs des Batteriemoduls mit/vom dritten Stromkreis und (ii) einen Schalter zum Verbinden und Trennen eines Ausgangs des Batteriemoduls mit/vom vierten Stromkreis aufweist, und  
 zumindest eins der Batteriemodule in der vierten Säule von Batteriemodulen (i) einen Schalter zum Verbinden und Trennen eines Hauptausgangs des Batteriemoduls mit/vom dritten Stromkreis und (ii) einen Schalter zum Verbinden und Trennen eines Ausgangs des Batteriemoduls mit/vom vierten Stromkreis aufweist. 35 40 45 50
13. Batterievorrichtung nach Anspruch 12, wobei der Haupt-Controller betriebsfähig ist, Folgendes zu tun:  
 (a) Platzieren des Batteriepacks in eine erste Betriebsart, in welcher der Batteriepack eine Spannung  $V_1$  produziert; und  
 (b) Platzieren des Batteriepacks in eine zweite Betriebsart, in welcher der batteriepack eine Spannung  $V_2$  produziert, wobei  $V_2 > V_1$ . 55
14. Batterievorrichtung nach Anspruch 13, wobei zumindest eins der Batteriemodule umfasst:  
 Einen Schalter-Chip, umfassend: Eine Vielzahl von Schaltern, einen positiven Hauptpol, einen negativen Hauptpol, einen positiven Pol und einen negativen Pol; und  
 einen Satz von Zellen der (i) eine erste Zelle mit einem positiven Pol und einem negativen Pol umfasst, wobei der positive Pol mit einer ersten Zellenklemme des Schalter-Chips verbunden ist und der negative Pol mit einer zweiten Zellenklemme des Schalter-Chips verbunden ist und (ii) eine zweite Zelle mit einem positiven Pol und einem negativen Pol, wobei der positive Pol mit einer dritten Zellenklemme des Schalter-Chips verbunden ist und der negative Pol mit einer vierten Zellenklemme des Schalter-Chips verbunden ist. 55
15. Batterievorrichtung nach Anspruch 14, wobei der Haupt-Controller betriebsfähig ist, Folgendes zu tun:  
 (i) Bewirken, dass das zumindest eine der Bat-

teriemodule die Schalter der Vielzahl von Schaltern derartig konfiguriert, dass (a) die Zellen des Satzes von Zellen in Reihe verbunden sind, (b) Strom fähig ist, über den positiven Hauptpol (402) aus dem ersten Schalter-Chip zu fließen, aber unfähig ist, über den positiven Pol aus dem Schalter-Chip zu fließen, und (c) Strom fähig ist, über den negativen Hauptpol in den Schalter-Chip zu fließen aber unfähig ist, über den negativen Pol in den Schalter-Chip zu fließen, (ii) Bewirken, dass das zumindest eine der Batteriemodule die Schalter der Vielzahl von Schaltern derartig konfiguriert, dass (a) die Zellen des Satzes von Zellen in Reihe verbunden sind, (b) Strom fähig ist, über den positiven Pol aus dem Schalter-Chip zu fließen, aber unfähig ist, über den positiven Hauptpol aus dem ersten Schalter-Chip zu fließen, und (c) Strom fähig ist, über den negativen Pol in den Schalter-Chip zu fließen aber unfähig ist, über den negativen Hauptpol in den Schalter-Chip zu fließen, und (iii) Bewirken, dass das zumindest eine der Batteriemodule die Schalter der Vielzahl von Schaltern derartig konfiguriert, dass (a) die Zellen des Satzes von Zellen parallel verbunden sind, (b) Strom fähig ist, über den positiven Hauptpol (402) aus dem Schalter-Chip zu fließen, aber unfähig ist, über den positiven Pol aus dem ersten Schalter-Chip zu fließen, und (c) Strom fähig ist, über den negativen Hauptpol in den Schalter-Chip zu fließen aber unfähig ist, über den negativen Pol in den Schalter-Chip zu fließen.

## Revendications

1. Bloc-batterie comportant : un dispositif de commande principal, et une pluralité de puces de commutation servant chacune à des fins d'interconnexion d'une pluralité d'éléments de batterie, chaque puce de commutation de la pluralité de puces de commutation comportant :

une logique de commande de commutation ; et  
un circuit de communication ;  
le circuit de communication comportant :

un émetteur, et  
un récepteur,  
dans lequel le récepteur est connecté en communication lors de l'utilisation à soit le dispositif de commande principal soit un émetteur d'une puce de commutation adjacente de telle sorte que le récepteur sert à recevoir des commandes de commutation émises en provenance de soit le dispositif de commande principal soit l'émetteur de la puce de commutation adjacente, et dans le-

quel l'émetteur a pour objet d'émettre des commandes de commutation à une autre puce de commutation adjacente ;

le bloc-batterie comportant par ailleurs :

une borne négative principale (404) d'une première puce de commutation (301b) connectée à une borne positive principale d'une deuxième puce de commutation ;  
une borne négative (581) de la première puce de commutation (301b) ;  
une borne positive principale (402) de la première puce de commutation (301b) connectée à une borne positive principale d'une troisième puce de commutation (301) ;  
une borne positive (582) de la première puce de commutation connectée à une borne négative (581) d'une quatrième puce de commutation (301a) ;  
une pluralité de bornes d'élément ; et  
une pluralité de commutateurs, dans lequel la première puce de commutation est configurée de telle sorte que :

quand les éléments d'un ensemble d'éléments sont connectés à la première puce de commutation par le biais de la pluralité de bornes d'élément et quand les commutateurs d'un premier ensemble de la pluralité de commutateurs sont fermés et que les commutateurs restants de la pluralité de commutateurs sont ouverts, les éléments de l'ensemble d'éléments sont connectés en parallèle les uns par rapport aux autres et le courant est en mesure de s'écouler au travers de l'ensemble d'éléments et hors de la borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la borne positive (582),  
quand les éléments de l'ensemble d'éléments sont connectés à la première puce de commutation par le biais de la pluralité de bornes d'élément et quand les commutateurs d'un deuxième ensemble de la pluralité de commutateurs sont fermés et que les commutateurs restants de la pluralité de commutateurs sont ouverts, les éléments de l'ensemble d'éléments sont connectés en série les uns par rapport aux autres et le courant est en mesure de s'écouler au travers de l'ensemble d'éléments et hors de la borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la borne positive (582),  
quand les éléments de l'ensemble d'éléments sont connectés à la première puce de commutation par le biais de la pluralité

- de bornes d'élément et quand les commutateurs d'un troisième ensemble de la pluralité de commutateurs sont fermés et que les commutateurs restants de la pluralité de commutateurs sont ouverts, au moins deux des éléments dans l'ensemble d'éléments sont connectés en série l'un par rapport à l'autre et le courant est en mesure de s'écouler au travers de l'ensemble d'éléments et hors de la borne positive (582) mais n'est pas en mesure de s'écouler hors de la borne positive principale (402), quand les éléments de l'ensemble d'éléments sont connectés à la première puce de commutation par le biais de la pluralité de bornes d'élément et quand les commutateurs d'un quatrième ensemble de la pluralité de commutateurs sont fermés et que les commutateurs restants de la pluralité de commutateurs sont ouverts, les éléments d'un sous-ensemble de l'ensemble d'éléments sont connectés en parallèle les uns par rapport aux autres, au moins un élément est déconnecté électriquement de chacun des autres éléments dans l'ensemble d'éléments, et le courant est en mesure de s'écouler au travers de l'ensemble d'éléments et hors de la borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la borne positive (582), et quand les éléments de l'ensemble d'éléments sont connectés à la première puce de commutation par le biais de la pluralité de bornes d'élément et quand les commutateurs d'un cinquième ensemble de la pluralité de commutateurs sont fermés et que les commutateurs restants de la pluralité de commutateurs sont ouverts, des éléments d'un autre sous-ensemble de l'ensemble d'éléments sont connectés en série les uns par rapport aux autres et au moins un élément en provenance de l'ensemble d'éléments est déconnecté électriquement de chacun des autres éléments de l'ensemble.
2. Bloc-batterie selon la revendication 1, les puces de commutation comportant par ailleurs : un décodeur de commande configuré pour effectuer un contrôle d'erreurs au niveau des commandes reçues par le circuit de communication en provenance du dispositif de commande principal ou en provenance d'une autre puce de commutation et configuré pour bloquer les commandes erronées.
  3. Bloc-batterie selon la revendication 2, les puces de commutation comportant par ailleurs : la logique de commande de commutation connectée au décodeur de commande et configurée pour convertir les commandes reçues par le circuit de communication en provenance du dispositif de commande principal en des commandes de commutation marche-arrêt à des fins de commutation d'éléments dans le bloc-batterie.
  4. Bloc-batterie selon la revendication 3, les puces de commutation comportant par ailleurs : un séquenceur de commutation de sécurité configuré pour recevoir les commandes marche-arrêt en provenance de la logique de commande de commutation et configuré à des fins de mise en marche ou arrêt selon une séquence et une temporisation exactes d'un ou de plusieurs parmi les commutateurs en fonction des commandes marche-arrêt reçues.
  5. Bloc-batterie selon la revendication 1, les puces de commutation comportant par ailleurs :  
un terminal d'entrée esclave ;  
un terminal de sortie maître ;  
le récepteur étant un bloc formant module de communication esclave ;  
l'émetteur étant un bloc formant module de communication maître ;  
un bloc formant décodeur de commande ;  
un bloc formant séquenceur de commutation de sécurité.
  6. Bloc-batterie selon la revendication 1, dans lequel les commutateurs de la pluralité de commutateurs comportent une pluralité de MOSFET (metal-oxide semiconductor field effect transistors - transistors à effet de champ à semi-conducteur à oxyde métallique) de puissance.
  7. Appareil de batterie, comportant :  
une première puce de commutation (301b), une deuxième puce de commutation, une troisième puce de commutation, et une quatrième puce de commutation, servant chacune à des fins d'interconnexion d'une pluralité d'éléments de batterie ; et  
chaque puce de commutation de la première puce de commutation (301b), de la deuxième puce de commutation, de la troisième puce de commutation, et de la quatrième puce de commutation comportant : une logique de commande de commutation, et un circuit de communication, dans lequel le circuit de communication comporte :  
un émetteur, et un récepteur,  
dans lequel chaque récepteur est connecté en communication lors de l'utilisation à soit un dispositif de commande principal soit un émetteur d'une puce de commutation adjacente de telle sorte que le récep-

teur sert à recevoir des commandes de commutation émises en provenance de soit le dispositif de commande principal soit l'émetteur de la puce de commutation adjacente, et dans lequel l'émetteur a pour objet d'émettre des commandes de commutation à une autre puce de commutation adjacente ; la première puce de commutation (301b) comportant par ailleurs une première pluralité de commutateurs, une première borne positive principale (402), une première borne négative principale (404), une première borne positive (582) et une première borne négative (581) ; et un ensemble d'éléments, l'ensemble d'éléments comportant :

- (i) un premier élément ayant une borne positive et une borne négative, la borne positive du premier élément étant connectée à une première borne d'élément de la première puce de commutation et la borne négative du premier élément étant connectée à une deuxième borne d'élément de la première puce de commutation, et
- (ii) un deuxième élément ayant une borne positive et une borne négative, la borne positive du deuxième élément est connectée à une troisième borne d'élément de la première puce de commutation et la borne négative du deuxième élément est connectée à une quatrième borne d'élément de la première puce de commutation,

la deuxième puce de commutation comportant par ailleurs : une deuxième pluralité de commutateurs, une deuxième borne positive principale et une deuxième borne négative principale, la deuxième borne positive principale de la deuxième puce de commutation étant connectée à la première borne négative principale de la première puce de commutation ; la troisième puce de commutation (301a) comportant : une troisième pluralité de commutateurs, une troisième borne positive principale, une troisième borne négative principale, et une deuxième borne négative (581), la deuxième borne négative (581) de la troisième puce de commutation (301a), étant connectée à la première borne positive (582) de la première puce de commutation (301b) ; et la quatrième puce de commutation (301) comportant : une quatrième pluralité de commutateurs, une quatrième borne positive principale et une quatrième borne négative principale, la quatrième borne positive principale de la quatrième puce de commutation étant connectée à la première borne positive principale de la première puce de commutation, dans lequel la première puce de commutation sert à :

- (i) configurer la première pluralité de commutateurs de telle sorte que (a) les éléments de l'ensemble d'éléments sont connectés en série, (b) le courant est en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive, et (c) le courant est en mesure de s'écouler jusqu'à la première puce de commutation par le biais de la première borne négative principale,
- (ii) configurer la première pluralité de commutateurs de telle sorte que (a) les éléments des ensembles d'éléments sont connectés en série, (b) le courant est en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive mais n'est pas en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive principale, et (c) le courant est en mesure de s'écouler jusqu'à la première puce de commutation par le biais de la première borne négative, et
- (iii) configurer la première pluralité de commutateurs de telle sorte que (a) les éléments de l'ensemble d'éléments sont connectés en parallèle, (b) le courant est en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la première puce de commutation par le biais de la première borne positive, et (c) le courant est en mesure de s'écouler jusqu'à la première puce de commutation par le biais de la première borne négative principale.

8. Appareil de batterie selon la revendication 7, dans lequel les première, deuxième, troisième et quatrième puces de commutation comportent chacune par ailleurs : un décodeur de commande configuré pour effectuer un contrôle d'erreurs au niveau des commandes reçues par le circuit de communication en provenance du dispositif de commande principal ou en provenance d'une autre puce de commutation et configuré pour bloquer les commandes erronées.
9. Appareil de batterie selon la revendication 8, dans lequel les première, deuxième, troisième et quatrième puces de commutation comportent chacune par ailleurs : la logique de commande de commutation connectée au décodeur de commande et configurée pour convertir les commandes reçues par le circuit de communication en provenance du dispositif de commande principal en des commandes de commutation marche-arrêt à des fins de commutation d'éléments

dans l'appareil de batterie.

10. Appareil de batterie selon la revendication 9, dans lequel les première, deuxième, troisième et quatrième puces de commutation comportent chacune par ailleurs :  
un séquenceur de commutation de sécurité configuré pour recevoir les commandes marche-arrêt en provenance de la logique de commande de commutation et configuré à des fins de mise en marche ou arrêt selon une séquence et une temporisation exactes d'un ou de plusieurs parmi les commutateurs en fonction des commandes marche-arrêt reçues. 5 10
11. Appareil de batterie selon la revendication 7, dans lequel le premier élément est un microélément et le deuxième élément est un microélément. 15
12. Appareil de batterie selon la revendication 7 comportant un bloc-batterie, le bloc-batterie comportant : 20
- un premier groupe de modules de batterie comportant une première colonne de modules de batterie et une deuxième colonne de modules de batterie ; 25
- un premier circuit servant à connecter la première colonne de modules de batterie en parallèle avec la deuxième colonne de modules de batterie ;
- un deuxième circuit servant à connecter la première colonne de modules de batterie en série avec la deuxième colonne de modules de batterie ; 30
- un deuxième groupe de modules de batterie comportant une troisième colonne de modules de batterie et une quatrième colonne de modules de batterie ; 35
- un troisième circuit servant à connecter la troisième colonne de modules de batterie en parallèle avec la quatrième colonne de modules de batterie ; 40
- un quatrième circuit servant à connecter la troisième colonne de modules de batterie en série avec la quatrième colonne de modules de batterie, dans lequel 45
- au moins l'un des modules de batterie dans la première colonne de modules de batterie a (i) un commutateur servant à connecter et à déconnecter une sortie principale du module de batterie par rapport au premier circuit et (ii) un commutateur servant à connecter et à déconnecter une sortie du module de batterie par rapport au deuxième circuit, 50
- au moins l'un des modules de batterie dans la deuxième colonne de modules de batterie a (i) un commutateur servant à connecter et à déconnecter une sortie principale du module de batterie par rapport au premier circuit et (ii) un 55

commutateur servant à connecter et à déconnecter une sortie du module de batterie par rapport au deuxième circuit, au moins l'un des modules de batterie dans la troisième colonne de modules de batterie a (i) un commutateur servant à connecter et à déconnecter une sortie principale du module de batterie par rapport au troisième circuit et (ii) un commutateur servant à connecter et à déconnecter une sortie du module de batterie par rapport au quatrième circuit, et au moins l'un des modules de batterie dans la quatrième colonne de modules de batterie a (i) un commutateur servant à connecter et à déconnecter une sortie principale du module de batterie par rapport au troisième circuit et (ii) un commutateur servant à connecter et à déconnecter une sortie du module de batterie par rapport au quatrième circuit.

13. Appareil de batterie selon la revendication 12, dans lequel le dispositif de commande principal sert à :

- (a) placer le bloc-batterie dans un premier mode de fonctionnement dans lequel le bloc-batterie produit une tension  $V_1$  ; et  
(b) placer le bloc-batterie dans un deuxième mode de fonctionnement dans lequel le bloc-batterie produit une tension  $V_2$ , où  $V_2 > V_1$ .

14. Appareil de batterie selon la revendication 13, dans lequel au moins l'un des modules de batterie comporte :  
une puce de commutation comportant : une pluralité de commutateurs, une borne positive principale, une borne négative principale, une borne positive et une borne négative ; et  
un ensemble d'éléments comportant (i) un premier élément ayant une borne positive et une borne négative, la borne positive étant connectée à une première borne d'élément de la puce de commutation et la borne négative étant connectée à une deuxième borne d'élément de la puce de commutation, et (ii) un deuxième élément ayant une borne positive et une borne négative, la borne positive est connectée à une troisième borne d'élément de la puce de commutation et la borne négative est connectée à une quatrième borne d'élément de la puce de commutation.
15. Appareil de batterie selon la revendication 14, dans lequel le dispositif de commande principal sert à :

- (i) amener ledit au moins l'un des modules de batterie à configurer les commutateurs de la pluralité de commutateurs de telle sorte que (a) les éléments de l'ensemble d'éléments sont connectés en série, (b) le courant est en mesure de

s'écouler hors de la puce de commutation par le biais de la borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la puce de commutation par le biais de la borne positive, et (c) le courant est en mesure de s'écouler jus- 5  
que dans la puce de commutation par le biais de la borne négative principale mais n'est pas en mesure de s'écouler jusque dans la puce de commutation par le biais de la borne négative, 10  
(ii) amener ledit au moins l'un des modules de batterie à configurer les commutateurs de la pluralité de commutateurs de telle sorte que (a) les éléments de l'ensemble d'éléments sont connectés en série, (b) le courant est en mesure de s'écouler hors de la puce de commutation par le biais de la borne positive mais n'est pas en mesure de s'écouler hors de la puce de commutation par le biais de la borne positive principale, et (c) le courant est en mesure de s'écouler 15  
jusque dans la puce de commutation par le biais de la borne négative mais n'est pas en mesure de s'écouler jusque dans la puce de commutation par le biais de la borne négative principale, 20  
et  
(iii) amener ledit au moins l'un des modules de batterie à configurer les commutateurs de la pluralité de commutateurs de telle sorte que (a) les éléments de l'ensemble d'éléments sont connectés en parallèle, (b) le courant est en mesure de s'écouler hors de la puce de commutation 25  
par le biais de la borne positive principale (402) mais n'est pas en mesure de s'écouler hors de la puce de commutation par le biais de la borne positive, et (c) le courant est en mesure de s'écouler jusque dans la puce de commutation 30  
par le biais de la borne négative principale mais n'est pas en mesure de s'écouler jusque dans la puce de commutation par le biais de la borne négative. 35

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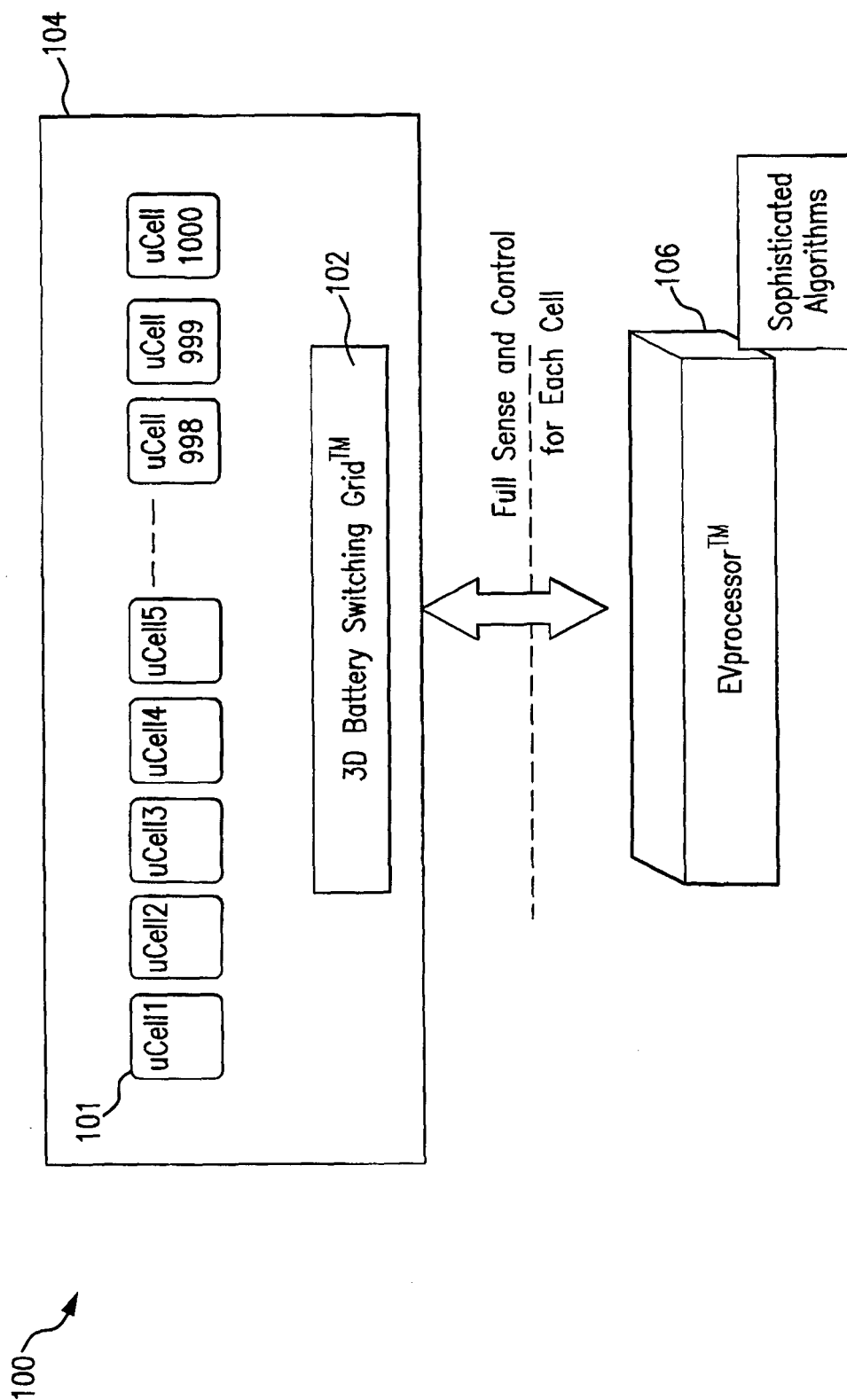


FIG.1

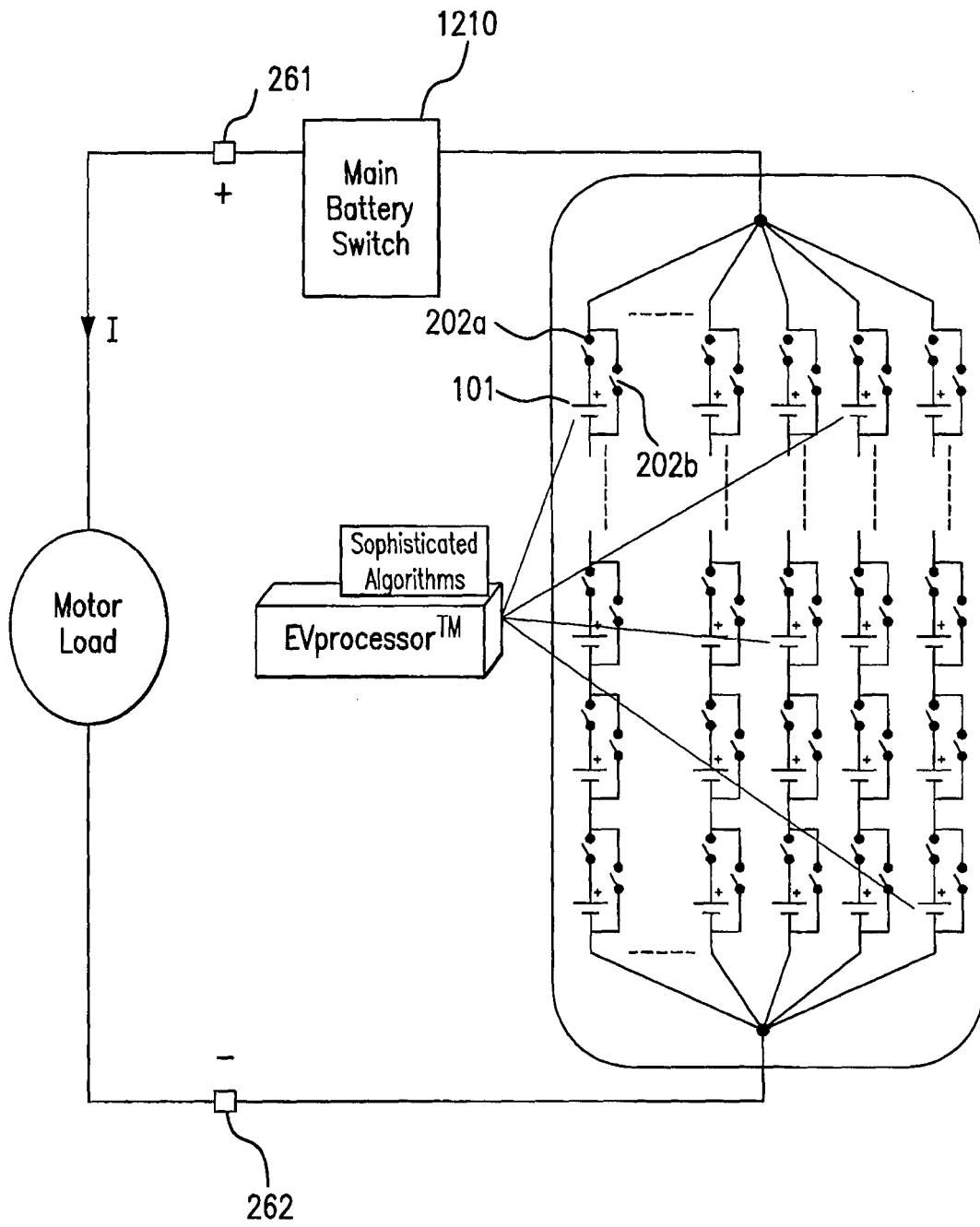


FIG.2



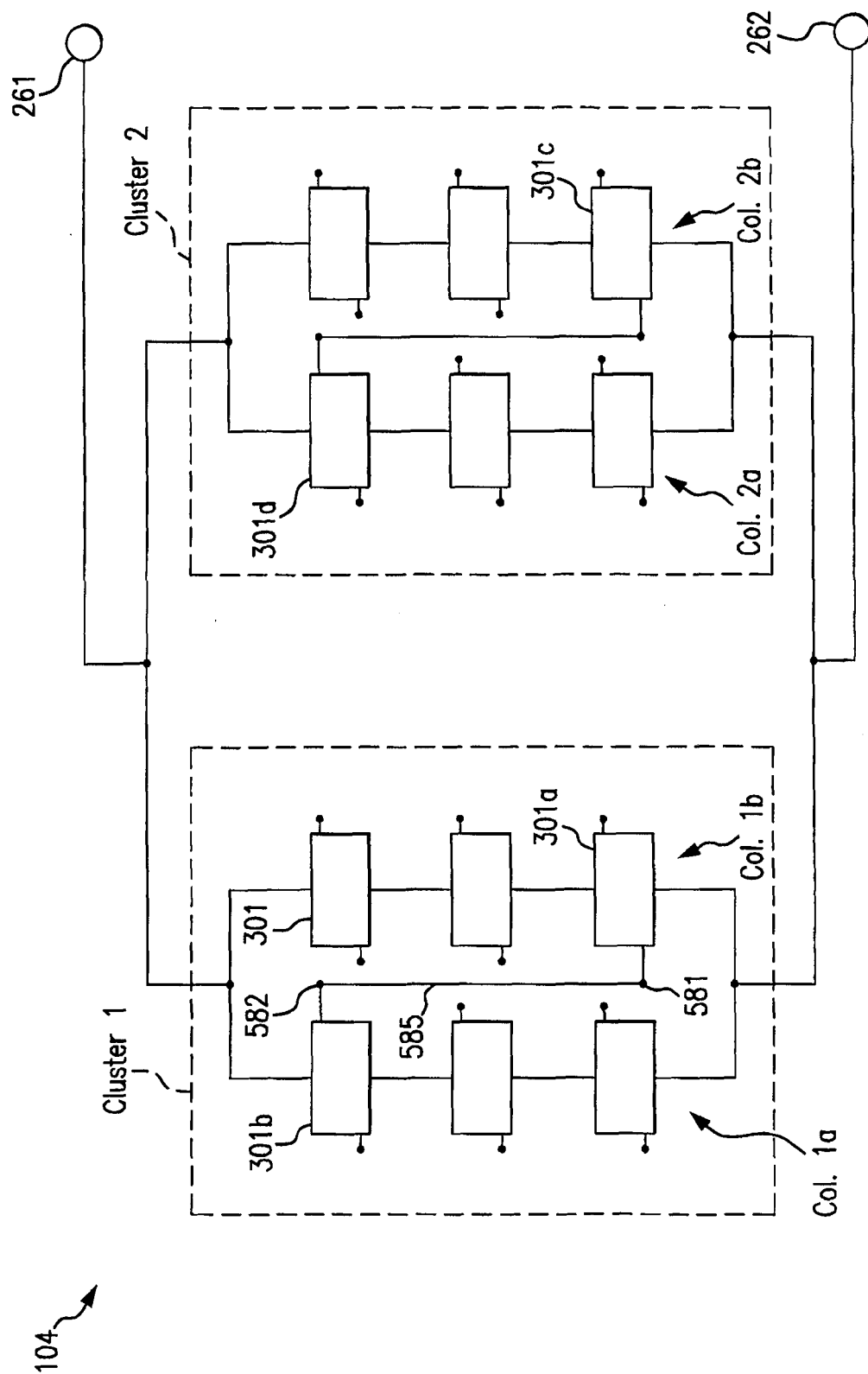


FIG.3

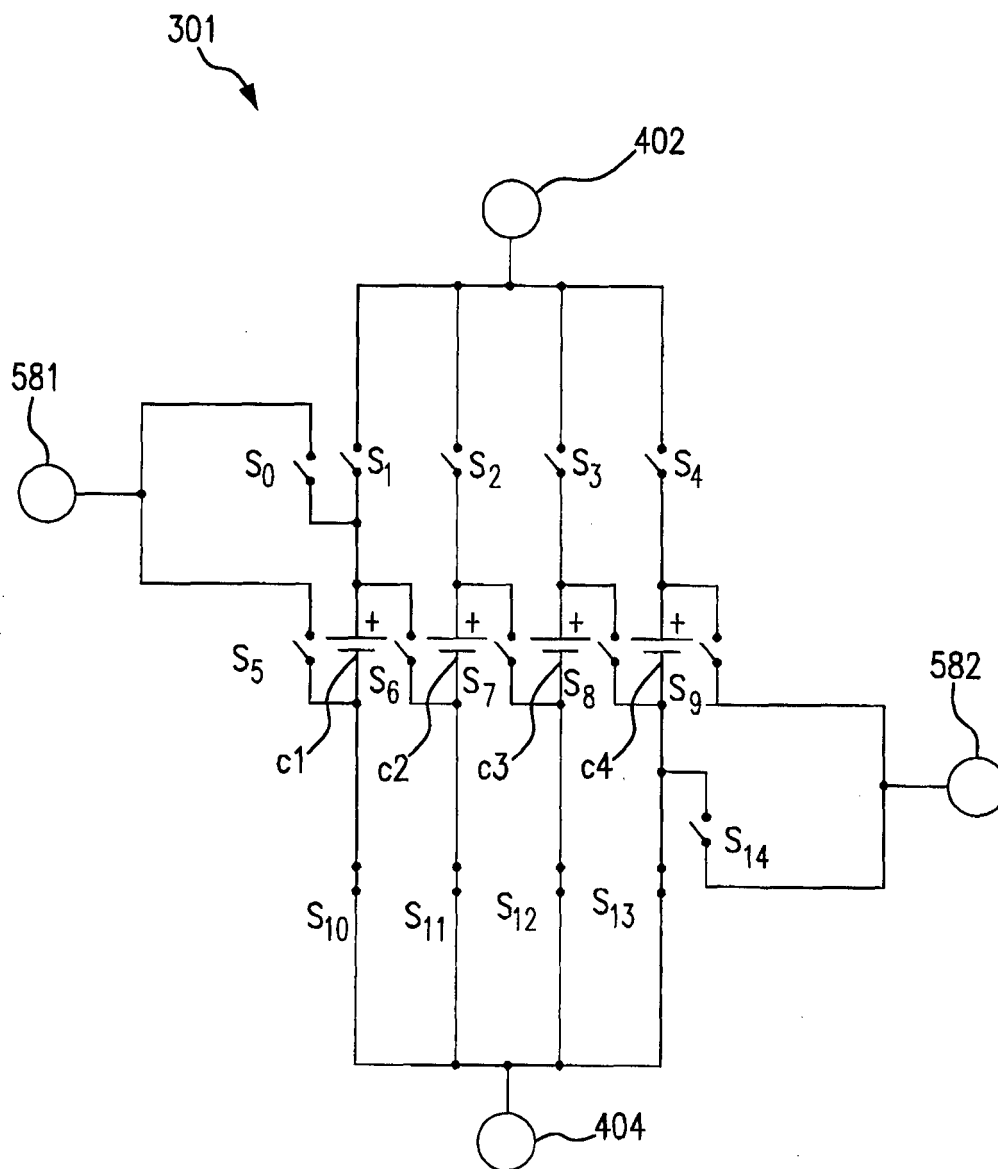


FIG.4

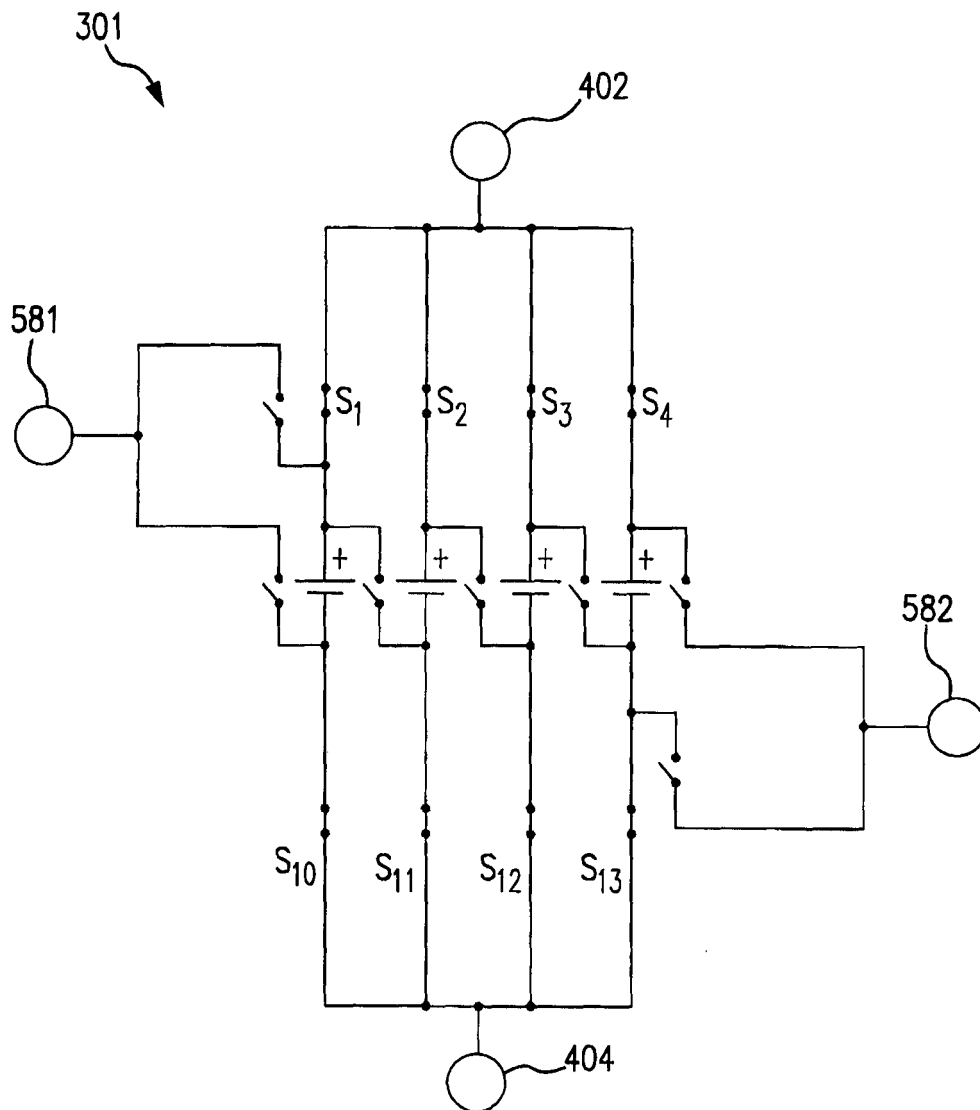


FIG.5

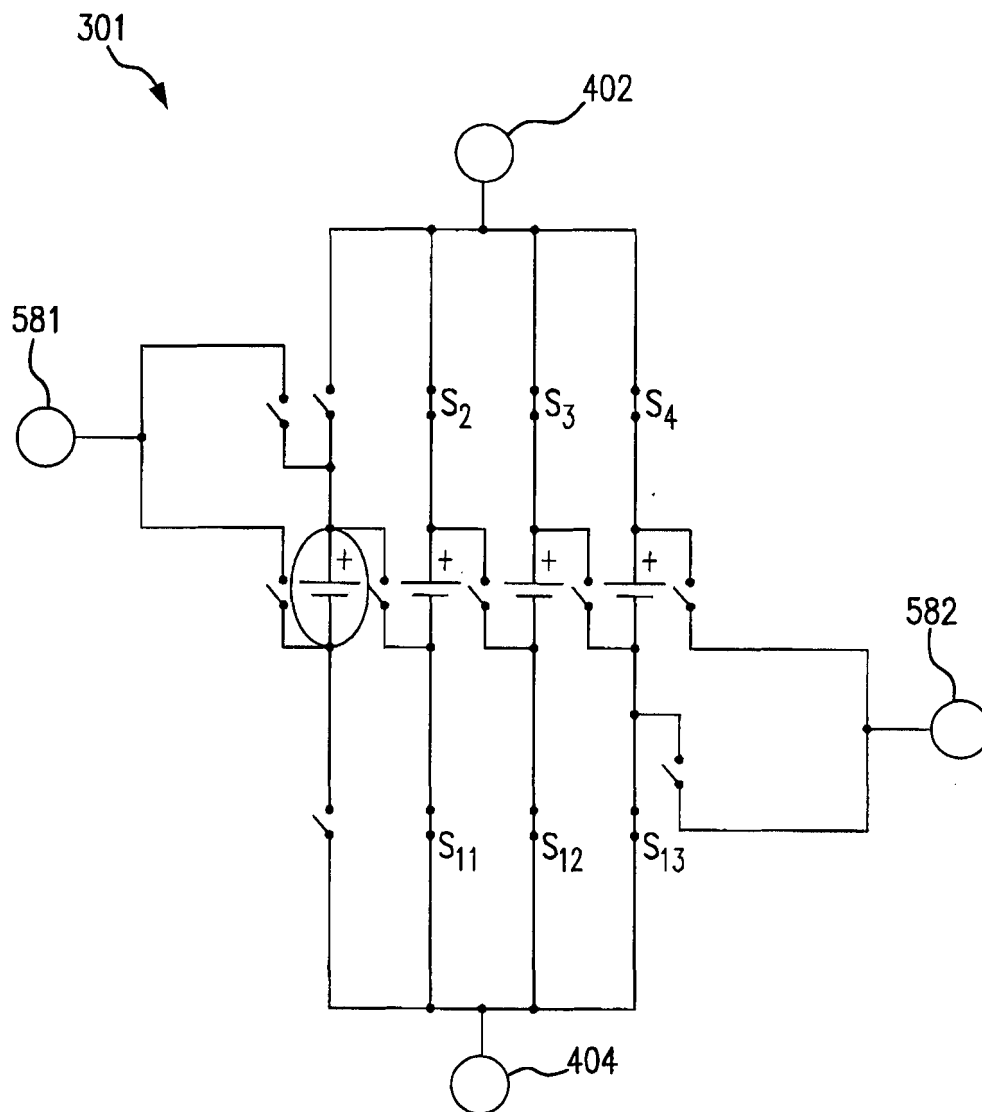


FIG.6

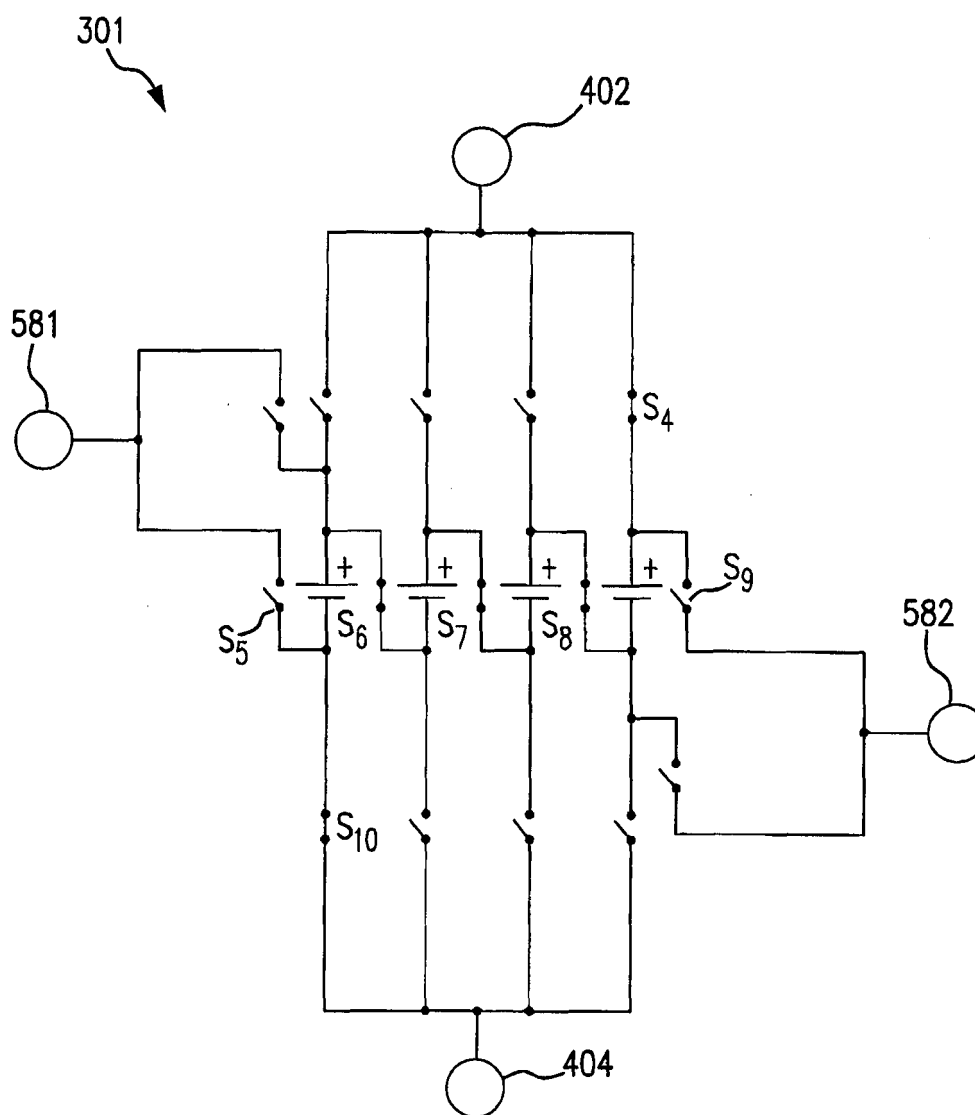


FIG.7

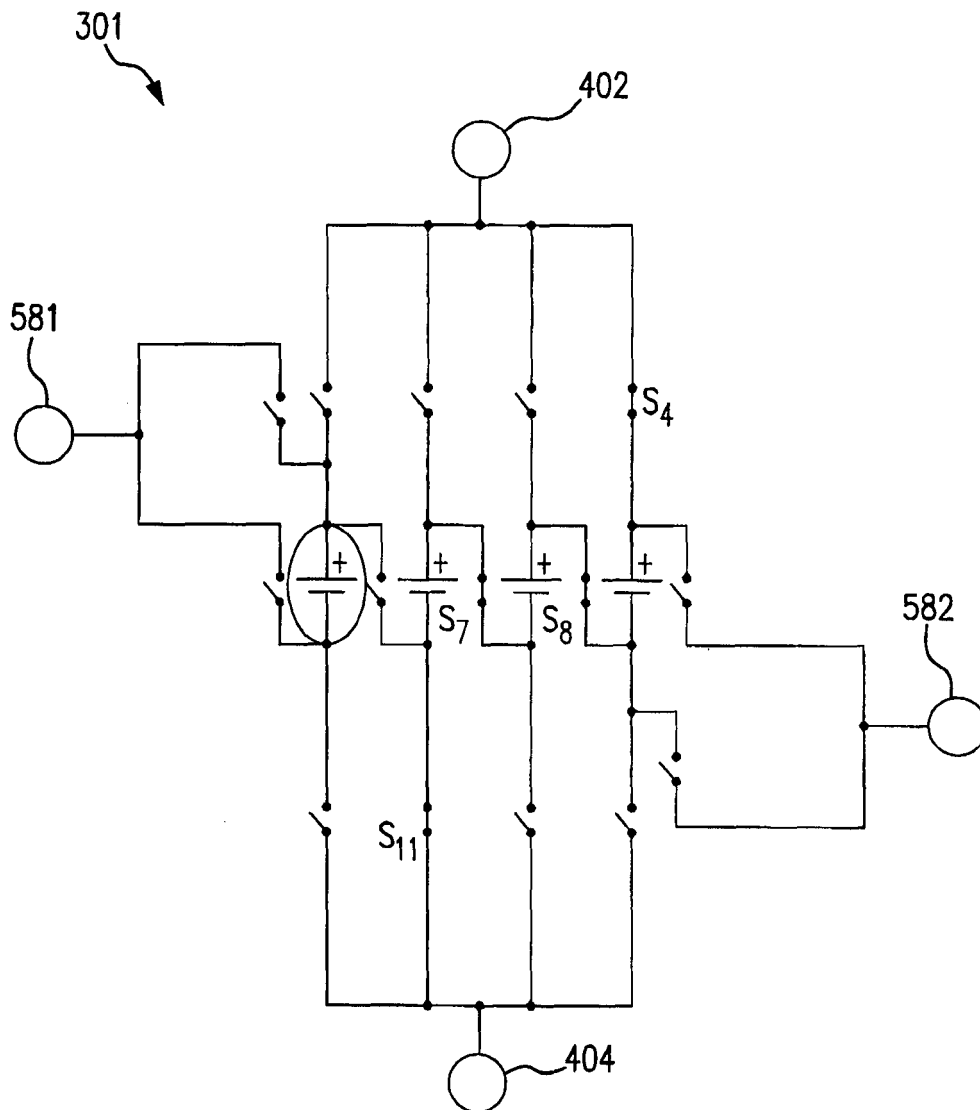


FIG.8

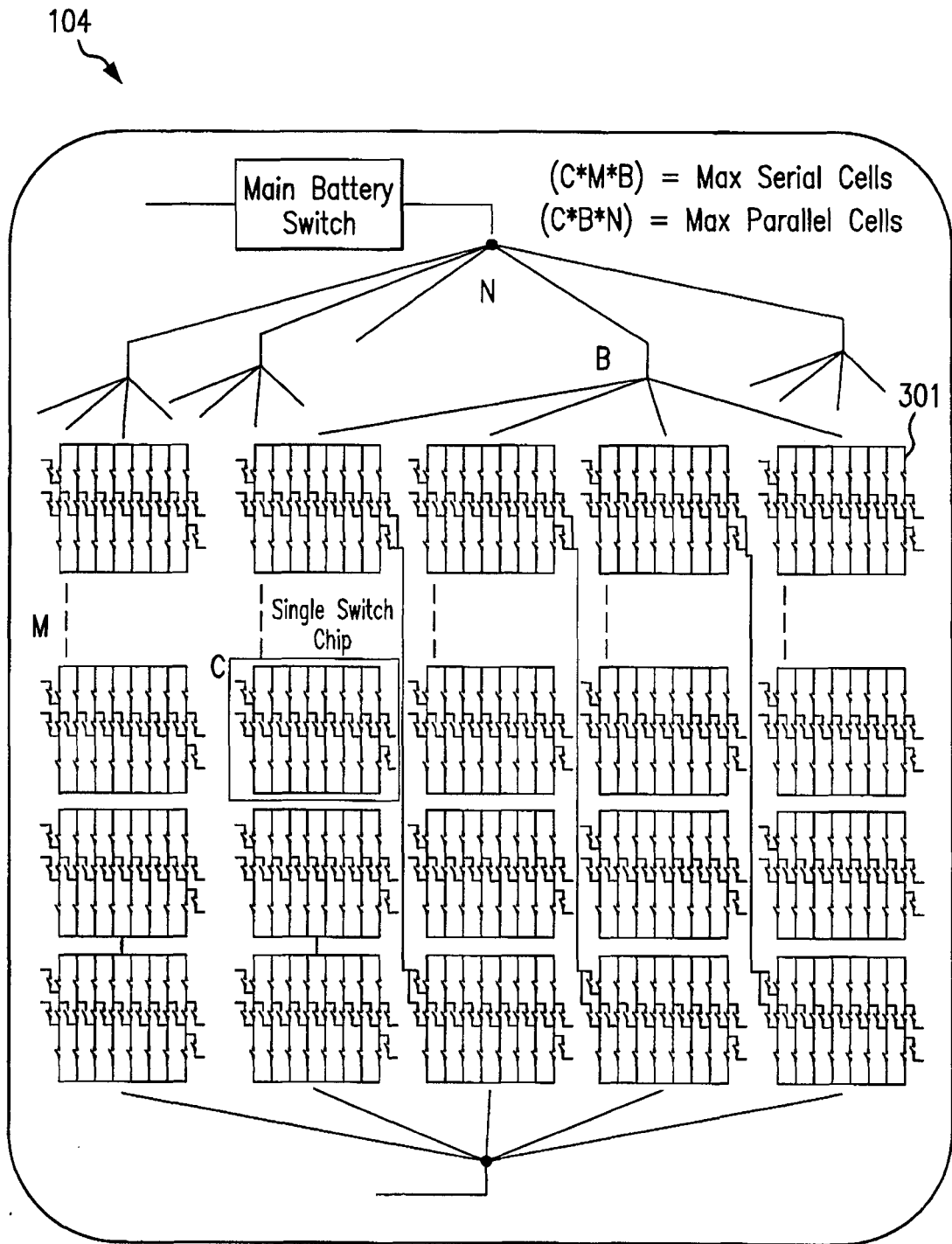
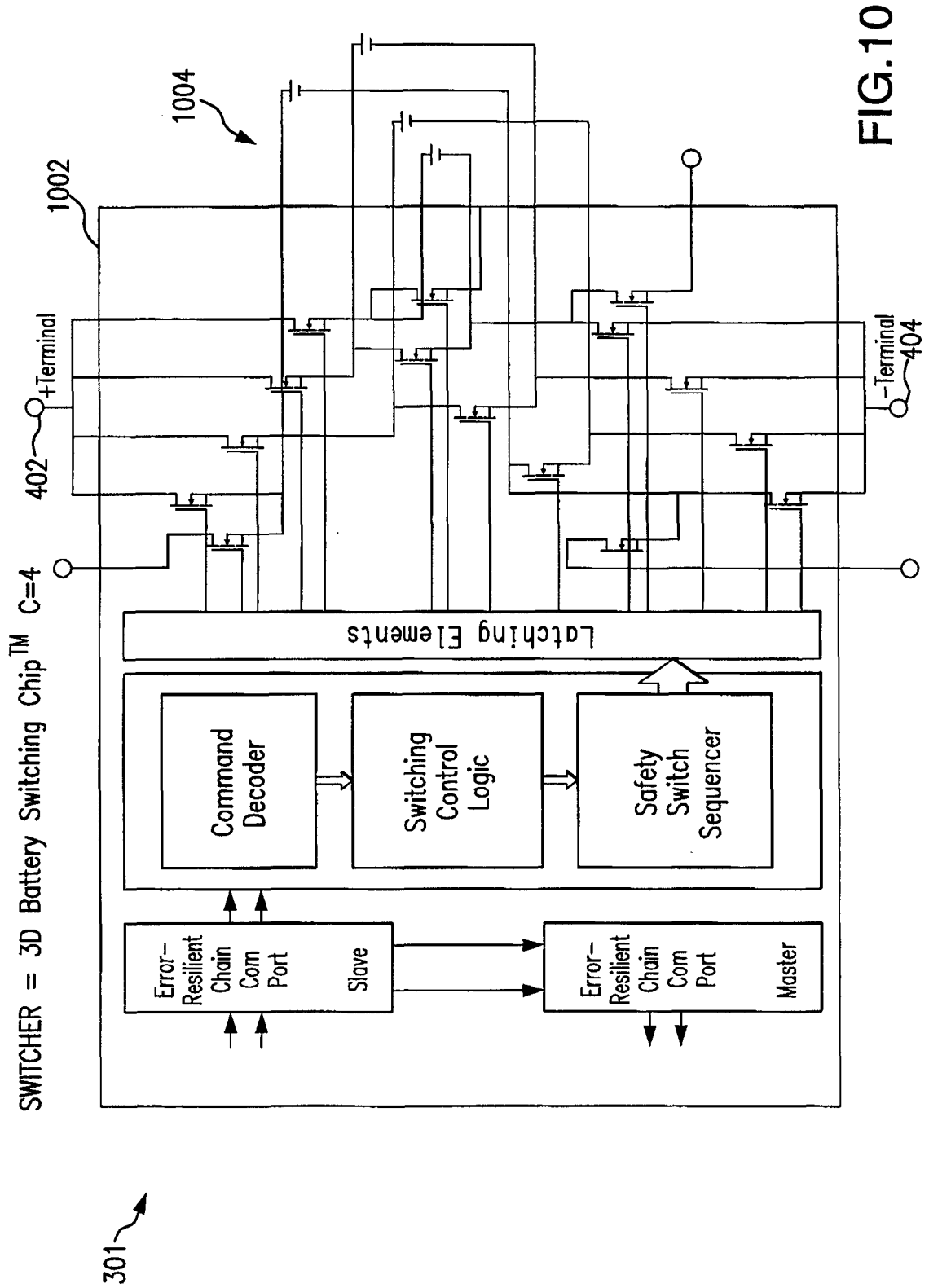


FIG. 9





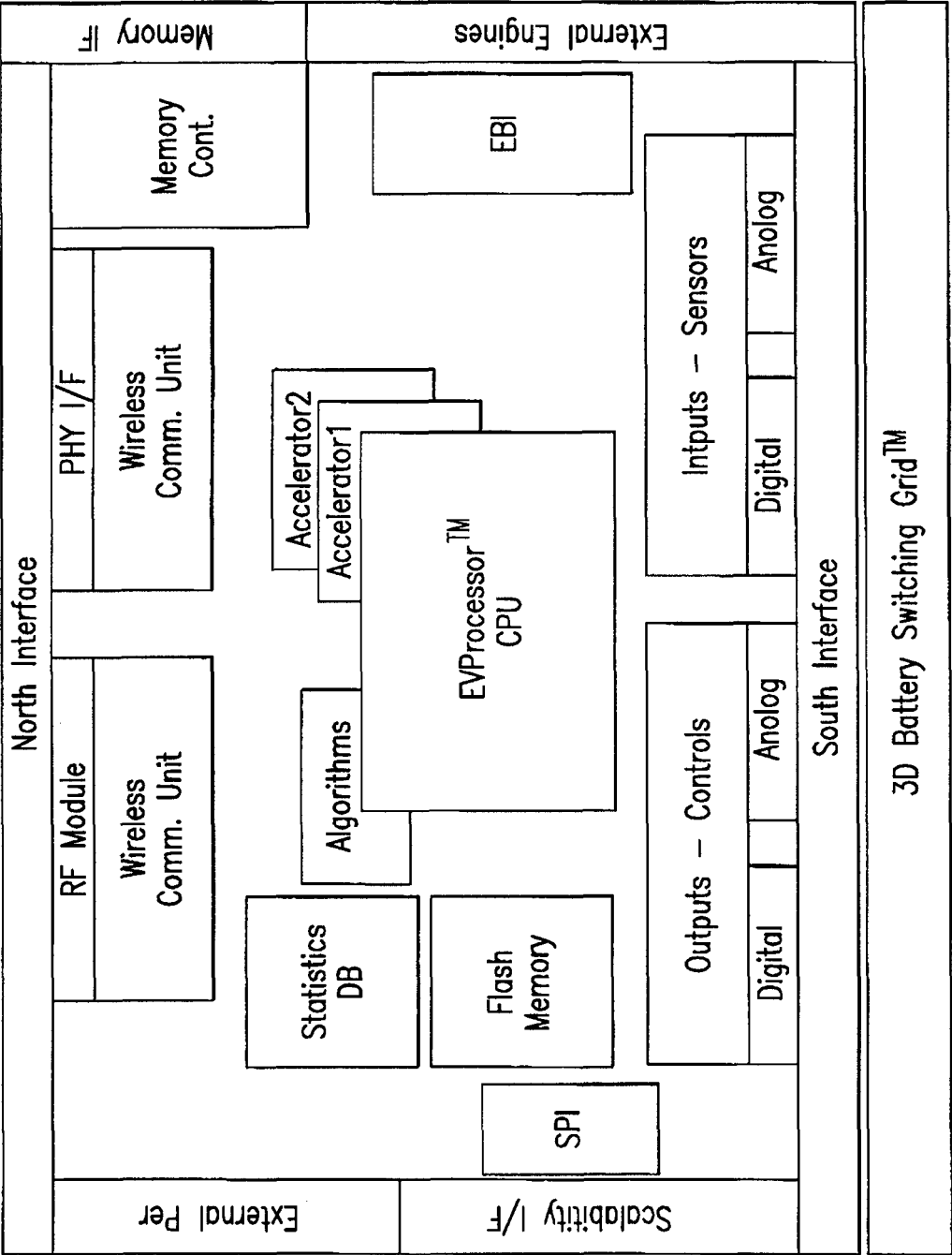


FIG.11

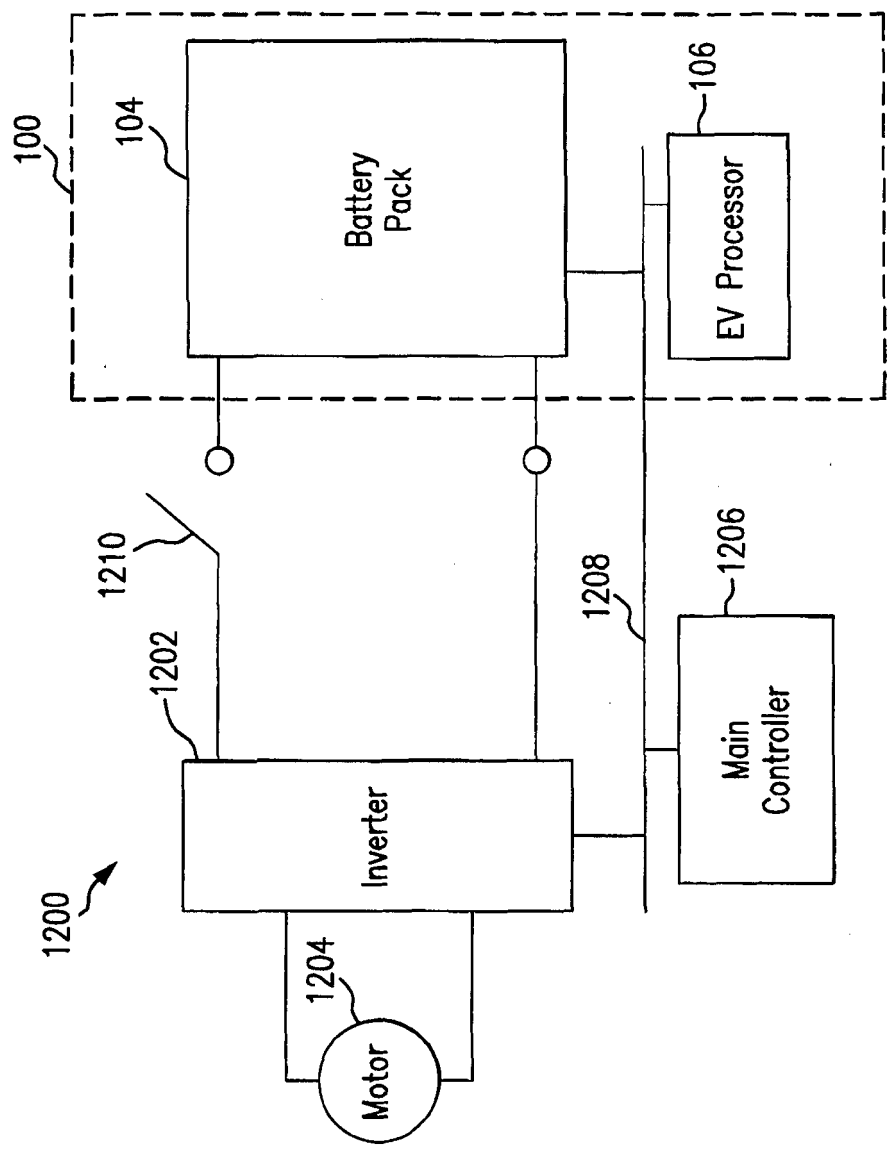


FIG.12

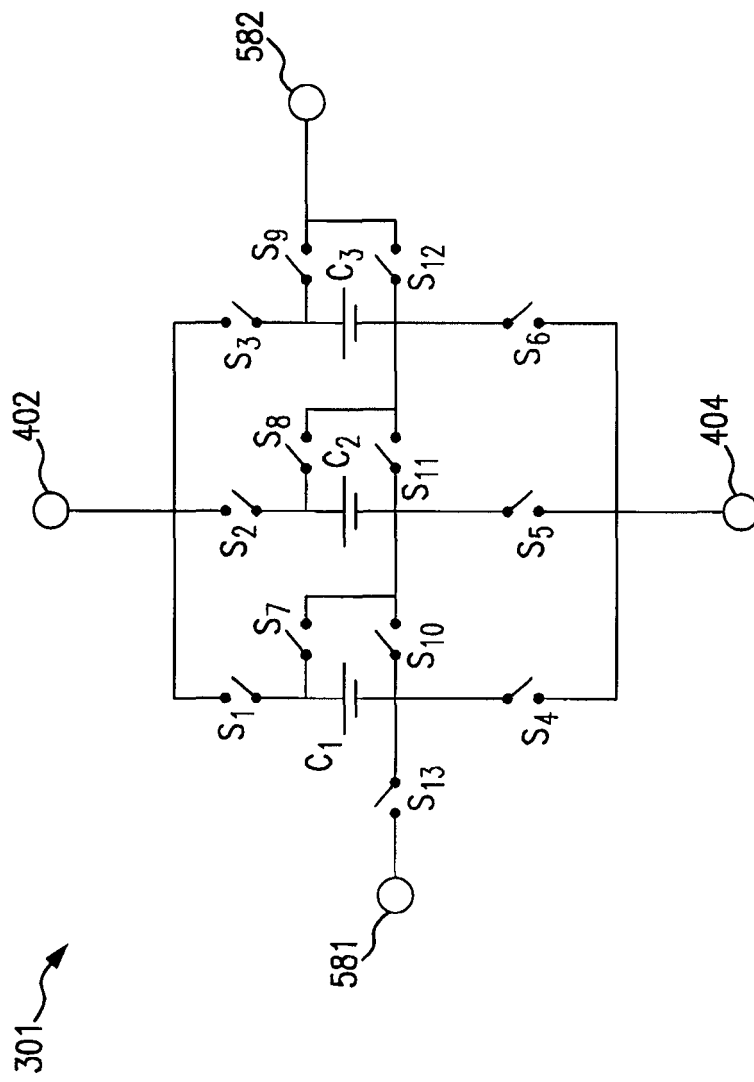


FIG.13

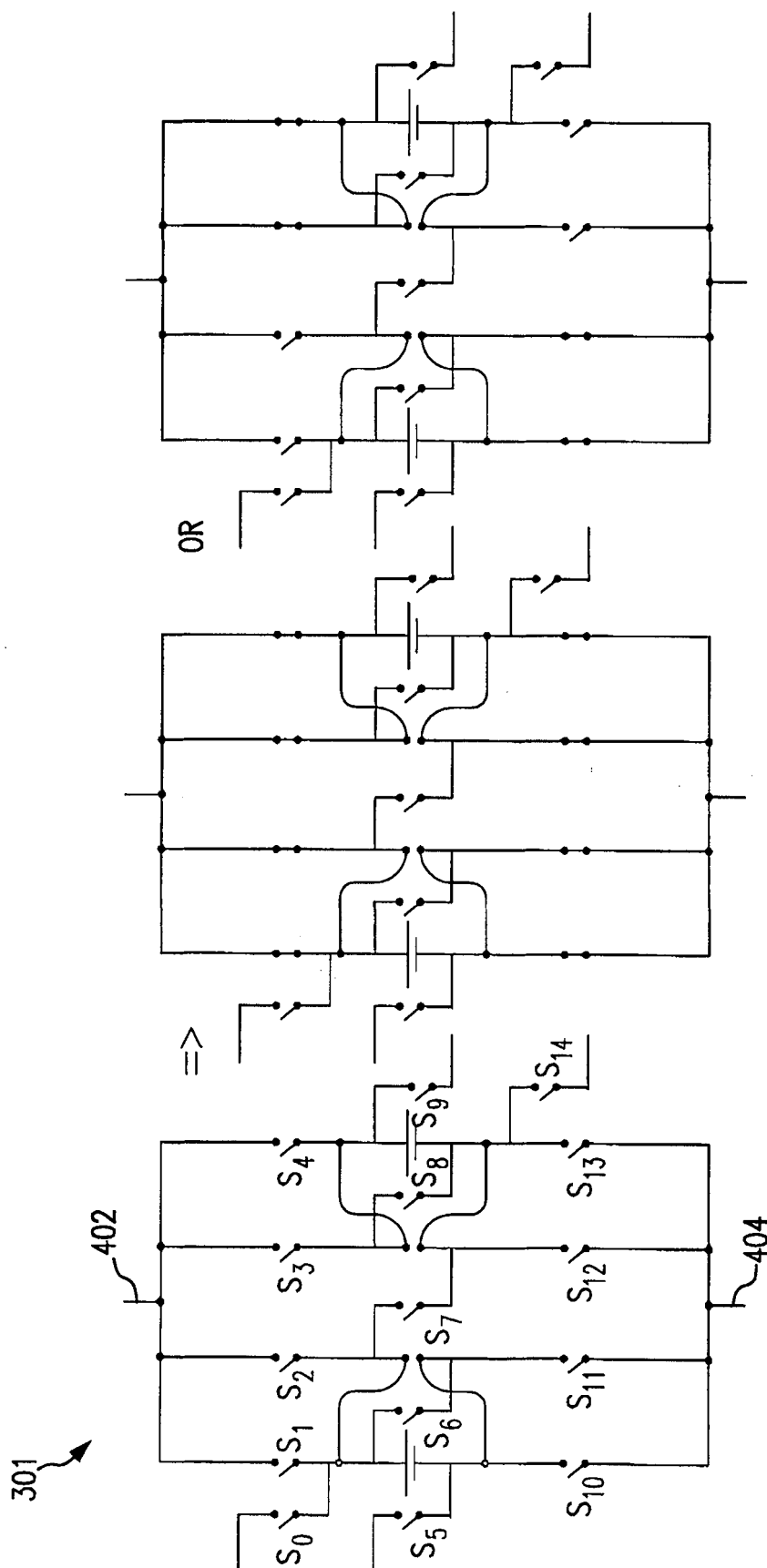


FIG. 14A

FIG. 14B

FIG. 14C

**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

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