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(54) METHODS OF FORMING AT LEAST ONE CONDUCTIVE ELEMENT, METHODS OF FORMING A SEMICONDUCTOR STRUCTURE, METHODS OF FORMING A MEMORY CELL AND RELATED SEMICONDUCTOR STRUCTURES

VERFAHREN ZUR HERSTELLUNG MINDESTENS EINES LEITFÄHIGEN ELEMENTS, VERFAHREN ZUR HERSTELLUNG EINER HALBLEITERANORDNUNG, VERFAHREN ZUR HERSTELLUNG EINER SPEICHERZELLE UND ZUGEHÖRIGE HALBLEITERSTRUKTUREN

PROCÉDÉS DE FORMATION D'AU MOINS UN ÉLÉMENT CONDUCTEUR, PROCÉDÉS DE FORMATION D'UNE STRUCTURE SEMI-CONDUCTRICE, PROCÉDÉS DE FORMATION D'UNE CELLULE DE MÉMOIRE ET STRUCTURES SEMI-CONDUCTRICES ASSOCIÉES

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(73) Proprietor: **Micron Technology, Inc.**
Boise, ID 83707-0006 (US)

(72) Inventors:
- **TANG, Sanh D.**
  Boise, Idaho 83709 (US)
- **SILLS, Scott E.**
  Boise, Idaho 83705 (US)
- **WEST, Whitney L.**
  Boise, Idaho 83704 (US)
- **GOODWIN, Rob B.**
  Eagle, Idaho 83616 (US)
- **SINHA, Nishant**
  Boise, Idaho 83716 (US)

(74) Representative: **Maury, Richard Philip**
Marks & Clerk LLP
90 Long Acre
London WC2E 9RA (GB)

(56) References cited:
US-A1- 2003 041 452
US-A1- 2003 143 838
US-A1- 2006 084 271
US-A1- 2007 145 586
US-A1- 2008 036 508
US-A1- 2008 253 165
US-A1- 2010 193 758

- **USHIKU Y. ET AL.: 'Planarized silver interconnect technology with a Ti self-p assivation technique for deep sub-micron ULSIs' VLSI TECHNOLOGY 1993 DIGEST OF TECHNICAL PAPERS 1993, pages 121 - 122, XP032368389**

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Description

TECHNICAL FIELD

[0001] Embodiments of the present disclosure relate to methods of forming conductive elements for semiconductor devices and, in addition, to semiconductor structures that include such conductive elements.

BACKGROUND

[0002] Integrated circuits (ICs), the key components in thousands of electronic systems, generally include interconnected networks of electrical components fabricated on a common foundation, or substrate. Conductive interconnects are used to electrically connect semiconductor devices, such as capacitors or transistors, or to define a specific IC, such as a computer memory or microprocessor. The quality of the conductive interconnects greatly affects overall manufacturability, performance and lifetime of the IC. Thus, the material used to form the conductive interconnects is increasingly determining the limits in performance, density and reliability of integrated circuits.

[0003] For example, electrical conductivity of interconnects is extremely significant to the operational speed of the integrated circuit (IC). Aluminum (Al) and alloys thereof have been widely used as interconnect materials in semiconductor devices based on their low resistivity and ready adhesion to interlayer dielectric materials, such as silicon dioxide (SiO_2). Unfortunately, aluminum is susceptible to corrosion and offers poor resistance to electromigration, which increases the potential for open circuits from voids or short circuits.

[0004] In an attempt to improve the performance, reliability, and density of the conductive interconnects, alternative metals to aluminum and aluminum alloys are being explored. To improve conductivity in the wiring, it has been proposed that copper (Cu) and alloys thereof be used to form conductive interconnects. However, copper rapidly diffuses through many conventional dielectric materials to form undesired copper oxide compounds. In addition, copper does not adhere well to conventional dielectric materials or to itself.

[0005] Silver (Ag) has also been proposed as a substitute for aluminum-containing conductive interconnects and is becoming increasingly significant in use as an electrochemically active material in electrodes of programmable memory cells, such as those of conductive bridge random access memory (CBRAM) cell. Silver has an extremely low resistivity, but is difficult to deposit in narrow gaps (e.g., gaps having a dimension of 20 nm or less) due to limitations on currently available deposition techniques. While silver may be deposited by sputtering (physical) deposition techniques, these techniques are not suitable for filling narrow gaps with silver. Furthermore, interconnects have been difficult to form from silver due to adhesion issues and agglomeration at increased temperatures. Since silver is resistant to dry etch processes, conventional techniques for forming semiconductor conductive elements (e.g., interconnects and electrodes) are impractical for making such conductive elements from silver.

[0006] Methods and structures of the prior art are described by US 2008 / 0253165 A1 and US 2003 / 0143838 A1.

SUMMARY

[0007] In one embodiment, the present disclosure provides a method of forming a semiconductor structure as defined by claim 1.

[0008] In yet another embodiment, the present disclosure includes a semiconductor structure as defined by claim 15.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

FIGS. 1A through 1E are partial cross-sectional views of a semiconductor structure and illustrate a method of forming an interconnect in accordance with embodiments of the present disclosure;

FIGS. 2A through 2E are partial cross-sectional views of a semiconductor structure and illustrate another method of forming an interconnect in accordance with embodiments of the present disclosure;

FIG. 3A is a partial cross-sectional view of a conductive bridge random access memory (CBRAM) cell; and

FIGS. 3B through 3D are partial cross-sectional views of a semiconductor structure and illustrate a method of forming the CBRAM cell shown in FIG. 3A in accordance with embodiments of the present disclosure.

MODE(S) FOR CARRYING OUT THE INVENTION

[0010] Methods of forming conductive elements, such as interconnects and electrodes, are disclosed, as are semiconductor structures and memory devices that include such conductive elements. The conductive element is formed from a silver material, such as silver or a silver alloy. Since silver has low resistivity and alloys and mixtures with other materials, the resistivity of the conductive element may be less than or equal to that of a conductive element formed from copper. In addition, use of a silver alloy or silver mixture may substantially reduce or eliminate issues with agglomeration associated with silver during thermal processing acts conducted at a later stage of semiconductor processing including such conductive elements. Using silver, a silver alloy or a silver mixture may also enable narrow openings, such as those having at least one dimension of less than about 20 nm, to be filled.

[0011] As used herein, the term "alloy" means and includes means and includes a homogeneous mixture or solid solution of a plurality of materials (e.g., metals or nonmetals), atoms of one of the materials occupying interstitial positions between atoms of another one of the materials. By way example and not limitation, an alloy may include a mixture of silver and a metal selected from platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium.

[0012] As used herein, the term "mixture" means and includes a material formed by mixing a plurality of metals, or a metal and a nonmetal. By way example and not limitation, a mixture may include a mixture of silver and a metal such as tungsten.

[0013] As used herein, the term "liner" means and includes any structure overlies a surface of at least one material. By way example and not limitation, a liner may include a layer of material disposed over another material.

[0014] As used herein, the term "adhesion material" means and includes a material selected to facilitate adhesion of a first material to a second material immediately adjacent the first material.

[0015] As used herein, the term "chalcogenide" means and includes a material, including a glass or crystalline material, that includes an element from Group VIA (also identifiable as Group 16) of the periodic table of elements. Group VIA elements, often referred to as "chalcogens," include sulfur (S), selenium (Se), tellurium (Te), polonium (Po) and oxygen (O). Examples of chalcogenides include, but are not limited to, germanium selenide (GeSe), germanium sulfide (GeS), germanium telluride (GeTe), indium selenide (InSe) and antimony selenide (SbSe). While the exemplary chalcogenides have a stoichiometry of one atom of each element, the chalcogenide may have other stoichiometries.

[0016] As used herein, the terms "redistribute" and "redistributing" mean and include spreading or smearing a material across a surface and into a partially filled, lined or, previously unfilled opening (e.g., via, trench) in a structure to fill or substantially fill the opening with the material.

[0017] As used herein, the term "substrate" means and includes a base material or construction upon which additional materials are formed. The substrate may be a semiconductor substrate, a base semiconductor layer on a supporting structure, a metal electrode or a semiconductor substrate having one or more layers, structures or regions formed thereon. The substrate may be a conventional silicon substrate or other bulk substrate comprising a layer of semiconductive material. As used herein, the term "bulk substrate" means and includes not only silicon wafers, but also silicon-on-insulator ("SOI") substrates, such as silicon-on-sapphire ("SOS") substrates and silicon-on-glass ("SOG") substrates, epitaxial layers of silicon on a base semiconductor foundation, and other semiconductor or optoelectronic materials, such as silicon-germanium, germanium, gallium arsenide, gallium nitride, and indium phosphide. The substrate may be doped or undoped.

[0018] The following description provides specific details, such as material types and processing conditions in order to provide a thorough description of embodiments of the present disclosure. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details. Indeed, the embodiments of the present disclosure may be practiced in conjunction with conventional semiconductor fabrication techniques employed in the industry. In addition, the description provided below does not form a complete process flow for manufacturing a semiconductor device. The semiconductor structures described below do not necessarily form a complete semiconductor device. Only those process acts and structures necessary to understand the embodiments of the present disclosure are described in detail below. Additional acts to form a complete semiconductor device from the semiconductor structures may be performed by conventional fabrication techniques.

[0019] FIGS. 1A through 1E are simplified partial cross-sectional views of a semiconductor structure 100 illustrating embodiments of a method of forming interconnects. Referring to FIG. 1A, the semiconductor structure 100 includes an opening 106 in a material 104 overlying a substrate 102. The material 104 may be formed from silicon nitride (Si_3N_4), silicon dioxide (SiO_2) or a silicon oxynitride (SiO_xN_y), for example. The material 104 may be formed over the substrate 102 using a conventional deposition process, such as a chemical vapor deposition process, an atomic layer deposition process or a physical vapor deposition process.

[0020] The semiconductor structure 100 may, optionally, include an electrode material 108 (shown in broken lines) between the material 104 and the substrate 102. The electrode material 108 may be formed from a conductive material, such as, tungsten (W), platinum (Pt), titanium nitride (TiN) or nickel (Ni). The electrode material 108 may be formed over the substrate 102 using conventional deposition process, such as, a chemical vapor deposition process or an atomic layer deposition process. While FIGs. 1A through 1E indicate that the electrode material 108 is present, it is understood that the electrode material 108 is optional and that material 104 may be in direct contact with substrate 102 with the opening 106 extending at least partially through material 104.

[0021] The opening 106 may be formed by removing a portion of the material 104 using, for example, conventional photolithography techniques (e.g., masking and etching) known in the art of integrated circuit fabrication. By way of non-limiting example, the opening 106 may extend longitudinally into a plane of FIG. 1 A. Removing the portion of the material 104 may expose a surface of the material 104 or, if present, a surface of the electrode material 108. By way of example and not limitation, the opening 106 may have a width w1 of less than about 100 nm and, more particularly, less than about 20 nm. The

aspect ratio of the opening 106 may be between about 1:1 and about 20:1 and, more particularly, between about 5:1 and about 10:1. The elements shown in the FIG. 1 A and the following figures have been drawn for the purposes of illustration and should not be understood as being drawn to scale.

[0022] Referring to FIG. 1B, a liner material 110 is formed over surfaces of the semiconductor structure 100 (i.e., exposed surfaces of the material 104 and, if present, the electrode material 108). For example, the liner material 110 may be formed over surfaces exposed within the opening 106 (i.e., exposed sidewalls of the material 104 and an exposed surface of the electrode material 108, if present) as well as exposed, unrecessed surfaces of the material 104. In embodiments in which the electrode material 108 is present, the liner material 110 may be formed from a material that facilitates adhesion to and reduces contact resistance in the electrode material 108, or provides both characteristics. For example, the liner material 110 may be formed from at least one of platinum (Pt), tantalum (Ta), aluminum (Al), tin (Sn), copper (Cu), iridium (Ir), titanium (Ti), nickel (Ni), cobalt (Co), ruthenium (Ru) and rhodium (Rh). The liner material 110 may be formed using a conventional deposition process, such as, a chemical vapor deposition process, a physical vapor deposition process or a sputtering process. By way of example and not limitation, the liner material 110 may be formed having a thickness of between about 0.5 nm and about 20 nm and, more particularly, between about 1 nm and about 5 nm.

[0023] Referring to FIG. 1C, a conductive material 112 is formed over the liner material 110. The conductive material 112 may be formed from silver (Ag) or an alloy or a mixture thereof using a conventional deposition process, such as, a physical vapor deposition process or a physical deposition process. Conventional vapor deposition processes (e.g., chemical vapor deposition and physical vapor deposition) may not effectively deposit silver in narrow openings (e.g., openings having at least one dimension of less than or equal to 20 nm). Thus, in embodiments in which at least one dimension (i.e., the width w1) of the opening 106 is less than or equal to about 20 nm, a sputtering process may be used to form the conductive material 112 within the opening 106. By way of non-limiting example, the conductive material 112 may be substantially conformally deposited over an entire exposed surface of the liner material 110. The conductive material 112 may be formed having a thickness sufficient to at least partially fill the remaining portion of the opening 106. As shown in FIG. 1 C, a portion of the opening 106 remains unfilled (i.e., unfilled region 116) after the conductive material 112 has been formed on the semiconductor structure 100. By way of example and not limitation, the conductive material 112 may be formed from silver and have a thickness of between about 5 nm and about 30 nm and, more particularly, between about 10 nm and about 20 nm.

[0024] The thicknesses of the liner material 110 and the conductive material 112 may be selected based on a desired ratio of materials. In embodiments in which the liner material 110 includes platinum and the conductive material 112 includes silver, a ratio of the liner material 110 to the conductive material 112 may be less than or equal to about 1 to 2.

[0025] Referring to FIG. 1D, in embodiments in which the liner material 110 (shown in broken lines) includes a material that forms an alloy with the conductive material 112, an annealing process is performed to form an alloy of the liner material 110 and the conductive material 112. By reacting the liner material 110 and the conductive material 112, an intermetallic compound is formed. For example, the conductive material 112 may include silver, the liner material 110 may include at least one material, such as, platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium, which reacts with the silver to form the alloy. By way of example and not limitation, the annealing process may include exposing the semiconductor structure 100 to a temperature of between about 100°C and about 500°C and, more particularly, a temperature of about 200°C. During the annealing process, a material 114 (shown in broken lines) that includes the alloy may be formed at an interface between the conductive material 112 and material 104 underlying the remaining (i.e., non-alloyed) portions of the conductive material 112. The alloy may include a substantially homogeneous mixture of the liner material 110 and the conductive material 112, or may be a heterogeneous mixture that includes regions having different ratios of the liner material 110 to the conductive material 112. In embodiments in which the liner material 110 includes platinum and the conductive material 112 includes silver, the semiconductor structure 100 may be exposed to a temperature of about 200°C such that the platinum and the silver combine to form a silver-platinum alloy. The liner material 110 may be at least substantially completely alloyed with the conductive material 112 to form the material 114, or a portion of the liner material 110 may remain at an interface between the material 114 and surfaces of the material 104 and the electrode material 108, if present.

[0026] In examples in which the liner material 110 is formed from a material that does not form an alloy with the conductive material 112, the annealing process may be bypassed and the liner material 110 may remain at the interface between the conductive material 112 and the material 104 and, if present, the electrode material 108 (as shown in FIG. 1C). For example, the conductive material 112 may include silver and the liner material 110 may comprise tantalum and the tantalum may be disposed between the silver and the material 104 and, if present, the electrode material 108.

[0027] An exposed surface of the semiconductor structure 100 is subjected to a material removal process, such as a so-called polishing process in the form of, for example, a chemical mechanical polishing (CMP) process or a mechanical polishing process, to form an interconnect

120, as shown in FIG. 1E. The employed process is used to remove portions of each of the liner material 110, the conductive material 112 and, if present, the material 114 overlying the material 104 (FIG. 1D). In addition, the process is used to redistribute at least one of the conductive material 112, the liner material 110 and the material 114, if present, into the -10-unfilled region 116 (FIG. 1D) of the opening 106 to substantially completely fill the opening 106. Without wishing to be bound by any particular theory, it is believed that malleable materials, such as the conductive material 112 and, optionally, the liner material 110 and the material 114, may be mechanically pushed or redistributed into voids (e.g., the unfilled region 116) during the polishing process, thus filling the unfilled region 116 of the opening 106. However, mechanical stresses exerted on the malleable materials during the polishing process may cause the malleable materials to pull out of the opening 106. Such mechanical stresses may be substantially reduced or eliminated by leaving a portion of the opening 106 unfilled and by improving adhesion between the conductive material 112 and the underlying material (i.e., material 104 or, if present, the electrode material 108). For example, in embodiments in which the conductive material 112 is formed from a material (e.g., silver) that exhibits poor adhesion with an underlying region (e.g., the electrode material 108), the liner material 110 may substantially improve adhesion between the conductive material 112 and the underlying region to prevent the conductive material 112 from being removed from the opening 106 by the mechanical stresses.

[0028] The polishing process may be a chemical mechanical polishing process that is performed using a conventional chemical mechanical polishing apparatus and a slurry that enables redistributing of the malleable materials (e.g., the conductive material 112 and, optionally, the liner material 110) into the unfilled region 116 of the opening 106 to form the interconnect 120. Such a slurry may be, for example, an alumina-based slurry at a neutral or slightly basic pH that is substantially free of oxidizer. The polishing process may also be a mechanical polishing process performed using the conventional chemical mechanical polishing apparatus and water (e.g., deionized water) instead of a chemical slurry. Using water as the liquid component in the polishing process, without addition of chemical etching agents, may enable redistribution of the conductive material 112 and the liner material 110, if present, into the unfilled region of the opening 106 without substantially removing such materials.

[0029] After forming the interconnect 120, another annealing process may, optionally, be performed. By way of example and not limitation, this annealing process may include exposing the semiconductor structure 100 of FIG. 1E to a temperature of between about 100°C and about 500°C and, more particularly, about 200°C. The annealing process may result in formation of an alloy of the materials of the interconnect 120 (conductive material 112 and the liner material 110), as previously discussed. After annealing, the interconnect 120 may include regions of the conductive material 112, the liner material 110 and the alloy or may substantially include the alloy.

[0030] For the sake of simplicity, the methods described with respect to FIGS. 1A through 1E illustrate a method of forming a single interconnect 120. However, as would be understood by one of ordinary skill in the art, a plurality of interconnects or a network of metal routing (e.g., a metallization layer) may be formed using the methods described with respect to FIGS. 1A through 1E. The interconnect 120 may be present in various semiconductor devices, as would be understood by one of ordinary skill in the art. For example, the interconnect 120 may be used to electrically connect active devices, such as transistors, capacitors, etc. The interconnect 120 may include a portion of a network of metal routing electrically connecting such active devices.

[0031] FIGS. 2A through 2E are simplified partial cross-sectional views of a semiconductor structure 200 illustrating embodiments of another method of forming an interconnect. As shown in FIG. 2A, the semiconductor structure 200 is formed including an opening 206 in a material 204 overlying a substrate 202. The opening 206 may have a width w2 of less than about 100 nm and, more particularly, less than about 20 nm. The opening 206 may expose a surface of the material 204 or, if present, an optional electrode material 208 disposed between the material 204 and the substrate 202. The semiconductor structure 200 shown in FIG. 2A may be formed using substantially the same methods used to form the semiconductor structure 100 shown in FIG. 1A. While FIGs. 2A through 2E indicate that the electrode material 208 is present, it is understood that the electrode material 208 is optional and that material 204 may be in direct contact with substrate 202 with the opening 206 extending at least partially through material 204.

[0032] Referring to FIG. 2B, a conductive material 212 is formed over the semiconductor structure 200 (e.g., over exposed surfaces of each of the material 204 and, if present, the electrode material 208). The conductive material 212 may be formed from silver (Ag) or an alloy thereof using a conventional deposition process, such as, a chemical vapor deposition process, a physical vapor deposition process or a physical deposition process. Conventional vapor deposition processes (e.g., chemical vapor deposition and physical vapor deposition) may not effectively deposit silver in narrow openings (e.g., openings having at least one dimension of less than or equal to 20 nm). Thus, in embodiments in which at least one dimension (i.e., the width w2) of the opening 206 is less than or equal to about 20 run, a sputtering process may be used to form the conductive material 212 within the opening 206. By way of non-limiting example, the conductive material 212 may be substantially conformally deposited over an entire exposed surface of the semiconductor structure 200. The conductive material 212 may be formed having a thickness sufficient to at least partially fill the opening 206. A portion of the opening 206

remains unfilled (i.e., unfilled region 216) after deposition of the conductive material 212. By way of example and not limitation, the conductive material 212 may be formed from silver and have a thickness of between about 5 nm and about 30 nm and, more particularly, between about 10 nm and about 20 nm.

[0033] Referring to FIG. 2C, a liner material 210 is formed over surfaces of the conductive material 212. The liner material 210 may be formed from a material that facilitates adhesion to and/or reduces contact resistance in an upper electrode (not shown) that may be formed over a completed interconnect, as will be discussed in further detail. For example, the liner material 210 may be formed from at least one of platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium. The liner material 210 may be formed using a conventional deposition process, such as, a chemical vapor deposition process, a physical vapor deposition process or a sputtering process. As shown in FIG. 2C, a portion of the unfilled region 216 of the opening 206 may remain after the liner material 210 has been formed over the conductive material 212. By way of example and not limitation, the liner material 210 may be formed having a thickness of between about 0.5 nm and about 20 nm and, more particularly, between about 1 nm and about 5 nm.

[0034] The thicknesses of the liner material 210 and the conductive material 212 may be selected based on a desired ratio of materials. In embodiments in which the liner material 210 includes platinum and the conductive material 212 includes silver, a ratio of the liner material 210 to the conductive material 212 may be less than or equal to about 1 to 2.

[0035] Referring to FIG. 2D, in embodiments in which the liner material 210 (shown in broken lines) includes a material that forms an alloy with the conductive material 212, an annealing process is performed to form an alloy of the conductive material 212 and the liner material 210. For example, the conductive material 212 may include silver, the liner material 210 may include at least one material, such as, platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium, which reacts with the silver to form the alloy. By way of example and not limitation, the annealing process may include exposing the semiconductor structure 200 to a temperature of between about 100°C and about 500°C and, more particularly, about 200°C. During the annealing process, at least a portion of the conductive material 212 and the liner material 210 may be converted to form a material 214 (shown in broken lines) that includes the alloy. The alloy in the material 214 may include a substantially homogeneous mixture of the liner material 210 and the conductive material 212, or may be a heterogeneous mixture that includes regions having different ratios of the liner material 210 to the conductive material 212. In embodiments in which the liner material 110 includes platinum and the conductive material 212 includes silver, the semiconductor structure 200 may be exposed to a temperature of about 200°C such that the platinum and the silver combine to form a silver-platinum alloy. The liner material 210 may be at least substantially completely alloyed with the conductive material 212 to form the material 214, or a portion of the liner material 210 may remain overlying the material 214.

[0036] In examples in which the liner material 210 is formed from a material that does not form an alloy with the conductive material 212, the annealing process may be bypassed and the liner material 210 may remain over the conductive material 212 (as shown in FIG. 2C). For example, the conductive material 212 may include silver and the liner material 210 may comprise tantalum and the tantalum may be disposed over the silver.

[0037] An exposed surface of the semiconductor structure 200 is subjected to a material removal process, such as so-called polishing process in the form of a chemical mechanical polishing (CMP) process or a mechanical polishing process, to form an interconnect 220, as shown in FIG. 2E. The employed process is used to remove portions of each of the conductive material 212 and, if present, the material 114 and/or the liner material 210 overlying the material 204 (FIG. 2D). In addition, the polishing process is used to redistribute at least one of the conductive material 212, the material 214 and/or the liner material 210 into the unfilled region 216 of the opening 206 (FIG. 2D) to substantially completely fill the opening 206. Without wishing to be bound by any particular theory, it is believed that malleable materials (e.g., the conductive material 212 and, optionally, the liner material 210 and/or the material 214), may be mechanically pushed or redistributed into voids (e.g., the unfilled region 216 of the opening 206) during the polishing process, thus filling the unfilled region 216 of the opening 206. However, mechanical stresses exerted on the malleable materials during the polishing process may cause the malleable materials to pull out of the opening 206. Such mechanical stresses may be substantially reduced or eliminated by leaving a portion of the opening 206 unfilled and by improving adhesion between the conductive material 212 and the underlying material (i.e., the material 204 or, if present, the electrode 208). The polishing process may be a chemical mechanical polishing process or mechanical polishing process, as previously discussed with respect to FIG. 1E.

[0038] After forming the interconnect 220, another annealing process may, optionally, be performed. By way of example and not limitation, the annealing process may include exposing the semiconductor structure 200 to a temperature of between about 100°C and about 500°C and, more particularly, to a temperature of about 200°C. The annealing process may result in formation of an alloy of the conductive material 212 and the liner material 210, as previously discussed. After annealing, the interconnect 220 may include regions of the conductive material 212, the liner material 210 and the alloy or may substantially include the alloy.

[0039] For the sake of simplicity, the methods described with respect to FIGS. 2A through 2E illustrate a

method of forming a single interconnect 220. However, as would be understood by one of ordinary skill in the art, a plurality of interconnects or a network of metal routing (e.g., a metallization layer) may be formed using the methods described with respect to FIGS. 2A through 2E. The interconnect 220 may be present in various semiconductor devices, as would be understood by one of ordinary skill in the art. For example, the interconnect 220 may be used to electrically connect active devices, such as transistors, capacitors, etc. The interconnect 220 may include a portion of a network of metal routing electrically connecting such active devices.

[0040] FIG. 3A through 3D are simplified partial cross-sectional views of a semiconductor structure 300 illustrating embodiments of a method of forming a conductive element for a semiconductor device, such as an electrode 311 of a conductive bridge random access memory (CBRAM) device. A CBRAM may include a plurality of memory cells, one of which is shown in FIG. 3A. The CBRAM cell 330 may include a memory material 309, disposed between a first electrode 308 and a second electrode 311. For example, the memory material 309 may be disposed over a surface of an underlying material or over exposed surfaces of an opening 306, as will be described in further detail. The memory material 309 and the second electrode 311 may overlie a conductive structure 303 that provides an electrical connection between the first and second electrodes 308 and 311. The second electrode 311 may be formed from silver.

[0041] While not wishing to be bound by any particular theory, it is believed that operation of the CBRAM cell 330 occurs due to selective formation and dissolution of a conductive bridge formed by electromigration of silver into the memory material 309. Thus, it is important to control diffusion of silver ions into the memory material 309 during deposition of the second electrode 311.

[0042] FIGS. 3B through 3D illustrate embodiments of a method of forming the CBRAM cell 330 shown in FIG. 3A. As shown in FIGS. 3B1, a semiconductor structure 300 is formed that includes an opening 306 in a dielectric material 304, the opening 306 overlying a conductive structure 303 in an interlayer dielectric material 305 overlying the first electrode 308. The first electrode 308 may be formed from a conductive material, such as, tungsten, platinum, titanium nitride (TiN) or nickel. The first electrode 308 may be formed over a substrate (not shown) using conventional deposition process, such as, a chemical vapor deposition process or an atomic layer deposition process. The semiconductor structure 300 includes the memory material 309 overlying surfaces of the conductive structure 303 and the interlayer dielectric material 305.

[0043] The interlayer dielectric material 305 may be formed from, for example, silicon nitride, silicon dioxide or a silicon oxynitride. The interlayer dielectric material 305 may be formed over the first electrode 308 using a conventional deposition process, such as a chemical vapor deposition process, an atomic layer deposition process or a physical vapor deposition process.

[0044] The conductive structure 303 may be formed from a conductive material, such as, at least one of titanium nitride, tungsten, tungsten nitride, tantalum and tantalum nitride. The conductive structure 303 may be formed in electrical connection with the first electrode 308. The conductive structure 303 may be formed in the interlayer dielectric material 305 using conventional techniques, the details of which are known in the art and, therefore, are not described in detail herein. For example, a conventional damascene process may be used to form the conductive structure 303 in the interlayer dielectric material 305 by forming a trench in the interlayer dielectric material 305, forming the conductive material over interlayer dielectric material 305 to fill the trench, and performing a chemical mechanical polishing (CMP) process to remove portions of the conductive material overlying the interlayer dielectric material 305.

[0045] The memory material 309 may be formed from a chalcogenide material, such as germanium selenide or germanium sulfide, or an oxide material, such as a high-k oxide material. Examples of suitable high-k dielectric materials include, but are not limited to, silicon dioxide, tantalum oxide, titanium oxide, nitrogen oxide, zirconium oxide and hafnium oxide. For example, the memory material 309 may be deposited using a conventional deposition process, such as, a physical vapor deposition process, a chemical vapor deposition process or an atomic layer deposition process.

[0046] The dielectric material 304 may be formed from, for example, silicon nitride, tetraethyl orthosilicate (TEOS), silicon dioxide or a silicon oxynitride. The dielectric material 304 may be formed over the interlayer dielectric material 305 and the conductive structure 303 using a conventional deposition process, such as, a chemical vapor deposition process, an atomic layer deposition process or a physical vapor deposition process. In some embodiments, the dielectric material 304 may be formed as a monolithic structure. In other embodiments, the dielectric material 304 may be formed as a stacked structure that includes a plurality of materials 304A, 304B, 304C, as shown in broken lines. For example, the materials 304A and 304C may be formed from silicon nitride and the material 304B may be formed from tetraethyl orthosilicate.

[0047] The opening 306 may be formed in the dielectric material 304 by removing a portion of the dielectric material 304 using, for example, conventional photolithography techniques (e.g., masking and etching) known in the art of integrated circuit fabrication. The portion of the dielectric material 304 removed to form the opening 306 may overlie the conductive structure 303 such that the opening 306 exposes a surface of the conductive structure 303 and, optionally, surfaces of the interlayer dielectric material 305 adjacent the surface of the conductive structure 303. By way of example and not limitation, the opening 306 may have a width w3 of less than about 100 nm and, more particularly, less than about 20 nm.

[0048] Referring to FIG. 3B2, the memory material 309 may alternatively be formed over sidewalls of the dielectric material 304 and surfaces of the conductive structure 303 and the interlayer dielectric material 305 after forming the dielectric material 304 and the opening 306 in the dielectric material 304. As previously discussed with respect to FIG. 3B1, The memory material 309 may be formed from a chalcogenide material, such as germanium selenide or germanium sulfide, or an oxide material, such as a high-k oxide material, using a conventional deposition process, such as, a physical vapor deposition process, a chemical vapor deposition process or an atomic layer deposition process.

[0049] After deposition of the memory material 309, an annealing process is performed. By way of example and not limitation, the annealing process may include exposing the semiconductor structure 300 to a temperature of between about 100°C and about 500°C and, more particularly, a temperature of about 200°C.

[0050] As shown in FIG. 3C, a conductive material 312 that includes silver may be formed over the memory material 309. For simplicity, the semiconductor structure 300 is shown with the memory material 309 (shown in broken lines) disposed over surfaces in the opening 306 and over surfaces of the dielectric material 304. However, as configured, the memory material 300 may also be disposed between the interlayer dielectric material 305 and the dielectric material 304 and the memory material 309 as shown in FIG. 3B1.

[0051] Forming silver using a conventional vapor deposition process, such as a physical vapor deposition (PVD) process or a chemical vapor deposition (CVD) process, may cause undesirable diffusion of the silver into the memory material 309 during formation of the second electrode 311. Such diffusion of the silver may results in variability in cell-to-cell operation of the CBRAM device. Thus, the conductive material 312 may be formed from silver (Ag) or a silver alloy using a conventional sputtering process. By way of example and not limitation, the conductive material 312 may be substantially conformally deposited over an entire exposed surface of the memory material 309. A thickness of the conductive material 312 is such that a portion of the opening 306 remains unfilled (i.e., unfilled region 316). By way of example and not limitation, the conductive material 312 may be formed having a thickness of between about 10 nm and about 20 nm.

[0052] Referring to FIG. 3D, a liner material 310 may be formed over surfaces of the conductive material 312. For example, the liner material is formed from tantalum and, in additional examples, may be formed from at least one of platinum, aluminum (Al), lead (Sb), copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium. The liner material 310 may be formed using a conventional deposition process, such as, a chemical vapor deposition process, a physical vapor deposition process or a sputtering process. By way of example and not limitation, the liner material 310 may be formed having a thickness of between about 0.5 nm and about 20 nm and, more particularly, between about 1 nm and about 5 nm.

[0053] Removal of silver from unwanted areas may be complicated as there are currently no known etchants for selectively removing the silver with respect to the other materials. Thus, material (i.e., the conductive material 312 and the liner material 310) is pushed or redistributed from upper surfaces of the dielectric material 304 into voids (e.g., the unfilled region 316 of the opening 306) by subjecting an exposed surface of the semiconductor structure 300 to a polishing process, as described with respect to FIG. 3D. During the polishing process, the unfilled region 316 (FIGS. 3C and 3D) may be filled to form the second electrode 311 shown in FIG. 3A. Optionally, an annealing process may then be performed to form an alloy of the conductive material 312 and the liner material 310. For example, in case the liner material 310 comprises platinum, aluminum (Al), lead (Sb), copper, iridium, titanium, nickel, cobalt, ruthenium and rhodium, the annealing process may be performed to form the alloy. In embodiments in which the annealing process is performed before deposition of the conductive material 312, the annealing process may be bypassed at this stage. The annealing process may include exposing the semiconductor structure 300 to a temperature of between about 100°C and about 500°C and, more particularly, about 200°C. By way of example and not limitation, the conductive material 312 may be formed from silver, the liner material 310 may be formed from platinum and a silver-platinum alloy may be formed during the annealing process. A majority of the alloy or substantially all of the alloy may be located in a region of the interconnect 320 opposite a surface of the memory material 309 such that a region of the interconnect 320 in contact with or adjacent to the memory material 309 substantially includes silver.

[0054] In FIGS. 3A through 3D, embodiments of methods of forming a silver-containing conductive element (i.e., second electrode 311) are illustrated in the CBRAM cell 330. However, such methods may also be used to form other conductive elements in a multitude of semiconductor structures and devices, as would be understood by one of ordinary skill in the art.

EXAMPLES

Example 1

[0055] A plurality of trenches was formed in a silicon dioxide material overlying a silicon wafer. The trenches of the plurality each had a depth of about 50 nm. Silver was deposited over the surface of the silicon wafer using a conventional sputtering process. The sputtering process was performed using a conventional sputter coater. The silver was sputtered over the surface of the silicon wafer for about two minutes, during which time the silver reached a thickness of about 15 nm. Platinum was then formed over the silver using the sputter coater. The plat-

inum was sputtered over the surface of the silicon wafer for about 30 seconds, during which time the platinum reached a thickness of about 6 nm.

[0056] A mechanical polishing process was performed on the silicon wafer having the silver and platinum thereon using deionized water and a conventional polishing pad. No chemical slurry was used during the mechanical polishing process. The surface of the platinum was polished using a pad rotation of about 100 RPM. After the mechanical polishing process, a scanning electron microscope (SEM) was used to observe that the trenches were substantially filled with material (e.g., the silver and the platinum).

[0057] An annealing process was then performed using a conventional industrial oven. The industrial oven was set to 200°C and the silicon wafer having the silver and platinum thereon was placed therein for about 10 minutes. It was confirmed that the post annealed silver-platinum alloy was substantially smooth with low resistance.

[0058] While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications and alternatives falling within the scope of the invention as defined by the following claims.

Claims

1. A method of forming a semiconductor structure (100, 200, 300), comprising:

forming a first conductive material (110, 212, 312) over a structure and within at least one opening (106, 206, 306) in the structure defined by sidewalls of a dielectric material (104, 204, 304), wherein the first conductive material comprises metal and wherein a portion (116, 216, 316) of the at least one opening remains unfilled;
forming a second conductive material (112, 210, 310) comprising silver over the first conductive material and within the at least one opening, wherein a portion (116, 216, 316) of the at least one opening remains unfilled;
annealing the structure to form an annealed material (114, 214) within the at least one opening and comprising at least a portion of the first conductive material and the second conductive material, the at least one opening comprising an unfilled region; and
redistributing at least one of the first conductive material, the second conductive material, and the annealed material into the unfilled region of the at least one opening.

2. The method of claim 1, wherein forming a first conductive material comprises forming the first conductive material over the sidewalls of the dielectric material and a surface of an electrode therebetween.

3. The method of claim 1, wherein forming a first conductive material comprises forming the first conductive material within the at least one opening having at least one dimension of less than about 20 nm.

4. The method of claim 1, wherein forming a second conductive material comprises forming the silver over the first conductive material without substantially filling the at least one opening.

5. The method of claim 1, wherein annealing the structure comprises annealing the structure to form a material comprising a mixture of silver and tantalum within the at least one opening.

6. The method of claim 1, wherein annealing the structure comprises annealing the structure to form a material comprising an alloy consisting of silver and at least one of platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium, and rhodium within the at least one opening.

7. The method of claim 1, wherein annealing the structure comprises exposing the structure to a temperature of between about 200°C and about 600°C.

8. The method of claim 1, wherein redistributing at least one of the first conductive material, the second conductive material, and the annealed material into the unfilled region of the at least one opening comprises filling the at least one opening with at least one of the first conductive material, the second conductive material, and the annealed material.

9. The method of claim 1, wherein redistributing at least one of the first conductive material, the second conductive material, and the annealed material into the unfilled region of the at least one opening comprises performing a polishing process using a liquid component consisting of water.

10. The method of claim 1, further comprising forming a memory material over the structure and within the at least one opening defined by sidewalls of the dielectric material.

11. The method of claim 10, wherein forming a memory material over the structure and within the at least one opening comprises forming at least one of a chalcogenide material and an oxide material over the structure and within the at least one opening.

12. The method of claim 10, wherein forming a memory

material over the structure and within the at least one opening comprises forming at least one of germanium sulfide, germanium selenide, silicon dioxide, tantalum oxide, titanium oxide, nitrogen oxide, zirconium oxide, and hafnium oxide over the structure and within the at least one opening.

13. The method of claim 1, wherein forming a first conductive material over a structure and within at least one opening defined by sidewalls of a dielectric material comprises forming the at least one opening having an aspect ratio of between 1:1 and about 20:1.

14. The method of claim 1, wherein forming a first conductive material over a structure and within the at least one opening comprises forming the first conductive material comprising at least one of platinum, tantalum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium, and rhodium over the structure and within the at least one opening.

15. A semiconductor structure (300), comprising:

a conductive structure (303) and an interlayer dielectric material (305) overlying an electrode (308);
a dielectric material (304) directly overlying the interlayer dielectric material;
at least one of a chalcogenide material and an oxide material (309) in direct contact with the dielectric material, the conductive structure, and the interlayer dielectric material; and
a conductive material (310, 311, 312) directly overlying the at least one of a chalcogenide material and an oxide material, the conductive material comprising silver and tantalum.

16. The semiconductor structure of claim 15, wherein the conductive material comprising silver and tantalum comprises tantalum overlying the silver.

17. The semiconductor structure of claim 15 or claim 16, wherein the conductive material comprising silver and tantalum and overlying the at least one of a chalcogenide material and an oxide material comprises an alloy of silver and at least one of platinum, aluminum, tin, copper, iridium, titanium, nickel, cobalt, ruthenium, and rhodium.

18. The semiconductor structure of claim 14, wherein the at least one of a chalcogenide material and an oxide material is in direct contact with sidewalls of the dielectric material and with upper surfaces of the conductive structure and the interlayer dielectric material.

19. The semiconductor structure of claim 14, wherein the at least one of a chalcogenide material and an oxide material is in direct contact with lower surfaces of the dielectric material and with upper surfaces of the conductive structure and the interlayer dielectric material.

Patentansprüche

1. Verfahren zum Formen einer Halbleiterstruktur (100, 200, 300), das Folgendes umfasst:

das Formen eines ersten leitfähigen Materials (110, 212, 312) über einer Struktur und innerhalb wenigstens einer Öffnung (106, 206, 306) in der Struktur, die durch Seitenwände eines dielektrischen Materials (104, 204, 304) definiert wird, wobei das erste leitfähige Material Metall umfasst und wobei ein Abschnitt (116, 216, 316) der wenigstens einen Öffnung ungefüllt bleibt,
das Formen eines zweiten leitfähigen Materials (112, 210, 310), das Silber umfasst, über dem ersten leitfähigen Material und innerhalb der wenigstens einen Öffnung, wobei ein Abschnitt (116, 216, 316) der wenigstens einen Öffnung ungefüllt bleibt, und
das Glühen der Struktur, um ein geglühtes Material (114, 214) zu formen, innerhalb der wenigstens einen Öffnung und umfassend wenigstens einen Abschnitt des ersten leitfähigen Materials und des zweiten leitfähigen Materials, wobei die wenigstens eine Öffnung einen ungefüllten Bereich umfasst, und
das Umverteilen wenigstens eines von dem ersten leitfähigen Material, dem zweiten leitfähigen Material und dem geglühten Material in den ungefüllten Bereich der wenigstens einen Öffnung.

2. Verfahren nach Anspruch 1, wobei das Formen eines ersten leitfähigen Materials das Formen des ersten leitfähigen Materials über den Seitenwänden des dielektrischen Materials und einer Oberfläche einer Elektrode zwischen denselben umfasst.

3. Verfahren nach Anspruch 1, wobei das Formen eines ersten leitfähigen Materials das Formen des ersten leitfähigen Materials innerhalb der wenigstens einen Öffnung, die wenigstens eine Abmessung von weniger als etwa 20 nm hat, umfasst.

4. Verfahren nach Anspruch 1, wobei das Formen eines zweiten leitfähigen Materials das Formen des Silbers über dem ersten leitfähigen Material, ohne die wenigstens eine Öffnung im Wesentlichen zu füllen, umfasst.

5. Verfahren nach Anspruch 1, wobei das Glühen der Struktur das Glühen der Struktur, um ein Material,

das ein Gemisch aus Silber und Tantal umfasst, innerhalb der wenigstens einen Öffnung zu formen, umfasst.

6. Verfahren nach Anspruch 1, wobei das Glühen der Struktur das Glühen der Struktur, um ein Material, das eine Legierung umfasst, die aus Silber und wenigstens einem von Platin, Aluminium, Zinn, Kupfer, Iridium, Titan, Nickel, Kobalt, Ruthenium und Rhodium besteht, innerhalb der wenigstens einen Öffnung zu formen, umfasst.

7. Verfahren nach Anspruch 1, wobei das Glühen der Struktur das Aussetzen der Struktur einer Temperatur von zwischen etwa 200°C und etwa 600°C umfasst.

8. Verfahren nach Anspruch 1, wobei das Umverteilen wenigstens eines von dem ersten leitfähigen Material, dem zweiten leitfähigen Material und dem geglühten Material in den ungefüllten Bereich der wenigstens einen Öffnung das Füllen der wenigstens einen Öffnung mit wenigstens einem von dem ersten leitfähigen Material, dem zweiten leitfähigen Material und dem geglühten Material umfasst.

9. Verfahren nach Anspruch 1, wobei das Umverteilen wenigstens eines von dem ersten leitfähigen Material, dem zweiten leitfähigen Material und dem geglühten Material in den ungefüllten Bereich der wenigstens einen Öffnung das Durchführen eines Poliervorgangs unter Verwendung eines flüssigen Bestandteils, der aus Wasser besteht, umfasst.

10. Verfahren nach Anspruch 1, das ferner das Formen eines Gedächtnismaterials über der Struktur und innerhalb der wenigstens einen Öffnung, die durch Seitenwände des dielektrischen Materials definiert wird, umfasst.

11. Verfahren nach Anspruch 10, wobei das Formen eines Gedächtnismaterials über der Struktur und innerhalb der wenigstens einen Öffnung das Formen wenigstens eines von einem Chalkogenidmaterial und einem Oxidmaterial über der Struktur und innerhalb der wenigstens einen Öffnung umfasst.

12. Verfahren nach Anspruch 10, wobei das Formen eines Gedächtnismaterials über der Struktur und innerhalb der wenigstens einen Öffnung das Formen wenigstens eines von Germaniumsulfid, Germaniumselenid, Siliziumdioxid, Tantaloxid, Titanoxid, Stickoxid, Zirkoniumoxid und Hafniumoxid über der Struktur und innerhalb der wenigstens einen Öffnung umfasst.

13. Verfahren nach Anspruch 1, wobei das Formen eines ersten leitfähigen Materials über einer Struktur und innerhalb wenigstens einer Öffnung, die durch Seitenwände eines dielektrischen Materials definiert wird, das Formen der wenigstens einen Öffnung, die ein Seitenverhältnis von zwischen 1:1 und etwa 20:1 hat, umfasst..

14. Verfahren nach Anspruch 1, wobei das Formen eines ersten leitfähigen Materials über einer Struktur und innerhalb der wenigstens einen Öffnung das Formen eines ersten leitfähigen Materials, das wenigstens eines von Platin, Tantal, Aluminium, Zinn, Kupfer, Iridium, Titan, Nickel, Kobalt, Ruthenium und Rhodium umfasst, über der Struktur und innerhalb der wenigstens einen Öffnung umfasst.

15. Halbleiterstruktur (300), die Folgendes umfasst:

eine leitfähige Struktur (303) und ein dielektrisches Zwischenschichtmaterial (305), die über einer Elektrode (308) liegen,
ein dielektrisches Material (304), das unmittelbar über dem dielektrischen Zwischenschichtmaterial liegt,
wenigstens eines von einem Chalkogenidmaterial und einem Oxidmaterial (309) in unmittelbarem Kontakt mit dem dielektrischen Material, der leitfähigen Struktur und dem dielektrischen Zwischenschichtmaterial und
ein leitfähiges Material (310, 311, 312), das über dem wenigstens einem von einem Chalkogenidmaterial und einem Oxidmaterial liegt, wobei das leitfähige Material Silber und Tantal umfasst.

16. Halbleiterstruktur nach Anspruch 15, wobei das leitfähige Material, das Silber und Tantal umfasst, Tantal, das über dem Silber liegt, umfasst.

17. Halbleiterstruktur nach Anspruch 15 oder Anspruch 16, wobei das leitfähige Material, das Silber und Tantal umfasst und über dem wenigstens einem von einem Chalkogenidmaterial und einem Oxidmaterial liegt, eine Legierung aus Silber und wenigstens einem von Platin, Aluminium, Zinn, Kupfer, Iridium, Titan, Nickel, Kobalt, Ruthenium und Rhodium umfasst.

18. Halbleiterstruktur nach Anspruch 14, wobei sich das wenigstens eine von einem Chalkogenidmaterial und einem Oxidmaterial in unmittelbarem Kontakt mit Seitenwänden des dielektrischen Materials und mit oberen Flächen der leitfähigen Struktur und des dielektrischen Zwischenschichtmaterials befindet.

19. Halbleiterstruktur nach Anspruch 14, wobei sich das wenigstens eine von einem Chalkogenidmaterial und einem Oxidmaterial in unmittelbarem Kontakt mit unteren Flächen des dielektrischen Materials

und mit oberen Flächen der leitfähigen Struktur und des dielektrischen Zwischenschichtmaterials befindet.

Revendications

1. Procédé de formation d'une structure semi-conductrice (100, 200, 300), comprenant les étapes consistant à :

   former un premier matériau conducteur (110, 212, 312) par-dessus une structure et au sein d'au moins une ouverture (106, 206, 306) de la structure, définie par des parois latérales d'un matériau diélectrique (104, 204, 304), dans lequel le premier matériau conducteur comprend du métal et dans lequel une partie (116, 216, 316) de la au moins une ouverture demeure non remplie ;
   former un deuxième matériau conducteur (112, 210, 310) comprenant de l'argent par-dessus le premier matériau conducteur et au sein de la au moins une ouverture, dans lequel une partie (116, 216, 316) de la au moins une ouverture demeure non remplie ;
   recuire la structure pour former un matériau recuit (114, 214) situé au sein de la au moins une ouverture et comprenant au moins une partie du premier matériau conducteur et du deuxième matériau conducteur, la au moins une ouverture comprenant une région non remplie ; et
   répartir à nouveau au moins un parmi le premier matériau conducteur, le deuxième matériau conducteur, et le matériau recuit dans la région non remplie de la au moins une ouverture.

2. Procédé selon la revendication 1, dans lequel l'étape de formation d'un premier matériau conducteur comprend une étape consistant à former le premier matériau conducteur par-dessus les parois latérales du matériau diélectrique et une surface d'une électrode située entre celles-ci.

3. Procédé selon la revendication 1, dans lequel l'étape de formation d'un premier matériau conducteur comprend une étape consistant à former le premier matériau conducteur au sein de la au moins une ouverture de manière à ce qu'elle présente au moins une dimension inférieure à environ 20 nm.

4. Procédé selon la revendication 1, dans lequel l'étape de formation d'un deuxième matériau conducteur comprend une étape consistant à former l'argent par-dessus le premier matériau conducteur sans remplir essentiellement la au moins une ouverture.

5. Procédé selon la revendication 1, dans lequel l'étape de recuit de la structure comprend une étape consistant à recuire la structure afin de former un matériau comprenant un mélange d'argent et de tantale au sein de la au moins une ouverture.

6. Procédé selon la revendication 1, dans lequel l'étape de recuit de la structure comprend une étape consistant à recuire la structure pour former un matériau comprenant un alliage constitué d'argent et d'au moins un parmi du platine, de l'aluminium, de l'étain, du cuivre, de l'iridium, du titane, du nickel, du cobalt, du ruthénium, et du rhodium au sein de la au moins une ouverture.

7. Procédé selon la revendication 1, dans lequel l'étape de recuit de la structure comprend une étape consistant à exposer la structure à une température comprise entre environ 200°C et environ 600°C.

8. Procédé selon la revendication 1, dans lequel l'étape de répartition à nouveau d'au moins un parmi le premier matériau conducteur, le deuxième matériau conducteur, et le matériau recuit dans la région non remplie de la au moins une ouverture comprend une étape consistant à remplir la au moins une ouverture avec au moins un parmi le premier matériau conducteur, le deuxième matériau conducteur, et le matériau recuit.

9. Procédé selon la revendication 1, dans lequel l'étape de répartition à nouveau d'au moins un parmi le premier matériau conducteur, le deuxième matériau conducteur, et le matériau recuit dans la région non remplie de la au moins une ouverture comprend une étape consistant à mettre en oeuvre un procédé de polissage utilisant un composant liquide constitué d'eau.

10. Procédé selon la revendication 1, comprenant en outre une étape consistant à former un matériau à mémoire par-dessus la structure et au sein de la au moins une ouverture définie par des parois latérales du matériau diélectrique.

11. Procédé selon la revendication 10, dans lequel l'étape de formation d'un matériau à mémoire par-dessus la structure et au sein de la au moins une ouverture comprend une étape consistant à former au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde par-dessus la structure et au sein de la au moins une ouverture.

12. Procédé selon la revendication 10, dans lequel l'étape de formation d'un matériau à mémoire par-dessus la structure et au sein de la au moins une ouverture comprend une étape consistant à former au moins un parmi du sulfure de germanium, du séléniure de germanium, du dioxyde de silicium, de l'oxyde de

tantale, de l'oxyde de titane, de l'oxyde d'azote, de l'oxyde de zirconium, et de l'oxyde d'hafnium par-dessus la structure et au sein de la au moins une ouverture.

13. Procédé selon la revendication 1, dans lequel l'étape de formation d'un premier matériau conducteur par-dessus une structure et au sein d'au moins une ouverture définie par les parois latérales d'un matériau diélectrique comprend une étape consistant à former la au moins une ouverture de manière à ce qu'elle présente un rapport d'aspect compris entre 1:1 et environ 20:1.

14. Procédé selon la revendication 1, dans lequel l'étape de formation d'un premier matériau conducteur par-dessus une structure et au sein de la au moins une ouverture comprend une étape consistant à former le premier matériau conducteur comprenant au moins un parmi du platine, du tantale, de l'aluminium, de l'étain, du cuivre, de l'iridium, du titane, du nickel, du cobalt, du ruthénium, et du rhodium par-dessus la structure et au sein de la au moins une ouverture.

15. Structure semi-conductrice (300), comprenant :

une structure conductrice (303) et un matériau diélectrique intercouche (305) situé au-dessus d'une électrode (308) ;
un matériau diélectrique (304) situé immédiatement au-dessus du matériau diélectrique intercouche ;
au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde (309) en contact direct avec le matériau diélectrique, la structure conductrice, et le matériau diélectrique intercouche ; et
un matériau conducteur (310, 311, 312) situé immédiatement au-dessus du au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde, le matériau conducteur comprenant de l'argent et du tantale.

16. Structure semi-conductrice selon la revendication 15, dans laquelle le matériau conducteur comprenant de l'argent et du tantale comprend du tantale situé au-dessus de l'argent.

17. Structure semi-conductrice selon la revendication 15 ou 16, dans laquelle le matériau conducteur comprenant de l'argent et du tantale et situé au-dessus du au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde comprend un alliage d'argent et d'au moins un parmi du platine, de l'aluminium, de l'étain, du cuivre, de l'iridium, du titane, du nickel, du cobalt, du ruthénium et du rhodium.

18. Structure semi-conductrice selon la revendication 14, dans laquelle le au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde est en contact direct avec des parois latérales du matériau diélectrique et avec des surfaces supérieures de la structure conductrice et du matériau diélectrique intercouche.

19. Structure semi-conductrice selon la revendication 14, dans laquelle le au moins un parmi un matériau à base de chalcogénure et un matériau à base d'oxyde est en contact direct avec des surfaces inférieures du matériau diélectrique et avec des surfaces supérieures de la structure conductrice et du matériau diélectrique intercouche.

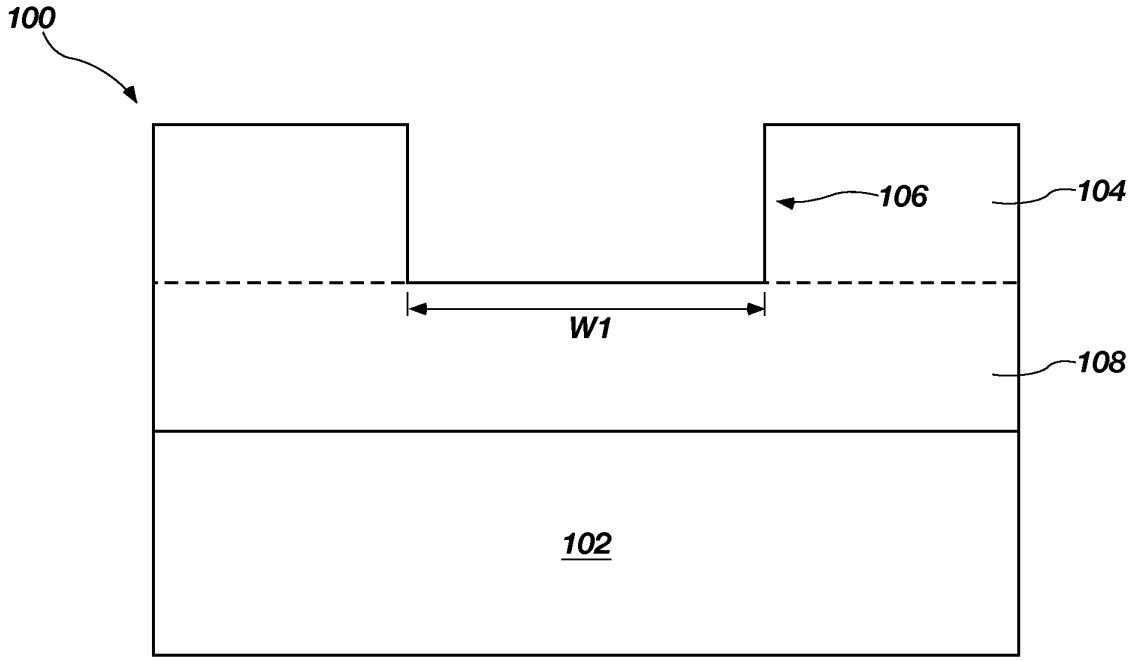

FIG. 1A

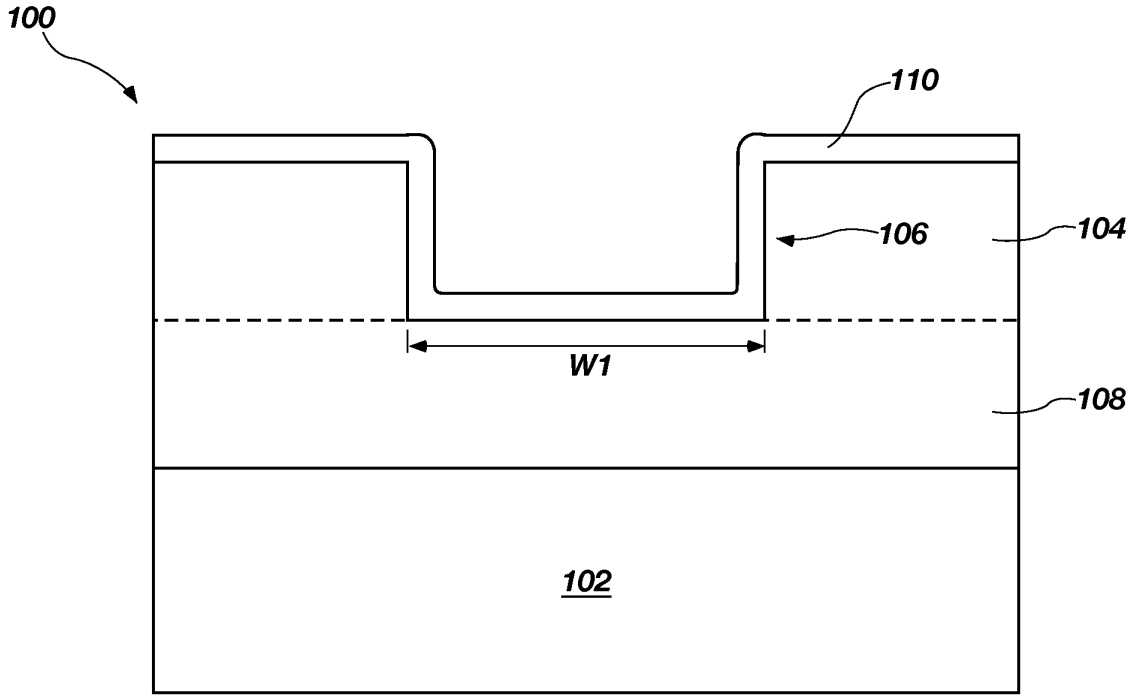

FIG. 1B

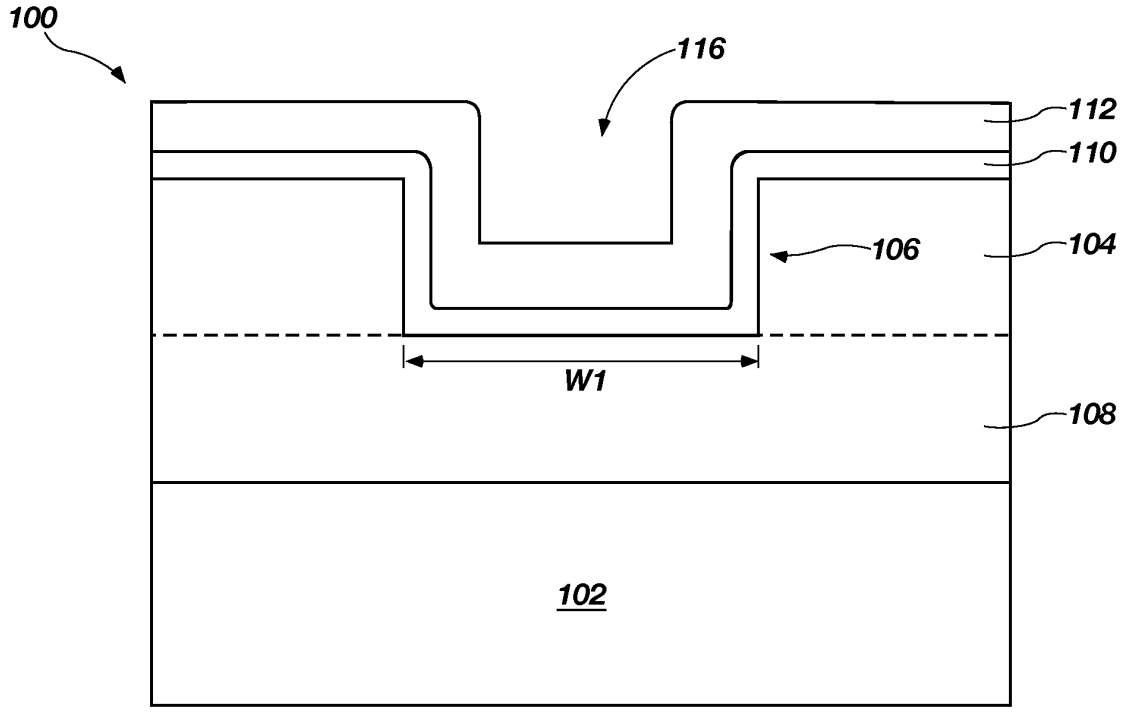
100
116
112
110
106
104
W1
108
102

FIG. 1C

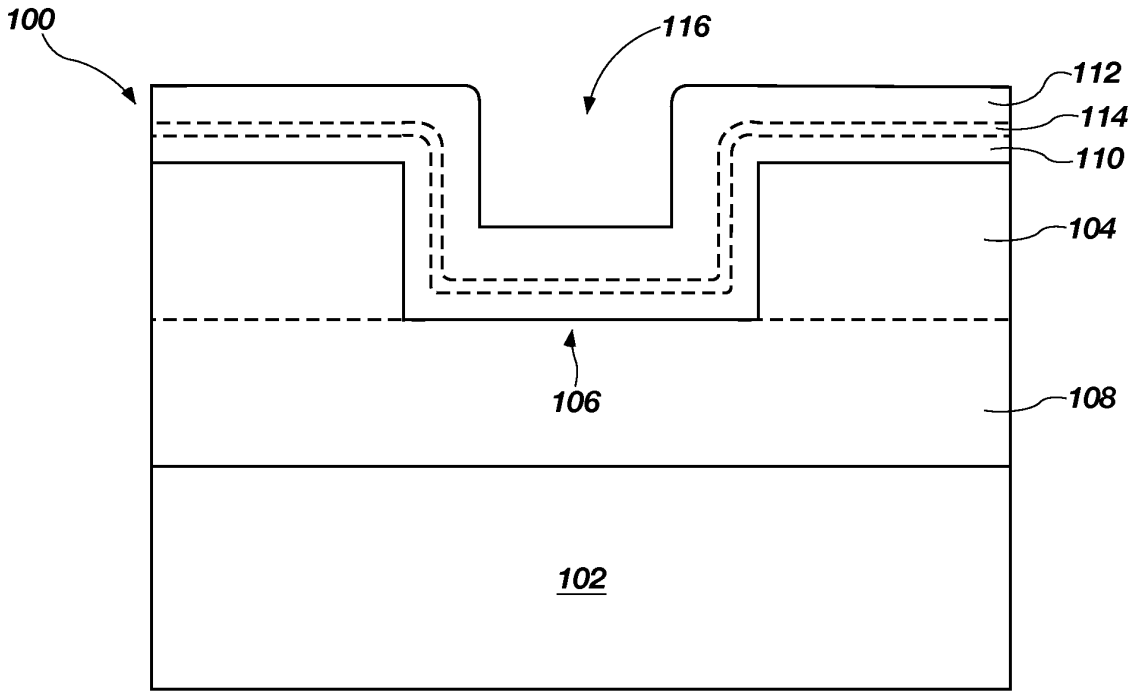
100
116
112
114
110
104
106
108
102

FIG. 1D

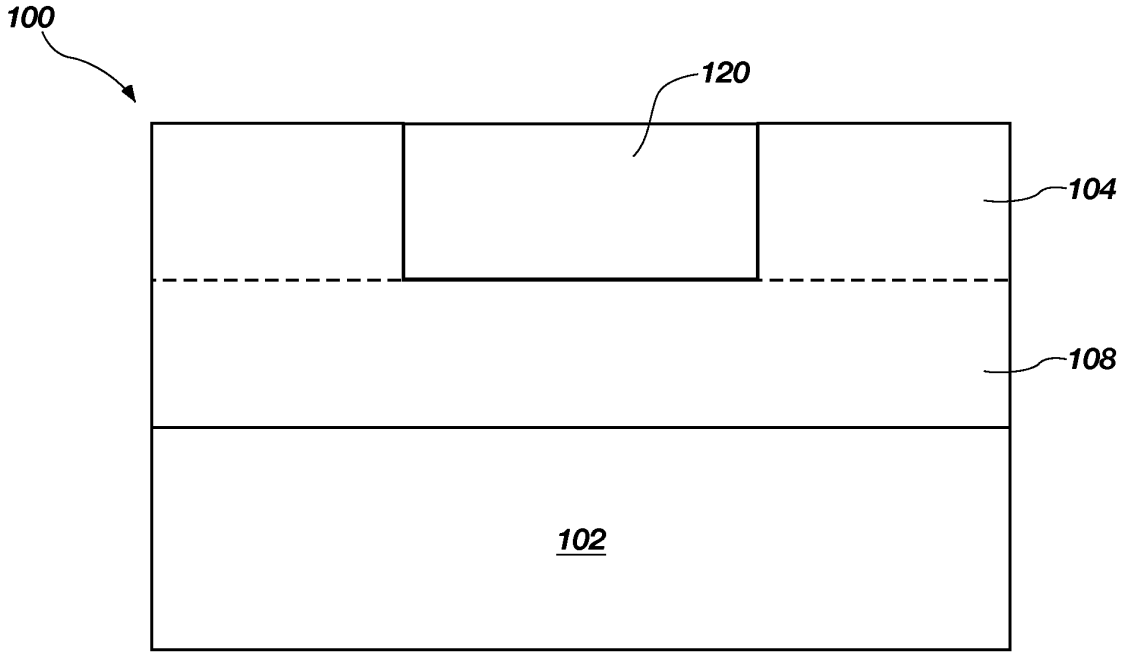

FIG. 1E

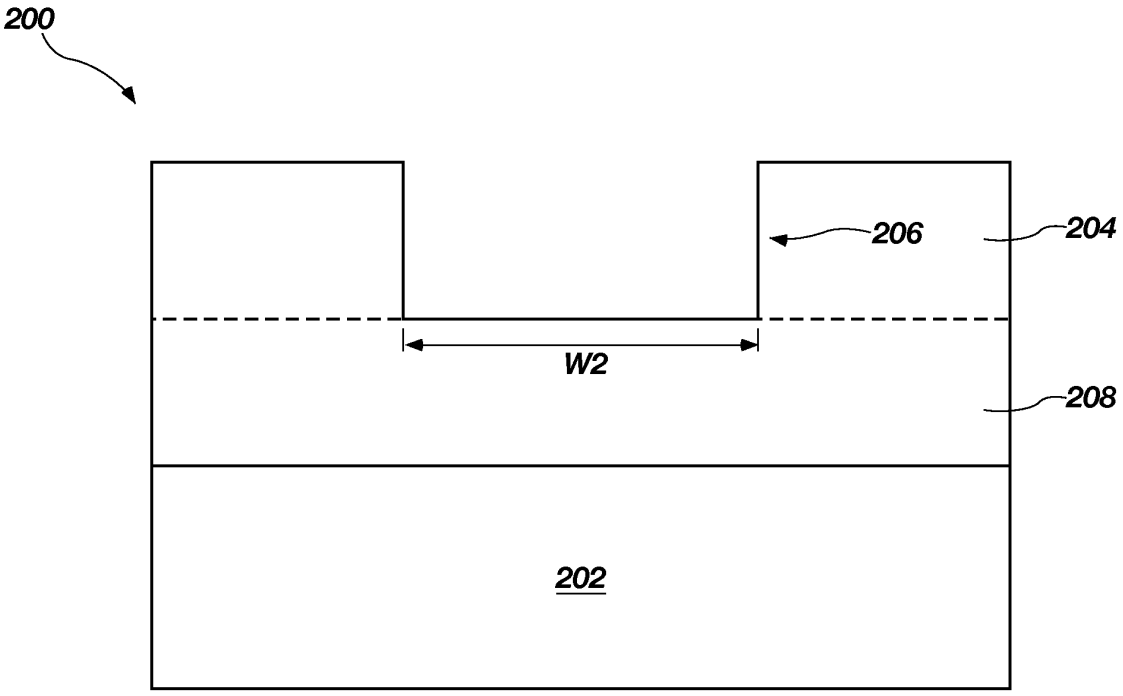

FIG. 2A

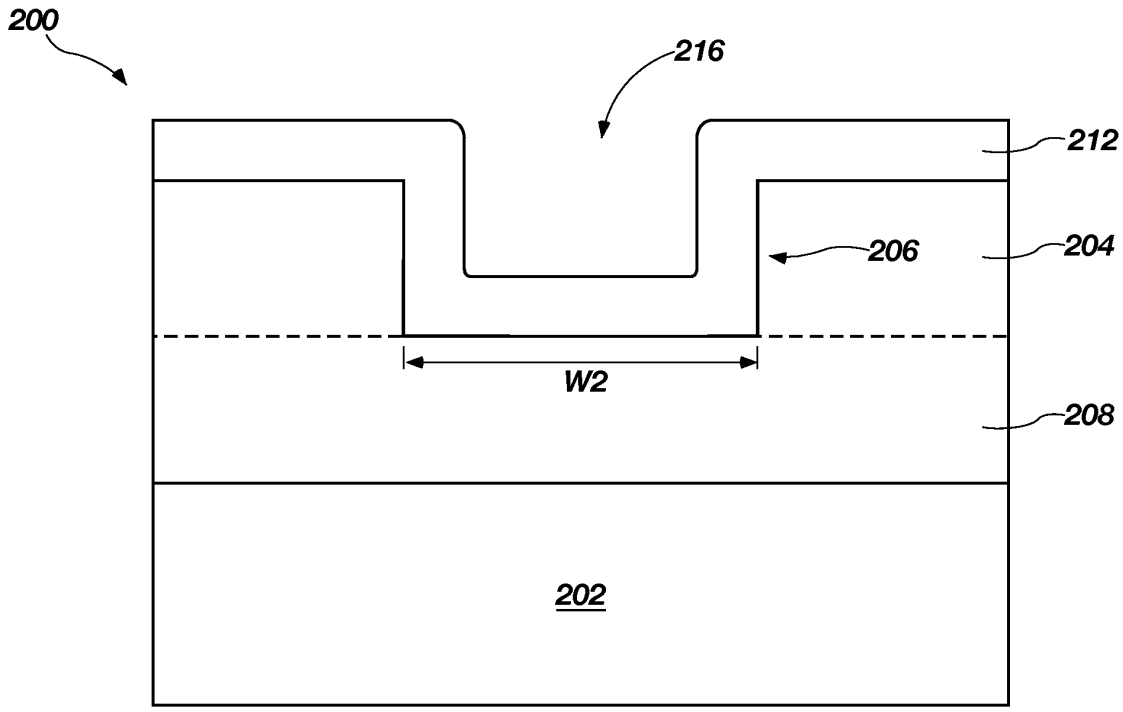

FIG. 2B

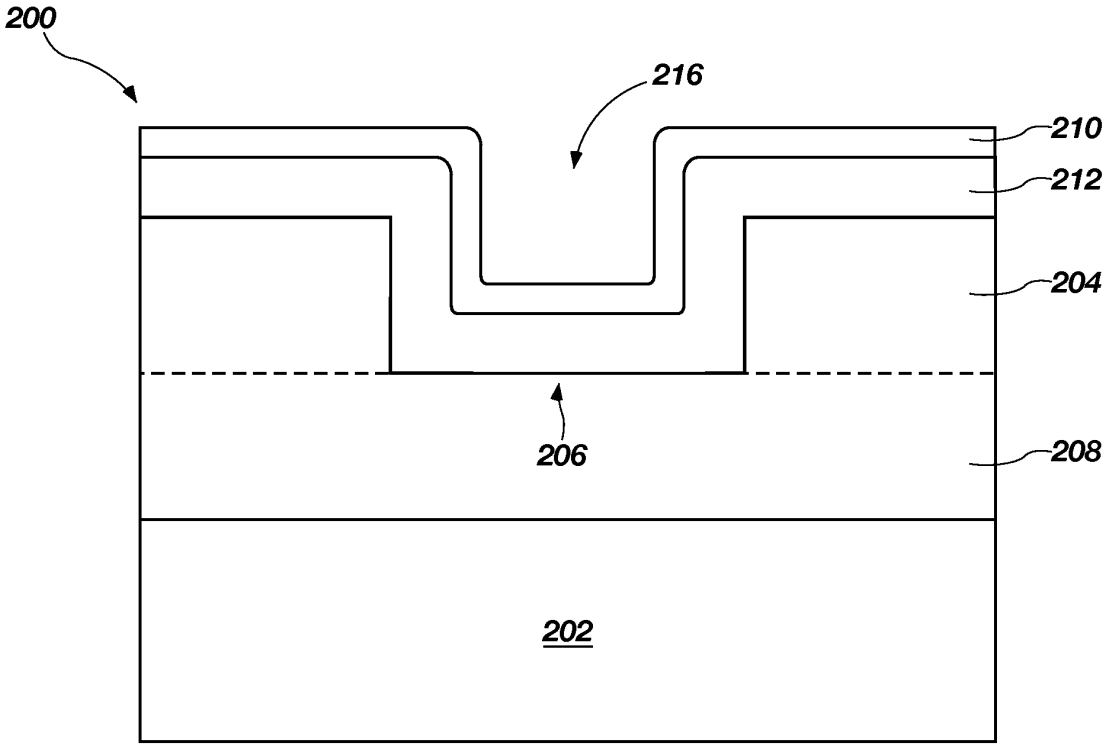

FIG. 2C

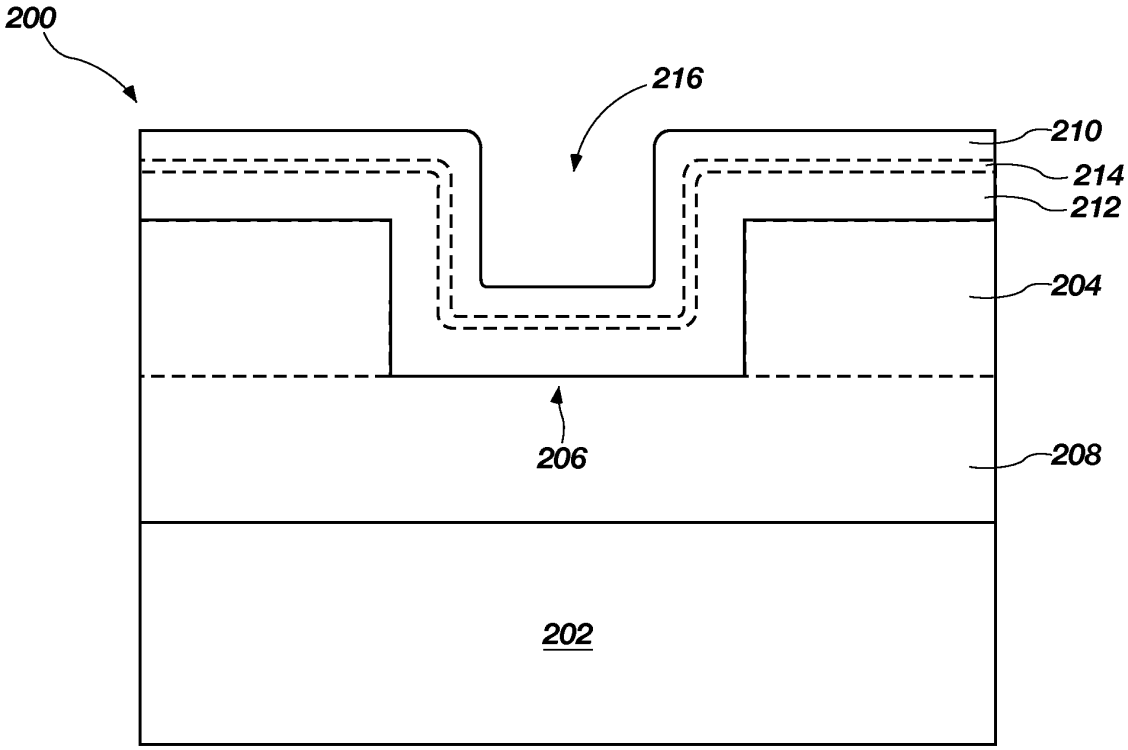

FIG. 2D

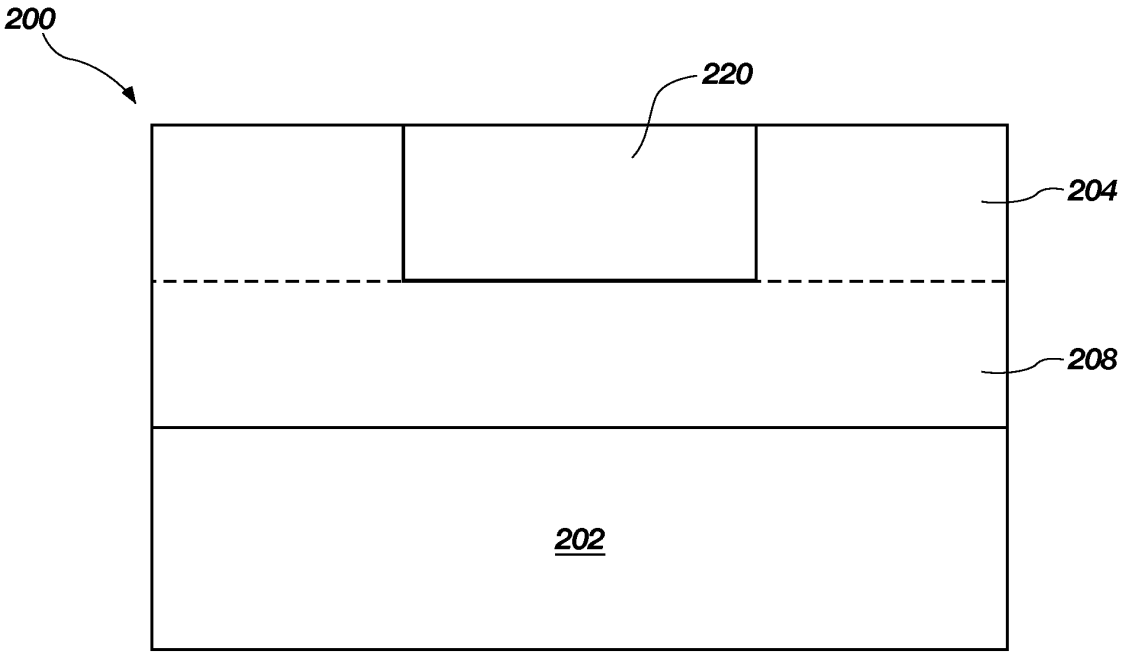

FIG. 2E

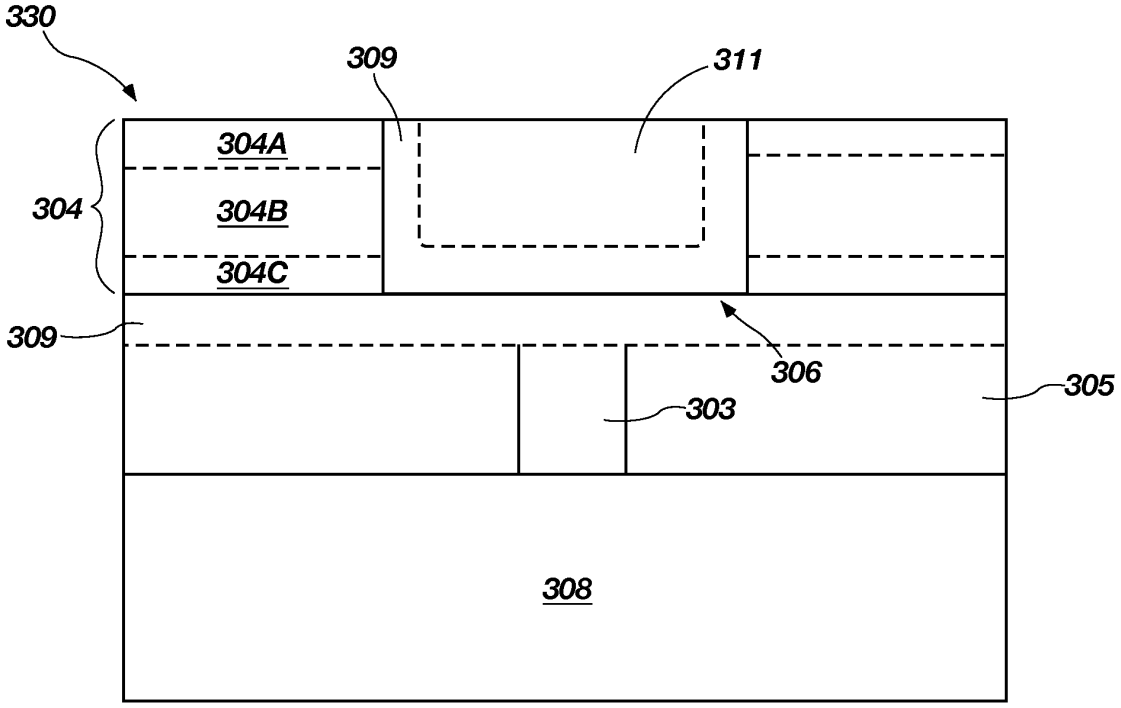

FIG. 3A

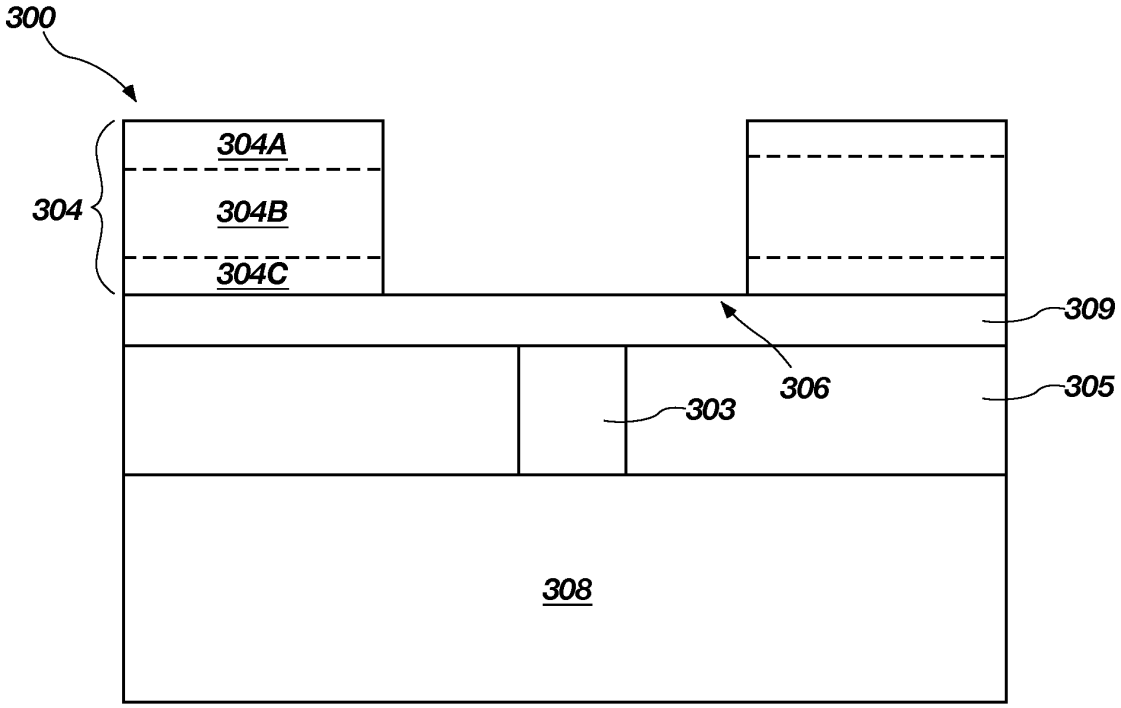

FIG. 3B1

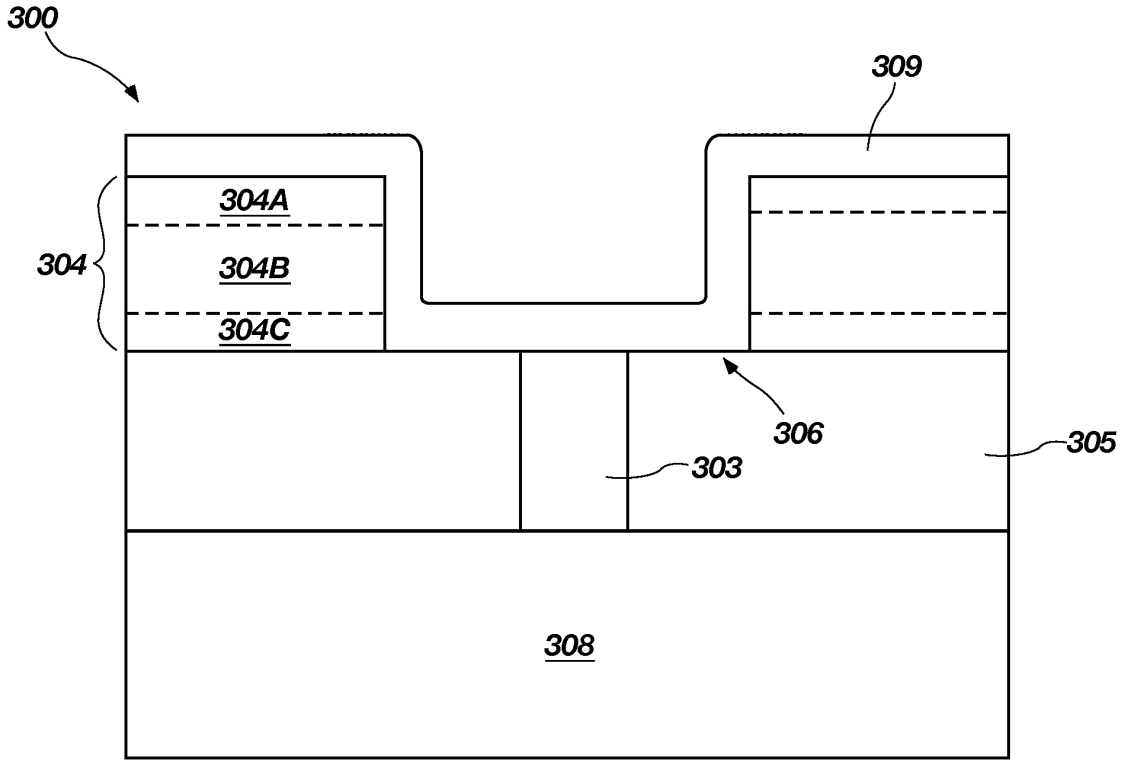

FIG. 3B2

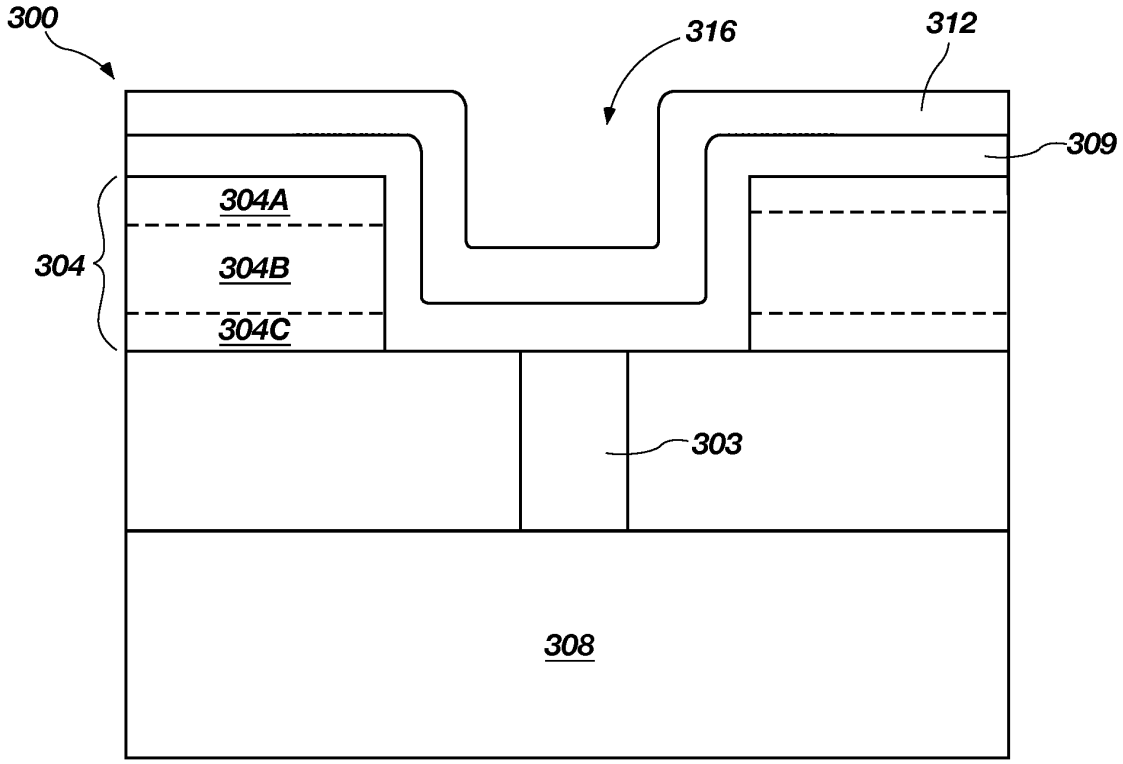

FIG. 3C

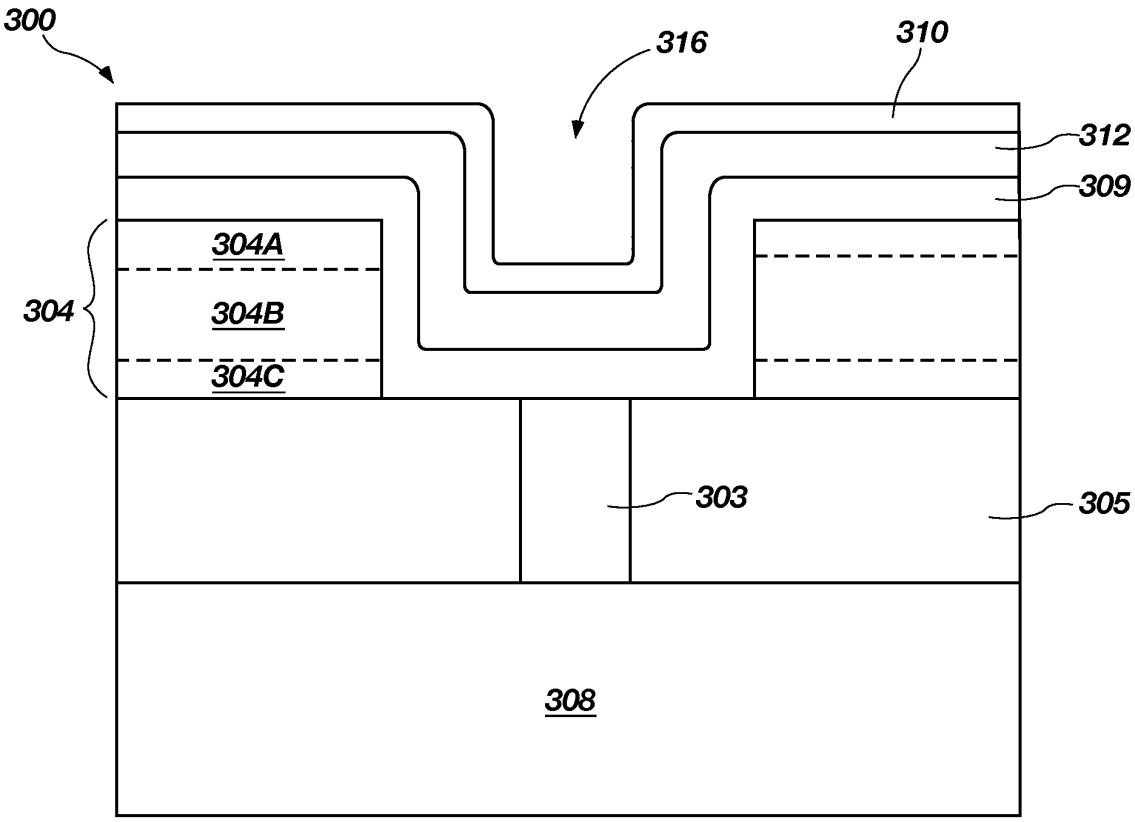

FIG. 3D

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20080253165 A1 **[0006]**
- US 20030143838 A1 **[0006]**