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(54) **Thin film transistor substrate and organic light emitting device using the same**

(57) Disclosed is a thin film transistor substrate (100) which facilitates to improve output and transfer characteristics of thin film transistor (T), wherein the thin film transistor substrate (100) comprises a thin film transistor (T) comprising a lower gate electrode (110) on a substrate, an active layer (130) on the lower gate electrode (110), source and drain electrodes (152, 154) on the ac-

tive layer (130), and an upper gate electrode (175) on the source electrode (152), drain electrode (154) and active layer (130), the upper gate electrode (175) for covering a channel region defined by the source and drain electrodes (152, 154); and a contact portion (180) for electrically connecting the lower gate electrode (110) with the upper gate electrode (175).

**FIG. 2A**

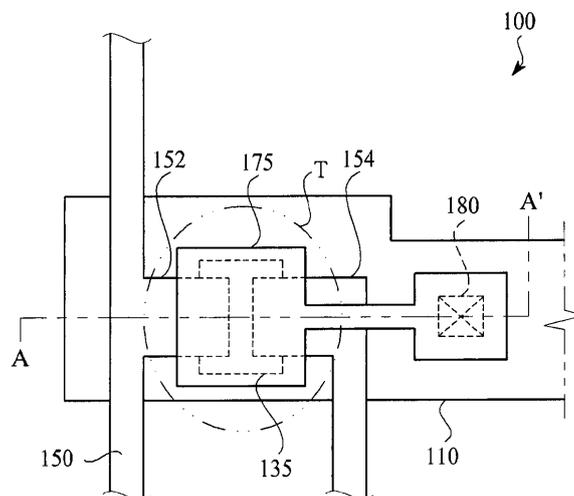
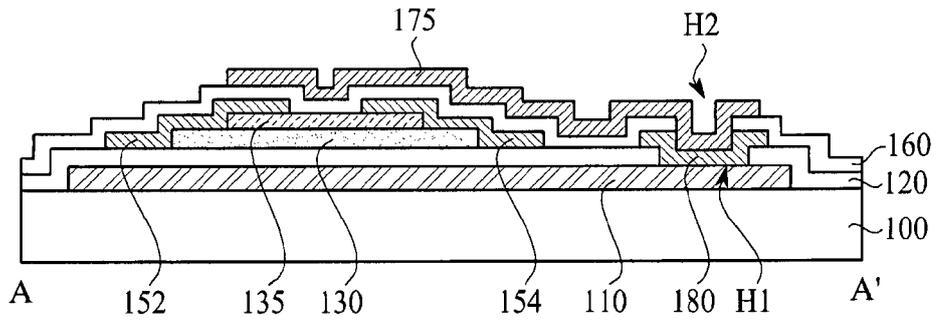


FIG. 2B



**Description****CROSS REFERENCE TO RELATED APPLICATIONS**

5 [0001] This application claims the benefit of the Korean Patent Application No. 10-2012-0088565 filed on August 13, 2012, which is hereby incorporated by reference as if fully set forth herein.

**BACKGROUND**10 **Field of the Invention**

[0002] The present invention relates to a display device, and more particularly, to a thin film transistor applied to a display device.

15 **Discussion of the Related Art**

[0003] A thin film transistor (TFT) is used as a switching element for controlling an operation of each pixel or a driving element for driving each pixel in a display device such as a liquid crystal display (LCD) or an organic light emitting device (OLED).

20 [0004] The thin film transistor includes a gate electrode, an active layer, and source/drain electrodes. Based on an arrangement of the electrodes, the thin film transistor may be classified into a staggered structure and a coplanar structure.

[0005] In case of the staggered structure, the gate electrode and the source/drain electrodes are vertically arranged with the active layer interposed therebetween. Meanwhile, in case of the coplanar structure, the gate electrode and the source/drain electrodes are arranged on the same plane.

25 [0006] According to a channel formation method, the thin film transistor of the staggered structure may be classified into a back channel etched (BCE) type and an etch stopper layer (ESL) type. In case of the ESL type, an etch stopper layer is formed on the active layer so that it is possible to prevent the active layer from being over-etched. Owing to this advantage, there is the increasing use of ESL type thin film transistor.

30 [0007] FIGs. 1A to 1E are cross sectional views illustrating a method for manufacturing an ESL type thin film transistor substrate.

[0008] First, as shown in FIG. 1A, a gate electrode 20 is formed on a substrate 10, and then a gate insulating layer 25 is formed on an entire surface of the substrate 10 including the gate electrode 20.

35 [0009] As shown in FIG. 1B, an active layer 30a and an etch stopper layer 40a are sequentially formed on the gate insulating layer 25. After that, as shown in FIG. 1C, the etch stopper layer 40a is patterned to thereby form a predetermined etch stopper 40. The etch stopper 40 functions as a stopper for an etching process to be described later.

[0010] Then, as shown in FIG. 1D, an ohmic contact layer 50a and a source/drain electrode layer 60a are sequentially formed on the entire surface of the substrate 10 including the etch stopper 40.

40 [0011] As shown in FIG. 1E, the source/drain electrode layer 60a is patterned to form a source electrode 62 and a drain electrode 64. Under the condition that the source/drain electrodes 62/64 are used as a mask, the ohmic contact layer 50a and active layer 30a positioned underneath the source/drain electrodes 62/64 are etched to thereby form an ohmic contact layer 50 and active layer 30 with a predetermined pattern.

[0012] The etch stopper 40 is not formed at left and right sides of the source/drain electrodes 62/64, whereby both the ohmic contact layer 50a and active layer 30a are etched together. However, since the etch stopper 40 is formed in a region between the source electrode 62 and the drain electrode 64, only the ohmic contact layer 50a is etched therein.

45 [0013] However, because the related art thin film transistor is formed in a single gate electrode structure with one gate electrode 20, as shown in FIGs. 1A to 1E, it is difficult to achieve output saturation characteristics. In addition, there is a non-negligible gap between transfer curves according to voltages between source and drain of a thin film transistor within a subthreshold region, whereby problems of crosstalk or non-uniform luminance such as spots may occur on a screen. Especially, if the thin film transistor with the single gate electrode structure is applied to the organic light emitting device, a compensation capacity may be deteriorated.

50 [0014] Also, in case of the related art thin film transistor with the etch stopper 40, the thin film transistor is inevitably increased in size due to an overlay rule in between each layer. Due to the increased size of thin film transistor, an overlap area between the gate electrode 20 and the source/drain electrodes 62/64 is increased in size, to thereby increase a capacitance of the thin film transistor.

55 **SUMMARY**

[0015] Accordingly, the present invention is directed to a thin film transistor substrate that substantially obviates one

or more problems due to limitations and disadvantages of the related art.

**[0016]** An aspect of the present invention is to provide a thin film transistor substrate which facilitates to improve output and transfer characteristics of thin film transistor.

**[0017]** Another aspect of the present invention is to provide a thin film transistor substrate which facilitates to restrict the increase of capacitance of a thin film transistor due to the increase of overlay rule.

**[0018]** Another aspect of the present invention is to provide an organic light emitting device using the above thin film transistor substrate.

**[0019]** Additional advantages and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

**[0020]** To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, there is provided a thin film transistor substrate comprising: a thin film transistor comprising a lower gate electrode on a substrate, an active layer on the lower gate electrode, source and drain electrodes on the active layer, and an upper gate electrode on the source electrode, drain electrode and active layer, the upper gate electrode for covering a channel region defined by the source and drain electrodes; and a contact portion for electrically connecting the lower gate electrode with the upper gate electrode.

**[0021]** In another aspect a method for manufacturing a thin film transistor substrate comprising: sequentially forming a lower gate electrode, a gate insulating layer and an active layer on a substrate; forming a first contact hole by patterning the gate insulating layer so as to expose the lower gate electrode; forming a source/drain electrode layer on the active layer; forming a source electrode, a drain electrode and a contact portion by patterning the source/drain electrode layer, wherein the contact portion is in contact with the lower gate electrode through the first contact hole; forming a passivation layer on an entire surface of the substrate including the source electrode, drain electrode, and contact portion; forming a second contact hole by patterning the passivation layer to expose the contact portion; and forming an upper gate electrode on the passivation layer, wherein the upper gate electrode covers a channel region defined by the source electrode and the drain electrode, and the upper gate electrode is brought into contact with the contact portion through the second contact hole.

**[0022]** In another aspect a method for manufacturing a thin film transistor substrate comprising: sequentially forming a lower gate electrode, a gate insulating layer and an active layer on a substrate; forming an etch stopper layer on an entire surface of the substrate including the active layer; forming a first contact hole by patterning the gate insulating layer and the etch stopper layer so as to expose the lower gate electrode; forming a source/drain electrode layer on the etch stopper layer; forming a source electrode, a drain electrode and a contact portion by patterning the source/drain electrode layer, wherein the contact portion is brought into contact with the lower gate electrode through the first contact hole; forming a passivation layer on the entire surface of the substrate including the source electrode, the drain electrode and the contact portion; forming a second contact hole by patterning the passivation layer to expose the contact portion; and forming an upper gate electrode on the passivation layer, wherein the upper gate electrode covers a channel region defined by the source electrode and the drain electrode, and the upper gate electrode is brought into contact with the contact portion through the second contact hole.

**[0023]** In a further aspect of the present invention, there is provided an OLED comprising: a substrate; a first thin film transistor on the substrate; a second thin film transistor connected with the first thin film transistor; a first contact portion connected with the first thin film transistor and the second thin film transistor; and an organic light emitting diode connected with the first thin film transistor, wherein the first thin film transistor comprises: a lower gate electrode on the substrate; an active layer on the lower gate electrode; source and drain electrodes on the active layer; and an upper gate electrode on the source electrode, the drain electrode and the active layer, the upper gate electrode for covering a channel region defined by the source electrode and the drain electrode, wherein the first contact portion is formed as a single body with the source electrode or drain electrode of the second thin film transistor so as to electrically connect the lower gate electrode and the upper gate electrode with each other.

**[0024]** It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0025]** The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

**[0026]** FIGs. 1A to 1E are cross sectional views illustrating a method for manufacturing an ESL type thin film transistor substrate;

[0027] FIG. 2A is a plane view illustrating a thin film transistor substrate according to the first embodiment of the present invention;

[0028] FIG. 2B is a cross sectional view along A-A' of FIG. 2A;

[0029] FIG. 3A is a graph illustrating characteristics of a thin film transistor according to the related art;

5 [0030] FIG. 3B is a graph illustrating characteristics of a thin film transistor according to the present invention;

[0031] FIGs. 4A to 4H are cross sectional views illustrating a method for manufacturing the thin film transistor substrate according to the first embodiment of the present invention;

[0032] FIG. 5A is a plane view illustrating a thin film transistor substrate according to the second embodiment of the present invention;

10 [0033] FIG. 5B is a cross sectional view along B-B' of FIG. 5A;

[0034] FIGs. 6A to 6H are cross sectional views illustrating a method for manufacturing the thin film transistor substrate according to the second embodiment of the present invention;

[0035] FIGs. 7A and 7B are cross sectional views of a thin film transistor substrate according to the first modified embodiment of the present invention;

15 [0036] FIG. 8 is a cross sectional view of a thin film transistor substrate according to the second modified embodiment of the present invention;

[0037] FIGs. 9A and 9B are cross sectional views of a thin film transistor substrate according to the third modified embodiment of the present invention; and

[0038] FIG. 10 is a cross sectional view of a storage capacitor according to one embodiment of the present invention.

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## DETAILED DESCRIPTION OF THE INVENTION

[0039] Reference will now be made in detail to the exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

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[0040] On explanation about the embodiments of the present invention, if it is mentioned that a first structure is positioned 'on or above' or 'under or below' a second structure, it should be understood that the first and second structures are brought into contact with each other, or a third structure is interposed between the first and second structures. However, if it is mentioned that a first structure is positioned 'directly on' or 'directly under' a second structure, it should be understood that the first and second structures are brought into contact with each other.

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### FIRST EMBODIMENT

[0041] Hereinafter, a thin film transistor substrate according to the first embodiment of the present invention and a method for manufacturing the same will be described with reference to FIGs. 2 and 3.

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### THIN FILM TRANSISTOR SUBSTRATE

[0042] FIG. 2A is a plane view illustrating a thin film transistor substrate according to the first embodiment of the present invention. FIG. 2B is a cross sectional view along A-A' of FIG. 2A.

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[0043] First, the thin film transistor substrate according to the first embodiment of the present invention will be described with reference to FIG. 2A.

[0044] As shown in FIG. 2A, a thin film transistor (T) and a contact portion 180 are formed on the thin film transistor substrate 100, wherein the thin film transistor (T) functions as a switching element for controlling an operation of each pixel, or a driving element for driving each pixel.

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[0045] The thin film transistor (T) includes a lower gate electrode 110, an etch stopper layer 135, a source electrode 152, a drain electrode 154, and an upper gate electrode 175.

[0046] The lower gate electrode 110 is formed on the thin film transistor substrate 100. The lower gate electrode 110 is electrically connected with the upper gate electrode 175 through the contact portion 180. The lower gate electrode 110 may be diverged from a gate line (not shown).

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[0047] The etch stopper layer 135 is formed between the source electrode 152 and the drain electrode 154. The etch stopper layer 135 prevents an active layer (not shown) formed thereunder from being over-etched.

[0048] The source electrode 152 is connected with a data line 150, and more particularly, the source electrode 152 may be diverged from the data line 150. The drain electrode 154 is formed on the active layer while being opposite to the source electrode 152. The drain electrode 154 is formed at a predetermined interval from the source electrode 152. A channel region is defined by the source electrode 152 and drain electrode 154.

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[0049] According to one embodiment of the present invention, the source electrode 152 or drain electrode 154 may be overlapped with at least a portion of the lower gate electrode 110, or may be overlapped with at least a portion of the

upper gate electrode 175.

**[0050]** The upper gate electrode 175 is formed above the etch stopper layer 135, to thereby cover the channel region defined by the source electrode 152 and drain electrode 154.

5 **[0051]** According to one embodiment of the present invention, if the thin film transistor substrate 100 is applied to an organic light-emitting device (OLED), the upper gate electrode 175 may be formed of an anode electrode of an organic light-emitting diode for the OLED.

**[0052]** The contact portion 180 electrically connects the lower gate electrode 110 with the upper gate electrode 175. According to one embodiment of the present invention, the contact portion 180 is formed at a predetermined interval from the drain electrode 154, wherein the contact portion 180 may be formed in an island shape. In this case, the contact  
10 portion 180 may be formed of the same material as that of the source electrode 152 or drain electrode 154.

**[0053]** As mentioned above, the thin film transistor (T) according to the present invention is formed in a dual gate electrode structure where the lower gate electrode 110 is formed below the active layer, and the upper gate electrode 175 is formed above the active layer. The lower gate electrode 110 and upper gate electrode 175 of the thin film transistor (T) are electrically connected with each other through the contact portion 180.

15 **[0054]** Hereinafter, the thin film transistor substrate according to the first embodiment of the present invention will be described in more detail with reference to FIG. 2B.

**[0055]** As shown in FIG. 2B, the lower gate electrode 110 is formed on the thin film transistor substrate 100, and then a gate insulating layer 120 is formed on an entire surface of the substrate 100 including the lower gate electrode 110.

20 **[0056]** According to one embodiment of the present invention, a first contact hole (H1) for exposing a predetermined portion of the lower gate electrode 110 so as to form the contact portion 180 is formed in the gate insulating layer 120.

**[0057]** The active layer 130 is formed on the gate insulating layer 120, and the etch stopper layer 135 is formed on the active layer 130. According to one embodiment of the present invention, the active layer 130 may be formed of an oxide semiconductor.

25 **[0058]** The source electrode 152 and drain electrode 154 are formed on the etch stopper layer 135. Also, the source electrode 152 and drain electrode 154 are formed on predetermined regions of the active layer 130, wherein the predetermined regions indicate the regions which are not overlapped with the etch stopper layer 135, to thereby protect the active layer 130. Although not shown, an ohmic contact layer may be additionally interposed between the active layer 130 and the source/drain electrodes 152/154.

30 **[0059]** A passivation layer 160 is formed on the entire surface of the substrate 100 including the source/drain electrodes 152/154. According to one embodiment of the present invention, a second contact hole (H2) is formed in the passivation layer 160. Through the second contact hole (H2), at least a portion of the contact portion 180 is exposed so that the contact portion 180 is brought into contact with the upper gate electrode 175.

35 **[0060]** According to one embodiment of the present invention, the first contact hole (H1) and second contact hole (H2) may be completely overlapped with each other. In a modified embodiment of the present invention, the first contact hole (H1) and second contact hole (H2) may be partially overlapped with each other, or may not be overlapped with each other.

**[0061]** The upper gate electrode 175 is formed on the passivation layer 160. The upper gate electrode 175 covers at least the channel region. Also, since the upper gate electrode 175 is filled in the second contact hole (H2), the upper gate electrode 175 is brought into contact with the contact portion 180 exposed through the second contact hole (H2), whereby the upper gate electrode 175 is electrically connected with the lower gate electrode 110.

40 **[0062]** According to one embodiment of the present invention, a material for the upper gate electrode 175 may be different from a material for the lower gate electrode 110. For example, the upper gate electrode 175 may be formed of a material whose transparency is higher than that of the lower gate electrode 110.

45 **[0063]** The contact portion 180 is filled in the first contact hole (H1) formed in the gate insulating layer 120. The contact portion 180 may be formed on predetermined portions of the gate insulating layer 120 in the periphery of the first contact hole (H1). According to one embodiment of the present invention, the contact portion 180 may be formed of the same material as those of the source/drain electrodes 152/154.

50 **[0064]** The contact portion 180 is brought into contact with the lower gate electrode 110 exposed through the first contact hole (H1), and is simultaneously brought into contact with the upper gate electrode 175 through the second contact hole (H2), whereby the lower gate electrode 110 and upper gate electrode 175 are electrically connected with each other.

55 **[0065]** In the aforementioned embodiment of the present invention, the reason why the two contact holes (H1 and H2) are used so as to electrically connect the lower gate electrode 110 and upper gate electrode 175 with each other is that etching the plurality of layers at once is difficult. However, if each of the multiple layers is thin, or an etching technology is highly developed, it is possible to form the hole by etching the plurality of layers at once. In this case, the lower gate electrode 110 and upper gate electrode 175 may be electrically connected with each other through one contact hole.

**[0066]** As described above, the thin film transistor (T) according to the first embodiment of the present invention is formed in the dual gate electrode structure where the lower gate electrode 110 is formed below the active layer 130, and the upper gate electrode 175 is formed above the active layer 130, whereby electrons drift using lower and upper

surfaces of the active layer 130.

**[0067]** As shown in graphs of FIGs. 3A and 3B, in comparison with the related art thin film transistor with the single gate electrode structure, the thin film transistor (T) with the dual gate electrode structure according to the present invention can obtain the improved output saturation characteristics. Also, it is possible to decrease a gap between transfer curves according to voltages between source and drain of the thin film transistor within a subthreshold region.

**[0068]** Accordingly, the thin film transistor (T) with the dual gate electrode structure according to the present invention facilitates to improve luminance uniformity of display device, current capacity and compensation capacity of thin film transistor, and to reduce power consumption.

**[0069]** In case of the present invention, it is possible to prevent external light from being incident on bottom and top surfaces of the thin film transistor (T) by the lower gate electrode 110 and upper gate electrode 175, to thereby improve bias temperature stress (BTS) characteristics of the thin film transistor (T). In addition, it is possible to prevent external gas (O<sub>2</sub>) or moisture (H<sub>2</sub>O) from penetrating into the bottom and top surfaces of the thin film transistor (T).

**[0070]** In the thin film transistor (T) according to the present invention, local and global luminance uniformity may be improved, and bright dot and black dot defect may be diminished by shielding an electric field in the bottom and top surfaces of the thin film transistor (T) using the lower gate electrode 110 and upper gate electrode 175.

#### METHOD FOR MANUFACTURING THIN FILM TRANSISTOR SUBSTRATE

**[0071]** FIGs. 4A to 4H are cross sectional views illustrating a method for manufacturing the thin film transistor substrate according to the first embodiment of the present invention, which are cross sectional views along A-A' of FIG. 2A.

**[0072]** First, as shown in FIG. 4A, the lower gate electrode 110 is formed on the substrate 100, and the gate insulating layer 120 is formed on the entire surface of the substrate 100 including the lower gate electrode 110. Then, the active layer 130 is formed on the gate insulating layer 120, and a material layer 135a for forming the etch stopper layer 135 is formed on the entire surface of the substrate 100 including the active layer 130.

**[0073]** As shown in FIG. 4B, the material layer 135a is patterned to form the etch stopper layer 135 on the active layer 130.

**[0074]** As shown in FIG. 4C, the first contact hole (H1) for exposing the lower gate electrode 110 is formed in the gate insulating layer 120.

**[0075]** As shown in FIG. 4D, a source/drain electrode layer 150a is formed on the entire surface of the substrate 100 including the etch stopper layer 135.

**[0076]** As shown in FIG. 4E, the source/drain electrode layer 150a is patterned, thereby forming the source electrode 152 and drain electrode 154 with a predetermined interval therebetween, and simultaneously forming the contact portion 180 inside the first contact hole (H1).

**[0077]** As shown in FIG. 4F, the passivation layer 160 is formed on the entire surface of the substrate 100 including the source/drain electrodes 152/154.

**[0078]** As shown in FIG. 4G, the second contact hole (H2) for exposing the contact portion 180 is formed in the passivation layer 160.

**[0079]** As shown in FIG. 4H, the upper gate electrode 175 is formed on the passivation layer 160. In this case, since the upper gate electrode 175 is filled in the second contact hole (H2), the upper gate electrode 175 is brought into contact with the contact portion 180, whereby the upper gate electrode 175 is electrically connected with the lower gate electrode 110.

#### SECOND EMBODIMENT

**[0080]** In the above description for the first embodiment of the present invention, the etch stopper layer 135 is formed only in the channel region on the active layer 130, whereby the source electrode 152 and drain electrode 154 cover all regions of the active layer 130 except the channel region.

**[0081]** However, in case of the second embodiment of the present invention, an etch stopper layer 135 is formed not only in the channel region but also in regions except the channel region on an active layer 130, whereby the etch stopper layer 135 covers the active layer 130.

**[0082]** Hereinafter, the thin film transistor substrate according to the second embodiment of the present invention will be described in more detail with reference to FIGs. 5 and 6. For the following description, wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts as those of the first embodiment of the present invention.

#### THIN FILM TRANSISTOR SUBSTRATE

**[0083]** FIG. 5A is a plane view illustrating a thin film transistor substrate according to the second embodiment of the

present invention. FIG. 5B is a cross sectional view along B-B' of FIG. 5A.

**[0084]** First, the thin film transistor substrate according to the second embodiment of the present invention will be described with reference to FIG. 5A. As shown in FIG. 5A, a thin film transistor (T) and a contact portion 180 are formed on a thin film transistor substrate 100, wherein the thin film transistor (T) functions as a switching element for controlling an operation of each pixel, or a driving element for driving each pixel.

**[0085]** The thin film transistor (T) includes a lower gate electrode 110, the etch stopper layer 135, a source electrode 152, a drain electrode 154, and an upper gate electrode 175.

**[0086]** The lower gate electrode 110 is formed on the thin film transistor substrate 100. The lower gate electrode 110 is electrically connected with the upper gate electrode 175 through the contact portion 180. The lower gate electrode 110 may be diverged from a gate line (not shown).

**[0087]** The etch stopper layer 135 prevents the active layer (not shown) formed thereunder from being over-etched. The etch stopper layer 135 according to the second embodiment of the present invention is formed on an entire surface of the substrate 100 including the lower gate electrode 110. In a modified embodiment of the present invention, the etch stopper layer 135 may be formed on a predetermined region of the substrate 100. For example, the etch stopper layer 135 may be formed on at least one of a first region and a second region of the substrate 100, wherein the first region may include the thin film transistor region and a line region, and the second region may include a region provided with a storage capacitor.

**[0088]** In order to bring the source electrode 152 and drain electrode 154 into contact with the active layer 130, as shown in FIG. 5A, third contact hole (H3) and fourth contact hole (H4) are formed in the etch stopper layer 135. For example, the source electrode 152 and active layer 130 are brought into contact with each other through the third contact hole (H3), and the drain electrode 154 and active layer 130 are brought into contact with each other through the fourth contact hole (H4).

**[0089]** The source electrode 152 is connected with a data line 150, and more particularly, the source electrode 152 may be diverged from the data line 150. The drain electrode 154 is formed on the active layer while being opposite to the source electrode 152, wherein the drain electrode 154 is formed at a predetermined interval from the source electrode 152. A channel region is defined by the source electrode 152 and drain electrode 154.

**[0090]** According to one embodiment of the present invention, the source electrode 152 or drain electrode 154 may be overlapped with at least a portion of the lower gate electrode 110, or may be overlapped with at least a portion of the upper gate electrode 175.

**[0091]** The upper gate electrode 175 is formed above the etch stopper layer 135, to thereby cover the channel region defined by the source electrode 152 and drain electrode 154.

**[0092]** According to one embodiment of the present invention, if the thin film transistor substrate 100 is applied to an organic light emitting device (OLED), the upper gate electrode 175 may be formed of an anode electrode of an organic light emitting diode for the OLED.

**[0093]** The contact portion 180 electrically connects the lower gate electrode 110 with the upper gate electrode 175. In the same manner as the first embodiment of the present invention, the contact portion 180 is formed at a predetermined interval from the drain electrode 154, wherein the contact portion 180 may be formed in an island shape. In this case, the contact portion 180 may be formed of the same material as that of the source electrode 152 or drain electrode 154.

**[0094]** Hereinafter, the thin film transistor substrate according to the second embodiment of the present invention will be described in more detail with reference to FIG. 5B.

**[0095]** As shown in FIG. 5B, the lower gate electrode 110 is formed on the thin film transistor substrate 100, and then a gate insulating layer 120 is formed on the entire surface of the substrate 100 including the lower gate electrode 110 (for example, the thin film transistor region and the line region except a region on which the storage capacitor is formed of the substrate 100). Then, the active layer 130 is formed on the gate insulating layer 120. According to one embodiment of the present invention, the active layer 130 may be formed of an oxide semiconductor.

**[0096]** The etch stopper layer 135 is formed on the entire surface of the substrate 100 including the active layer 130, as mentioned above. In this case, the third contact hole (H3) and fourth contact hole (H4) are formed in the etch stopper layer 135. For example, the source electrode 152 and active layer 130 are brought into contact with each other through the third contact hole (H3), and the drain electrode 154 and active layer 130 are brought into contact with each other through the fourth contact hole (H4).

**[0097]** In case of the thin film transistor (T) according to the first embodiment of the present invention, the source/drain electrodes 152/154 cover all regions of the active layer 130 except the channel region, whereby the overlap area between the source/drain electrodes 152/154 and the lower gate electrode 110 is increased in size. However, in case of the second embodiment of the present invention, the etch stopper layer 135 is formed on the entire surface of the substrate 100, whereby the etch stopper layer 135 covers all regions of the active layer 130 except the contact region between the source/drain electrodes 152/154 and the active layer 130.

**[0098]** Thus, in comparison with the first embodiment of the present invention, the second embodiment of the present invention is provided with the decreased overlap area between the lower gate electrode 110 and the source/drain

electrodes 152/154. As shown in the following Table 1, when the thin film transistor (T) is turned-on/off, a capacitance of the thin film transistor (T) according to the second embodiment of the present invention is reduced largely in comparison with the first embodiment of the present invention.

5 [Table 1]

		First embodiment		Second embodiment		Off cap ratio		On cap ratio	
kind	Completion value	Off cap		On cap		First embodiment/ Second embodiment (%)		First embodiment/ Second embodiment (%)	
Sw. TFT	5/11.4	14.2		33.15		79%		82%	
Sc. TFT	10/11.4	20.5		50.45		79%		82%	
Dr. TFT	100/11.4	CGS	CGD	288	CGS	CGD	256.33	CGS	CGD
		141.2	53.3		109	53.3		77%	The same

25 **[0099]** Also, the contact region between the active layer 130 and the source/drain electrodes 152/154 is determined based on a design rule of the etch stopper layer 135, whereby an overlay rule of the active layer 130 and the source/drain electrodes 152/154 has no influence on the left direction (for example, the direction facing from the drain electrode toward the source electrode in FIG. 5B) and the right direction (for example, the direction facing from the source electrode toward the drain electrode in FIG. 5B).

30 **[0100]** Also, if the active layer 130 is formed of the oxide semiconductor, passivation of the active layer 130 has a large influence on reliability of the thin film transistor (T). In case of the second embodiment of the present invention, the etch stopper layer 135 protects not only channel region but also all regions of the active layer 130 except the contact region between the active layer 130 and the source/drain electrodes 152/154, whereby reliability of the thin film transistor (T) may be improved.

35 **[0101]** As mentioned above, a parasitic capacitance of the thin film transistor (T) is minimized owing to the structure of the etch stopper layer 135, to thereby reduce a line resistance.

**[0102]** For forming the contact portion 180, a first contact hole (H1) for exposing a predetermined portion of the lower gate electrode 110 is formed in the gate insulating layer 120 and etch stopper layer 135.

40 **[0103]** The source/drain electrodes 152/154 are formed on the etch stopper layer 135. As mentioned above, the source/drain electrodes 152/154 are brought into contact with the active layer 130 through the third and fourth contact holes (H3, H4). Although not shown, an ohmic contact layer may be additionally interposed between the active layer 130 and the source/drain electrodes 152/154.

**[0104]** A passivation layer 160 is formed on the entire surface of the substrate 100 including the source/drain electrodes 152/154. Then, a second contact hole (H2) for exposing at least a portion of the contact portion 180 is formed in the passivation layer 160, to thereby bring the contact portion 180 into contact with the upper gate electrode 175.

45 **[0105]** The first contact hole (H1) and second contact hole (H2) may be completely overlapped with each other. According to a modified embodiment of the present invention, the first contact hole (H1) and second contact hole (H2) may be partially overlapped with each other, or may not be overlapped with each other.

50 **[0106]** The upper gate electrode 175 is formed on the passivation layer 160, wherein the upper gate electrode 175 covers at least the channel region. Also, since the upper gate electrode 175 is filled in the second contact hole (H2), the upper gate electrode 175 is brought into contact with the contact portion 180 exposed through the second contact hole (H2), whereby the upper gate electrode 175 is electrically connected with the lower gate electrode 110.

**[0107]** According to one embodiment of the present invention, a material for the upper gate electrode 175 may be different from a material for the lower gate electrode 110. For example, the upper gate electrode 175 may be formed of a material whose transparency is higher than that of the lower gate electrode 110.

55 **[0108]** The contact portion 180 is formed inside the first contact hole (H1) formed in the gate insulating layer 120 and etch stopper layer 135. The contact portion 180 may be formed not only inside the first contact hole (H1) but also on predetermined portions of the etch stopper layer 135 in the periphery of the first contact hole (H1). According to one embodiment of the present invention, the contact portion 180 may be formed of the same material as those of the source/

drain electrodes 152/154. The contact portion 180 is brought into contact with the lower gate electrode 110 exposed through the first contact hole (H1), and is simultaneously brought into contact with the upper gate electrode 175 exposed through the second contact hole (H2), whereby the lower gate electrode 110 and upper gate electrode 175 are electrically connected with each other.

5 **[0109]** In the aforementioned embodiment of the present invention, the reason why the two contact holes (H1 and H2) are used so as to electrically connect the lower gate electrode 110 and upper gate electrode 175 with each other is that etching the plurality of layers at once is difficult. However, if each of the multiple layers is thin, or an etching technology is highly developed, it is possible to form the hole by etching the plurality of layers at once. In this case, the lower gate electrode 110 and upper gate electrode 175 may be electrically connected with each other through one contact hole.

10 **[0110]** As mentioned above, the thin film transistor (T) according to the second embodiment of the present invention is formed in a dual gate electrode structure, and the etch stopper layer 135 is formed on the entire surface of the substrate 110. Thus, the thin film transistor (T) according to the second embodiment of the present invention enables to have efficiency of the thin film transistor (T) of the dual gate electrode structure disclosed in the first embodiment of the present invention, and also to reduce the line resistance and capacitance of thin film transistor (T).

#### 15 METHOD FOR MANUFACTURING THIN FILM TRANSISTOR SUBSTRATE

**[0111]** FIGs. 6A to 6H are cross sectional views illustrating a method for manufacturing the thin film transistor substrate according to the second embodiment of the present invention, which are cross sectional views along B-B' of FIG. 5A.

20 **[0112]** First, as shown in FIG. 6A, the lower gate electrode 110 is formed on the substrate 100, and the gate insulating layer 120 is formed on the entire surface of the substrate 100 including the lower gate electrode 110. Then, the active layer 130 is formed on the gate insulating layer 120, and a material layer 135a for forming the etch stopper layer 135 is formed on the entire surface of the substrate 100 including the active layer 130.

25 **[0113]** As shown in FIG. 6B, the material layer 135a is patterned to form the etch stopper layer 135 including the third and fourth contact holes (H3, H4) for exposing the active layer 130.

**[0114]** As shown in FIG. 6C, the first contact hole (H1) for exposing the lower gate electrode 110 is formed by patterning the gate insulating layer 120 and etch stopper layer 135.

30 **[0115]** In FIGs. 6B and 6C, the process for forming the third and fourth contact holes (H3, H4) and the process for forming the first contact hole (H1) are performed separately. According to a modified embodiment of the present invention, the process for forming the third and fourth contact holes (H3, H4) and the process for forming the first contact hole (H1) may be performed through single etching process.

**[0116]** Then, as shown in FIG. 6D, a source/drain electrode layer 150a is formed on the entire surface of the substrate 100 including the etch stopper layer 135.

35 **[0117]** As shown in FIG. 6E, the source/drain electrode layer 150a is patterned, thereby forming the source electrode 152 and drain electrode 154 with a predetermined interval therebetween, and simultaneously forming the contact portion 180 inside the first contact hole (H1). Accordingly, the source electrode 152 is brought into contact with the active layer 130 through the third contact hole (H3), and the drain electrode 154 is brought into contact with the active layer 130 through the fourth contact hole (H4).

40 **[0118]** As shown in FIG. 6F, the passivation layer 160 is formed on the entire surface of the substrate 100 including the source/drain electrodes 152/154.

**[0119]** As shown in FIG. 6G, the second contact hole (H2) for exposing the contact portion 180 is formed in the passivation layer 160.

45 **[0120]** As shown in FIG. 6H, the upper gate electrode 175 is formed on the passivation layer 160. In this case, since the upper gate electrode 175 is filled in the second contact hole (H2), the upper gate electrode 175 is brought into contact with the contact portion 180, whereby the upper gate electrode 175 is electrically connected with the lower gate electrode 110.

#### FIRST MODIFIED EMBODIMENT

50 **[0121]** In the above first and second embodiments of the present invention, the contact portion 180 for electrically connecting the lower gate electrode 110 and upper gate electrode 175 of the thin film transistor (T1) is formed in the island shape. However, according to the first modified embodiment of the present invention, as shown in FIGs. 7A and 7B, a contact portion 180 may be formed as a single body with a source electrode or drain electrode (S or D) of a thin film transistor (T2).

55 **[0122]** Also, in the above first and second embodiments of the present invention, the source electrode 152 is connected with the data line 150. However, according to the first modified embodiment of the present invention, a source electrode 152 may be connected with a power line.

SECOND MODIFIED EMBODIMENT

**[0123]** If the thin film transistor substrate 100 according to the aforementioned embodiment of the present invention is applied to a bottom emission type OLED, as shown in FIG. 8, a connection electrode 176 is formed on a passivation layer 160, wherein the connection electrode 176 is provided at a predetermined interval from an upper gate electrode 175. On the connection electrode 176, there are a color filter layer 800, a planarization layer 810, and passivation layer 820 formed sequentially. Then, a pixel electrode 830 is additionally formed on the passivation layer 820, wherein the pixel electrode 830 functions as an anode electrode of a light emitting device.

**[0124]** In this case, the connection electrode 176 is formed of the same material as that of the upper gate electrode 175, and the connection electrode 176 is formed together with the upper gate electrode 175.

**[0125]** Through the connection electrode 176, the pixel electrode 830 may be electrically connected with the source or drain electrode 152 or 154. In more detail, as shown in FIG. 8, the connection electrode 176 is brought into contact with the source or drain electrode 152 or 154 through a fifth contact hole (H5) formed in the passivation layer 160; and the pixel electrode 830 is brought into contact with the connection electrode 176 through a sixth contact hole (H6) formed in the planarization layer 810 and passivation layer 820, whereby the pixel electrode 830 is electrically connected with the source or drain electrode 152 or 154.

**[0126]** This structure reduces a contact resistance by preventing oxidation of the source/drain electrodes 152/154, and also increases a capacitance of the thin film transistor substrate because a dual or triple capacitor is provided by additionally forming the connection electrode 176 between the lower gate electrode 110 and the pixel electrode 830, wherein the connection electrode 176 is formed of the same material as that of the upper gate electrode 175.

**[0127]** For convenience of explanation, FIG. 8 illustrates that the thin film transistor (T) has the structure shown in the second embodiment of the present invention. However, the thin film transistor (T) of FIG. 8 may have the structure shown in the first embodiment of the present invention.

THIRD MODIFIED EMBODIMENT

**[0128]** In the above embodiments of the present invention, one contact portion is formed for each thin film transistor on the thin film transistor substrate. However, in case of the third modified embodiment of the present invention, as shown in FIGs. 9A and 9B, a thin film transistor substrate may be provided in such a manner that two thin film transistors use one contact portion in common.

**[0129]** In more detail, as shown in FIG. 9, if the first thin film transistor (T1) and second thin film transistor (T2) use one lower gate electrode 110 in common, upper gate electrodes 175 of the first thin film transistor (T1) and second thin film transistor (T2) are formed as a single body, both the electric connection between the lower gate electrode 110 and upper gate electrode 175 of the first thin film transistor (T1) and the electric connection between the lower gate electrode 110 and upper gate electrode 175 of the second thin film transistor (T2) may be realized through the use of one contact portion 180.

**[0130]** In this case, as mentioned above, the contact portion 180 may be formed in an island shape.

ORGANIC LIGHT EMITTING DEVICE (OLED)

**[0131]** If the thin film transistor substrate according to the above embodiment of the present invention is applied to an OLED, the thin film transistors shown in FIGs. 2A/2B and FIGs. 3A/3B may be used as one or more switching thin film transistors constituting the OLED. Also, thin film transistors shown in FIGs. 7A and 7B may be used as driving thin film transistors constituting the OLED.

**[0132]** If the OLED includes two or more switching thin film transistors, at least two thin film transistors may electrically connect lower and upper gate electrodes with each other through the use of common contact portion shown in FIGs. 9A and 9B.

**[0133]** Also, in case of a storage capacitor for the OLED, it may be formed in a structure shown in FIG. 10.

**[0134]** In more detail, as shown in FIG. 10, a lower gate electrode 110, a gate insulating layer 120, an etch stopper layer 135 are sequentially formed on a substrate 100. Then, a seventh contact hole (H7) for exposing the lower gate electrode 110 is formed in the gate insulating layer 120 and etch stopper layer 135.

**[0135]** In this case, a contact portion 1080 is filled in the seventh contact hole (H7), wherein the contact portion 1080 is formed of the same material as those of source/drain electrodes (not shown).

**[0136]** Also, a passivation layer 160 is formed on the etch stopper layer 135, and an eighth contact hole (H8) for exposing the contact portion 1080 is formed in the passivation layer 160.

**[0137]** On the passivation layer 160, there is an upper gate electrode 175. According as the upper gate electrode 175 is filled in the eighth contact hole (H8), the upper gate electrode 175 is brought into contact with the contact portion 1080, whereby the upper gate electrode 175 is electrically connected with the lower gate electrode 110.

**[0138]** Also, a pixel electrode 1090 is formed on the upper gate electrode 175. According to one embodiment of the present invention, the pixel electrode 1090 may be formed of the same material as that of an anode electrode of an organic light emitting diode.

**[0139]** In the above embodiments of the present invention, the etch stopper layers are necessarily included. However, in case of modified embodiments of the present invention, the etch stopper layer may be omitted. In this case, the source and drain electrodes may be directly formed on the active layer.

**[0140]** According to the present invention, the lower gate electrode 110 is formed below the active layer 130, and the upper gate electrode 175 is formed above the active layer 130, whereby the electrons drift through both the lower and upper surfaces of the active layer 130, thereby achieving the output saturation characteristics, and, decreasing a gap between transfer curves according to voltages between source and drain of the thin film transistor within a subthreshold region.

**[0141]** According to the present invention, owing to the improved output and transfer characteristics of the thin film transistor, it is possible to improve luminance uniformity of display device, current capacity of thin film transistor and compensation capacity, and to reduce the power consumption.

**[0142]** According to the present invention, it is possible to prevent external light from being incident on the bottom and top surfaces of the thin film transistor (T) by the lower gate electrode 110 and upper gate electrode 175, to thereby improve bias temperature stress (BTS) characteristics of the thin film transistor (T). In addition, it is possible to prevent external gas (O<sub>2</sub>) or moisture (H<sub>2</sub>O) from penetrating into the bottom and top surfaces of the thin film transistor (T).

**[0143]** According to the present invention, the local and global luminance uniformity may be improved, and bright dot and black dot defect may be diminished by shielding the electric field in the bottom and top surfaces of the thin film transistor (T) using the lower gate electrode 110 and upper gate electrode 175.

**[0144]** According to the present invention, the upper gate electrode 175 is positioned between the pixel electrode 830 and the source/drain electrodes 152/154, to thereby reduce the contact resistance by preventing oxidation of the source/drain electrodes 152/154.

**[0145]** According to the present invention, the dual or triple capacitor is provided by additionally forming the upper gate electrode 175 between the lower gate electrode 110 and the pixel electrode 830, to increase the capacitance of the thin film transistor substrate

**[0146]** According to the present invention, the etch stopper layer 135 is formed on the thin film transistor region and the line region except the storage capacitor, and then the etch stopper layer 135 is patterned based on the minimum design rule for the contact between the active layer 130 and the source/drain electrodes 152/154, so that it is possible to decrease the overlap area between the gate electrode and the source/drain electrodes 152/154. Thus, the capacitance of thin film transistor according to the present invention is reduced when the thin film transistor is turned-on/off.

**[0147]** According to the present invention, the etch stopper layer 135 is formed at left and right sides of the channel region on the active layer 130, whereby the active layer 130 is protected by the etch stopper layer 135.

**[0148]** It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

## Claims

1. A thin film transistor substrate comprising:

a thin film transistor comprising a lower gate electrode on a substrate, an active layer on the lower gate electrode, source and drain electrodes on the active layer, and an upper gate electrode on the source electrode, drain electrode and active layer, the upper gate electrode covering a channel region defined by the source and drain electrodes; and  
a contact portion electrically connecting the lower gate electrode with the upper gate electrode.

2. The thin film transistor substrate according to claim 1, wherein the contact portion is formed of the same material as those of the source and drain electrodes.

3. The thin film transistor substrate according to claim 1, wherein the thin film transistor further includes an etch stopper layer formed on an entire surface of the substrate including the active layer.

4. The thin film transistor substrate according to claim 3, wherein the thin film transistor further includes:

- a gate insulating layer interposed between the lower gate electrode and the active layer; and  
a first passivation layer interposed between the upper gate electrode and the source/drain electrodes,  
wherein a first contact hole is formed in the gate insulating layer and etch stopper layer, and a second contact  
5 hole is formed in the first passivation layer,  
the contact portion fills at least the first contact hole, and the upper gate electrode fills at least the second contact  
hole, and  
the lower gate electrode and contact portion are in contact with each other through the first contact hole, and  
the upper gate electrode and contact portion are in contact with each other through the second contact hole.
- 10 **5.** The thin film transistor substrate according to claim 4, wherein the first contact hole and second contact hole are  
not overlapped with each other.
- 6.** The thin film transistor substrate according to claim 3,  
wherein a first contact hole and a second contact hole exposing the active layer are formed in the etch stopper layer,  
15 wherein the source electrode is in contact with the active layer through the first contact hole, and the drain electrode  
is in contact with the active layer through the second contact hole.
- 7.** The thin film transistor substrate according to claim 1, wherein the contact portion is formed in an island shape or  
is formed as a single body with the source electrode or drain electrode of another thin film transistor.
- 20 **8.** The thin film transistor substrate according to claim 1, wherein the upper gate electrode is formed of a material  
whose transparency is higher than that of the lower gate electrode.
- 9.** The thin film transistor substrate according to claim 1, further comprising:  
25 a first passivation layer interposed between the upper gate electrode and the source/drain electrodes;  
a connection electrode at a predetermined interval from the upper gate electrode on the first passivation layer,  
the connection electrode formed of a same material as that of the upper gate electrode;  
a planarization layer on the connection electrode;  
30 a second passivation layer on the planarization layer; and  
a pixel electrode on the second passivation layer,  
wherein the pixel electrode is electrically connected with the source electrode or drain electrode through the  
connection electrode.
- 35 **10.** The thin film transistor substrate according to claim 9,  
wherein a first contact hole exposing the connection electrode and the source or drain electrode is formed in the  
first passivation layer, and  
a second contact hole for exposing the connection electrode is formed in the planarization layer and second pas-  
sivation layer,  
40 wherein the connection electrode fills at least the first contact hole, and the pixel electrode fills at least the second  
contact hole, and  
the connection electrode is in contact with the source or drain electrode through the first contact hole, and the pixel  
electrode is in contact with the connection electrode through the second contact hole.
- 45 **11.** The thin film transistor substrate according to claim 1, wherein the upper gate electrode functions as an anode  
electrode of an organic light emitting diode.
- 12.** The thin film transistor substrate according to claim 1, wherein the active layer is formed of an oxide semiconductor.
- 50 **13.** An organic light emitting device (OLED) comprising:  
a substrate;  
a first thin film transistor on the substrate;  
a second thin film transistor connected with the first thin film transistor;  
55 a first contact portion connected with the first thin film transistor and the second thin film transistor; and  
an organic light emitting diode connected with the first thin film transistor,  
wherein the first thin film transistor comprises:

a lower gate electrode on the substrate;  
an active layer on the lower gate electrode;  
source and drain electrodes on the active layer; and  
an upper gate electrode on the source electrode, the drain electrode, and the active layer, the upper gate  
electrode for covering a channel region defined by the source electrode and the drain electrode,

wherein the first contact portion is formed as a single body with a source electrode or drain electrode of the  
second thin film transistor so as to electrically connect the lower gate electrode and the upper gate electrode  
with each other.

**14.** The OLED according to claim 13, further comprising a second contact portion connected with the second thin film  
transistor,  
wherein the second thin film transistor comprises a lower gate electrode, a source electrode, a drain electrode, and  
an upper gate electrode, and  
the second contact portion is formed in an island shape, and the second contact portion electrically connects the  
lower gate electrode and upper gate electrode of the second thin film transistor with each other.

**15.** The OLED according to claim 14, further comprising a third thin film transistor connected with the second thin film  
transistor,  
wherein the third thin film transistor comprises a lower gate electrode, a source electrode, a drain electrode, and  
an upper gate electrode, and  
wherein the lower gate electrode of the third thin film transistor is formed as a single body with the lower gate  
electrode of the second thin film transistor, and the upper gate electrode of the third thin film transistor is formed as  
a single body with the upper gate electrode of the second thin film transistor, and  
wherein the second contact portion electrically connects the lower gate electrode and upper gate electrode of the  
third thin film transistor with each other.

FIG. 1A

[ Related Art ]

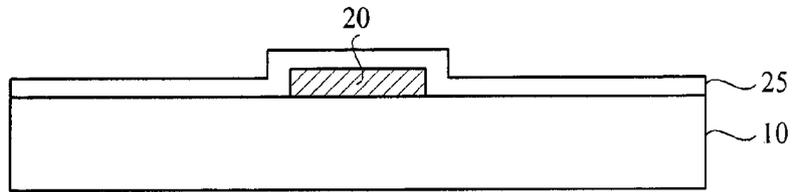


FIG. 1B

[ Related Art ]

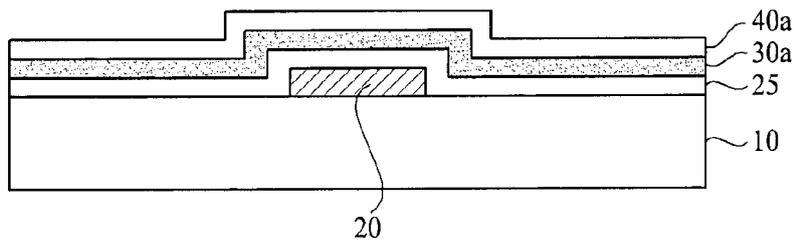


FIG. 1C

[ Related Art ]

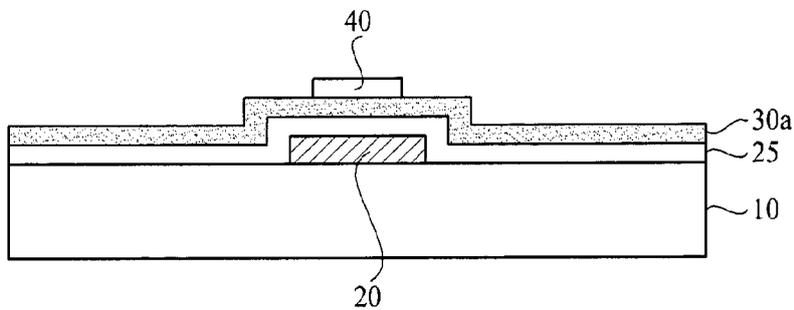


FIG. 1D

[ Related Art ]

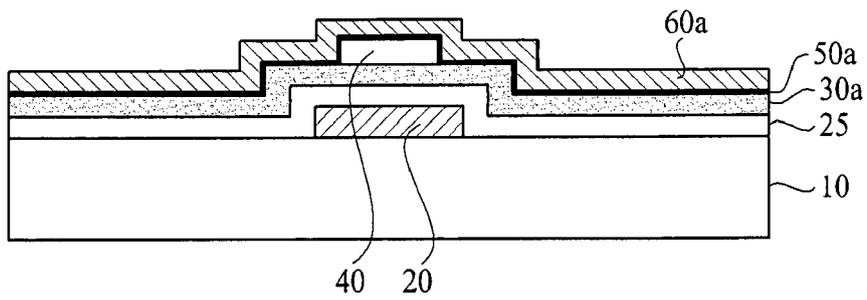


FIG. 1E

[ Related Art ]

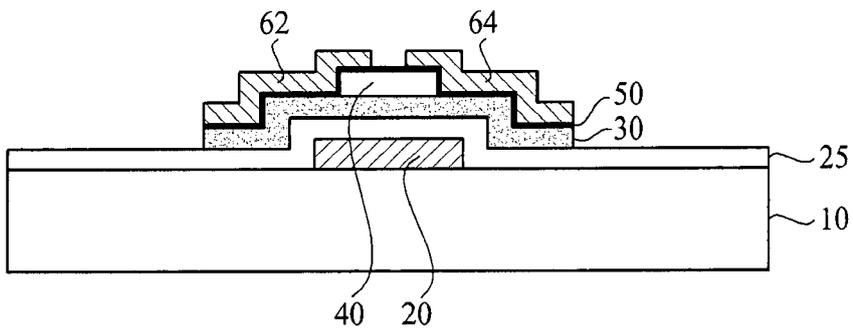


FIG. 2A

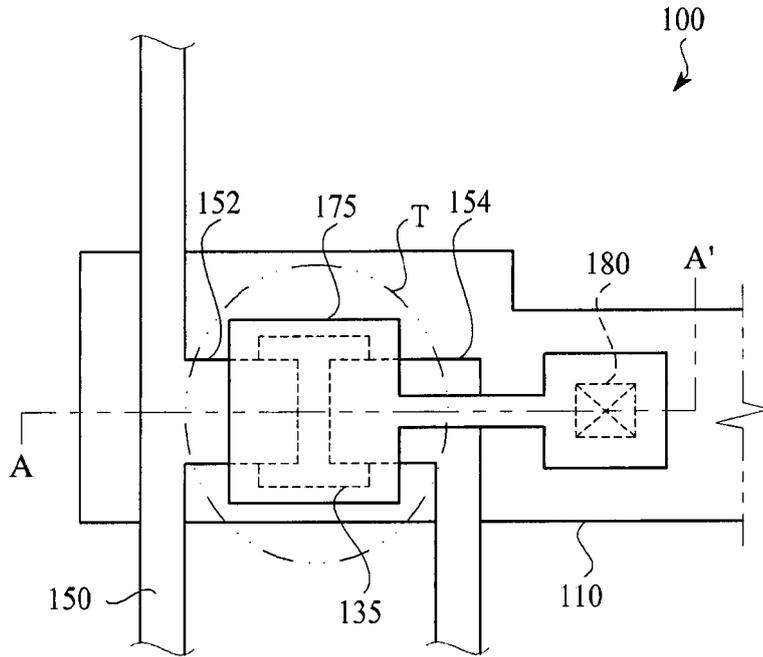


FIG. 2B

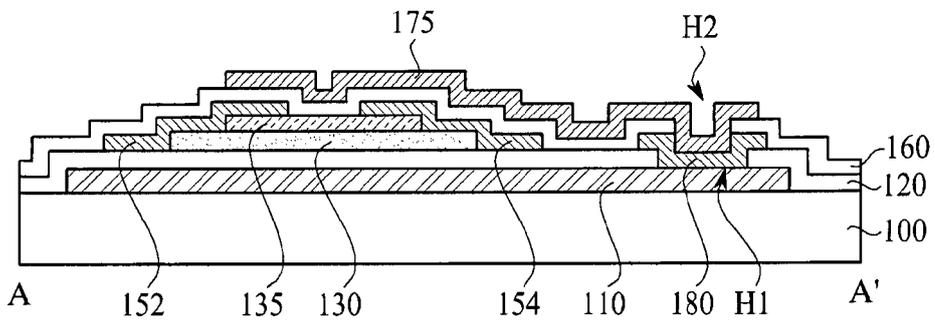


FIG. 3A

SINGLE GATE ELECTRODE THIN FILM TRANSISTOR CHARACTERISTICS

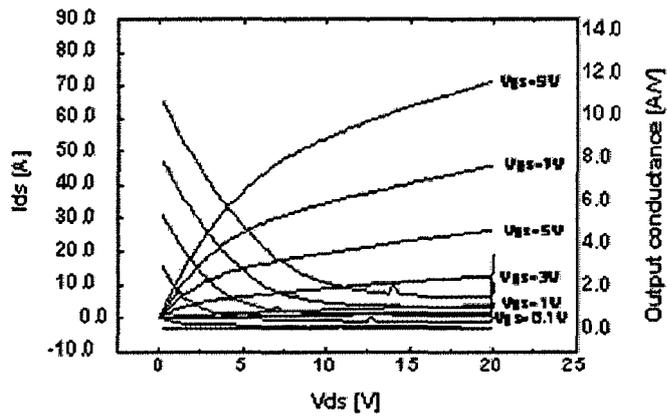


FIG. 3B

DUAL GATE ELECTRODE THIN FILM TRANSISTOR CHARACTERISTICS

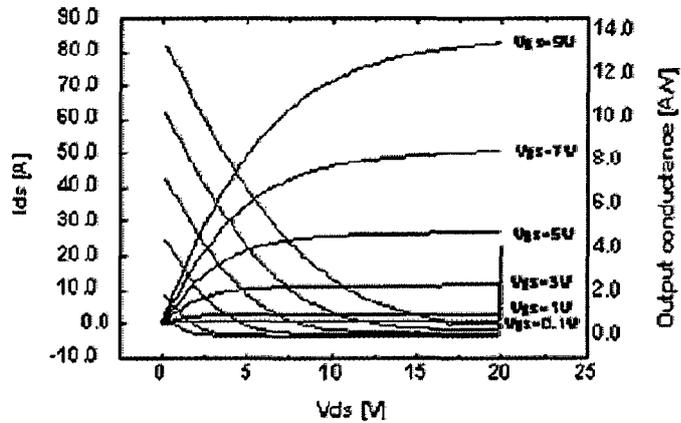


FIG. 4A

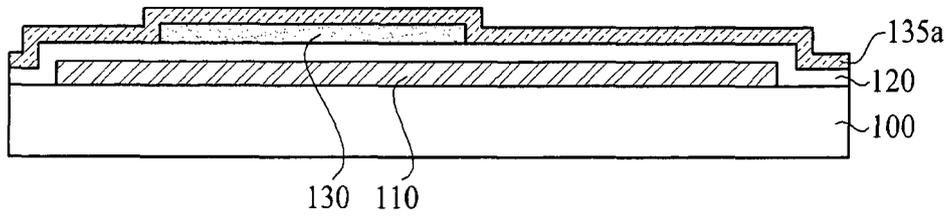


FIG. 4B

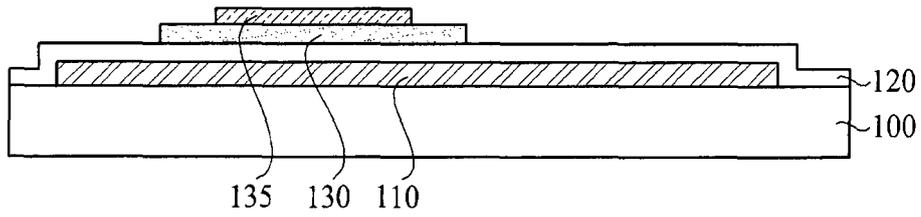


FIG. 4C

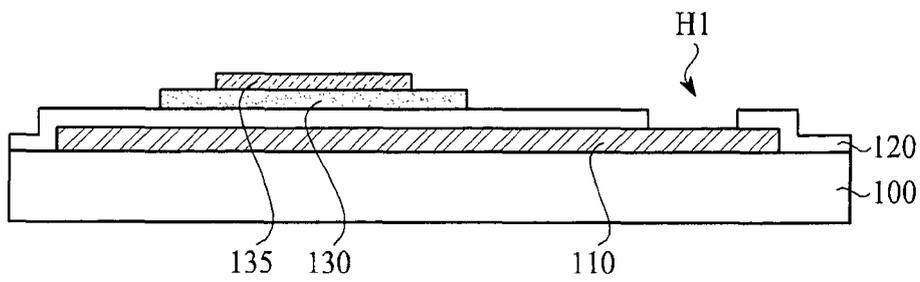


FIG. 4D

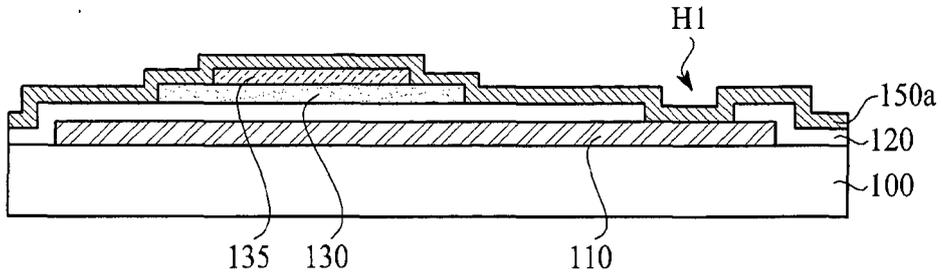


FIG. 4E

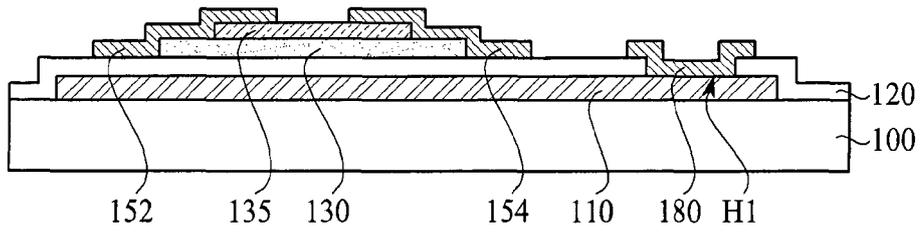


FIG. 4F

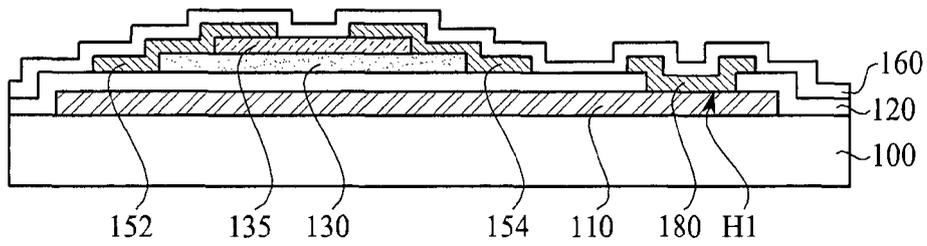


FIG. 4G

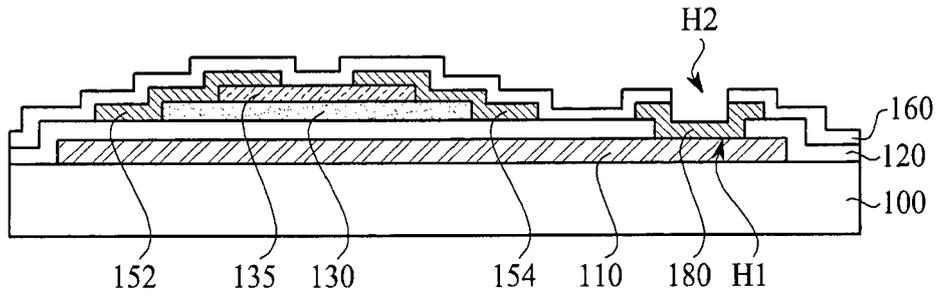


FIG. 4H

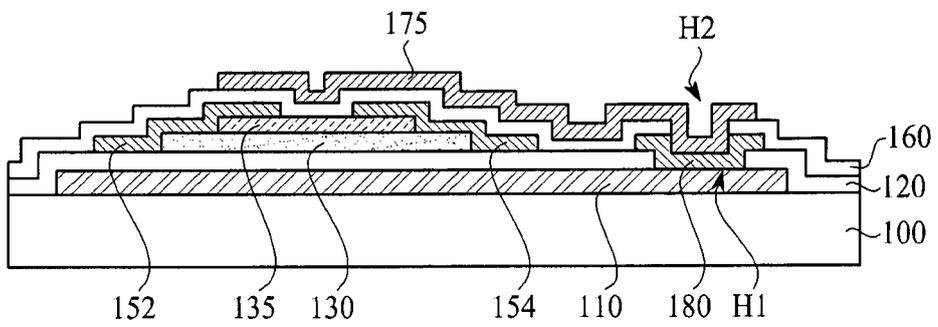


FIG. 5A

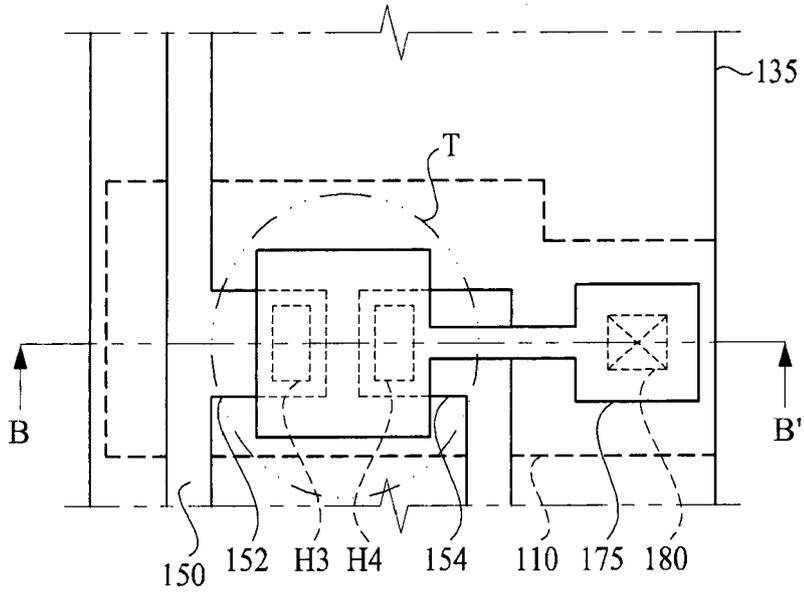


FIG. 5B

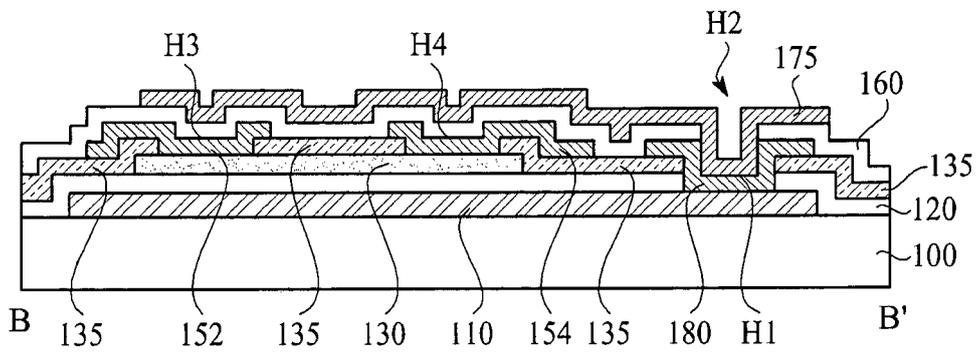


FIG. 6A

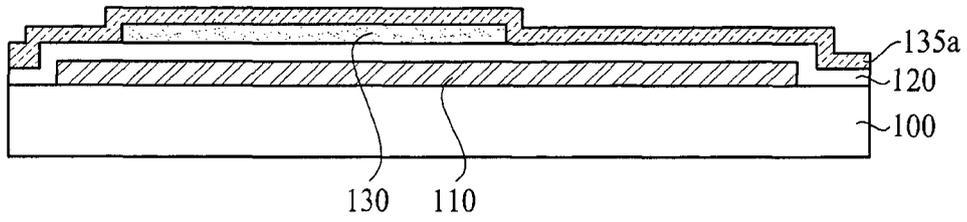


FIG. 6B

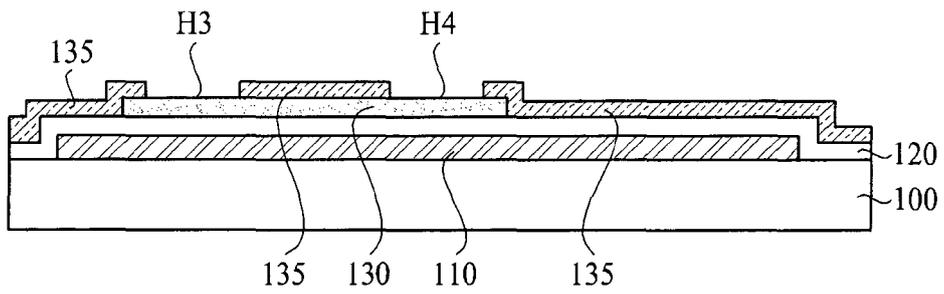


FIG. 6C

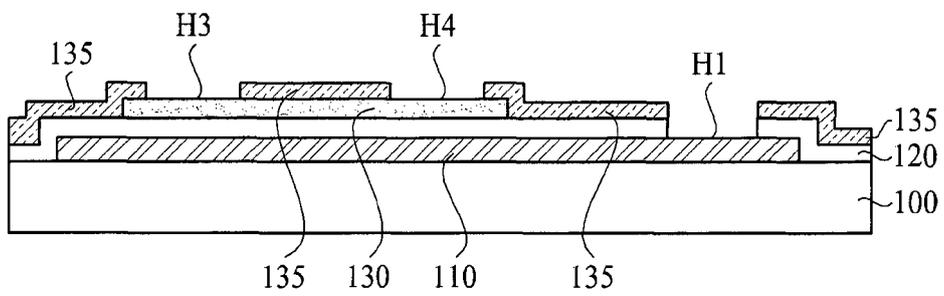


FIG. 6D

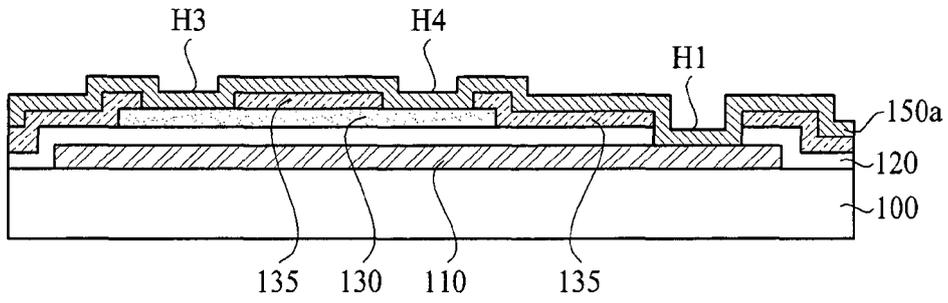


FIG. 6E

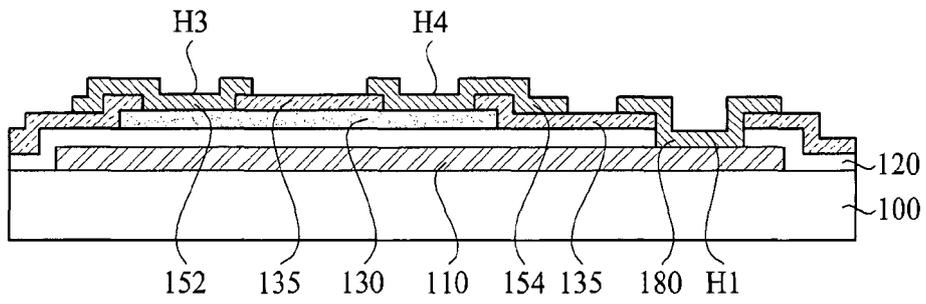


FIG. 6F

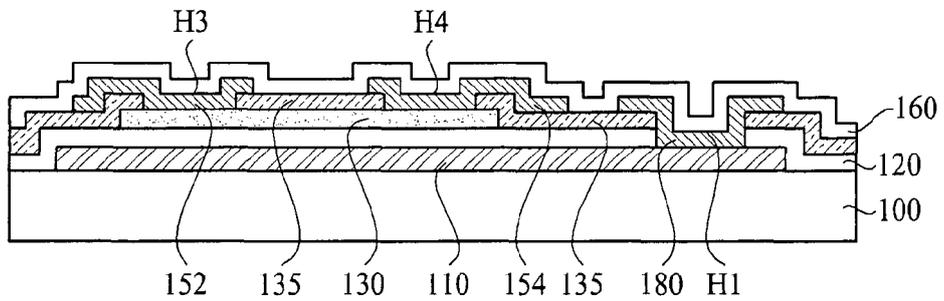


FIG. 6G

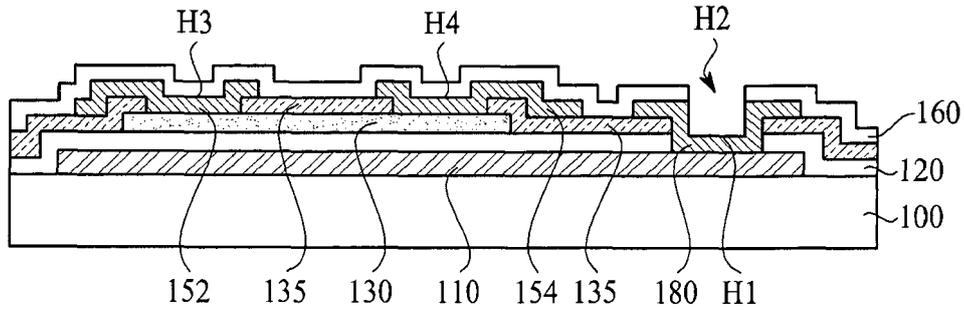


FIG. 6H

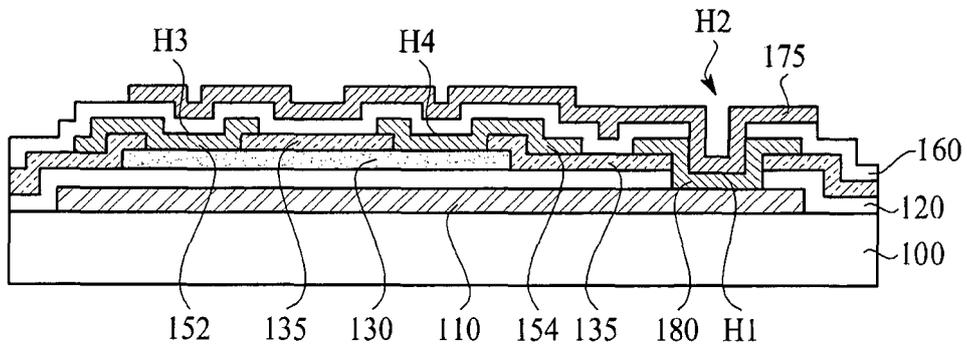


FIG. 7A

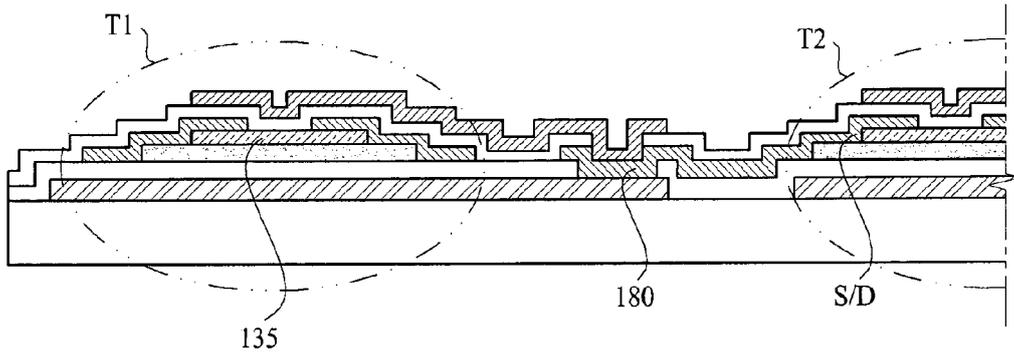


FIG. 7B

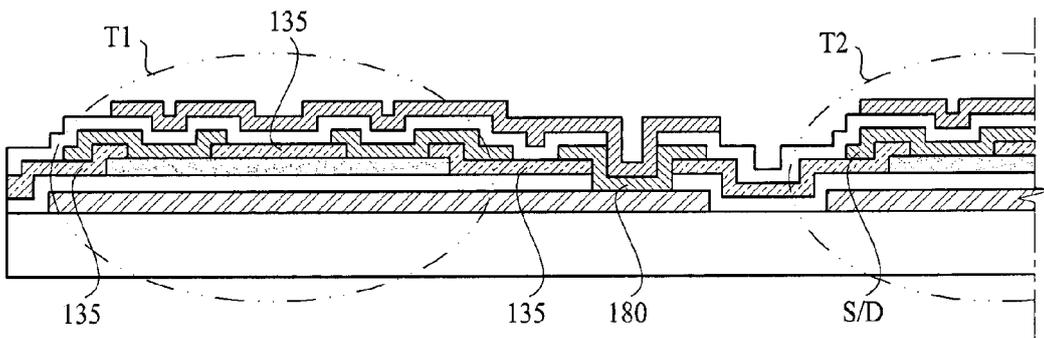




FIG. 9A

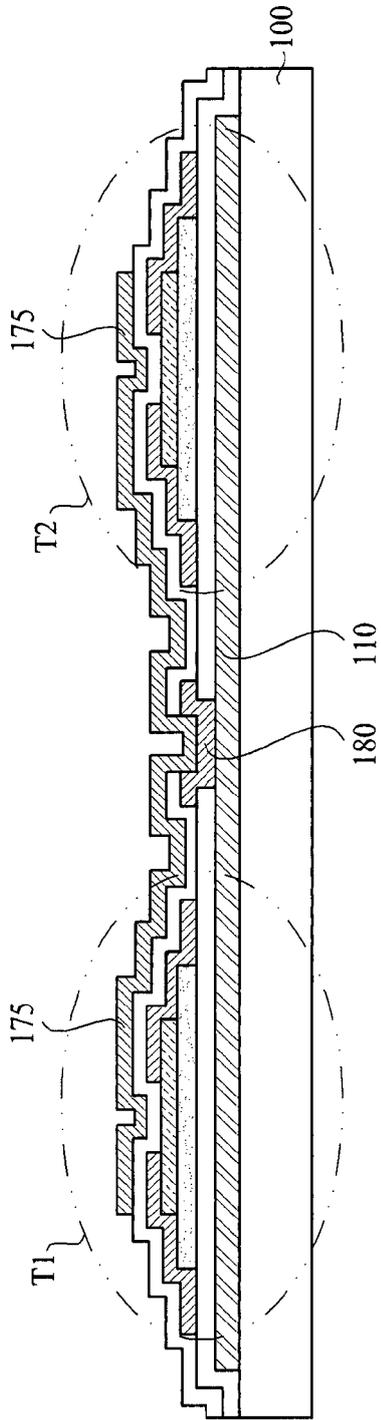


FIG. 9B

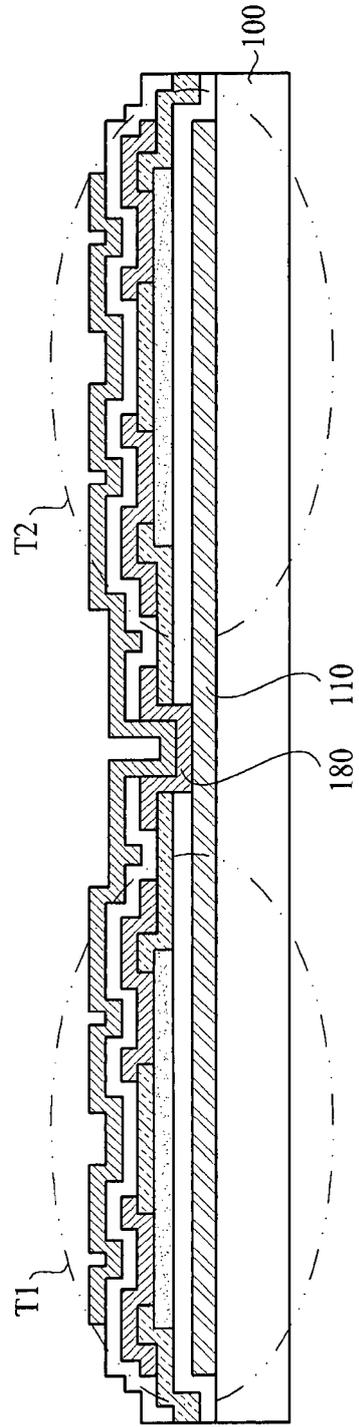
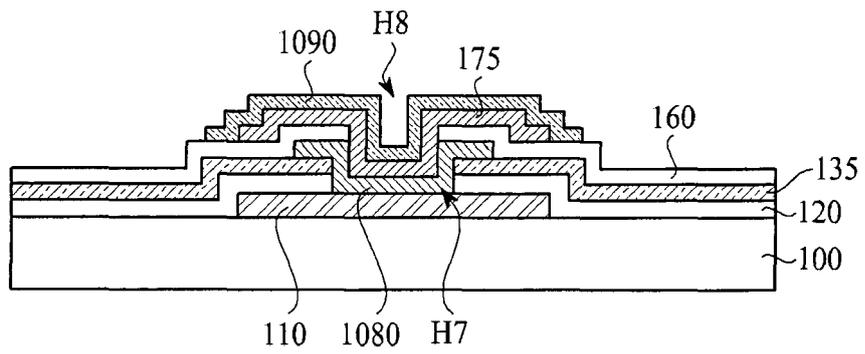


FIG. 10





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