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(54) **An integrated circuit with an external reference resistor network**

Integrierte Schaltung mit einem externen Referenzwiderstandsnetzwerk

Circuit intégré avec un réseau de résistances de références externes

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Description

[0001] The invention relates to an integrated circuit comprising an integrated reference current generation circuit connected via network connection pins to an external reference resistor network.

[0002] In many applications an integrated circuit IC integrated on a chip comprises an integrated reference current generation circuit which is provided to generate a reference current for different circuits integrated on the chip. An on-chip reference current is created in conventional integrated circuits by means of an external resistor across which the reference circuit maintains a constant and well-defined reference voltage V_{ref}. This can be accomplished by means of a differential amplifier which regulates the gate voltage of a MOSFET in a closed loop manner. A current flowing through the transistor is equal to $I_{ref} = V_{ref}/R$, wherein R forms the resistance of the external reference resistor. The reference current I_{ref} provided by the integrated reference current generation circuit connected to the external reference resistor can therefore be adjusted in a wide range of values by selecting the external resistor value R accordingly. The generated reference current can be used within the integrated circuit for different functionalities such as adjusting a frequency, output current or a delay time etc.

[0003] Further, it may happen that the external resistor is partly damaged or broken with the consequence that the integrated circuit receives a reference current I_{ref} generated by the integrated reference current generation circuit connected to the external reference resistor with a wrong current strength and operates outside specified parameter ranges. Moreover, a deviation of the generated reference current from a desired set reference current cannot be detected or diagnosed and no correction of the situation will be performed.

[0004] Fig. 1 shows a conventional circuit which is used in a conventional integrated circuit to avoid the above-mentioned disadvantages, in particular a situation where a reference current with a wrong reference current value is generated because an external reference resistor has been damaged or a wire to the external reference resistor has been cut. As can be seen in Fig. 1 the integrated circuit IC comprises a reference voltage source V_{ref} which supplies a reference voltage to corresponding amplifiers that regulate a gate voltage of an associated MOSFET in a closed loop manner, wherein a current flowing through each MOSFET is given by: $I_{ref} = V_{ref}/R_{ref}$. As can be seen the integrated circuit IC comprises the reference current generation circuit three times each circuit being connected to a corresponding external resistor R_{ref}. The reference current generation circuits in the conventional integrated circuit IC as shown in Fig. 1 are connected to an arbiter circuit which monitors if any of the three reference currents is deviating more than a preset percentage from the other two reference currents. If the arbiter circuit detects that one of the reference currents I_{ref} is deviating too far from the other two reference currents, it selects one of the unaffected two other reference currents and outputs an error flag indicating that an error in one of the reference current generation circuits has occurred.

[0005] A disadvantage of the conventional integrated circuit IC shown in Fig. 1 is that three network connection pins have to be used to connect three external reference resistors R_{ref} to the integrated circuit IC. Further, the space for providing pins connecting the integrated circuit IC to the external electronic circuitry is limited. Moreover, each network connection pin used for one of the integrated reference current generation circuits can not be used for other purposes so that the functionality of the integrated circuit IC is limited.

[0006] US 2008/0073976 A1 relates to a method for increasing the availability and redundancy of an analogue current output. A first set of current sources is activated to generate an output current. A current source of this first set of current sources is cyclically checked for serviceability, and a resulting output current is generated in equal parts by other current sources of the first set of current sources. If an unserviceability of a checked current source is determined, the respective current source is disconnected.

[0007] Accordingly, it is an object of the present invention to provide an integrated circuit having an integrated reference current generation circuit which provides a constant reference current even when one external resistor value deviates from a set value and which needs less connection pins for connecting external reference resistors to the integrated circuit.

[0008] This object is achieved by an integrated circuit comprising the features of claim 1.

[0009] Accordingly, the integrated circuit according to the present invention provides an integrated reference circuit that detects any deviation of a resistor value and compensates this deviation such that the value of the generated reference current I_{ref} remains unaffected and unchanged.

[0010] In a further possible embodiment of the integrated circuit according to the present invention a fourth integrated switch is adapted to interrupt a first external current flowing through an integrated transistor and a first network connection pin of said integrated circuit to said external reference resistor network in response to a control signal applied to said fourth switch by said integrated control circuit.

[0011] In a further possible embodiment of the integrated circuit according to the present invention further a fifth integrated switch is adapted to interrupt a second external current flowing through an integrated transistor via a second network connection pin of said integrated circuit to said external reference resistor network in response to a control signal applied to said fifth switch by said integrated control circuit.

[0012] In a further possible embodiment of the integrated circuit according to the present invention if said integrated control circuit detects a change from a predetermined ratio between the first and second external current it turns off

consecutively the first external current and the second external current by controlling the fourth and fifth integrated switch and compares measured voltages at the first and second network connection pin of said integrated circuit with expected voltages at the first and second network connection pin of said integrated circuit to identify a failing resistor of said external reference resistor network.

[0013] In a further possible embodiment of the integrated circuit according to the present invention the control circuit is adapted to control the integrated switches such that the identified failing resistor of said external reference resistor network is shortened to maintain the reference current generated by said integrated reference current generation circuit constant.

[0014] In a further possible embodiment of the integrated circuit according to the present invention the reference resistor network is connected via wires to the network connection pins of said integrated circuit and comprises resistors each having a predetermined reference resistance.

[0015] In a further possible embodiment of the integrated circuit according to the present invention the external reference resistor network comprises three reference resistors in a Π-configuration connected to a first and second network connection pin of said integrated circuit.

[0016] In a further possible embodiment of the integrated circuit according to the present invention a first reference resistor of said external reference resistor network is connected between both network connection pins of said integrated circuit.

[0017] In a further possible embodiment of the integrated circuit according to the present invention a second reference resistor of said external reference resistor network is connected between a first network connection pin of said integrated circuit and a reference potential.

[0018] In a further possible embodiment of the integrated circuit according to the present invention a third reference resistor is connected between a second network connection pin of said integrated circuit and a reference potential.

[0019] In a further possible embodiment of the integrated circuit according to the present invention the integrated reference current generation circuit comprises

a first reference voltage source adapted to generate a first reference voltage and

a second reference voltage source adapted to generate a second reference voltage being higher than the first reference voltage by a predetermined voltage ratio.

[0020] In a further possible embodiment of the integrated circuit according to the present invention the reference current is a weighted sum of the first external current flowing through a first integrated transistor and the first connection pin of said integrated circuit to said external reference resistor network and of the second external current flowing through a second integrated transistor of the second network connection pin of said integrated circuit to said external reference resistor network,

wherein the reference current I_{ref} is given by:

$$I_{ref} = I_1 + m \cdot I_2,$$

wherein m is a predetermined weighting factor.

[0021] In a further possible embodiment of the integrated circuit according to the present invention the reference current generated by said integrated reference current generation circuit is in a normal operation of said integrated circuit given by:

$$I_{ref} = \left[\frac{1}{R2} + (m-1)(K-1)\frac{1}{R1} + m \cdot K \frac{1}{R3} \right] \cdot \frac{Vref1}{2}$$

wherein R1, R2, R3 are resistance values of the first, second and third reference resistors of said reference resistor network,

m is the weighting factor,

K is the predetermined voltage ratio,

V_{ref} is the reference voltage generated by the first reference voltage source of the integrated circuit.

[0022] In a further possible embodiment of the integrated circuit according to the present invention the sum of the weighting factor m and the voltage ratio K is set to the value two:

$$m + K = 2$$

with

the weighting factor (m) being smaller than one (m < 1), and the voltage ratio (K) being higher than one (K > 1).

[0023] In a further possible embodiment of the integrated circuit according to the present invention the resistance value of the first and second reference resistors of said reference resistor network are equal (R1 = R2 = R).

[0024] In a further possible embodiment of the integrated circuit according to the present invention the voltage ratio K is set to K = 1,5 and the weighting factor m is set to m = 0,5 and the third reference resistor has a resistance value of 3/5 R with R being the resistance values of the first and second reference resistors R1, R2 of said reference resistor network.

[0025] In a further possible embodiment of the integrated circuit according to the present invention if a wire connecting said external reference resistor network with said integrated circuit is cut the reference current generated by said integrated reference current generation circuit is maintained and does decrease by a predetermined percentage.

[0026] In a further possible embodiment of the integrated circuit according to the present invention the integrated control circuit generates an error flag signal indicating that a failure has occurred in said external reference resistor network if such a failure is detected by said integrated control circuit.

[0027] In the following possible embodiments of the integrated circuit having an integrated reference current generation circuit connected to an external reference resistor network are explained in more detail with reference to the enclosed figures.

Fig. 1 shows a conventional circuit as used in a conventional integrated circuit for detecting a faulty resistor of an external reference resistor network;

Fig. 2 shows a block diagram for illustrating a possible embodiment of an integrated circuit comprising an integrated reference current generation circuit connected to an external reference resistor network according to the present invention;

Fig. 3 shows a circuit diagram of a possible implementation of an integrated circuit comprising an integrated reference current generation circuit connected to an external reference resistor network according to the present invention;

Fig. 4 shows a possible circuit board design which can be used for connecting an external reference resistor network to an integrated reference current generation circuit used by an integrated circuit according to the present invention.

[0028] As can be seen from Fig. 2 the integrated circuit IC 1 according to the present invention comprises at least one integrated reference current generation circuit 2 generating an internal reference current I_{ref} used by circuits of the integrated circuit IC for different functions such as adjusting a frequency, an output current or a delay time etc. The reference current generation circuit 2 is connected to an integrated control circuit 3 of the IC 1. The reference current generation circuit 2 of the IC 1 is connected via a first and second network connection pin 4-1, 4-2 to an external reference resistor network 5 comprising in the shown implementation three resistors 6-1, 6-2, 6-3 connected to each other in a Π circuit configuration and having the reference resistor values R1, R2, R3, respectively. The integrated reference current generation circuit 2 is adapted to generate a reference current I_{ref} for the integrated circuit 1 and has reference voltage sources each supplying a reference voltage via a first and second integrated switch to a corresponding amplifier that is adapted to regulate a control voltage of an integrated transistor connected to the respective amplifier such that the generated reference current is a weighted sum of the external currents I_1, I_2 each flowing through one of the integrated transistors via the network connections pins 4-1, 4-2 of the integrated circuit 1 to the external reference resistor network 5 connected to the integrated circuit 1 as shown in Fig. 2. The network connection pins 4-1, 4-2 are connectable to each other by means of a third integrated switch SW3 and to a reference potential GND by means of a first switch SW1 and second switch SW2 integrated in the integrated circuit IC 1 as shown in Fig. 3.

[0029] The integrated control circuit 3 as shown in Fig. 2 is adapted to detect a failure in the external reference resistor network 5 on the basis of the monitored external currents I_1, I_2 of the integrated switches IC such that the reference current I_{ref} generated by said integrated reference current generation circuit 2 is maintained constant even if a failure occurs in said external reference resistor network 5.

[0030] Fig. 3 shows a possible embodiment of an integrated circuit 1 according to the present invention in more detail. As can be seen in Fig. 3 the integrated reference current generation circuit 2 comprises a first reference voltage source 7 connected by means of a connection pin 8 to a reference potential GND as shown in Fig. 3. Moreover, the integrated

circuit 1 comprises a second reference voltage source 9 generating a second reference voltage. The second reference voltage source 9 is adapted to generate a second reference voltage V_{ref2} being higher than the first reference voltage V_{ref1} generated by the first reference voltage source 7 by a predetermined voltage ratio K ($V_{ref2} = K \cdot V_{ref1}$). The first reference voltage source 7 is connected via first controllable switch SW1 of the IC 1 to a corresponding amplifier 10 being a differential amplifier that is adapted to regulate a control voltage of an integrated transistor 11 connected to the output of the respective differential amplifier 10 such that a first external current I_1 flows through the first network connection pin 4-1 to the external reference resistor network 5. The second reference voltage source 9 supplies the generated reference voltage also to an input of a differential amplifier 12 whose output is connected to a second transistor 13. The differential amplifier 12 is connected to regulate a control voltage of the integrated second transistor 13 connected to the differntial amplifier such that a second current I_2 flows through the second network connection pin 4-2 to the external reference resistor network 5. The currents flowing to the external reference resistor network 5 are split or minored with predefined ratios using associated transistors connected in parallel to the transistors 11, 13, respectively. As can be seen transistor 11 is a MOSFET having a gate connected to the output of the operational amplifier 10 to which a similar transistor 11' is connected in parallel such that the external current I_1 flowing through the connection pin 4-1 is split according to a 1:1 ratio so that half of the amplitude of the external current I_1 is applied to integrated control circuit 3 if a fourth integrated switch SW4 of the IC 1 is closed. In the same manner the transistors 13', 13" are connected in parallel to the other transistor 13 so that the external current I_2 is split and a predetermined fraction of the current I_2 is applied to the integrated control circuit 3 if the switch SW5 of the IC 1 is closed. As can be seen in Fig. 3 the generated reference current I_{ref} is output by the integrated reference current generation circuit 2 **???** is a weighted sum of the external currents I_1, I_2 flowing through one of the integrated transistors 11, 13 and the network connection pins 4-1, 4-2 of said integrated circuit 1 to the external reference resistor network 5 connected to the integrated circuit 1.

[0031] As can be seen from Fig. 3 the first and second network connection pin 4-1, 4-2 can be connected to each other by means of a third integrated switch SW3 controlled by the integrated control circuit 3. Moreover, the network connection pins 4-1, 4-2 can also be connected to a reference potential GND by means of the controlled first and second switch SW1, SW2 as shown in Fig. 3.

[0032] The integrated circuit 1 further comprises a fourth integrated switch SW4 which is adapted to interrupt a first external current I_1 flowing through a first integrated transistor 11 of the first network connection pin 4-1 of said integrated circuit 1 to said external reference resistor network 5 in response to a control signal applied to the fourth switch SW4 by said integrated control circuit 3 as shown in Fig. 3.

[0033] The fifth integrated switch SW5 is adapted to interrupt the second external current I_2 flowing through an integrated transistor 13 of the second network connection pin 4-2 of said integrated circuit 1 to said external reference resistor network 5 in response to a control signal applied to said fifth switch SW5 by said integrated control circuit 3.

[0034] In a possible embodiment of the integrated circuit 1 according to the present invention if the integrated control circuit 3 detects a change from a predetermined ratio between the first and second external current I_1, I_2 it turns off consecutively the first external current I_1 and the second external current I_2 by controlling the fourth and fifth integrated switch SW4, SW5 and then compares the measured voltages at the first and second network connection pin 4-1, 4-2 of said integrated circuit IC 1 with expected voltages at the first and second network connection pin 4-1, 4-2 of said integrated circuit 1 to identify a failing resistor of the external reference resistor network 5.

[0035] The integrated control circuit 3 is further adapted to control the integrated switches SW1, SW2, SW3, SW4, SW5 such that the identified failing resistor of the external reference resistor network 5 is shortcut to maintain the reference current I_{ref} generated by the integrated reference current generation circuit 2 constant.

[0036] In the embodiment shown in Fig. 3 the external reference resistor network 5 comprises three reference resistors 6-1, 6-2, 6-3 with a Π configuration connected to the first and second network connection pin 4-1, 4-2 of the integrated circuit 1. The first reference resistor 6-1 of said external reference resistor network 5 is connected between both network connection pins 4-1, 4-2 of the integrated circuit 1. A second reference resistor 6-2 of said external reference resistor network is connected between a first network connection pin 4-1 of said integrated circuit 1 and a reference potential that can be formed by a ground potential GND. A third reference resistor 6-3 of the reference resistor network 5 is connected between the second network connection pin 4-2 of said integrated circuit 1 and the reference potential GND as shown in Fig. 3.

[0037] The generated reference current I_{ref} is a weighted sum of the first external current I_1 flowing through the first integrated transistor 11 of the IC 1 and the first network connection pin 4-1 of the integrated circuit IC 1 to said external reference resistor network 5 and of the second external current I_2 flowing through a second integrated transistor 13 of the IC 1 and the second network connection pin 4-2 of said integrated circuit 1 to said external reference resistor network 5, wherein the reference current I_{ref} is given by:

$$I_{ref} = I_1 + m \cdot I_2,$$

wherein m is a predetermined weighting factor.

[0038] In a possible implementation the reference current I_{ref} generated by said integrated reference current generation circuit 2 is given by:

$$I_{ref} = \left[\frac{1}{R2} + (m-1)(K-1)\frac{1}{R1} + m \cdot K \frac{1}{R3} \right] \cdot \frac{Vref1}{2}$$

wherein R1, R2, R3 are resistance values of the first, second and third reference resistors 6-1, 6-2, 6-3 of the reference resistor network 5,
m is the predetermined weighting factor,
K is the predetermined voltage ratio, and
V_{ref1} is the reference voltage generated by the first reference voltage source 7 of the integrated circuit 1.

[0039] In a possible implementation the sum of the predetermined weighting factor m and the voltage ratio K is set to a value 2:

$$m + K = 2$$

wherein in a possible implementation the weighting factor (m) is smaller than one (m < 1), and the voltage ratio (K) is higher than one (K > 1).

[0040] In a possible embodiment the resistance value of the first and second resistor R1, R2 of said reference resistor network 5 are equal (R1 = R2 = R). In a possible implementation if the voltage ratio is set to K = 1,5 and the weighting factor m is set to m = 0,5 the third reference resistor 6-3 comprises a resistance value of 3/5 R wherein R is the resistance values of the two other reference resistors 6-1, 6-2 of the reference resistor network 5. Other combinations such as K = 4/3 and m = 2/3 are also possible leading to R3 = 8 x R. After a detection of a deviation of a resistor the control circuit 3 can identify the failing resistor by consecutively switching off I_1 and I_2 and by comparing the sensed voltage at the terminals with expected reference voltages. Accordingly, the integrated control circuit 3 is able to identify at each of the three resistors 6-1, 6-2, 6-3 within the external reference resistor network 5 an occurred malfunction and then to shortcut the identified faulty resistor such that the generated reference current I_{ref} is maintained constant.

[0041] If one of the resistors 6-1, 6-2, 6-3 has a resistor value R1, R2, R3 deviating from a preset value R_{set} more than 10% the control circuit 3 can deactivate the identified faulty resistor by controlling the integrated switches SW1, SW2, SW 3 accordingly. By closing switch SW3 the first resistor 6-1 is shortcut in case that its resistance value deviates from a preset value too much. Consequently, if a single faulty resistor within the external resistor network 5 is detected the control circuit 3 can perform a switching operation such that the generated reference current I_{ref} is constant and is unaffected by the faulty resistor. In case of another type of malfunction where a wire connecting the external reference resistor network 5 of the integrated circuit 1 is cut the reference current I_{ref} generated by the integrated reference current generation circuit 2 is maintained constant and decreases by a predetermined percentage. Accordingly, in this scenario or situation the circuit according to the present invention operates such that a predetermined percentage of the reference current I_{ref} is still generated although a wire has been cut. In a possible embodiment if a wire cut is detected this causes a decrease of the reference current I_{ref} of less than 19%.

[0042] In a possible embodiment the control circuit 3 generates in case of a malfunction an error signal (ERROR) indicating that a malfunction of the external reference resistor network 5 has occurred. This error signal can also indicate what type of malfunction has occurred, i.e. it can indicate whether there is a faulty resistor 6 in the reference resistor network 5 or a cut wire. In a possible embodiment the ERROR signal also indicates which resistor 6-i is faulty or which wire has been interrupted to a higher software layer.

[0043] Fig. 4 shows a possible printed circuit board PCB design which can be used for connecting an integrated circuit 1 according to the present invention with an external reference resistor network 5. As can be seen in Fig. 4 the separation of wires for all three resistors 6-1, 6-2, 6-3 reduces the risk of a wire cut. Moreover, a wire cut error can only occur as a soldering error or a IC pin to the PCB. This is diagnosed and has an effect in reducing less than 19% of the reference current I_{ref} generated by the reference current generation circuit 2. Further, a loss of ground wire is prevented by double ground wires via ground connection of the integrated circuit 1. In a possible embodiment the integrated circuit 1 according to the present invention can be used in automotive applications. The integrated circuit IC 1 is compliant with ISO 26262 being an automotive safety standard.

Claims

1. An integrated circuit, IC, (1) connectable to an external resistor network (5) comprising three resistors (6-1, 6-2, 6-3) in a π-configuration, the integrated circuit (1) comprising:

   - an integrated reference current generation circuit (2) adapted to generate a reference current (I_{ref}) for said integrated circuit (1) and having a first reference voltage source (7), a first integrated switch (SW1), a first amplifier (10), a first integrated transistor (11), a first network connection pin (4-1), a second reference voltage source (9), a second integrated switch (SW2), a second amplifier (12,) a second integrated transistor (13) and a second network connection pin (4-2),
   - wherein said first reference voltage source (7) supplying a reference voltage (V_{ref1}) via said first integrated switch (SW1) to said first amplifier (10);
   - said second reference voltage source (9) supplying a reference voltage (V_{ref2}) via said second integrated switch (SW2) to said second amplifier (12);
   - the generated reference current (I_{ref}) is a weighted sum of a first current (I_1) flowing through said integrated first transistor (11) via said first network connection pin (4-1) and a second current (I_2) flowing through said integrated second transistor (13) via said second network connection pin (4-2) of said integrated circuit (1) to said external reference resistor network (5) connectable to said integrated circuit, IC (1); and
   - said network connection pins (4-1, 4-2) are connectable to each other by means of a third integrated switch (SW3) and to a reference potential (GND) by means of said first and second switch (SW1, SW2);
   - the said integrated circuit (1) further comprising an integrated control circuit (3) adapted to detect a failure in said external reference resistor network (5) on the basis of the first and the second current (I_1, I_2) and to control said integrated switches (SW1, SW2, SW3) such that the reference current (I_{ref}) generated by said integrated reference current generation circuit (2) is maintained constant if a failure occurs in said external reference resistor network (5) ;
   - a fourth integrated switch (SW4) adapted to interrupt the first current (I_1) flowing through said first integrated transistor (11) and said first network connection pin (4-1) of said integrated circuit (1) to said external reference resistor network (5) in response to a control signal applied to said fourth switch (SW4) by said integrated control circuit (3); and
   - a fifth integrated switch (SW5) adapted to interrupt said second current (I_2) flowing through an said second integrated transistor (13) via said second network connection pin (4-2) of said integrated circuit (1) to said external reference resistor network (5) in response to a control signal applied to said fifth switch (SW5) by said integrated control circuit (3).

2. The integrated circuit according to claim 1,
   wherein if said integrated control circuit (3) detects a change from a predetermined ratio between the first and second external current (I_1, I_2) it turns off consecutively the first current (I_1) and the second current (I_2) by controlling the fourth and fifth integrated switch (SW4, SW5) and compares measured voltages at the first and second network connection pin (4-1, 4-2) of said integrated circuit (1) with expected voltages at the first and second network connection pin (4-1, 4-2) of said integrated circuit (1) to identify a failing resistor (6-1) of said external reference resistor network (5).

3. The integrated circuit according to claim 2,
   wherein the integrated control circuit (3) is adapted to control the integrated switches (SW1, SW2, SW3, SW4, SW5) such that the identified failing resistor of said external reference resistor network (5) is shortened to maintain the reference current (I_{ref}) generated by said integrated reference current generation circuit (2) constant.

4. The integrated circuit according to one of the preceding claims 1 to 3,
   wherein said reference resistor network (5) is connectable via wires to the network connection pins (4-1, 4-2) of said integrated circuit (1) and comprises resistors (6) each having a predetermined reference resistance.

5. The integrated circuit according to one of the preceding claims 1 to 4,
   wherein the three reference resistors (6-1, 6-2, 6-3) of said external reference resistor network (5) are connectable to said first and second network connection pins (4-1, 4-2) of said integrated circuit (1).

6. The integrated circuit according to one of the preceding claims 1 to 5,

   - wherein a first reference resistor (6-1) of said external reference resistor network (5) is connectable between

both network connection pins (4-1, 4-2) of said integrated circuit,
- a second reference resistor (6-2) of said external reference resistor network (5) is connectable between a first network connection pin (4-1) of said integrated circuit (1) and a reference potential, and
- a third reference resistor (6-3) is connectable between a second network connection pin (4-2) of said integrated circuit (1) and said reference potential.

7. The integrated circuit according to one of the preceding claims 1 to 6,
wherein said second reference voltage (V_{ref2}) being higher than the first reference voltage by a predetermined voltage ratio (K).

8. The integrated circuit according to one of the preceding claims 1 to 7,
wherein said reference current (I_{ref}) is a weighted sum of the first current (I_1) flowing through a first integrated transistor (11) and the first connection pin (4-1) of said integrated circuit (1) to said external reference resistor network (5) and of the second current (I_2) flowing through a second integrated transistor (13) and the second network connection pin (4-2) of said integrated circuit to said external reference resistor network (5):

$$I_{ref} = I_1 + m \cdot I_2,$$

wherein m is a predetermined weighting factor.

9. The integrated circuit according to claim 8,
wherein the reference current (I_{ref}) generated by said integrated reference current generation circuit (2) in a normal operation given by:

$$I_{ref} = \left[\frac{1}{R2} + (m-1)(K-1)\frac{1}{R1} + m \cdot K \frac{1}{R3} \right] \cdot \frac{Vref1}{2}$$

wherein R1, R2, R3 are resistance values of the first, second and third reference resistors (6-1, 6-2, 6-3) of said reference resistor network (5),
m is the weighting factor,
K is the predetermined voltage ratio,
V_{ref1} is the reference voltage generated by the first reference voltage source (7).

10. The integrated circuit according to claim 8 or 9,
wherein the sum of the weighting factor (m) and the voltage ratio (K) is set to the value two:

$$m + K = 2$$

with

the weighting factor (m) being smaller than one (m < 1), and
the voltage ratio (K) being higher than one (K > 1).

11. The integrated circuit according to one of the preceding claims 5 to 10,
wherein the resistance value (R1, R2) of the first and second reference resistors (6-1, 6-2) of said reference resistor network (5) are equal (R1 = R2 = R).

12. The integrated circuit according to claim 10 or 11,
wherein for the voltage ratio (K) being set to K = 1,5 and the weighting factor (m) being set to m = 0,5 the third reference resistor (6-3) has a resistance value of 3/5 R with R being the resistance values of the first and second reference resistors (6-1, 6-2) of said reference resistor network (5).

13. The integrated circuit according to one of the preceding claims 1 to 12,
wherein if a wire connecting said external reference resistor network (5) with said integrated circuit (1) is cut the

reference current (I_{ref}) generated by said integrated reference current generation circuit (2) is maintained and does decrease by a predetermined percentage.

14. The integrated circuit according to one of the preceding claims 1 to 13, wherein said integrated control circuit (3) generates an error flag signal indicating that a failure has occurred in said external reference resistor network (5) if such a failure is detected by said integrated control circuit (3).

Patentansprüche

1. Integrierter Schaltkreis (IC) (1), der mit einem externen Widerstandsnetzwerk (5) verbunden werden kann, das drei Widerstände (6-1, 6-2, 6-3) in einer π-Konfiguration umfasst, wobei der integrierte Schaltkreis (1) Folgendes umfasst:

- einen integrierten Referenzstromerzeugungskreis (2), der dafür ausgelegt ist, einen Referenzstrom (I_{ref}) für den integrierten Schaltkreis (1) zu generieren, und Folgendes aufweist: eine erste Referenzspannungsquelle (7), einen ersten integrierten Schalter (SW1), einen ersten Verstärker (10), einen ersten integrierten Transistor (11), einen ersten Netzwerkverbindungsanschluss (4-1), eine zweite Referenzspannungsquelle (9), einen zweiten integrierten Schalter (SW2), einen zweiten Verstärker (12) einen zweiten integrierten Transistor (13), und einen zweiten Netzwerkverbindungsanschluss (4-2), wobei:
- die erste Referenzspannungsquelle (7) eine Referenzspannung (V_{ref1}) über den ersten integrierten Schalter (SW1) in den ersten Verstärker (10) einspeist;
- die zweite Referenzspannungsquelle (9) eine Referenzspannung (V_{ref2}) über den zweiten integrierten Schalter (SW2) in den zweiten Verstärker (12) einspeist;
- der generierte Referenzstrom (I_{ref}) eine gewichtete Summe eines ersten Stroms (I_1), der durch den integrierten ersten Transistor (11) über den ersten Netzwerkverbindungsanschluss (4-1) fließt, und eines zweiten Stroms (I_2) ist, der durch den integrierten zweiten Transistor (13) über den zweiten Netzwerkverbindungsanschluss (4-2) des integrierten Schaltkreises (1) zu dem externen Referenzwiderstandsnetzwerk (5), das mit dem integrierten Schaltkreis (IC) (1) verbunden werden kann, fließt; und
- die Netzwerkverbindungsanschlüsse (4-1, 4-2) mittels einen dritten integrierten Schalters (SW3) miteinander und mittels des ersten und des zweiten Schalters (SW1, SW2) mit einem Referenzpotenzial (GND) verbunden werden können;
- der integrierte Schaltkreis (1) des Weiteren einen integrierten Steuerkreis (3) umfasst, der dafür ausgelegt ist, einen Fehler in dem externen Referenzwiderstandsnetzwerk (5) auf der Basis des ersten und des zweiten Stroms (I_1, I_2) zu detektieren und die integrierten Schalter (SW1, SW2, SW3) so zu steuern, dass der durch den integrierten Referenzstromerzeugungskreis (2) generierte Referenzstrom (I_{ref}) konstant gehalten wird, wenn ein Fehler in dem externen Referenzwiderstandsnetzwerk (5) eintritt;
- einen vierten integrierten Schalter (SW4), der dafür ausgelegt ist, den ersten Strom (I_1), der durch den ersten integrierten Transistor (11) und den ersten Netzwerkverbindungsanschluss (4-1) des integrierten Schaltkreises (1) zu dem externen Referenzwiderstandsnetzwerk (5) fließt, in Reaktion auf ein Steuerungssignal, das durch den integrierten Steuerkreis (3) an den vierten Schalter (SW4) angelegt wird, zu unterbrechen; und
- einen fünften integrierten Schalter (SW5), der dafür ausgelegt ist, den zweiten Strom (I_2), der durch den zweiten integrierten Transistor (13) über den zweiten Netzwerkverbindungsanschluss (4-2) des integrierten Schaltkreises (1) zu dem externen Referenzwiderstandsnetzwerk (5) fließt, in Reaktion auf ein Steuerungssignal, das durch den integrierten Steuerkreis (3) an den fünften Schalter (SW5) angelegt wird, zu unterbrechen.

2. Integrierter Schaltkreis nach Anspruch 1,
wobei, wenn der integrierte Steuerkreis (3) eine Änderung von einem zuvor festgelegten Verhältnis zwischen dem ersten und dem zweiten externen Strom (I_1, I_2) detektiert, er nacheinander den ersten Strom (I_1) und den zweiten Strom (I_2) abschaltet, indem er den vierten und den fünften integrierten Schalter (SW4, SW5) steuert und gemessene Spannungen an dem ersten und dem zweiten Netzwerkverbindungsanschluss (4-1, 4-2) des integrierten Schaltkreises (1) mit erwarteten Spannungen an dem ersten und dem zweiten Netzwerkverbindungsanschluss (4-1, 4-2) des integrierten Schaltkreises (1) vergleicht, um einen fehlerhaften Widerstand (6-1) des externen Referenzwiderstandsnetzwerks (5) zu identifizieren.

3. Integrierter Schaltkreis nach Anspruch 2,
wobei der integrierte Steuerkreis (3) dafür ausgelegt ist, die integrierten Schalter (SW1, SW2, SW3, SW4, SW5) so zu steuern, dass der identifizierte fehlerhafte Widerstand des externen Referenzwiderstandsnetzwerks (5) kurzgeschlossen wird, um den durch den integrierten Referenzstromerzeugungskreis (2) generierten Referenzstrom (I_{ref})

konstant zu halten.

4. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 3,
wobei das Referenzwiderstandsnetzwerk (5) über Leitungen mit den Netzwerkverbindungsanschlüssen (4-1, 4-2) des integrierten Schaltkreises (1) verbunden werden kann und Widerstände (6) umfasst, die jeweils einen zuvor festgelegten Referenzwiderstand besitzen.

5. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 4,
wobei die drei Referenzwiderstände (6-1, 6-2, 6-3) des externen Referenzwiderstandsnetzwerks (5) mit dem ersten und dem zweiten Netzwerkverbindungsanschluss (4-1, 4-2) des integrierten Schaltkreises (1) verbunden werden können.

6. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 5, wobei:

- ein erster Referenzwiderstand (6-1) des externen Referenzwiderstandsnetzwerks (5) zwischen beiden Netzwerkverbindungsanschlüsseb (4-1, 4-2) des integrierten Schaltkreises verbunden werden kann,
- ein zweiter Referenzwiderstand (6-2) des externen Referenzwiderstandsnetzwerks (5) zwischen einem ersten Netzwerkverbindungsanschluss (4-1) des integrierten Schaltkreises (1) und einem Referenzpotenzial verbunden werden kann, und
- ein dritter Referenzwiderstand (6-3) zwischen einem zweiten Netzwerkverbindungsanschluss (4-2) des integrierten Schaltkreises (1) und dem Referenzpotenzial verbunden werden kann.

7. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 6,
wobei die zweite Referenzspannung (V_{ref2}) um ein zuvor festgelegtes Spannungsverhältnis (K) höher ist als die erste Referenzspannung.

8. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 7,
wobei der Referenzstrom (I_{ref}) eine gewichtete Summe des ersten Stroms (I_1), der durch einen ersten integrierten Transistor (11) und den ersten Verbindungsanschluss (4-1) des integrierten Schaltkreises (1) zu dem externen Referenzwiderstandsnetzwerk (5) fließt, und des zweiten Stroms (I_2) ist, der durch einen zweiten integrierten Transistor (13) und den zweiten Netzwerkverbindungsanschluss (4-2) des integrierten Schaltkreises zu dem externen Referenzwiderstandsnetzwerk (5) fließt:

$$I_{ref} = I_1 + m \cdot I_2,$$

wobei m ein zuvor festgelegter Gewichtungsfaktor ist.

9. Integrierter Schaltkreis nach Anspruch 8,
wobei der Referenzstrom (I_{ref}), der durch den integrierten Referenzstromerzeugungskreis (2) in einem normalen Betrieb generiert wird, gegeben ist durch:

$$I_{ref} = \left[\frac{1}{R2} + (m-1)(K-1)\frac{1}{R1} + m \cdot K \frac{1}{R3} \right] \cdot \frac{Vref1}{2}$$

wobei

R1, R2, R3 Widerstandswerte der ersten, zweiten und dritten Referenzwiderstände (6-1, 6-2, 6-3) des Referenzwiderstandsnetzwerks (5) sind,
m der Gewichtungsfaktor ist,
K das zuvor festgelegte Spannungsverhältnis ist, und
V_{ref1} die durch die erste Referenzspannungsquelle (7) generierte Referenzspannung ist.

10. Integrierter Schaltkreis nach Anspruch 8 oder 9, wobei die Summe des Gewichtungsfaktors (m) und des Spannungsverhältnisses (K) auf den Wert zwei eingestellt wird:

$$m + K = 2$$

wobei

der Gewichtungsfaktor (m) kleiner als eins ist (m < 1), und
das Spannungsverhältnis (K) größer als eins ist (K > 1).

11. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 5 bis 10,
wobei der Widerstandswert (R1, R2) des ersten und des zweiten Referenzwiderstands (6-1, 6-2) des Referenzwiderstandsnetzwerks (5) gleich sind (R1 = R2 = R).

12. Integrierter Schaltkreis nach Anspruch 10 oder 11,
wobei für den Fall, dass das Spannungsverhältnis (K) auf K = 1,5 eingestellt ist und der Gewichtungsfaktor (m) auf m = 0,5 eingestellt ist, der dritte Referenzwiderstand (6-3) einen Widerstandswert von 3/5 R hat, wobei R die Widerstandswerte des ersten und des zweiten Referenzwiderstands (6-1, 6-2) des Referenzwiderstandsnetzwerks (5) darstellt.

13. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 12,
wobei, wenn eine Leitung, die das externe Referenzwiderstandsnetzwerk (5) mit dem integrierten Schaltkreis (1) verbindet, durchtrennt wird, der durch den integrierten Referenzstromerzeugungskreis (2) generierte Referenzstrom (I_{ref}) beibehalten wird und um einen zuvor festgelegten Prozentsatz abnimmt.

14. Integrierter Schaltkreis nach einem der vorangehenden Ansprüche 1 bis 13,
wobei der integrierte Steuerkreis (3) ein Fehlerflag-Signal generiert, das anzeigt, dass ein Fehler in dem externen Referenzwiderstandsnetzwerk (5) eingetreten ist, wenn ein solcher Fehler durch den integrierten Steuerkreis (3) detektiert wird.

Revendications

1. Circuit intégré, CI, (1) pouvant être connecté à un réseau de résistances externes (5) comprenant trois résistances (6-1, 6-2, 6-3) selon une configuration en n, le circuit intégré (1) comprenant :

- un circuit intégré de production de courant de référence (2) conçu pour produire un courant de référence (I_{ref}) destiné audit circuit intégré (1), et comportant une première de source tension de référence (7), un premier interrupteur intégré (SW1), un premier amplificateur (10), un premier transistor intégré (11), une première broche de connexion au réseau (4-1), une seconde source de tension de référence (9), un deuxième interrupteur intégré (SW2), un second amplificateur (12), un second transistor intégré (13) et une seconde broche de connexion au réseau (4-2),
- dans lequel ladite première source de tension de référence (7) fournit une tension de référence (V_{ref1}) par l'intermédiaire dudit premier interrupteur intégré (SW1) audit premier amplificateur (10) ;
- ladite seconde source de tension de référence (9) fournit une tension de référence (V_{ref2}) par l'intermédiaire dudit deuxième interrupteur intégré (SW2) audit second amplificateur (12) ;
- le courant de référence produit (I_{ref}) est une somme pondérée d'un premier courant (I_1) circulant à travers ledit premier transistor intégré (11) par l'intermédiaire de ladite première broche de connexion au réseau (4-1), et d'un second courant (I_2) circulant à travers ledit second transistor intégré (13) par l'intermédiaire de ladite seconde broche de connexion au réseau (4-2) dudit circuit intégré (1), vers ledit réseau de résistances étalons externes (5) pouvant être connecté audit circuit intégré, CI (1) ; et
- lesdites broches de connexion au réseau (4-1, 4-2) peuvent être connectées l'une à l'autre au moyen d'un troisième interrupteur intégré (SW3) et à un potentiel de référence (GND) au moyen desdits premier et deuxième interrupteurs (SW1, SW2) ;
- ledit circuit intégré (1) comprenant en outre un circuit intégré de commande (3) conçu pour détecter une défaillance dans ledit réseau de résistances étalons externes (5) sur la base des premier et second courants (I_1, I_2) et pour commander lesdits interrupteurs intégrés (SW1, SW2, SW3), de manière que le courant de référence (I_{ref}) produit par ledit circuit intégré de production de courant de référence (2) soit maintenu constant si une défaillance survient dans ledit réseau de résistances étalons externes (5) ;

- un quatrième interrupteur intégré (SW4) conçu pour interrompre le premier courant (I_1) circulant à travers ledit premier transistor intégré (11) et ladite première broche de connexion au réseau (4-1) dudit circuit intégré (1) vers ledit réseau de résistances étalons externes (5), en réponse à un signal de commande appliqué audit quatrième interrupteur (SW4) par ledit circuit intégré de commande (3) ; et
- un cinquième interrupteur intégré (SW5) conçu pour interrompre ledit second courant (I_2) circulant à travers ledit second transistor intégré (13) par l'intermédiaire de ladite seconde broche de connexion au réseau (4-2) dudit circuit intégré (1) vers ledit réseau de résistances étalons externes (5), en réponse à un signal de commande appliqué audit cinquième interrupteur (SW5) par ledit circuit intégré de commande (3).

2. Circuit intégré selon la revendication 1,
dans lequel si le circuit intégré de commande (3) détecte une variation par rapport à un rapport prédéterminé entre le premier et le second courant externe (I_1, I_2), il coupe successivement le premier courant (I_1) et le second courant (I_2) en commandant les quatrième et cinquième interrupteurs intégrés (SW4, SW5) et compare des tensions mesurées au niveau des première et seconde broches de connexion au réseau (4-1, 4-2) dudit circuit intégré (1) avec des tensions attendues au niveau des première et seconde broches de connexion au réseau (4-1, 4-2) dudit circuit intégré (1) pour identifier une résistance défaillante (6-1) dudit réseau de résistances étalons externes (5).

3. Circuit intégré selon la revendication 2,
dans lequel le circuit intégré de commande (3) est conçu pour commander les interrupteurs intégrés (SW1, SW2, SW3, SW4, SW5), de manière que la résistance défaillante identifiée dudit réseau de résistances étalons externes (5) soit mise en court-circuit pour maintenir le courant de référence (I_{ref}) produit par ledit circuit intégré de production de courant de référence (2) constant.

4. Circuit intégré selon l'une des revendications 1 à 3 précédentes,
dans lequel ledit réseau de résistances étalons (5) peut être connecté par l'intermédiaire de fils aux broches de connexion au réseau (4-1, 4-2) dudit circuit intégré (1) et comprend des résistances (6) ayant chacune une valeur de résistance de référence prédéterminée.

5. Circuit intégré selon l'une des revendications 1 à 4 précédentes,
dans lequel les trois résistances étalons (6-1, 6-2, 6-3) dudit réseau de résistances étalons externes (5) peuvent être connectées auxdites première et seconde broches de connexion au réseau (4-1, 4-2) dudit circuit intégré (1).

6. Circuit intégré selon l'une des revendications 1 à 5 précédentes,

- dans lequel une première résistance étalon (6-1) dudit réseau de résistances étalons externes (5) peut être connectée entre les deux broches de connexion au réseau (4-1, 4-2) dudit circuit intégré,
- une deuxième résistance étalon (6-2) dudit réseau de résistances étalons externes (5) peut être connectée entre une première broche de connexion au réseau (4-1) dudit circuit intégré (1) et un potentiel de référence, et
- une troisième résistance étalon (6-3) peut être connectée entre une seconde broche de connexion au réseau (4-2) dudit circuit intégré (1) et ledit potentiel de référence.

7. Circuit intégré selon l'une des revendications 1 à 6 précédentes,
dans lequel ladite seconde tension de référence (V_{ref2}) est supérieure à la première tension de référence d'un rapport de tension prédéterminé (K).

8. Circuit intégré selon l'une des revendications 1 à 7 précédentes,
dans lequel ledit courant de référence (I_{ref}) est une somme pondérée du premier courant (I_1) circulant à travers un premier transistor intégré (11) et la première broche de connexion (4-1) dudit circuit intégré (1) vers ledit réseau de résistances étalons externes (5), et du second courant (I_2) circulant à travers un second transistor intégré (13) et la seconde broche de connexion au réseau (4-2) dudit circuit intégré vers ledit réseau de résistances étalons externes (5) :

$$I_{ref} = I_1 + m \cdot I_2,$$

où m est un facteur de pondération prédéterminé.

9. Circuit intégré selon la revendication 8,
dans lequel le courant de référence (I_{ref}) produit par ledit circuit intégré de production de courant de référence (2) au cours d'un fonctionnement normal est donné par :

$$I_{ref} = \left[\frac{1}{R2} + (m-1)(K-1)\frac{1}{R1} + m \cdot K\frac{1}{R3}\right] \cdot \frac{Vref1}{2}$$

où

R1, R2, R3 sont des valeurs de résistance des première, deuxième et troisième résistances étalons (6-1, 6-2, 6-3) dudit réseau de résistances étalons (5),
m est le facteur de pondération,
K est le rapport de tension prédéterminé,
V_{ref1} est la tension de référence produite par la première source de tension de référence (7).

10. Circuit intégré selon la revendication 8 ou 9, dans lequel la somme du facteur de pondération (m) et du rapport de tension (K) est fixée à la valeur de 2 :

$$m + K = 2$$

le facteur de pondération (m) étant inférieur à 1 ($m < 1$), et
le rapport de tension (K) étant supérieur à 1 ($K > 1$).

11. Circuit intégré selon l'une des revendications 5 à 10 précédentes,
dans lequel les valeurs de résistance (R1, R2) des première et deuxième résistances étalons (6-1, 6-2) dudit réseau de résistances étalons (5) sont égales (R1 = R2 = R).

12. Circuit intégré selon la revendication 10 ou 11, dans lequel pour que le rapport de tension (K) soit réglé à K = 1,5 et que le facteur de pondération (m) soit réglé à m = 0,5, la troisième résistance étalon (6-3) a une valeur de résistance égale à 3/5 R, R représentant les valeurs de résistance des première et deuxième résistances étalons (6-1, 6-2) dudit réseau de résistances étalons (5).

13. Circuit intégré selon l'une des revendications 1 à 12 précédentes,
dans lequel si un fil connectant ledit réseau de résistances étalons externes (5) audit circuit intégré (1) est coupé, le courant de référence (I_{ref}) produit par ledit circuit intégré de production de courant de référence (2) est maintenu et ne diminue pas d'un pourcentage prédéterminé.

14. Circuit intégré selon l'une des revendications 1 à 13 précédentes,
dans lequel ledit circuit intégré de commande (3) produit un signal indicateur d'erreur indiquant qu'une défaillance est survenue dans ledit réseau de résistances étalons externes (5) si une telle défaillance est détectée par ledit circuit intégré de commande (3).

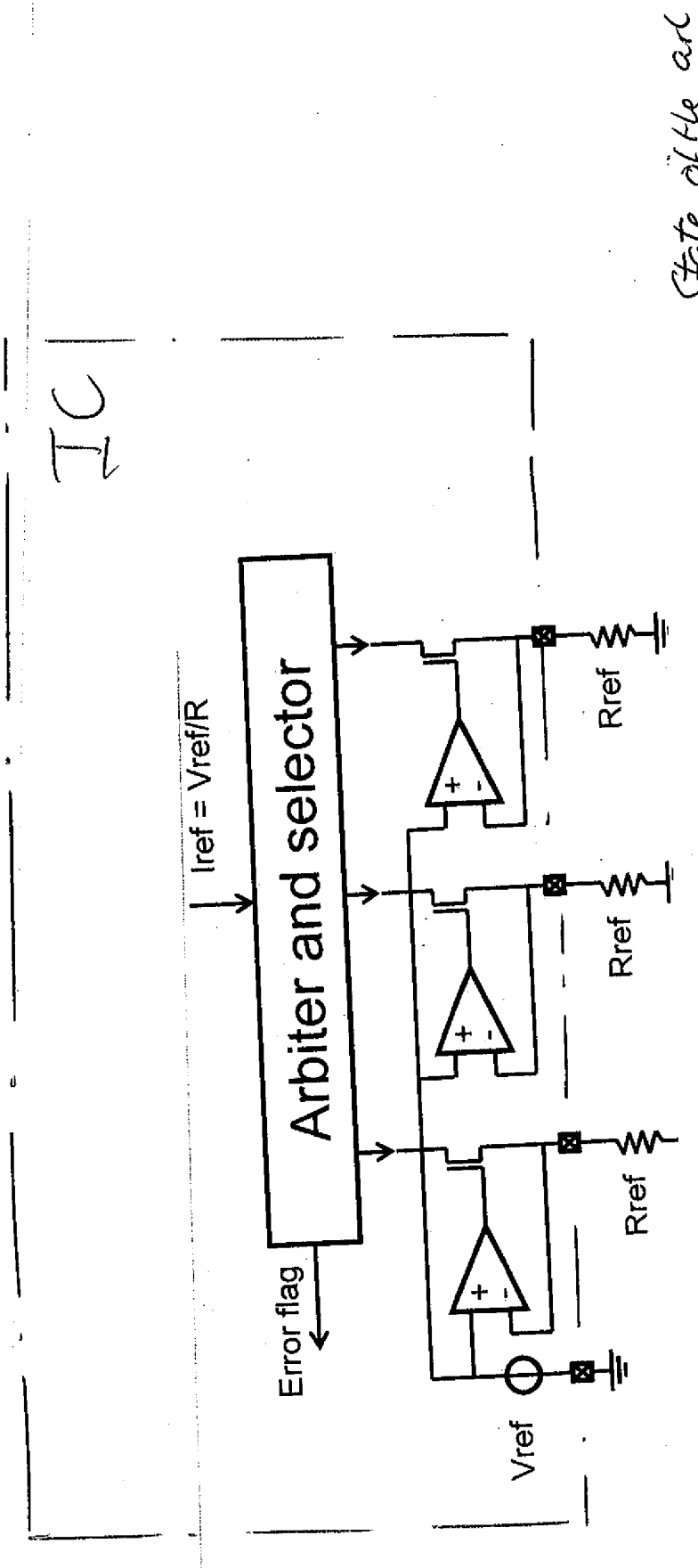

IC
State of the art
Arbiter and selector
Iref = Vref/R
Error flag
Rref
Rref
Rref
Vref

Fig 1

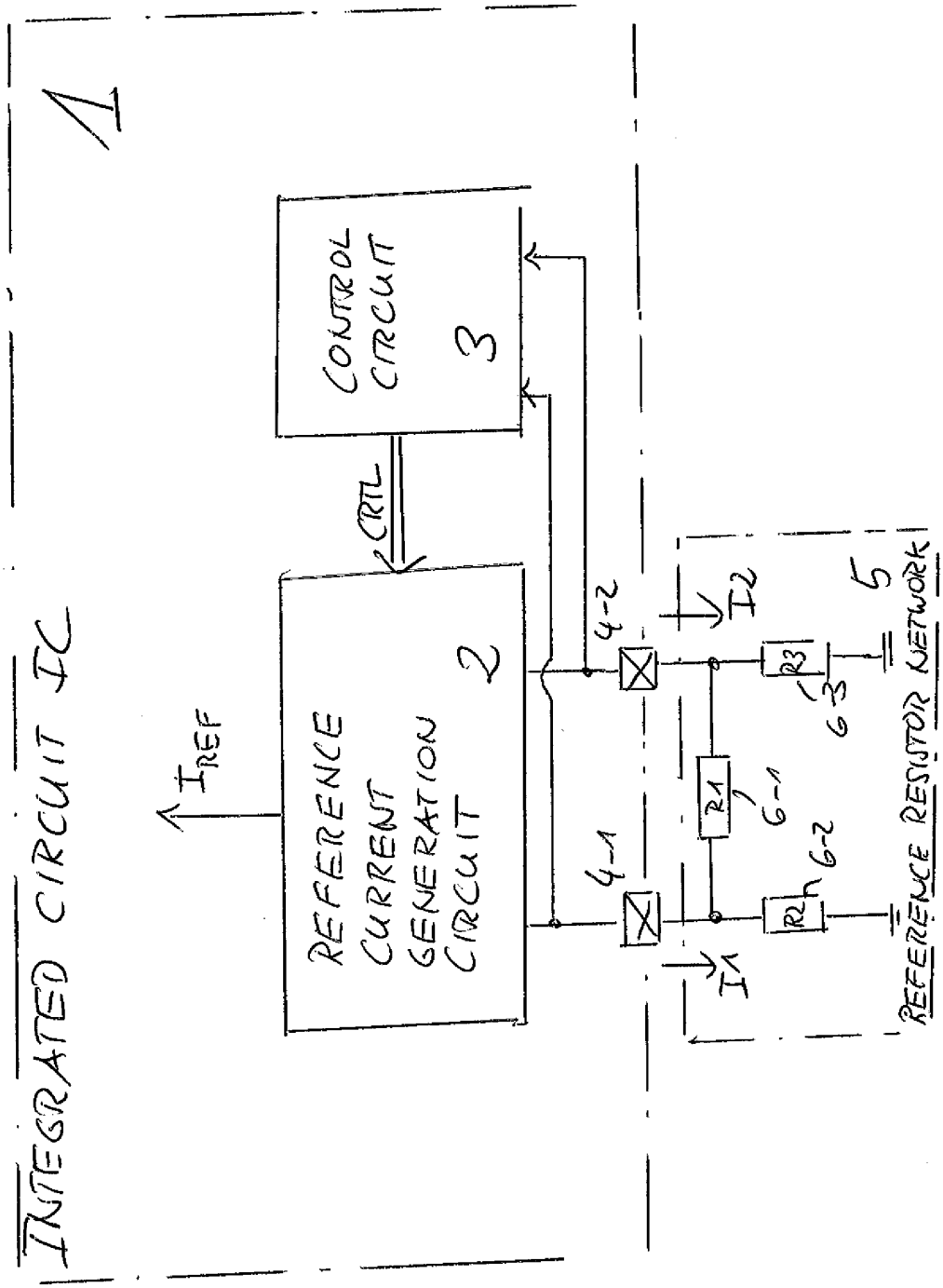

1
INTEGRATED CIRCUIT IC
CONTROL CIRCUIT
3
CRTL
REFERENCE CURRENT GENERATION CIRCUIT
2
I_{REF}
4-1
4-2
I_1
I_2
R1
R2
R3
6-1
6-2
6-3
5
REFERENCE RESISTOR NETWORK

Fig 2

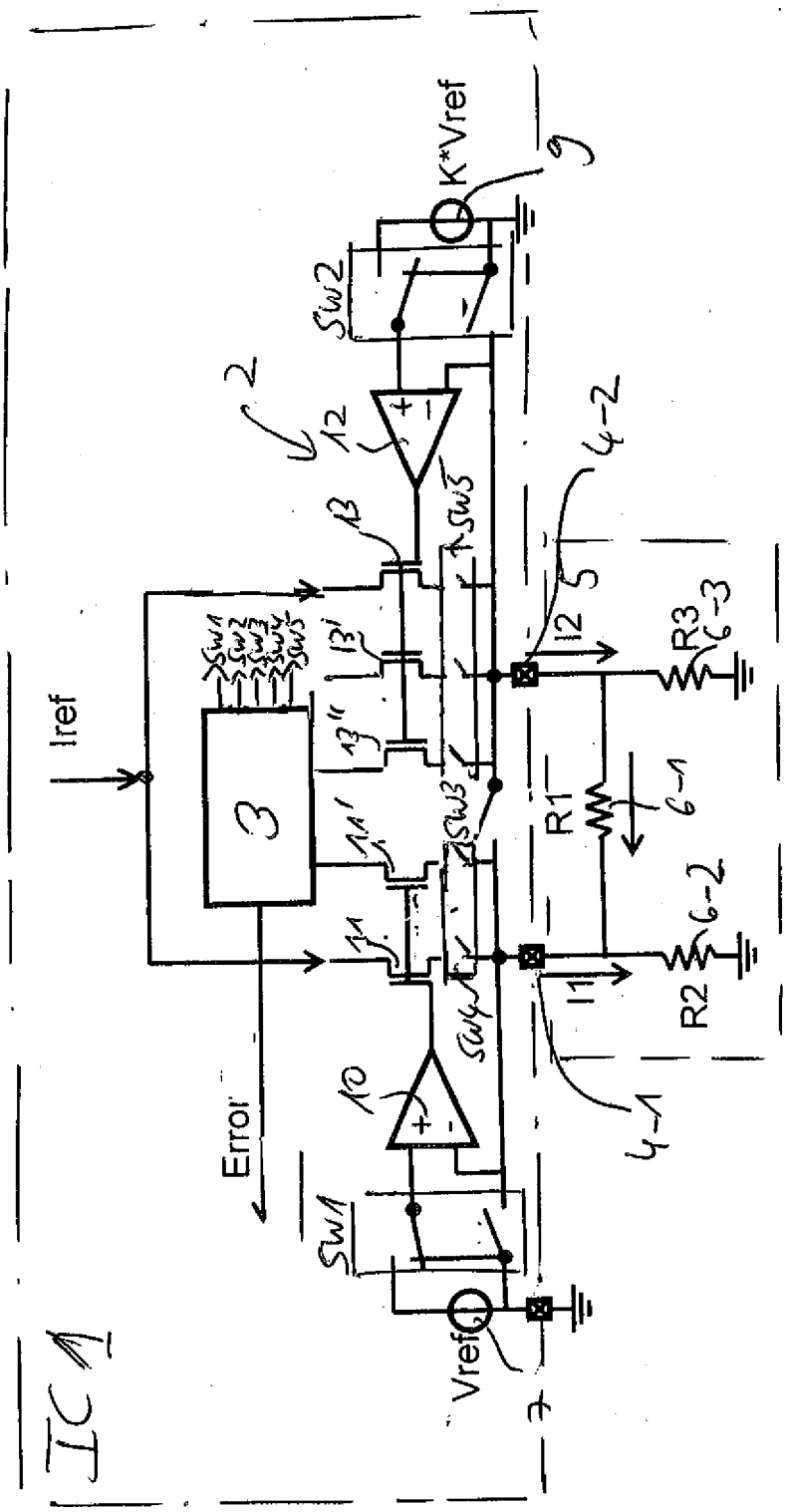

IC1
Iref
3
Error
Vref
K*Vref
SW1
SW2
SW3
SW4
SW5
10
11
11'
12
13
13'
R1
R2
R3
6-1
6-2
6-3
4-1
4-2
5
7
9

Fig 3

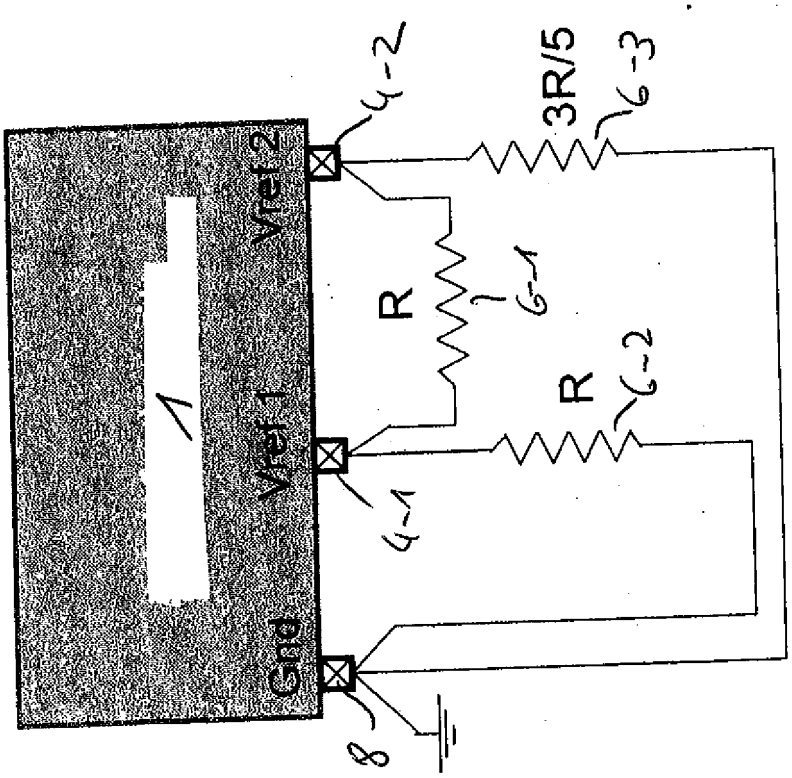


Fig 4

REFERENCES CITED IN THE DESCRIPTION

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