(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 725 446 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
30.04.2014 Bulletin 2014/18

(51) Int Cl.:
G05F 1/56 *(2006.01)* ***H03K 3/00*** *(2006.01)*

(21) Application number: **13275211.4**

(22) Date of filing: **12.09.2013**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **23.10.2012 KR 20120118083**

(71) Applicant: **Samsung Electro-Mechanics Co., Ltd**
Suwon, Gyunggi-Do (KR)

(72) Inventors:
- **Kim,, Myeung Su**
  Gyunggi-do (KR)
- **CHO,, Koon Shik**
  Gyunggi-do (KR)
- **Lim,, Joon Hyung**
  Gyunggi-do (KR)

(74) Representative: **Powell, Timothy John**
Potter Clarkson LLP
The Belgrave Centre
Talbot Street
Nottingham NG1 5GG (GB)

(54) Electronic circuit arrangement with ground and reference electric potential

(57) There is provided an electronic circuit arrangement with ground and reference electric potentials, the arrangement including: a first circuit part disposed between a supply voltage node and a ground node and using the supply voltage as an operating voltage thereof so as to provide a predetermined reference voltage; and a second circuit part disposed between the supply voltage node and the reference voltage node and using a difference voltage between the supply voltage and the reference voltage as an operating voltage thereof.

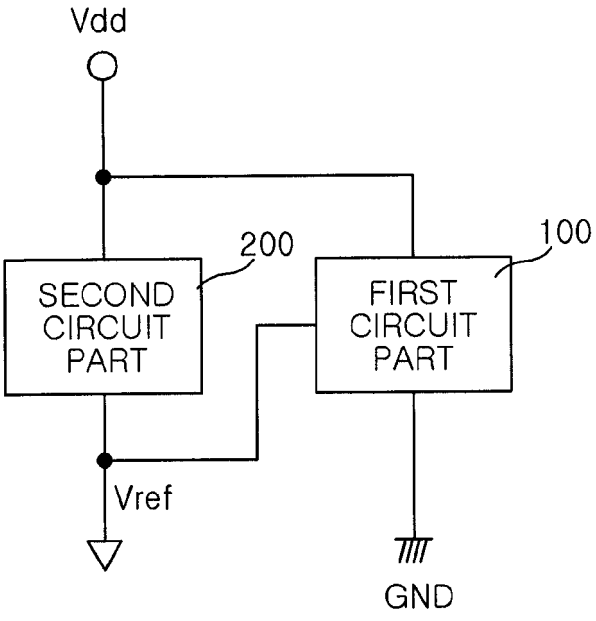

FIG. 1

EP 2 725 446 A1

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Patent Application No. 10-2012-0118083 filed on October 23, 2012, with the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an electronic circuit arrangement which is applicable to an electronic shelf label (ESL) system and the like and having an isolated reference electric potential from the ground for ground isolation.

Description of the Related Art

[0003] In general, an electronic shelf label (ESL) system is a system for automatically providing merchandise information and may include a plurality of tag devices (terminals indicating prices), a relay (e.g., a gateway) and a server.

[0004] The tags may establish a wireless network to perform wireless communication with the relay (GW, gateway), and the relay may perform wired or wireless communication with the server.

[0005] The tag devices of such an electronic shelf label system may include a plurality of circuit chips and communication chips.

[0006] As the technology of semiconductor processing evolves, line widths are getting smaller and most communication chips are fabricated as system on chips (SOCs). In addition, analog and digital circuits are integrated into a single chip. The biggest problem arising in the case of analog and digital circuits being integrated into a single chip is power noise.

[0007] In particular, in a voltage-controlled oscillator generating frequencies, noise generated in a power source directly causes phase noise to be lowered. For this reason, the power source of a voltage controlled oscillator is physically separated from the power sources of other circuits.

[0008] Often, in order to reduce clock noise in a digital circuit, a guard ring or a deep N well is used for reducing power noise coming through a substrate.

[0009] In order to reduce noise between circuits, it is common to use separate independent power sources.

[0010] However, the increased number of independent power sources results in an increased chip size, and isolation between blocks may not be obtained unless the ground is isolated.

[0011] Further, although a method of using a guard ring to reduce noise between blocks is effective, provided that the guard ring is thick and a spacing distance is sufficient, providing a guard ring for each block increases the number of the guard rings used and thus a chip area may be increased.

[0012] Patent Document 1 relates to a mike circuit and discloses separated ground, but does not disclose a circuit having a separated reference electric potential for ground isolation.

[Related Art Document]

[0013]

(Patent Document 1) Korean Patent Laid-Open Publication No. 10-2005-0028587

SUMMARY OF THE INVENTION

[0014] An aspect of the present invention provides an electronic circuit arrangement having a reference electric potential isolated from a ground for ground isolation.

[0015] According to an aspect of the present invention, there is provided an electronic circuit arrangement including: a first circuit part disposed between a supply voltage node and a ground node and using the supply voltage as an operating voltage thereof so as to provide a predetermined reference voltage; and a second circuit part disposed between the supply voltage node and the reference voltage node and using a difference voltage between the supply voltage and the reference voltage as an operating voltage thereof.

[0016] The first circuit part may generate the reference voltage to be lower than the supply voltage and higher than the ground potential.

[0017] The first circuit part may include a regulator generating the predetermined reference voltage so that the difference voltage corresponds to the rated voltage of the second circuit part.

[0018] The second circuit part may use the reference voltage as a reference electric potential.

[0019] The second circuit part may include a voltage-controlled oscillator generating a predetermined oscillation signal by using the difference voltage as an operating voltage thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The above and other aspects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of an electronic circuit arrangement according to an embodiment of the present invention;

FIG. 2 is a block diagram in which an electronic circuit arrangement according to an embodiment of the

present invention is implemented; and
FIGS. 3 and 4 are graphs showing phase noise characteristics.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. The invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Throughout the drawings, the same or like reference numerals will be used to designate the same or like elements.

[0022] FIG. 1 is a block diagram of an electronic circuit arrangement according to an embodiment of the present invention.

[0023] Referring to FIG. 1, the electronic circuit arrangement according to the embodiment of the present invention may include a first circuit part 100 and a second circuit part 200.

[0024] The first circuit part 100 has the ground as its reference electric potential, while the second circuit part 200 does not have the ground but has the reference voltage Vref provided from the first circuit part 100 as its reference electric potential.

[0025] The first circuit part 100 is disposed between the supply voltage Vdd node and the ground node so that it may provide a predetermined reference voltage Vref to the reference electric potential node of the second circuit part 200 using the supply voltage Vdd as the operating voltage.

[0026] The second circuit part 200 is disposed between the supply voltage Vdd node and the reference voltage Vref node so that it may use the difference voltage Vdif between the supply voltage Vdd and the reference voltage Vref as the operating voltage.

[0027] If the reference electric potential node of the second circuit part 200 is connected to the ground as in the related art, the first and second circuit parts 100 and 200 share the ground so that they are influenced by phase noise through the ground.

[0028] In contrast, according to the embodiment of the present invention, the reference electric potential node of the second circuit part 200 is connected not to the ground but to the reference voltage Vref node in order to receive the reference voltage Vref provided from the first circuit part 100.

[0029] FIG. 2 is a block diagram in which an electronic circuit arrangement according to an embodiment of the present invention is implemented.

[0030] Referring to FIG. 2, the first circuit part 100 may generate the reference voltage Vref lower than the supply voltage Vdd and higher than the ground potential.

[0031] The first circuit part 100 may include a regulator that generates the predetermined reference voltage Vref such that the difference voltage Vdif corresponds to the rated voltage of the second circuit part 200.

[0032] For example, assuming that the supply voltage Vdd is 3.0 V and the rated voltage of the second circuit part 200 is 1.8 V, in case that the first circuit part 100 is a regulator, the regulator is operated by the supply voltage Vdd of 3.0 V, generates the reference voltage Vref of 1.2 V, and provides it to the reference electric potential node of the second circuit part 200.

[0033] The second circuit part 200 may be configured to use the reference voltage Vref as the reference electric potential.

[0034] The second circuit part 200 may include a voltage-controlled oscillator VCO that uses the difference voltage Vdif as the operating voltage to generate a predetermined oscillation signal.

[0035] For example, assuming that the supply voltage Vdd is 3.0 V and the rated voltage of the second circuit part 200 is 1.8 V, in case that the second circuit part 200 is a voltage-controlled oscillator VCO, the voltage-controlled oscillator VCO uses 1.8 V as the operating voltage which is the difference voltage Vdif between the supply voltage Vdd of 3.0 V and the reference voltage Vref of 1.2 V from the first circuit part 100.

[0036] The voltage-controlled oscillator VCO may use the difference voltage Vdif of 1.8 V as the operating voltage so as to generate a predetermined oscillation signal.

[0037] As described above, the embodiment of the present invention is designed to use a certain voltage as the reference electric potential instead of the lowest voltage GND which is vulnerable to noise. This design enables a power source to be connected to the main power of a chip so that a power noise source can be prevented. In addition, since there is a difference between the ground GND and the ground GND of other circuit blocks, it is resistant to noise of other circuit blocks.

[0038] Moreover, since the regulator does not have any load current so that no amplifier for amplitude or gain is necessary, and no large capacitor for stabilizing is required, it is not necessary to lead the output line of the regulator out of a chip so that I/O of the chip may be efficiently utilized. Further, the range of the operating voltage of the voltage-controlled oscillator VCO may be widened by designing the circuit to be varied according to the supply voltage Vdd.

[0039] FIGS. 3 and 4 are graphs showing phase noise characteristics.

[0040] FIG. 3 is a graph showing phase noise in a case that the supply voltage Vdd is 2.0 V and the second circuit part 200 is a voltage-controlled oscillator, and FIG. 4 is a graph showing phase noise in a case that the supply voltage Vdd is 3.0 V and the second circuit part 200 is a voltage-controlled oscillator.

[0041] As can be seen from FIGS. 3 and 4, the voltage-controlled oscillator according to the embodiment of the present invention exhibits an excellent phase noise of 100 dBc/Hz or less even with a higher operating voltage

or a lower supply voltage, regardless of the number of capacitors used.

[0042] As set forth above, according to embodiments of the present invention, power noise source can be blocked by way of using a reference electric potential separated from the ground for ground isolation, and thereby isolation between the ground and the reference electric potential can be obtained.

[0043] While the present invention has been shown and described in connection with the embodiments, it will be apparent to those skilled in the art that modifications and variations can be made without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. An electronic circuit arrangement comprising:

   a first circuit part disposed between a supply voltage node and a ground node and using the supply voltage as an operating voltage thereof so as to provide a predetermined reference voltage; and
   a second circuit part disposed between the supply voltage node and the reference voltage node and using a difference voltage between the supply voltage and the reference voltage as an operating voltage thereof.

2. The arrangement of claim 1, wherein the first circuit part generates the reference voltage to be lower than the supply voltage and higher than the ground potential.

3. The arrangement of claim 1, wherein the first circuit part includes a regulator generating the predetermined reference voltage so that the difference voltage corresponds to the rated voltage of the second circuit part.

4. The arrangement of claim 1, wherein the second circuit part uses the reference voltage as a reference electric potential.

5. The arrangement of claim 1, wherein the second circuit part includes a voltage-controlled oscillator generating a predetermined oscillation signal by using the difference voltage as an operating voltage thereof.

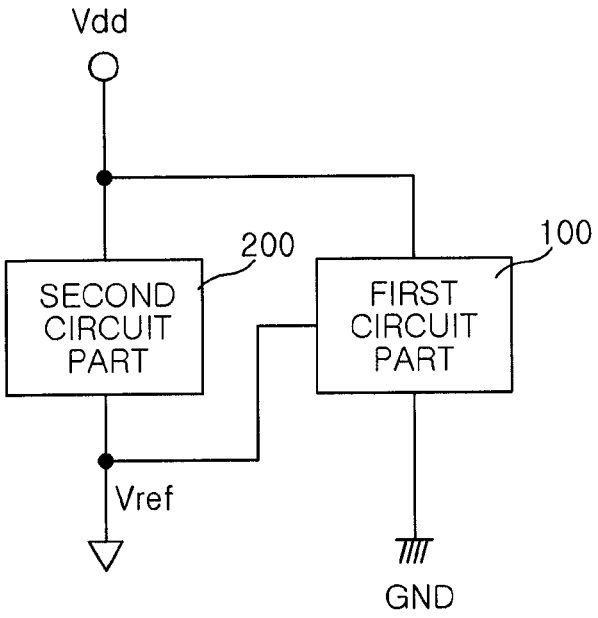
Vdd
200
100
SECOND CIRCUIT PART
FIRST CIRCUIT PART
Vref
GND

FIG. 1

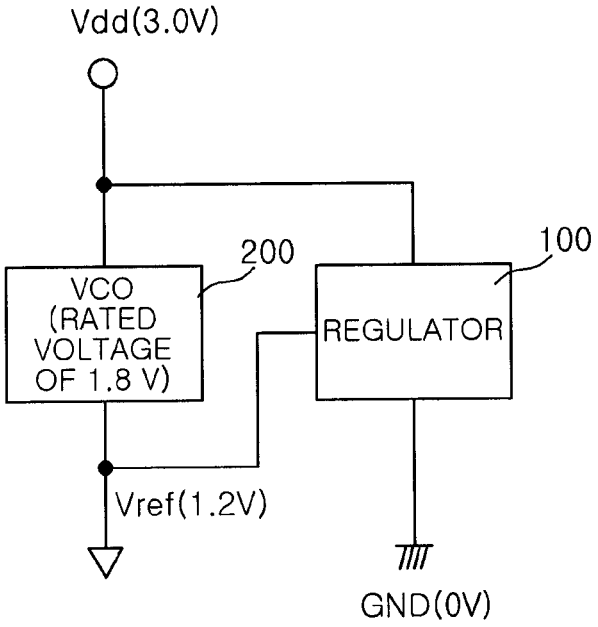
Vdd(3.0V)
200
100
VCO (RATED VOLTAGE OF 1.8 V)
REGULATOR
Vref(1.2V)
GND(0V)

FIG. 2

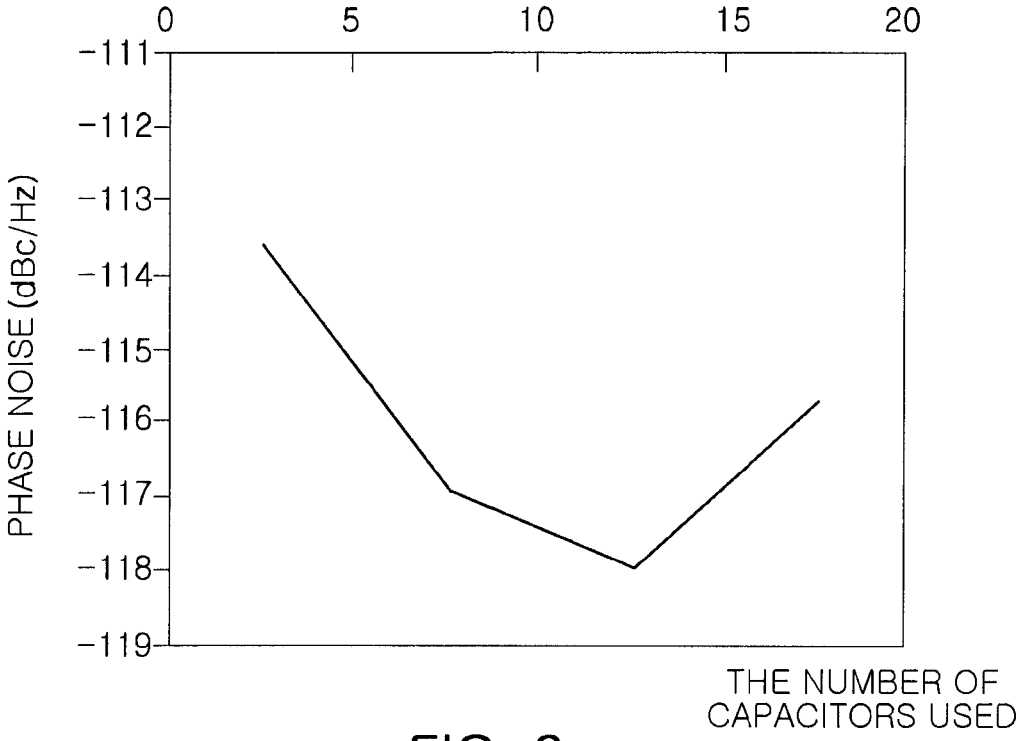
0
5
10
15
20
-111
-112
-113
-114
-115
-116
-117
-118
-119
PHASE NOISE (dBc/Hz)
THE NUMBER OF CAPACITORS USED

FIG. 3

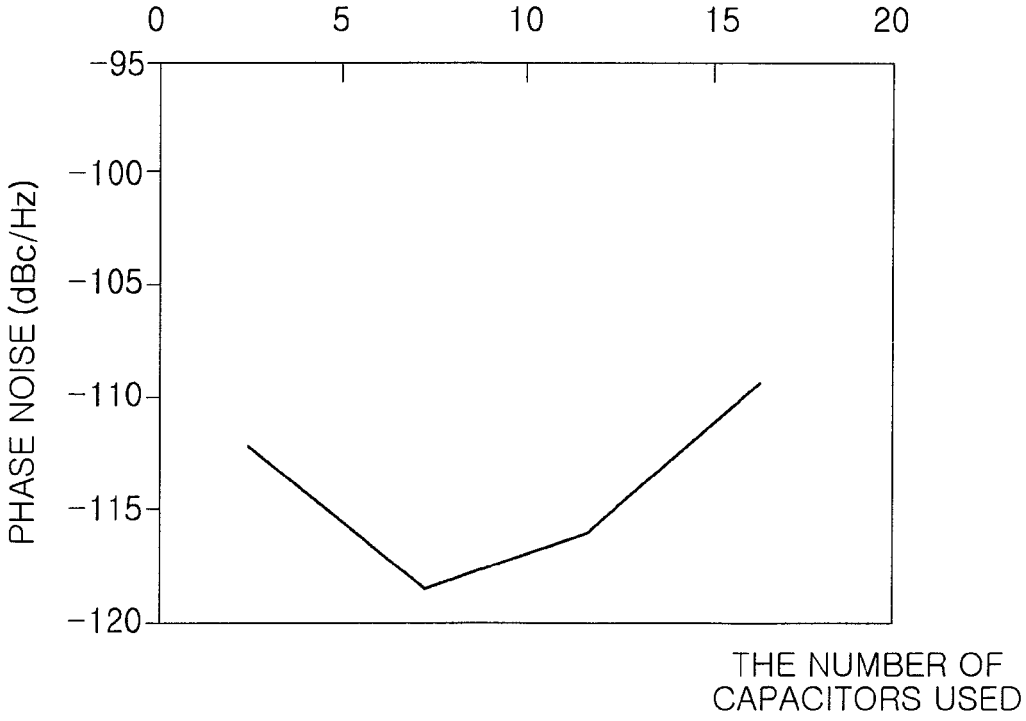
0
5
10
15
20
-95
-100
-105
-110
-115
-120
PHASE NOISE (dBc/Hz)
THE NUMBER OF CAPACITORS USED

FIG. 4

Europäisches Patentamt
European Patent Office
Office européen des brevets

EUROPEAN SEARCH REPORT

Application Number
EP 13 27 5211

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2007/241737 A1 (YEN CHIH-JEN [TW] ET AL) 18 October 2007 (2007-10-18) * abstract; figures 1,2,5 * -----	1-5	INV. G05F1/56 H03K3/00
X	US 3 581 104 A (THEW DONALD G) 25 May 1971 (1971-05-25) * abstract; figure 1 * -----	1-5	
X	JP S59 188715 A (FUJITSU LTD) 26 October 1984 (1984-10-26) * abstract; figure 1 * -----	1-5	
X	US 2011/115554 A1 (PELLEY PERRY H [US]) 19 May 2011 (2011-05-19) * abstract; figure 1 * -----	1-5	
X	WO 2004/102628 A2 (UNIV COLUMBIA [US]; SHEPARD KENNETH [US]; SARAVANAN RAJAPANDIAN [US]) 25 November 2004 (2004-11-25) * abstract; figure 1 * -----	1-5	

TECHNICAL FIELDS SEARCHED (IPC)

G05F
H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	19 February 2014	Arias Pérez, Jagoba

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 13 27 5211

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-02-2014

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007241737 A1	18-10-2007	TW I309758 B US 2007241737 A1	11-05-2009 18-10-2007
US 3581104 A	25-05-1971	NONE	
JP S59188715 A	26-10-1984	NONE	
US 2011115554 A1	19-05-2011	NONE	
WO 2004102628 A2	25-11-2004	US 2005127756 A1 WO 2004102628 A2	16-06-2005 25-11-2004

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020120118083 **[0001]**
- KR 1020050028587 **[0013]**