



(11) **EP 2 739 123 A2**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
04.06.2014 Bulletin 2014/23

(51) Int Cl.:
H05B 37/02 (2006.01)

(21) Application number: **13194825.9**

(22) Date of filing: **28.11.2013**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(72) Inventors:
• **Vanderzon, James**
Rose Park, South Australia 5067 (AU)
• **Quick, Ashleigh Glen**
Rose Park, South Australia 5067 (AU)

(30) Priority: **03.12.2012 AU 2012101745**

(74) Representative: **Vigars, Christopher Ian et al**
Astrum ElementOne Limited
Tower House
Fairfax Street
Bristol BS1 3BN (GB)

(71) Applicant: **Gerard Lighting Pty Ltd**
5067 Rose Park South Australia (AU)

(54) **DALI power supply with reduced dissipation**

(57) A power supply for a DALI system wherein the output current limit is reduced when a DALI low signal is

being transmitted. This allows a significant reduction in the power dissipated in the supply.

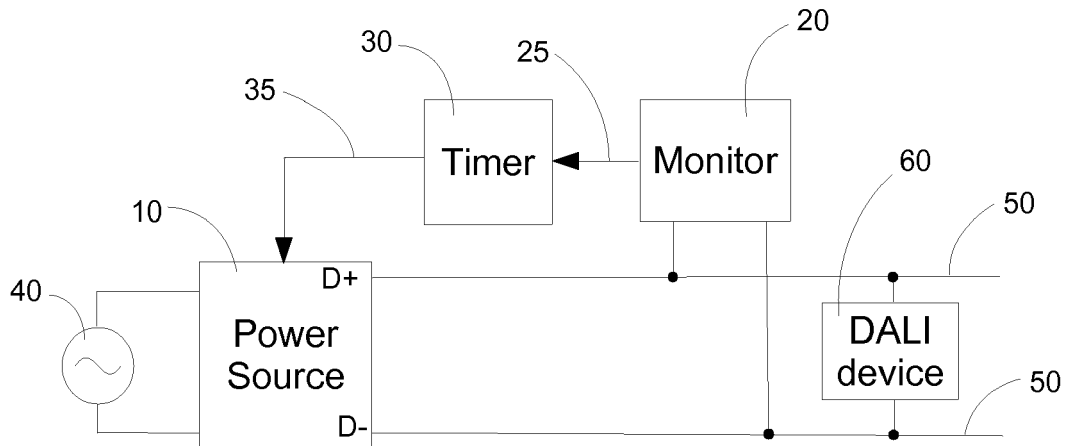


Fig.1

EP 2 739 123 A2

Description

FIELD OF THE INVENTION

[0001] This invention relates to a power supply, in particular a reduced dissipation power supply for use in a DALI (Digital Addressable Lighting Interface) lighting system. The requirements for a DALI system are set out in the IEC 62386 series of technical standards, which are maintained by the International Electrotechnical Commission.

BACKGROUND TO THE INVENTION

[0002] A DALI power supply is required on a DALI line. This supplies a small amount of power, normally used in device transceivers, and supports communication. Some products with low power demand can also be powered completely from the DALI line - for example sensors. The DALI line operating voltage is normally in the range of approximately 15 - 22 V, and the current is limited to a maximum of 250 mA.

[0003] Communication in a DALI system is made by shorting the DALI line, this reduces the voltage seen by a receiver to approximately 0V (in practice, up to about 6V is considered a logical low). During the time period where the line is pulled low, the power supply must be in its current limiting mode, delivering not more than 250 mA. Clearly, the transmitting device must be capable of sinking the 250 mA being supplied by the power supply.

[0004] A power supply can then be considered to have several functional blocks: Mains voltage (240V ac) is converted to a lower voltage; and the lower voltage then has some form of current limiting which will ensure that no more than 250 mA can be supplied. The power supply is designed to tolerate (and withstand continuously) the delivery into a short circuit.

[0005] Because no electronic design is perfect, there will be losses in each of the stages of power conversion: there is a loss in the conversion of AC mains to the lower internal voltage, and a linear output current limiting stage must dissipate power, even if it were ideal.

[0006] These losses are manifest as heat dissipated. (The input power = output power + heat losses.) When delivering full rated power to the DALI line, assuming a line voltage of 18V and 250 mA current, the power delivered is $P = V * I = 18 * 0.25 = 4.5W$. The losses can be assumed as being between about 10% and 5% - i.e. between about 0.45 W and 0.225 W. A reasonable assumption is that the losses are about 0.3 W.

[0007] Clearly, also during the period where the DALI line is short circuited by a transmitting device, the losses are extreme because the power delivered into the load is small. When the load has a high impedance the power capable of being delivered $P = V * I = 18 * 0.25 = 4.5W$ (assuming a nominal delivery voltage of 18V). But when a transmitting device is shorting the line, so the power supply sees a low impedance, the power delivered $P = I$

$* I / R = 0.25 * 0.25 * (\text{low value, perhaps } 0.5 \text{ Ohms}) = 0.03 \text{ W}$. The power is no longer being delivered to the devices in the line, but must be absorbed (and turned into heat) inside the power supply.

[0008] When the DALI data coding, as well as frame timing, is taken into account, the worst case is for the DALI line to be considered in the low state for about 30% of the time. This means that the average amount of power converted into heat due to communication (in addition to the smaller static losses) is about $4.5 \text{ W} * 0.3 = 1.35 \text{ W}$. The losses of approximately 0.3W are then added to this, giving an average dissipation inside the power supply of about 1.6 to 1.7 W.

[0009] Because DALI power supplies are expected to be physically small, and the electronics is mounted in an electrical switchboard with poor ventilation, there can be a significant heat rise to the electronics of the power supply, brought about by the need to dissipate about 1.6 to 1.7W. This temperature rise can be > 30 degrees C. When the ambient temperature is taken into account along with the temperature rise, it is very easy to find that the electronic components are operating outside their rating.

[0010] The object of this invention is to provide a DALI power supply with reduced power dissipation compared with existing designs, or at least provides the public with a useful alternative.

SUMMARY OF THE INVENTION

[0011] In one form of the invention there is a power supply comprising a power source, monitor circuit and timer circuit wherein the power source is selectably operable at a first or a second current limiting level by a control signal, the monitor circuit monitors the output of the power source to determine when the power source enters the first current limiting level and asserts a trigger signal in response, and in response to the trigger signal the timer asserts the control signal for a first predetermined time thereby setting the power source to operate with the second current limiting level.

[0012] Preferably if the trigger signal is asserted for longer than a second predetermined time the control signal is asserted for a third predetermined time thereby setting the power source to operate with the second current limiting level.

[0013] The monitor circuit may monitor the output voltage of the power source by measuring: the output voltage of the power source; the output current of the power source; or the operation of current limiting circuitry in the power source.

[0014] In preference the second current limiting level is between 10 mA and 50 mA.

[0015] It should be noted that any one of the aspects mentioned above may include any of the features of any of the other aspects mentioned above and may include any of the features of any of the embodiments described below as appropriate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate various implementations of the invention and, together with the description, serve to explain the advantages and principles of the invention. In the drawings:

Figure 1 is a block diagram of a preferred embodiment of the invention.

Figure 2 is an example circuit of an implementation of a power supply with variable current limiting.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The following detailed description of the invention refers to the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings and the following description to refer to the same and like parts.

[0018] The invention is in essence a DALI power supply that can detect when communication is happening, and switch off or substantially reduce the delivery of power for a short period of time. When power delivery is turned off, or reduced, the current flowing through a DALI transmitting device is reduced, and the power flowing through the power supply internal current limiting elements is also reduced. This means that during the period of a DALI low state in communication, the power to be dissipated inside the power supply is also commensurately reduced.

[0019] The DALI communication signal uses Manchester coding which codes each data bit (0 or 1) as 2 states in a pair: LOW, HIGH or HIGH, LOW. The period of each high or low state is nominally 416 microseconds (+/- 10%). If when a DALI transmitting device pulls the line into the LOW state, the power delivery is turned off for (say) 300 microseconds, then the dissipation in a LOW state is reduced by a factor of $300 / 416 = 72\%$ - that is, the power being dissipated as heat drops to about about 28% of what it would otherwise be. In practice, tolerances mean that the reduction is more likely to be in the range 80 % (for low state of 416 microseconds - 10%) to 65% (for a low state of 416 microseconds + 10%).

[0020] Nevertheless, the power reduction is significant, and if this simple figure were extrapolated for the general case of communication, the power to be dissipated (due to communication) changes from about 1.35 W to about 0.4 W (after rounding up). When the static losses are included, the total dissipation inside a power supply enclosure is reduced from about 1.7 W; to instead fall to about $0.4 \text{ W} + 0.3 \text{ W} = 0.7 \text{ W}$. This will therefore more than halve the internal temperature rise.

[0021] A complication arises when Manchester coding is used, because this codes a bit as a HIGH, LOW state pair, or a LOW, HIGH state pair. When coded in this manner, alternating bits lead to states that are adjacent - for

example the bits 0, 1 would appear as a state sequence HIGH, LOW, LOW, HIGH on the DALI line. The use of a 300 microsecond power turn-off would be of assistance in reducing the power consumption of the first LOW state, but not the second.

[0022] In practice, the data stream should be assumed to have a random distribution of bits, where the probability of any bit being 0 or 1 is the same: 50%. This means that when considering bit pairs, there are 4 possible cases: 00, 01, 10, 11, and each one of these combinations has a 25% probability of being seen. The only case which is important is where 2 LOW states appear in a row, which is the case of bit pair "10" (and not "01"). Therefore, for 1/4 of bits in the data stream, there will be no benefit from the power reduction.

[0023] This reduces the average efficiency improvement so that the net power reduction factor is only $300 / 416 * 0.75 = 54\%$ (the power to be dissipated, on average will be 46% of what it would otherwise be). This is not so attractive but still represents a power dissipation reduction of > 50%.

[0024] If this reduction were insufficient, there is a solution: once the power is turned back on, a sensing delay of about 200 microseconds can be used. If after this delay the DALI line is still low, the power delivery can be interrupted, again, this time for about another 200 microseconds.

[0025] A block diagram of a preferred embodiment of the invention is shown in Figure 1. The invention comprises a power source 10, monitor 20 and timer 30. The power source 10 is connected to a mains supply 40 and feeds DALI lines 50 which supply power to DALI devices 60.

[0026] The power source 10 is a 240 V ac to 18V dc @ 250 mA power supply which can be implemented by various means as is known in the art. It is characterized in that it can operate at either of two current limiting levels and has a control input to select between the two current limit levels. The first current limit is 250 mA to support normal operation in a DALI system. The second current limit is much lower than the first, the exact level is unimportant. A nominal level of 10-50 mA is chosen as it is desirable to always have some current available in a DALI system. Some DALI devices use an SCR in their transmitting circuit and switch off (stop conducting) when there is no current flowing through them and may not resume correct operation when power is returned. Therefore use of some current, albeit reduced, helps to ensure no disruption to normal operation of the many DALI devices presently available in the market.

[0027] The monitor 20 senses that current limiting has started in a DALI line (due to a transmitting device pulling the line low) and initiates selection of the lower current limit by the power supply by asserting a trigger signal 25 to the timer 30. This can be done in a number of ways, for example:

- a signal derived from current limiting components in

the power source 10;

- a current monitor might be used (e.g. precision low value resistors used to obtain a voltage, which is then compared with a reference);
- monitoring the DALI line voltage, and when this is pulled to a LOW state, then a transmitting device is holding the line low.

[0028] The timer 30 produces a timed control signal 35 for selecting the lower current limit level. The timer can be implemented using a simple mono-stable circuit as is well known in the art. The duration of the control signal is a nominal 300 microseconds as discussed above. In principle any means which delivers timing with a suitable accuracy can be used.

[0029] In an alternative embodiment the timer 30 is implemented using a microprocessor. The cost is expected to be (slightly) greater, but this allows the use of more sophisticated measurement and timing adaption methods. For example, using a microprocessor would allow measurement (over time) of the characteristics of different DALI transmitting devices and adaptive determination of an optimal period after which power delivery should be removed. A microprocessor would also allow more precise timing and measurement of the widths of states to determine how two back-back low states should be handled.

[0030] Use of a microprocessor, or programmable logic device, would also allow for the ready implementation of a retrigger function as discussed above in which case if the DALI line was held low for a successive bit period then the lower current limit would be retriggered. This could come into effect for two consecutive low states (discussed above), a short circuit fault or a framing error (both discussed further below).

[0031] Of consideration is the fault condition when a DALI continuous short circuit is applied. The simple (1-shot) power reduction method will not see a regular tripping and reduction of dissipation. This means that the linear current limiting part of the power source would enter a continuous period of high dissipation. This condition can be mitigated by a temperature sensing mechanism which acts to reduce the output current level, or turn the output off, when some pre-set abnormal high temperature is reached. Such a temperature sensing mechanism is a good, prudent design practice and would be expected to be implemented in any design.

[0032] Sometimes devices use deliberate injection of a long DALI LOW state, for example this is used to inject or signify a framing error in a DALI backward frame; and injection of several LOW states may also be used to signify a collision. These cases are exceptions rather than norms. The power reduction is unlikely to deliver significant benefits (of reduced power) but nor is it expected to disruption normal communication operation.

[0033] Preferably the power source 10 is a linear power

supply. An alternative approach to reducing power dissipation is to use a switched-mode topology power supply. This approach would use hysteretic current regulation, and a switching frequency much greater than the basic DALI data bit transmission rate in order to achieve a rapid response time. A limitation of this approach is that it is very difficult to make such a power source that can also withstand the abnormal condition (as required by the DALI standards) for continuous application of mains voltage across the DALI terminals.

[0034] The present invention is capable of being implemented in various forms by those skilled in the art. Figure 2 shows one example of how this may be done. Figure 2 is a schematic of a power supply with current limiting that is switched between a first and second value for a finite period of time in response to a DALI low condition.

[0035] The ac line voltage is converted to a 20 Vdc extra low voltage via the mains power supply functional block. This could be implemented by any of a number of well-known schemes.

[0036] The primary 250 mA current-limiting function is achieved with an op-amp comparator arrangement (IC1), to compare a current-sense signal (CS1) developed across a current sense resistance (R1 in parallel with R2) with a reference value (Vref 1), then regulating the drive signal to a current-controlling MOSFET (Q1).

[0037] The primary current path comprises MOSFET Q1, resistors R1 in parallel with R2, and MOSFET Q2 - which is normally in the fully conducting state. The value of current-sense resistance is selected to be relatively low in order to minimise associated power dissipation, therefore a suitable value for R1 (for a target current limit of 250mA) is about 1 Ω , whilst a corresponding suitable value for R2 is about 10 Ω . The corresponding reference voltage Vref 1 for above value of current-sense resistance is about 250mV, to achieve the 250mA current-limiting output level. MOSFET Q2 is normally on, hence is selected to have small on-state resistance in comparison to R1, in so far as to not significantly contribute to the magnitude of current sense signal.

[0038] To select the reduced current-limiting mode there is a monostable drive arrangement for MOSFET Q2 comprising capacitor C1, resistor R3 and op-amp comparator IC2.

[0039] Under DALI idle conditions (i.e. DALI line voltage is not pulled low) the voltage across resistor R3 is zero, hence due to positive reference voltage Vref 2 (e.g. 13.5 V), IC2 drives MOSFET Q2 to a fully on state. When a DALI communicating device shorts the DALI line, the corresponding rise in Q1 drain terminal voltage is coupled through C1 to result in immediate switch off of Q2, upon which DALI output current can then only flow through R2. Since value of R2 is approximately 10 times R1, this results in reduction of current limiting to about one-tenth of the original value, hence a reduction in Q1 power dissipation. The value of C1 and R3 are selected such that time-constant, R3 times C1, is about 75% of the DALI-

low bit period associated with DALI communication. The diode D1 serves to reduce the reset time of the monostable function, and to simultaneously limit the negative going voltage amplitude appearing to IC2 inverting input at the return to DALI idle condition. Since MOSFET Q2 does not perform a current limiting function it therefore does not incur high power dissipation.

[0040] The reader will now appreciate the benefits of the present invention in providing a DALI power supply with lower power dissipation and subsequent less heating inside the power supply enclosure. The invention allows a DALI power supply to deliver the full 250 mA current specified by the DALI standard when implemented in a 2-module (sealed) DIN enclosure at a 50 degree C ambient temperature.

[0041] Whilst the above description is addressed at a DALI system, the invention could be readily applied to any similar system in which power is applied to a line which is also used for signaling by pulling the line low.

[0042] Further advantages and improvements may very well be made to the present invention without deviating from its scope. Although the invention has been shown and described in what is conceived to be the most practical and preferred embodiment, it is recognized that departures may be made therefrom within the scope and spirit of the invention, which is not to be limited to the details disclosed herein but is to be accorded the full scope of the claims so as to embrace any and all equivalent devices and apparatus. Any discussion of the prior art throughout the specification should in no way be considered as an admission that such prior art is widely known or forms part of the common general knowledge in this field.

[0043] In the summary of the invention, except where the context requires otherwise due to express language or necessary implication, the word "comprising" is used in the sense of "including", i.e. the features specified may be associated with further features in various embodiments of the invention.

Claims

1. A power supply comprising a power source, monitor circuit and timer circuit wherein:

the power source is selectably operable at a first or a second current limiting level by a control signal;

the monitor circuit monitors the output of the power source to determine when the power source enters the first current limiting level and asserts a trigger signal in response; and in response to the trigger signal the timer asserts the control signal for a first predetermined time thereby setting the power source to operate with the second current limiting level.

2. A power supply as in claim 1, wherein if the trigger signal is asserted for longer than a second predetermined time, the control signal is asserted for a third predetermined time thereby setting the power source to operate with the second current limiting level.
3. A power supply as in claim 1 or claim 2, wherein the monitor circuit monitors the output voltage of the power source by measuring the output voltage of the power source.
4. A power supply as in claim 1 or claim 2, wherein the monitor circuit monitors the output voltage of the power source by measuring the output current of the power source.
5. A power supply as in claim 1 or claim 2, wherein the monitor circuit monitors the output voltage of the power source by monitoring the operation of current limiting circuitry in the power source.
6. A power supply as in any of the preceding claims, wherein the second current limiting level is between 10 mA and 50 mA.

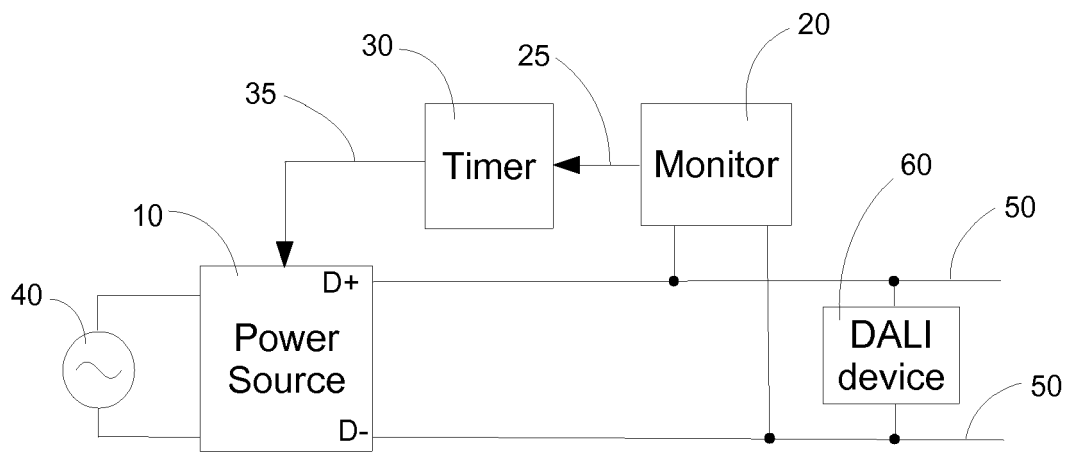


Fig.1

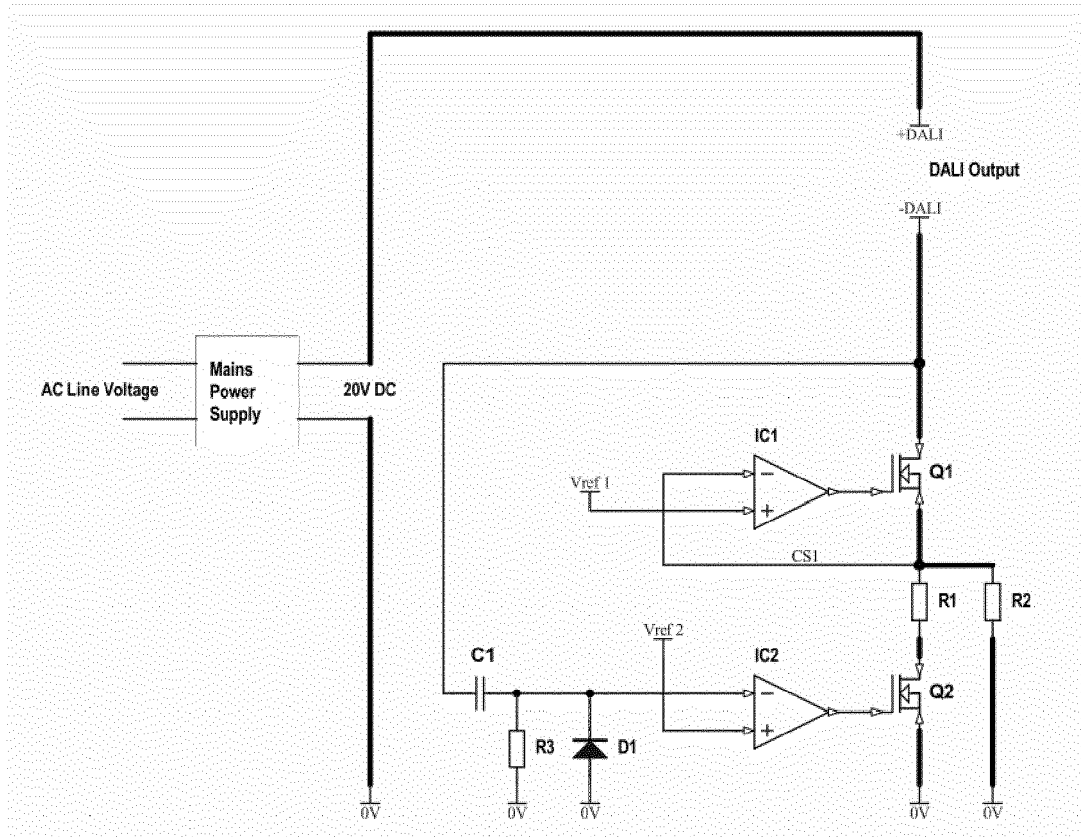


Fig.2