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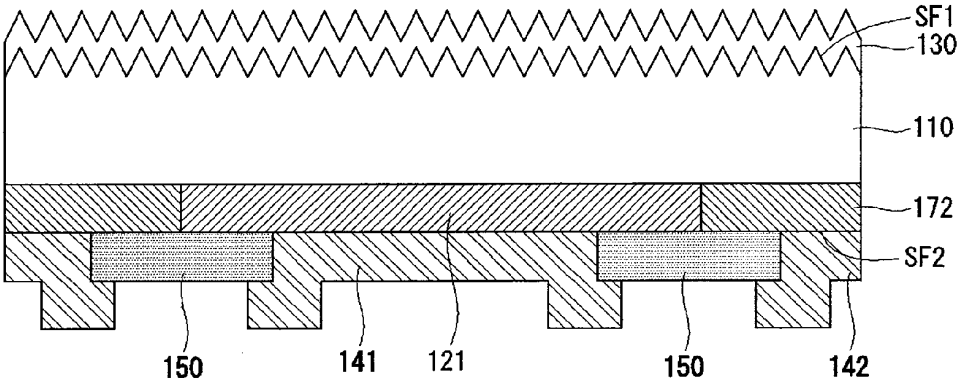
(54) Solar cell and method for manufacturing the same

(57) A solar cell and a method for manufacturing the solar cell are discussed. An embodiment of the method includes forming an emitter region (121) containing impurities of a second conductive type opposite a first conductive type at a back surface of a semiconductor substrate (110) containing impurities of the first conductive type, forming a passivation layer paste (150) containing impurities of the first conductive type on the emitter region, selectively performing a thermal process on a first partial area of the passivation layer paste to form a back surface field region (172) containing impurities of the first conductive type at a partial area of the emitter region, forming a plurality of openings in partial areas of the passivation layer paste to form a passivation layer, forming a first electrode (141) connected to the emitter region (121), and forming a second electrode (142) connected to the back surface field region (172).

FIG. 2



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Description

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2013-0004935 filed in the Korean Intellectual Property Office on January 16, 2013, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] Embodiments of the invention relate to a solar cell and a method for manufacturing the same.

Description of the Related Art

[0003] Recently, as existing energy sources such as petroleum and coal are expected to be depleted, interests in alternative energy sources for replacing the existing energy sources are increasing. Among the alternative energy sources, solar cells for generating electric energy from solar energy have been particularly spotlighted.

[0004] A solar cell generally includes semiconductor parts, which respectively have different conductive types, for example, a p-type and an n-type and thus form a p-n junction, and electrodes respectively connected to the semiconductor parts of the different conductive types.

[0005] When light is incident on the solar cell, a plurality of electron-hole pairs are produced in the semiconductor parts. The electron-hole pairs are separated into electrons and holes. The electrons move to the n-type semiconductor part, and the holes move to the p-type semiconductor part under the influence of the p-n junction of the semiconductor parts. Then, the electrons and the holes are collected by the different electrodes respectively connected to the n-type semiconductor part and the p-type semiconductor part. The electrodes are connected to each other using electric wires to thereby obtain electric power.

SUMMARY OF THE INVENTION

[0006] In one aspect, there is a method for manufacturing a solar cell including forming an emitter region containing impurities of a second conductive type opposite a first conductive type at a back surface of a semiconductor substrate containing impurities of the first conductive type, forming a passivation layer paste containing impurities of the first conductive type on the emitter region, selectively performing a thermal process on a first partial area of the passivation layer paste to form a back surface field region containing impurities of the first conductive type at a partial area of the emitter region, forming a plurality of openings in a second partial area of the passivation layer paste positioned on the emitter region and a third partial area of the passivation layer pasted positioned on the back surface field region to form a passivation layer, forming a first electrode connected to the emitter region, and forming a second electrode connected to the back surface field region.

[0007] In the forming of the passivation layer paste, a concentration of the impurities of the first conductive type contained in the passivation layer paste is higher than a concentration of the impurities of the second conductive type contained in the emitter region.

[0008] The passivation layer paste contains aluminum oxide (AlOx).

[0009] In the forming of the passivation layer paste, a formation thickness of the passivation layer paste is 10 nm to 25 nm.

[0010] The forming of the back surface field region includes diffusing the impurities of the first conductive type contained in the passivation layer paste into the partial area of the emitter region by selectively irradiating a laser beam onto the partial area of the passivation layer paste to form the back surface field region.

[0011] The forming of the emitter region includes diffusing impurities of the second conductive type into the back surface of the semiconductor substrate using a process gas containing impurities of the second conductive type in a diffusion furnace. In this instance, the emitter region is formed at a process temperature of 800 °C to 900 °C, and the process gas includes $POCl_3$ gas.

[0012] The forming of the plurality of openings in the passivation layer paste includes selectively irradiating the laser beam onto the second partial area of the passivation layer paste positioned on the emitter region and the third partial area of the passivation layer paste positioned on the back surface field region to form the plurality of openings.

[0013] A power of the laser beam used to form the plurality of openings in the passivation layer paste is greater than a power of the laser beam used to form the back surface field region.

[0014] The forming of the plurality of openings in the passivation layer paste includes forming a mask having a plurality of openings on the passivation layer paste, and etching the first and second partial areas of the passivation layer paste exposed through the plurality of openings of the mask to form the plurality of openings in the passivation layer paste.

[0015] In another aspect, there is a solar cell including a semiconductor substrate containing impurities of a first conductive type, an emitter region which is positioned at a partial area of a back surface of the semiconductor substrate and contains impurities of a second conductive type opposite the first conductive type, a back surface field region which is positioned at a remaining partial area of the back surface of the semiconductor substrate and contains impurities of the first conductive type at a concentration higher than the semiconductor substrate, a passivation layer which is positioned on the emitter region and the back surface field region, has a plurality of openings exposing the emitter region and the back surface field region, and contains impurities of the first con-

ductive type, a first electrode connected to the emitter region, and a second electrode connected to the back surface field region.

[0016] The passivation layer contains aluminum oxide (AlOx), and a thickness of the passivation layer is 10 nm to 25 nm.

[0017] A concentration of the impurities of the first conductive type contained in the passivation layer is higher than a concentration of the impurities of the second conductive type contained in the emitter region.

[0018] According to the above-described aspects, embodiments of the invention may use the passivation layer paste as a dopant injection source of the back surface field region, and at the same time may use the passivation layer paste as the passivation layer of the solar cell. Hence, the method for manufacturing the solar cell may be further simplified.

[0019] In addition, the embodiments of the invention may use the laser process to form the back surface field region having a p-type semiconductor region, instead of exposing the semiconductor substrate in the diffusion furnace at a relatively high temperature for a long time. As a result, a reduction in characteristics of the semiconductor substrate may be minimized, and the efficiency of the solar cell may be further improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIGS. 1 and 2 illustrate a solar cell according to an example embodiment of the invention; and

FIGS. 3 to 9 illustrate a method for manufacturing a solar cell according to an example embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0021] Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. It will be paid attention that a detailed description of known arts will be omitted if it is determined that the known arts can obscure the embodiments of the invention.

[0022] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Further, it will be understood that when an element such as a layer, film, region, or substrate is referred to as being "entirely" on other element, it may be on the entire surface of the other element and may not be on a portion of an edge of the other element.

[0023] Exemplary embodiments of the invention will be described with reference to FIGS. 1 to 9.

[0024] FIGS. 1 and 2 illustrate a solar cell according to an example embodiment of the invention. More specifically, FIG. 1 is a partial perspective view of a solar cell according to an example embodiment of the invention, and FIG. 2 is a cross-sectional view taken along line II-II of FIG. 1.

[0025] As shown in FIGS. 1 and 2, a solar cell 1 according to an example embodiment of the invention includes a semiconductor substrate 110, an anti-reflection layer 130 positioned on a first surface SF1 (for example, a front surface) of the semiconductor substrate 110, a plurality of emitter regions 121 positioned at a second surface SF2 (for example, a back surface) opposite the first surface SF1 of the semiconductor substrate 110, a plurality of back surface field (BSF) regions 172 which are positioned on the second surface SF2 of the semiconductor substrate 110 and extend in parallel with the plurality of emitter regions 121, a plurality of first electrodes 141 respectively positioned on the plurality of emitter regions 121, a plurality of second electrodes 142 respectively positioned on the plurality of back surface field regions 172, and a plurality of passivation layers 150, each of which is positioned between the first and second electrodes 141 and 142 on the second surface SF2 of the semiconductor substrate 110. The embodiment of the invention describes the solar cell 1 including the anti-reflection layer 130 as an example. However, the anti-reflection layer 130 may be omitted, if necessary or desired.

[0026] As shown in FIGS. 1 and 2, when the anti-reflection layer 130 is formed, a photoelectric efficiency of the solar cell 1 may be further improved. Therefore, in the following description, the solar cell 1 including the anti-reflection layer 130 is described as an example.

[0027] The semiconductor substrate 110 may be a crystalline semiconductor substrate formed of first conductive type silicon, for example, n-type silicon, though not required. Silicon used in the semiconductor substrate 110 may be crystalline silicon such as single crystal silicon and polycrystalline silicon. When the semiconductor substrate 110 is of an n-type, the semiconductor substrate 110 may be doped with impurities of a group V element such as phosphorus (P), arsenic (As), and antimony (Sb). Alternatively, the semiconductor substrate 110 may be of a p-type and/or may be formed of a semiconductor material other than silicon. If the semiconductor substrate 110 is of the p-type, the semiconductor sub-

strate 110 may be doped with impurities of a group III element such as boron (B), gallium (Ga), and indium (In).

[0028] An incident surface (for example, the front surface SF1) of the semiconductor substrate 110 is textured to form a textured surface corresponding to an uneven surface or having uneven characteristics. FIG. 1 shows that only an edge of the semiconductor substrate 110 has the textured surface for the sake of brevity and ease of description. However, the entire front surface SF1 of the semiconductor substrate 110 substantially has the textured surface, and thus the anti-reflection layer 130 positioned on the front surface SF1 of the semiconductor substrate 110 has the textured surface.

[0029] Alternatively, unlike the structure shown in FIGS. 1 and 2, the back surface SF2 as well as the front surface SF1 of the semiconductor substrate 110 may have the textured surface. In the following description, the solar cell 1, in which only the front surface SF1 of the semiconductor substrate 110 has the textured surface, is described as an example.

[0030] The anti-reflection layer 130 positioned on the front surface SF1 of the semiconductor substrate 110 increases selectivity of a predetermined wavelength band of light incident on the solar cell 1 and reduces a reflectance of the incident light. Further, the anti-reflection layer 130 performs a passivation function, which reduces a defect, for example, dangling bonds existing at and around the front surface SF1 of the semiconductor substrate 110 to thereby prevent or reduce a recombination and/or a disappearance of carriers (i.e., electrons or holes) moving to the front surface SF1 of the semiconductor substrate 110.

[0031] As a result, the anti-reflection layer 130 may increase the efficiency of the solar cell 1. The anti-reflection layer 130 may be formed using at least one of silicon oxide (SiOx), silicon oxynitride (SiOxNy), silicon nitride (SiNx), zinc oxide (ZnO), and aluminum zinc oxide (AZOx). Other materials may be used for the anti-reflection layer 130.

[0032] In the embodiment of the invention, FIGS. 1 and 2 show the anti-reflection layer 130 having a single-layered structure. However, the anti-reflection layer 130 may have a multi-layered structure, for example, a double-layered structure.

[0033] The plurality of emitter regions 121 and the plurality of back surface field regions 172 are alternately positioned on the back surface SF2 of the semiconductor substrate 110 and extend in parallel with each other in a fixed direction.

[0034] Each emitter region 121 is formed on the back surface SF2 of the semiconductor substrate 110 and has a second conductive type (for example, p-type) opposite the first conductive type (for example, n-type) of the semiconductor substrate 110. Hence, the emitter regions 121 of the second conductive type form a p-n junction along with the semiconductor substrate 110 of the first conductive type.

[0035] Carriers, i.e., a plurality of electron-hole pairs produced by light incident on the semiconductor substrate 110 are separated into electrons and holes due to the p-n junction between the semiconductor substrate 110 and the emitter regions 121. The electrons move to the n-type semiconductor, and the holes move to the p-type semiconductor. Thus, when the semiconductor substrate 110 is of the n-type and the emitter regions 121 are of the p-type, the separated holes move to the emitter regions 121, and the separated electrons move to the back surface field regions 172 having an impurity concentration higher than the semiconductor substrate 110. Because the emitter regions 121 form the p-n junction along with the semiconductor substrate 110, the emitter regions 121 may be of the n-type when the semiconductor substrate 110 is of the p-type unlike the embodiment described above. In this instance, the separated electrons move to the emitter regions 121, and the separated holes move to the back surface field regions 172.

[0036] Returning to the embodiment of the invention, when the emitter regions 121 are of the p-type, the emitter regions 121 may be doped with impurities of a group III element such as B, Ga, and In. On the contrary, when the emitter regions 121 are of the n-type, the emitter regions 121 may be doped with impurities of a group V element such as P, As, and Sb.

[0037] The emitter regions 121 are formed by diffusing impurities of the second conductive type into the back surface SF2 of the semiconductor substrate 110.

[0038] Each of the back surface field regions 172 is a region (for example, an n^+-type region) which is more heavily doped than the semiconductor substrate 110 with impurities of the same conductive type as the semiconductor substrate 110. For example, when the semiconductor substrate 110 contains n-type impurities, each back surface field region 172 is an n^+-type region.

[0039] The back surface field regions 172 are disposed at the back surface SF2 of the semiconductor substrate 110 and extend in a fixed direction in parallel with the emitter regions 121. As shown in FIGS. 1 and 2, the back surface field regions 172 and the emitter regions 121 may be formed to contact each other.

[0040] A potential barrier is formed by a difference between impurity concentrations of the semiconductor substrate 110 and the back surface field regions 172. The potential barrier prevents or reduces holes from moving to the back surface field regions 172 used as a moving path of electrons and makes it easier for electrons to move to the back surface field regions 172. Thus, the back surface field regions 172 reduce an amount of carriers lost by a recombination and/or a disappearance of the electrons and the holes at and around the back surface field regions 172 or at and around the first and second electrodes 141 and 142, and accelerate a movement of desired carriers (for example, electrons), thereby increasing the movement of carriers to the back surface field regions 172.

[0041] The plurality of first electrodes 141 are respectively positioned on the plurality of emitter regions 121,

extend along the emitter regions 121, and are electrically and physically connected to the emitter regions 121. Each first electrode 141 collects carriers (for example, holes) moving to the corresponding emitter region 121.

[0042] The plurality of second electrodes 142 are respectively positioned on the plurality of back surface field regions 172, extend along the back surface field regions 172, and are electrically and physically connected to the back surface field regions 172. Each second electrode 142 collects carriers (for example, electrons) moving to the corresponding back surface field region 172.

[0043] The first and second electrodes 141 and 142 may be formed of a conductive metal material, for example, at least one conductive metal material selected from the group consisting of nickel (Ni), copper (Cu), silver (Ag), aluminum (Al), tin (Sn), zinc (Zn), indium (In), titanium (Ti), gold (Au), and a combination thereof. Other materials may be used. For example, the first and second electrodes 141 and 142 may be formed of a transparent conductive metal containing transparent conductive oxide (TCO).

[0044] Each of the plurality of passivation layers 150 is positioned between the first and second electrodes 141 and 142 on the second surface SF2 of the semiconductor substrate 110. Namely, each passivation layer 150 is formed to contact both the emitter region 121 and the back surface field region 172.

[0045] Each passivation layer 150 insulates the first electrode 141 from the second electrode 142 and also performs a passivation function, which reduces a defect, for example, dangling bonds existing at and around the front surface SF1 of the semiconductor substrate 110 to thereby prevent or reduce a recombination and/or a disappearance of carriers (i.e., electrons or holes) moving to the front surface SF1 of the semiconductor substrate 110.

[0046] An operation of the solar cell 1 having the above-described structure according to the embodiment of the invention is described below.

[0047] When light irradiated onto the solar cell 1 is incident on the semiconductor substrate 110, a plurality of electron-hole pairs are generated in the semiconductor substrate 110 by light energy produced by the light incident on the semiconductor substrate 110. The electron-hole pairs are separated into electrons and holes by the p-n junction between the semiconductor substrate 110 and the emitter regions 121. The separated electrons move to the n-type semiconductor substrate 110, and the separated holes move to the p-type emitter regions 121. Then, the electrons moving to the semiconductor substrate 110 are transferred to the second electrodes 142 and are collected by the second electrodes 142, and the holes moving to the emitter regions 121 are transferred to the first electrodes 141 and are collected by the first electrodes 141. When the first electrodes 141 are connected to the second electrodes 142 using electric wires, electric current flows therein to thereby enable use of the current for electric power.

[0048] In the embodiment of the invention, the passivation layers 150 may contain a non-conductive insulating material and may contain impurities of the same conductive type as the semiconductor substrate 110, so as to reduce a manufacturing time of the solar cell 1 and prevent a reduction in characteristics of the semiconductor substrate 110.

[0049] For example, if the semiconductor substrate 110 contains p-type impurities, the emitter regions 121 contain n^+-type impurities, and the back surface field regions 172 contain p^+-type impurities, the passivation layers 150 may contain p-type impurities of the same conductive type as the back surface field regions 172. In this instance, it is preferable, but not required, that each passivation layer 150 is formed of aluminum oxide (AlOx) containing aluminum as the p-type impurities and has a thickness of about 10 nm to 25 nm.

[0050] A concentration of the impurities contained in the passivation layer 150 is higher than a concentration of the impurities contained in the emitter region 121.

[0051] For example, when the semiconductor substrate 110 contains p-type impurities, the emitter regions 121 contain n^+-type impurities, the back surface field regions 172 contain p^+-type impurities, and the passivation layers 150 contain p-type impurities, a concentration of the p-type impurities contained in the passivation layer 150 is higher than a concentration of the n^+-type impurities contained in the emitter region 121.

[0052] An effect of the passivation layer 150 is described in detail through a method for manufacturing the solar cell 1 according the embodiment of the invention.

[0053] FIGS. 3 to 9 illustrate a method for manufacturing a solar cell according the embodiment of the invention.

[0054] As shown in FIG. 3, a semiconductor substrate 110 containing impurities of a first conductive type or impurities of a second conductive type opposite the first conductive type is provided. For example, the semiconductor substrate 110 may be a semiconductor substrate containing p-type impurities or n-type impurities.

[0055] It is preferable, but not required, that a front surface SF1 of the semiconductor substrate 110 is textured.

[0056] Next, as shown in FIG. 4, an emitter region 121 containing impurities of the second conductive type is formed at an entire back surface SF2 of the semiconductor substrate 110. For example, the emitter region 121 is formed as an n^+-type region which highly contains n-type impurities as the impurities of the second conductive type.

[0057] The emitter region 121 is formed by diffusing the impurities of the second conductive type into the entire back surface SF2 of the semiconductor substrate 110 at a process temperature of about 800 °C to 900 °C using a process gas (for example, $POCl_3$ gas) containing the impurities of the second conductive type in a diffusion furnace.

[0058] As described above, because the process for forming the emitter region 121 containing the n-type im-

purities is performed at the relatively low temperature, carrier lifetime, which is one of characteristics of the semiconductor substrate 110, is scarcely reduced.

[0059] When the semiconductor substrate 110 in the diffusion furnace is exposed at a temperature equal to or higher than about 1,000 °C for a long time (for example, about 1 hour) so as to inject impurities into the semiconductor substrate 110, the carrier lifetime of the semiconductor substrate 110 may be affected. However, when the emitter region 121 containing the impurities of the second conductive type is formed at the entire back surface SF2 of the semiconductor substrate 110 using $POCl_3$ gas, the carrier lifetime of the semiconductor substrate 110 is scarcely reduced as described above because the process temperature is relatively low.

[0060] Next, as shown in FIG. 5, a passivation layer paste P150 containing impurities of the same conductive type (i.e., the first conductive type) as the semiconductor substrate 110 is formed on the emitter region 121 containing the impurities of the second conductive type.

[0061] More specifically, the passivation layer paste P150 containing the impurities of the first conductive type is applied to the emitter region 121 using an application method or a deposition method and then is dried at a relatively low temperature (for example, a temperature equal to or lower than about 200 °C).

[0062] The passivation layer paste P150 thus formed may serve as a dopant paste, which is an injection source of the impurities of the first conductive type, when a back surface field region 172 containing the impurities of the first conductive type is formed in a subsequent process, and also may passivate the back surface SF2 of the semiconductor substrate 110.

[0063] A concentration of the impurities of the first conductive type contained in the passivation layer paste P150 is higher than a concentration of the impurities of the second conductive type contained in the emitter region 121.

[0064] A reason why the concentration of the impurities of the first conductive type contained in the passivation layer paste P150 is higher than the concentration of the impurities of the second conductive type contained in the emitter region 121 is that when the impurities of the first conductive type contained in the passivation layer paste P150 are injected into the emitter region 121, which has been already formed, in a subsequent process, the impurities of the first conductive type are injected at a concentration higher than the concentration of the impurities of the second conductive type contained in the emitter region 121 to form the back surface field region 172 containing the impurities of the first conductive type through the overcompensation.

[0065] For example, the passivation layer paste P 150 is formed using aluminum oxide (AlOx) containing aluminum as the impurities of the first conductive type. It is preferable, but not required, that the passivation layer paste P150 has a thickness T150 of about 10 nm to 25 nm.

[0066] In the embodiment of the invention, when the thickness T150 of the passivation layer paste P150 is equal to or greater than about 10 nm, a passivation function of the passivation layer paste P 150 may be smoothly performed, and the concentration of the impurities of the first conductive type contained in the passivation layer paste P 150 may be maintained at a sufficient level. Hence, when a portion S 172 of the emitter region 121 is converted into the back surface field region 172 in a subsequent process, the overcompensation of the impurities of the first conductive type may be sufficiently performed.

[0067] Further, when the thickness T150 of the passivation layer paste P150 is equal to or less than about 25 nm, the passivation function and the overcompensation function of the passivation layer paste P150 may be sufficiently performed. Hence, the consumption of an unnecessary material may be minimized.

[0068] Next, as shown in FIG. 6, a thermal process is selectively performed on the portion S172 of the passivation layer paste P150 to form the back surface field region 172 containing the impurities of the first conductive type at the portion S 172 of the emitter region 121.

[0069] More specifically, the embodiment of the invention selectively performs the thermal process on the portion S172 of the passivation layer paste P150 and diffuses the first conductive type impurities of a high concentration contained in the passivation layer paste P150 into the portion S172 of the emitter region 121 containing the second conductive type impurities to perform the overcompensation of the first conductive type impurities of the high concentration on the portion S 172 of the emitter region 121. Hence, the portion S 172 of the emitter region 121 is formed as (or changed into) the back surface field region 172 containing the first conductive type impurities.

[0070] For example, the selective thermal process on the portion S172 of the passivation layer paste P150 may be performed by irradiating a laser beam having a wavelength of about 532 nm using a first laser irradiation device LRA1 or selectively (or partially) irradiating a femtosecond laser beam onto the portion S 172 of the passivation layer paste P 150.

[0071] Hence, the first conductive type impurities of the high concentration contained in the portion S172 of the passivation layer paste P150, onto which the laser beam is irradiated, are diffused and injected into the portion S172 of the emitter region 121. The characteristics of the emitter region 121 obtained by the second conductive type impurities of a low concentration, which has been already contained in the emitter region 121, disappear by the overcompensation of the first conductive type impurities of the high concentration of the passivation layer paste P150. As a result, the portion S172 has characteristics obtained by only the first conductive type impurities to form the back surface field region 172 containing the impurities of the first conductive type.

[0072] As described above, the diffusion process performed at a high temperature and the formation of oxide

used as a barrier in the diffusion process are not required to form the back surface field region 172. Therefore, the carrier lifetime may be prevented from being reduced by the thermal process.

[0073] More specifically, when the p-type impurities as a dopant are diffused into the semiconductor substrate 110 in the diffusion furnace to form the back surface field region 172 in a conventional process, BBr_3 gas is generally used as the process gas. In this instance, a temperature of a process for injecting boron (B) into the semiconductor substrate 110 in the diffusion furnace has to be about 1,050 °C, and an exposure time has to be about 1 hour or longer. Thus, the semiconductor substrate 110 is greatly affected by the thermal process, and the carrier lifetime is greatly reduced. As a result, the efficiency of the solar cell 1 is reduced.

[0074] On the other hand, in the embodiment of the invention, because the thermal process is selectively performed only on a portion of the semiconductor substrate 110 using a laser beam, so that the entire semiconductor substrate 110 is not exposed to an environment of the high temperature, a reduction in the characteristics of the semiconductor substrate 110 may be minimized.

[0075] Referring again to FIG. 6, the back surface field regions 172 containing the impurities of the first conductive type and the emitter regions 121 containing the impurities of the second conductive type are formed at the back surface SF2 of the semiconductor substrate 110. The back surface field region 172 and the emitter region 121 are positioned adjacent to each other. Further, the back surface field region 172 and the emitter region 121 are formed in the same pattern as FIGS. 1 and 2.

[0076] Next, as shown in FIGS. 7A and 7B, partial areas SC of the passivation layer paste P150 positioned on the emitter regions 121 and the back surface field regions 172 are etched. Hence, as shown in FIG. 8, a passivation layer 150 having a plurality of openings OP 150, through which the emitter regions 121 and the back surface field regions 172 are exposed, is formed.

[0077] Various known methods including a method using a laser beam and a wet etching method using a mask may be used to form the plurality of openings OP 150 in the passivation layer paste P150.

[0078] First, as shown in FIG. 7A, the method using the laser beam is to selectively irradiate a laser beam onto the partial area SC of the passivation layer paste P 150 positioned on the emitter region 121 and the partial area SC of the passivation layer paste P150 positioned on the back surface field region 172 using a second laser irradiation device LRA2 to form the plurality of openings OP 150 in the passivation layer paste P150.

[0079] In this instance, as shown in (a) of FIG. 7A, the plurality of openings OP150 may be formed in the partial area SC of the passivation layer paste P150 using only the laser beam. However, as shown in (b) of FIG. 7A, to minimize a reduction in the characteristics of the semiconductor substrate 110 resulting from the laser beam, the laser beam may be selectively irradiated onto the partial area SC of the passivation layer paste P150 to form a plurality of grooves so that a minimum thickness R150 of each groove (i.e., laser irradiation area) is equal to or less than several nanometers to the extent that the openings OP150 are not formed in (or do not punch through) the passivation layer paste P150. Then, the passivation layer paste P150 remaining in the grooves (with a minimum thickness R150) may be wet-etched and removed to form the openings OP150 in the passivation layer paste P150.

[0080] In this instance, it is preferable, but not required, that a width WSC of each of the plurality of openings OP 150 is less than a width W172 of each of the back surface field regions 172. Hence, a position of a boundary surface between the back surface field region 172 and the emitter region 121 may overlap a position of the passivation layer 150.

[0081] The laser beam output from the second laser irradiation device LRA2 used to form the plurality of openings OP150 in the passivation layer paste P150 has to etch the partial area SC of the passivation layer paste P150. Therefore, power of the laser beam output from the second laser irradiation device LRA2 is greater than the power of the laser beam output from the first laser irradiation device LRA1 used to form the back surface field regions 172.

[0082] Further, as shown in FIG. 7B, an etching method using a mask M150 may be used to form the plurality of openings OP150 in the passivation layer paste P150.

[0083] More specifically, as shown in FIG. 7B, the mask M150 having a plurality of openings OM150 is formed on the passivation layer paste P150, and then the partial area SC of the passivation layer paste P150 exposed by the openings OM150 of the mask M150 is etched. Hence, the plurality of openings OP 150 are formed in the passivation layer paste P 150.

[0084] As shown in FIG. 8, a pattern of the passivation layer 150 may be positioned on the boundary surface between the back surface field region 172 and the emitter region 121. Namely, the passivation layer 150 may have the pattern, in which partial areas of the back surface field regions 172 and partial areas of the emitter regions 121 are alternately exposed through the plurality of openings OP 150 formed in the passivation layer 150.

[0085] Next, as shown in FIG. 9, a plurality of first electrodes 141 connected to the emitter regions 121 through the openings OP150 of the passivation layer 150 are formed, and a plurality of second electrodes 142 connected to the back surface field regions 172 through the openings OP150 of the passivation layer 150 are formed.

[0086] The first electrodes 141 and the second electrodes 142 may be formed using a screen printing method or a plating method. However, it is preferable, but not required, that the plating method is used to form the first electrodes 141 and the second electrodes 142 in consideration of an influence on the characteristics (for example, the carrier lifetime) of the semiconductor substrate 110 in an alignment process.

[0087] Further, an anti-reflection layer 130 is formed on the front surface SF1 of the semiconductor substrate 110. Hence, the solar cell 1 shown in FIGS. 1 and 2 is formed.

[0088] The method for manufacturing the solar cell 1 according the embodiment of the invention may use the passivation layer paste P150 as the dopant injection source of the back surface field region 172, and at the same time may use the passivation layer paste P150 as the passivation layer 150 of the solar cell 1. Hence, the method for manufacturing the solar cell 1 according the embodiment of the invention may be further simplified.

[0089] In addition, the method for manufacturing the solar cell 1 according the embodiment of the invention uses the laser process to form the back surface field region or the emitter region having a p-type semiconductor region, instead of exposing the semiconductor substrate in the diffusion furnace at the relatively high temperature for a long time. As a result, a reduction in the characteristics of the semiconductor substrate may be minimized, and the efficiency of the solar cell may be further improved.

[0090] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A method for manufacturing a solar cell comprising:

forming an emitter region containing impurities of a second conductive type opposite a first conductive type at a back surface of a semiconductor substrate containing impurities of the first conductive type;

forming a passivation layer paste containing impurities of the first conductive type on the emitter region;

selectively performing a thermal process on a first partial area of the passivation layer paste to form a back surface field region containing impurities of the first conductive type at a partial area of the emitter region;

forming a plurality of openings in a second partial area of the passivation layer paste positioned on the emitter region and a third partial area of the passivation layer pasted positioned on the back surface field region to form a passivation layer;

forming a first electrode connected to the emitter region; and

forming a second electrode connected to the back surface field region.

2. The method of claim 1, wherein in the forming of the passivation layer paste, a concentration of the impurities of the first conductive type contained in the passivation layer paste is higher than a concentration of the impurities of the second conductive type contained in the emitter region.

3. The method of claim 1, wherein the passivation layer paste contains aluminum oxide (AlOx).

4. The method of claim 1, wherein in the forming of the passivation layer paste, a formation thickness of the passivation layer paste is about 10 nm to 25 nm.

5. The method of claim 1, wherein the forming of the back surface field region includes diffusing the impurities of the first conductive type contained in the passivation layer paste into the partial area of the emitter region by selectively irradiating a laser beam onto the partial area of the passivation layer paste to form the back surface field region.

6. The method of claim 1, wherein the emitter region is formed at a process temperature of 800 °C to 900 °C.

7. The method of claim 6, wherein the forming of the emitter region includes diffusing impurities of the second conductive type into the back surface of the semiconductor substrate using a process gas containing impurities of the second conductive type in a diffusion furnace.

8. The method of claim 7, wherein the process gas includes $POCl_3$ gas.

9. The method of claim 5, wherein the forming of the plurality of openings in the passivation layer paste includes selectively irradiating the laser beam onto the second partial area of the passivation layer paste positioned on the emitter region and the third partial area of the passivation layer paste positioned on the back surface field region to form the plurality of openings.

10. The method of claim 9, wherein a power of the laser beam used to form the plurality of openings in the passivation layer paste is greater than a power of the laser beam used to form the back surface field region.

11. The method of claim 1, wherein the forming of the

plurality of openings in the passivation layer paste includes:

forming a mask having a plurality of openings on the passivation layer paste; and
etching the first and second partial areas of the passivation layer paste exposed through the plurality of openings of the mask to form the plurality of openings in the passivation layer paste.

12. A solar cell comprising:

a semiconductor substrate containing impurities of a first conductive type;
an emitter region which is positioned at a partial area of a back surface of the semiconductor substrate and contains impurities of a second conductive type opposite the first conductive type;
a back surface field region which is positioned at a remaining partial area of the back surface of the semiconductor substrate and contains impurities of the first conductive type at a concentration higher than the semiconductor substrate;
a passivation layer which is positioned on the emitter region and the back surface field region, has a plurality of openings exposing the emitter region and the back surface field region, and contains impurities of the first conductive type;
a first electrode connected to the emitter region; and
a second electrode connected to the back surface field region.

13. The solar cell of claim 12, wherein the passivation layer contains aluminum oxide (AlOx).

14. The solar cell of claim 12, wherein a thickness of the passivation layer is 10 nm to 25 nm.

15. The solar cell of claim 12, wherein a concentration of the impurities of the first conductive type contained in the passivation layer is higher than a concentration of the impurities of the second conductive type contained in the emitter region.

FIG. 1

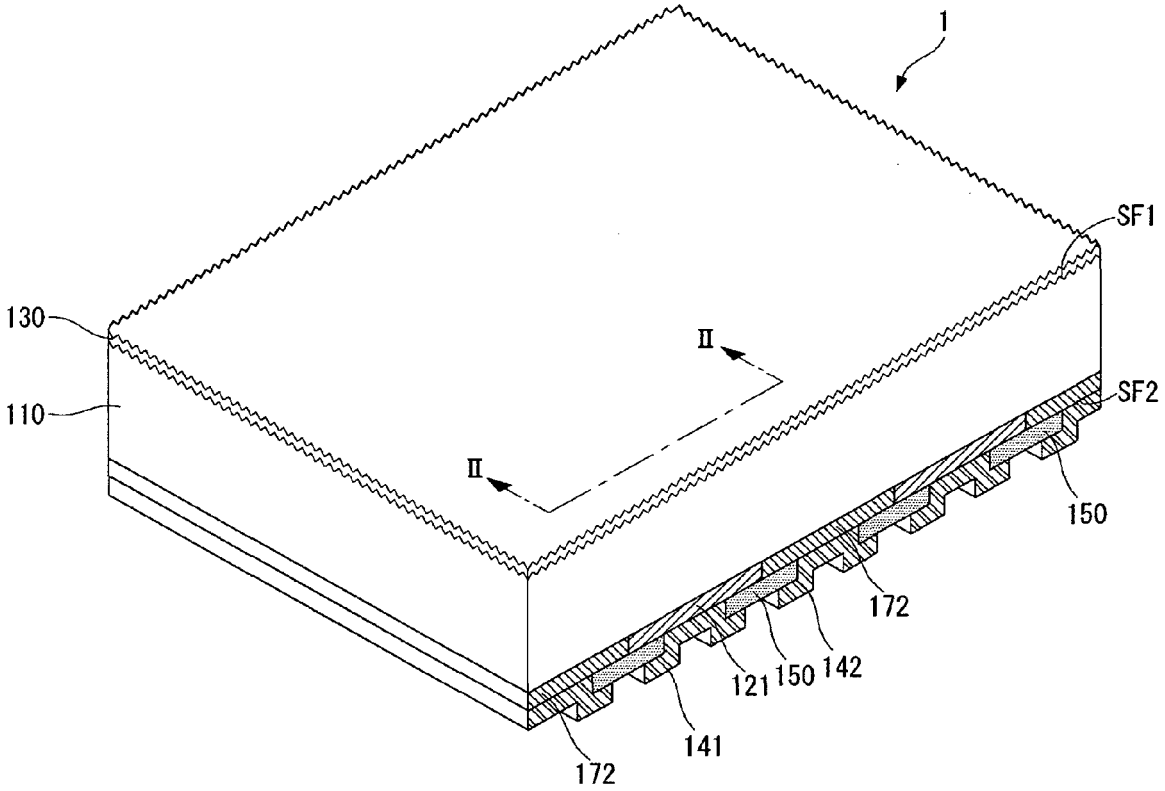


FIG. 2

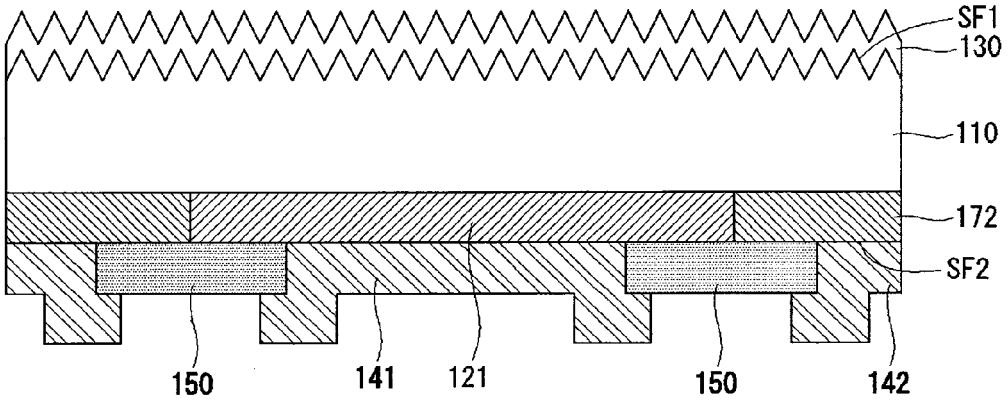


FIG. 3

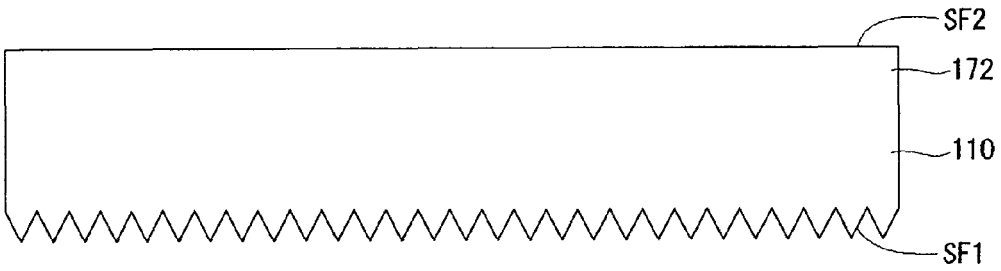


FIG. 4

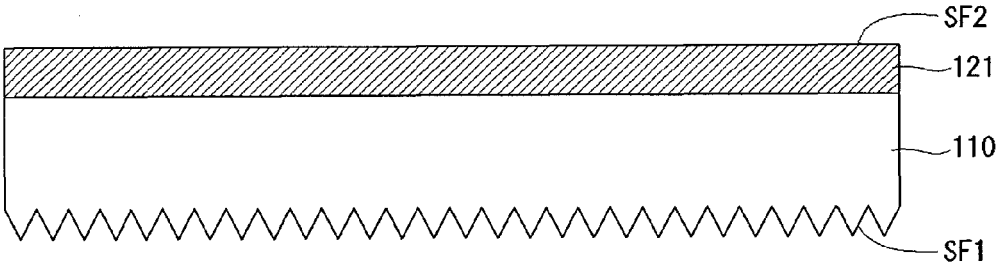


FIG. 5

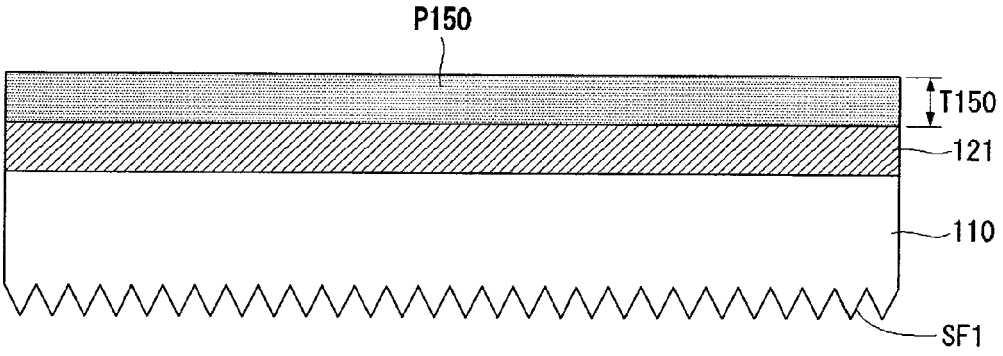

P150
T150
121
110
SF1

FIG. 6

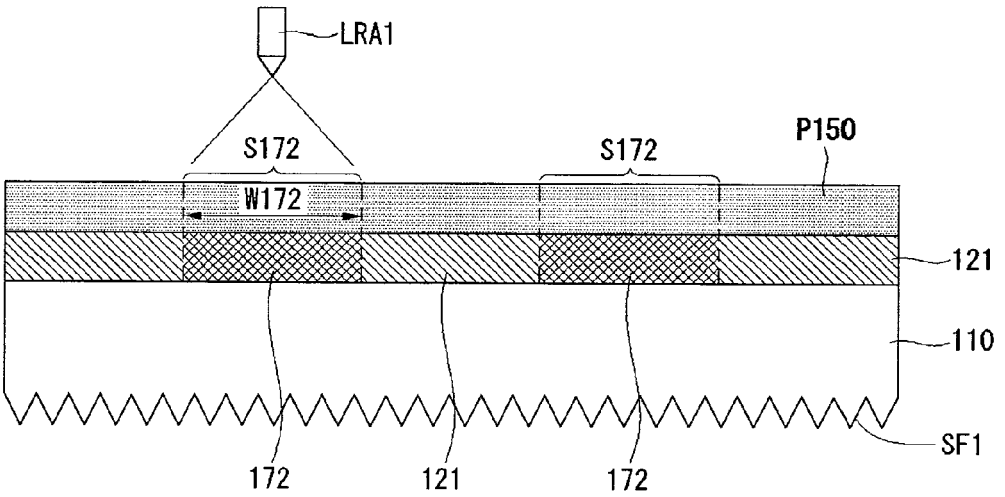
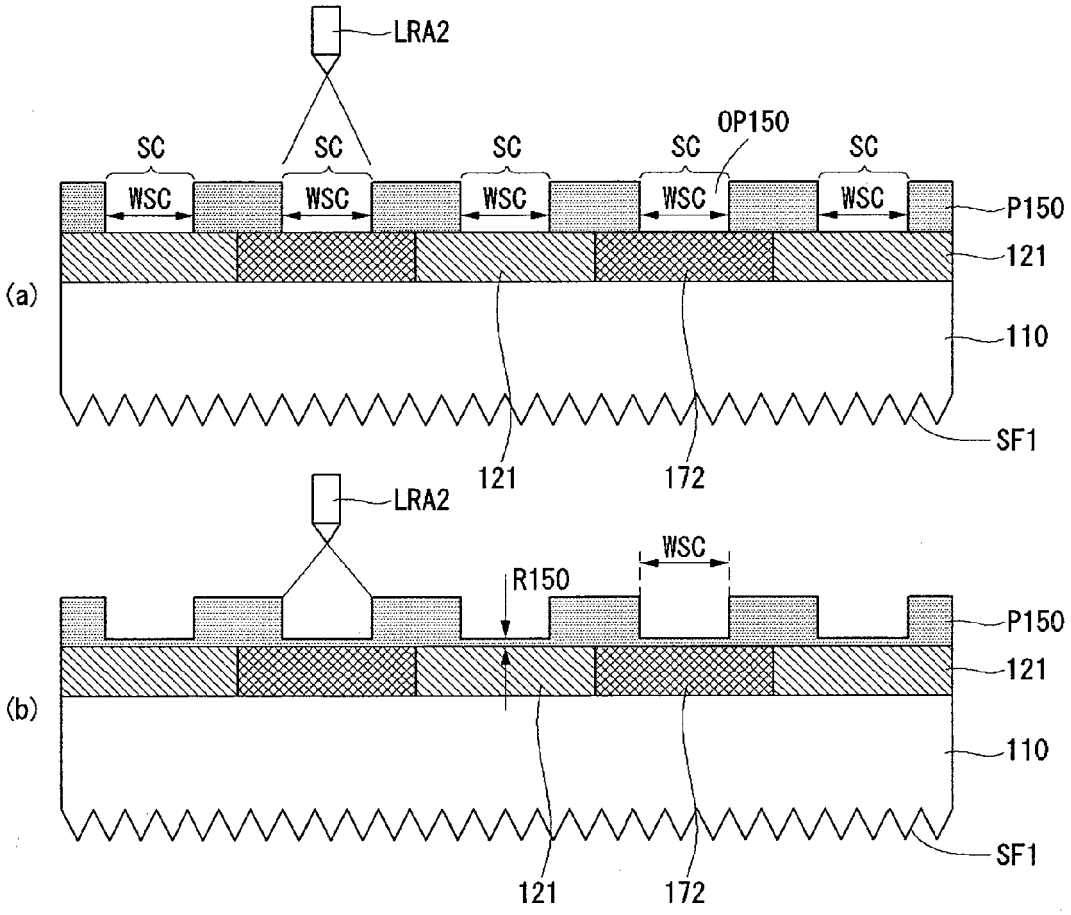

LRA1
S172
S172
P150
W172
121
110
SF1
172
121
172

FIG. 7A


LRA2
SC
SC
SC
SC
SC
OP150
WSC
WSC
WSC
WSC
WSC
P150
121
(a)
110
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121
172
LRA2
WSC
R150
P150
121
(b)
110
SF1
121
172

FIG. 7B

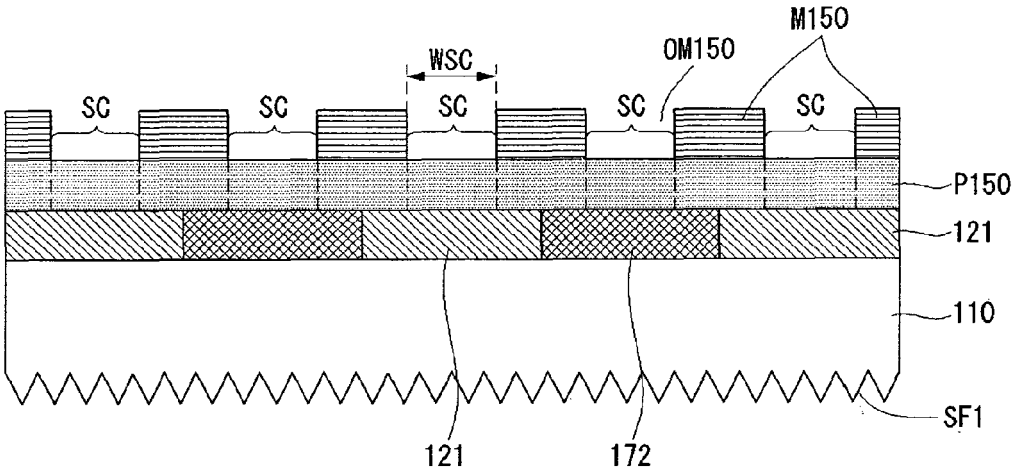


FIG. 8

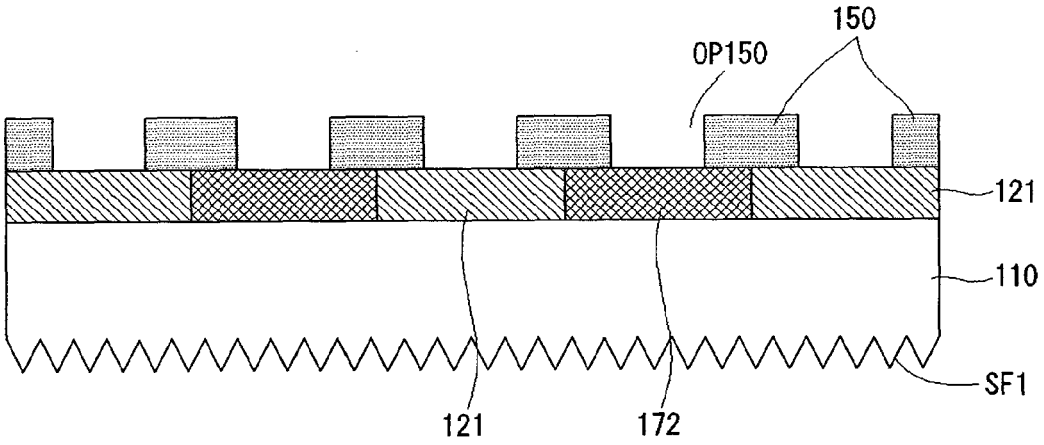
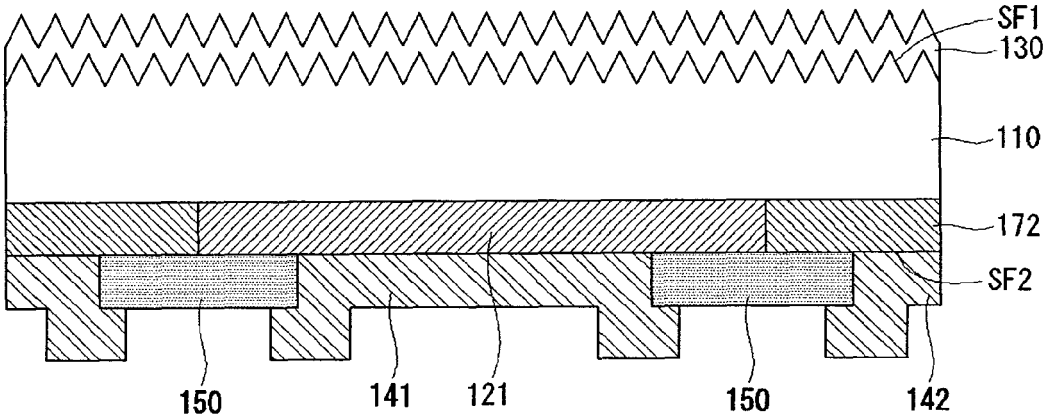

150
OP150
121
110
SF1
121
172

FIG. 9


SF1
130
110
172
SF2
150
141
121
150
142

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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