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(54) MEMORY CELLS, INTEGRATED DEVICES, AND METHODS OF FORMING MEMORY CELLS

**SPEICHERZELLEN, INTEGRIERTE VORRICHTUNGEN UND VERFAHREN ZUR HERSTELLUNG
VON SPEICHERZELLEN**

**CELLULES DE MÉMOIRE, DISPOSITIFS INTÉGRÉS ET PROCÉDÉS PERMETTANT DE FORMER
DES CELLULES DE MÉMOIRE**

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(56) References cited:

WO-A1-2005/041196 US-A1- 2004 188 668

US-A1- 2005 006 681 US-A1- 2007 075 347

US-A1- 2009 039 333 US-A1- 2009 108 247

US-A1- 2009 166 601 US-A1- 2009 302 300

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Description

TECHNICAL FIELD

[0001] Memory cells, integrated devices, and methods of forming memory cells.

BACKGROUND

[0002] Memory is one type of integrated circuitry, and is used in electronic systems for storing data. Integrated memory is usually fabricated in one or more arrays of individual memory cells. The memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store more than two levels or states of information.

[0003] One type of memory is phase change memory (PCM). Such memory utilizes phase change material as a programmable material. Example phase change materials that may be utilized in PCM are chalcogenide materials.

[0004] The phase change materials reversibly transform from one phase to another through application of appropriate electrical stimulus. Each phase may be utilized as a memory state, and thus an individual PCM cell may have two selectable memory states that correspond to two inducible phases of the phase change material.

[0005] A problem that may occur during programming of the memory cells of a PCM array is that there may be thermal transfer between adjacent memory cells (so-called "thermal disturb"). Accordingly, the memory state of a memory cell may be disturbed when an adjacent memory cell is programmed, which can lead to unreliability of data storage within a memory array. The problem can increase with increasing downsizing of integration.

[0006] It would be desirable to develop PCM cell architectures which alleviate or prevent the above-discussed problem, and to develop methods of forming such PCM cell architectures.

[0007] US2009/166601 A1 discloses electrically programmable phase-change memory where the phase change material that may be a chalcogenide material where the phase change memory element exhibits a non-uniform temperature profile.

US2004188668 A1 discloses a memory cell device that includes a storage medium having programmable thermal impedance, and a heater in thermal communication with the storage medium. WO2005041196 A1 discloses phase change memory where the switching zone is located along a lateral extension of the phase change memory and a current signal is used to induce phase change. US2007075347 A1 discloses a phase change memory device and method of forming the same. The device may include a heat sink layer between the phase change layer and the top electrode.

SUMMARY

[0008] According to the present invention there is provided a memory cell device as set out in claim 1 and a method of forming memory cells as set out in claim 7.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

FIGS. 1-5 are diagrammatic cross-sectional views of a construction at various process stages of an example embodiment method of forming memory cells.

FIGS. 6-8 are diagrammatic cross-sectional views of a construction at various process stages of another example embodiment method of forming memory cells. The process stage of FIG. 6 may follow that of FIG. 1.

FIGS. 9 and 10 are diagrammatic cross-sectional views of a construction at various process stages of another example embodiment method of forming memory cells. The process stage of FIG. 9 may follow that of FIG. 1.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0010] Programming of a PCM cell may comprise heating of a chalcogenide material within the memory cell to cause a phase change within the chalcogenide material. Only a fraction of the total volume of the chalcogenide material within the cell may be heated. Some embodiments include recognition that thermal disturbance between adjacent memory cells may be reduced by controlling the size of the heated fraction of chalcogenide material within a memory cell during programming of the memory cell.

[0011] A PCM cell may comprise chalcogenide material between a heater and a top electrode. The chalcogenide material may be heated with the heater to cause the desired phase change within the chalcogenide material during programming. The size of the heated fraction of the chalcogenide material may be influenced by the overall thermal resistance along the chalcogenide material to the top electrode, including difference thermal resistance contributions. The difference thermal resistance contributions may include: chalcogenide material thermal resistance, top electrode thermal resistance, and interface thermal resistance between the two materials.

[0012] The embodiments include the provision of an interlayer to reduce (and in some cases, minimize) interface thermal resistance. Such an interlayer is referred to as a "thermal sink material." The thermal sink material is between chalcogenide material and a top electrode, and alters thermal resistance along an upper region of the chalcogenide material relative to a conventional PCM cell. The utilization of such thermal sink material may

alleviate or prevent thermal disturb between adjacent PCM cells during programming of a memory array.

[0013] Example embodiments are described with reference to FIGS. 1-10.

[0014] Referring to FIG. 1, a construction 10 comprises a pair of electrically conductive interconnects 14 and 16 extending through a dielectric material 12.

[0015] The dielectric material 12 may comprise any suitable composition or combination of compositions; and in some embodiments may comprise, consist essentially of, or consist of one or more of silicon dioxide, silicon nitride, and any of various doped silicate glasses (for instance, borophosphosilicate glass, phosphosilicate glass, fluorosilicate glass, etc.).

[0016] The interconnects 14 and 16 comprise electrically conductive material 15. Such electrically conductive material may comprise any suitable composition or combination of compositions; and in some embodiments may comprise, consist essentially of, or consist of tungsten.

[0017] The dielectric material 12, and interconnects 14 and 16, may be supported by a semiconductor base (not shown). Such base may comprise monocrystalline silicon, and may be referred to as a semiconductor substrate, or as a portion of a semiconductor substrate. The terms "semiconductive substrate," "semiconductor construction" and "semiconductor substrate" mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0018] The interconnects 14 and 16 be representative of a large number of interconnects formed across a semiconductor base. Ultimately, each interconnect is connected to a memory cell of a memory array (with example memory cells being shown in FIG. 5). The interconnects 14 and 16 are diagrammatically illustrated to be electrically connected to circuitry 18 and 20, respectively. Such circuitry may include control circuitry utilized for providing electrical input to individual memory cells during programming operations and during reading operations. The circuitry may also include access/sense lines (e.g., wordlines and bitlines) which electrically couple the memory cells to the control circuitry. In some embodiments, the illustrated interconnects 14 and 16 may be coupled to a common access/sense line, and in other embodiments the interconnects may be coupled to separate access/sense lines.

[0019] A planarized surface 17 extends across materials 12 and 15. Such planarized surface may be formed with any suitable processing, including, for example, chemical-mechanical polishing (CMP).

[0020] Heater material 22 is formed across the interconnects 14 and 16. The heater material is ultimately patterned into heater components of PCM cells (as de-

scribed below with reference to FIG. 3), and may comprise any suitable composition or combination of compositions. In some embodiments, the heater material may comprise, consist essentially of, or consist of titanium and nitrogen. Such heater material may comprise TiN in some embodiments, where the chemical formula shows the components of the composition and is not utilized to indicate a specific stoichiometry. The heater material may be, for example, a TiN composite, doped TiN, etc. The heater material may be formed with any suitable processing, including, for example, one or more of atomic layer deposition (ALD), chemical vapor deposition (CVD) and physical vapor deposition (PVD).

[0021] Chalcogenide material 24 is formed over the heater material. The chalcogenide material comprises, consists essentially of, or consists of germanium, antimony and tellurium, and may be referred to as GST. In some embodiments, the chalcogenide material may correspond to $\text{Ge}_2\text{Sb}_2\text{Te}_5$. The chalcogenide material may be formed utilizing any suitable processing, including, for example, one or more of ALD, CVD and PVD. The chalcogenide material may be utilized as memory material in PCM cells in some embodiments (with example PCM cells being shown in FIG. 5).

[0022] Referring to FIG. 2, thermal sink material 26 is formed over the chalcogenide material, and an electrically conductive capping material 28 is formed over the thermal sink material. In some embodiments, the material 28 may be referred to as a top electrode material.

[0023] The thermal sink material 26 comprises a composition containing antimony and at least one element in common with the capping material 28.

[0024] In some example embodiments, the material 28 comprises, consists essentially of, or consists of titanium (for instance, comprises elemental titanium or titanium nitride); the chalcogenide material comprises, consists essentially of, or consists of GST; and the thermal sink material comprises, consists essentially of, or consists of titanium in combination with one or both of tellurium and antimony.

[0025] As another example, in some embodiments the material 28 comprises, consists essentially of, or consists of a combination of titanium, aluminum and nitrogen (for instance, may be described by the chemical formula TiAlN , where such formula shows the components of the composition and is not utilized to indicate a specific stoichiometry); the chalcogenide material comprises, consists essentially of, or consists of GST; and the thermal sink material comprises, consists essentially of, or consists of one or both of titanium and aluminum in combination with antimony.

[0026] As another example, in some embodiments the material 28 comprises, consists essentially of, or consists of tantalum (for instance, comprises elemental tantalum or tantalum nitride); the chalcogenide material comprises, consists essentially of, or consists of GST; and the thermal sink material comprises, consists essentially of, or consists of tantalum in combination with antimony.

[0027] As another example, in some embodiments the material 28 comprises, consists essentially of, or consists of tungsten (for instance, comprises elemental tungsten or tungsten nitride); the chalcogenide material comprises, consists essentially of, or consists of GST; and the thermal sink material comprises, consists essentially of, or consists of tungsten in combination with antimony.

[0028] The thermal sink material 26 may be formed with any suitable processing, and in some embodiments may be deposited utilizing one or more of ALD, CVD and PVD. In the embodiment of FIG. 2, the thermal sink material is deposited directly onto the chalcogenide material 24.

[0029] The thermal sink material may improve thermal dissipation within a memory cell to alleviate or prevent the thermal disturb problem discussed above in the "background" section of this disclosure.

[0030] The thermal sink material may be formed to any suitable thickness. In some embodiments, the thermal sink material may be kept very thin so that it does not substantially alter programming characteristics of an individual memory cell relative to an analogous memory cell lacking the thermal sink material. For instance, the thermal sink material may be formed to a thickness of less than or equal to about 5 nanometers; and in some embodiments may be formed to a thickness of from about 1 nanometer to about 5 nanometers. Such thin regions of thermal sink material may be sufficient to alleviate or prevent the thermal disturb problem, while having little impact on the programming characteristics of an individual memory cell.

[0031] The electrically conductive capping material 28 may be formed with any suitable processing, and in some embodiments may be deposited utilizing one or more of ALD, CVD and PVD. In the embodiment of FIG. 2, the electrically conductive capping material 28 is formed directly on an upper surface of the thermal sink material 26.

[0032] Referring to FIG. 3, the materials 22, 24, 26 and 28 are patterned into memory cells 30 and 32. The memory cell 30 is directly over and electrically coupled with interconnect 14; and the memory cell 32 is directly over and electrically coupled with interconnect 16. Materials 22, 24, 26 and 28 may be patterned with any suitable processing. For instance, a patterned mask (not shown) may be formed over material 28; a pattern from such mask may be transferred into the underlying materials 22, 24, 26 and 28 with one or more suitable etches; and then the mask may be removed to leave the construction shown in FIG. 3. The patterned mask may comprise any suitable composition, such as, for example, photolithographically-patterned photoresist and/or one or more materials patterned utilizing pitch-multiplication methodologies. The material 28 may be considered to correspond to top electrodes of the memory cells in some embodiments.

[0033] Referring to FIG. 4, an electrically insulative liner 34 is formed along and between the memory cells 30 and 32, and a dielectric material 36 is formed over the

electrically insulative liner. The liner may comprise any suitable composition or combination of compositions, and in some embodiments may comprise, consist essentially of, or consist of silicon nitride. The dielectric material 36 may comprise any suitable composition or combination of compositions, and in some embodiments may comprise, consist essentially of, or consist of silicon dioxide and/or any of various doped silicate glasses.

[0034] Referring to FIG. 5, electrically conductive structures 38 and 40 are formed over memory cells 30 and 32, respectively. The electrically conductive structures may be lines that extend in and out of the page relative to the cross-sectional view of FIG. 5. In the shown embodiment, each of the electrically conductive structures comprises a conductive core material 42 and a barrier material 44 along an outer periphery of the core material. In some embodiments, the core material may comprise, consist essentially of, or consist of copper; and the barrier material may be a barrier to copper migration. In such embodiments, the barrier material may comprise any suitable composition, and may, for example, comprise a ruthenium-containing material. In some embodiments, other conductive materials besides the shown materials 42 and 44 may be utilized in conductive structures 38 and 40. If the conductive core material 42 does not comprise components which migrate, the barrier material 44 may be omitted.

[0035] The structures 38 and 40 are shown connected to circuitry 46 and 48, respectively. In some embodiments, structures 38 and 44 may correspond to access/sense lines, and the circuitry 46 and 48 may be utilized to control electrical flow through such access/sense lines. The memory cells 30 and 32 may be representative of a large number of cells of a PCM array, and each memory cell of such array may be uniquely addressed through the combination of an access/sense line connected to the illustrated bottoms of the cells through conductive material 15, and an access/sense line connected to the illustrated tops of the cells through electrically conductive capping material 28.

[0036] The thermal sink material 26 can reduce heating within the memory cells during programming relative to heating which may otherwise occur in the absence of such thermal sink material, and thus can alleviate or prevent thermal disturb between the adjacent memory cells 30 and 32 relative to the thermal disturb that may otherwise occur in the absence of the thermal sink material. The same applies for cells in the perpendicular directions in the array (for instance, memory cells connected to the same bitline in some embodiments). Accordingly, the incorporation of the thermal sink material 26 into memory cells 30 and 32 may beneficially alleviate or prevent the thermal disturb problem that may be associated with some conventional PCM arrays.

[0037] The utilization of thermal sink material 26 having components in common with both the chalcogenide material 24 and the electrically conductive capping material 28 alleviates thermal mismatch that may otherwise occur.

Specifically, one surface of the thermal sink material is directly against the chalcogenide material, and another surface of the thermal sink material is directly against the electrically conductive capping material. The formulation of the thermal sink material to have antimony in common with the chalcogenide material may alleviate or prevent thermal mismatch that may otherwise occur between the thermal sink material and the chalcogenide material (with "thermal mismatch" including, for example, substantially different coefficients of thermal expansion that may lead to peeling or separation between the adjacent materials during changes in temperature). Similarly, the formulation of the thermal sink material to have a component in common with the electrically conductive capping material may alleviate or prevent thermal mismatch that may otherwise occur between the thermal sink material and such electrically conductive capping material.

[0038] The utilization of thermal sink material 26 having components in common with both the chalcogenide material 24 (antimony) and the electrically conductive capping material 28 may improve adhesion between the chalcogenide material and the capping material in some embodiments, and specifically may improve adhesion as compared to structures lacking such thermal sink material.

[0039] The various materials of the memory cells 30 and 32 shown in FIG. 5 may comprise any suitable thicknesses. For instance, material 22 may be formed to a thickness of at least about 30 nanometers, material 24 may be formed to a thickness within a range of from about 30 nanometers to about 50 nanometers, material 26 may be formed to a thickness within a range of from about 1 nanometer to about 5 nanometers, and material 28 may be formed to a thickness within a range of from about 20 nanometers to about 50 nanometers.

[0040] The embodiment of FIGS. 1-5 forms thermal sinks within PCM cells by depositing thermal sink material 26 directly onto chalcogenide material 24. Such is one of many methods for forming thermal sinks within PCM cells. Another example embodiment method is described with reference to FIGS. 6-8.

[0041] Referring to FIG. 6, a construction 10a is shown at a processing stage subsequent to that of FIG. 1. The construction comprises a precursor material 50 formed directly on an upper surface of chalcogenide material 24. The precursor material ultimately combines with a component from the chalcogenide material 24 and/or from the electrically conductive capping material 28 (shown in FIG. 7) to form a thermal sink comprising components in common with both the chalcogenide material and the electrically conductive capping material. In some embodiments, the precursor material 50 may comprise a component in common with the capping material, and may be configured to react with the chalcogenide material 24 to form a thermal sink. For instance, in some embodiments the precursor material may comprise one or more of titanium, tantalum, tungsten and aluminum. The precursor material may be configured for reaction with the

chalcogenide material by incorporating a leaving group into the precursor. For instance, the precursor may comprise a metallo-organic, a metal halide, etc.

[0042] Referring to FIG. 7, the electrically conductive capping material 28 is formed directly on the precursor material 50.

[0043] Referring to FIG. 8, construction 10a is subjected to thermal processing which converts precursor material 50 (FIG. 7) into a thermal sink material 52 comprising a component in common with chalcogenide material 24 and a component in common with electrically conductive capping material 28. The thermal processing may comprise, for example, heating of the precursor material 50 and the chalcogenide material 24 to a temperature of at least about 400°C to induce reaction of the precursor material with the chalcogenide material. For instance, in some embodiments the chalcogenide material may comprise GST, the precursor material may comprise titanium, and the thermal treatment may form titanium telluride. As another example, in some embodiments the chalcogenide material may comprise GST, the precursor material may comprise tungsten, and the thermal treatment may form tungsten telluride.

[0044] The above-described thermal treatment may be conducted before, during and/or after formation of the electrically conductive capping material 28 in various embodiments. For instance, the electrically conductive capping material may be deposited under conditions having a high enough temperature to achieve the thermal treatment of the precursor material and the chalcogenide material. Alternatively, the precursor material and the chalcogenide material may be heated to the thermal treatment temperature prior to deposition of the electrically conductive capping material. In other embodiments, the precursor material and the chalcogenide material may be heated to the thermal treatment temperature after deposition of the electrically conductive capping material.

[0045] The construction 10a of FIG. 8 may be subsequently subjected to processing analogous to that described above with reference to FIGS. 3-5 to form an array of memory cells from such construction.

[0046] Another example embodiment method for forming a thermal sink within PCM cells is described with reference to FIGS. 9 and 10.

[0047] Referring to FIG. 9, a construction 10b is shown at a processing stage subsequent to that of FIG. 1. The construction comprises the electrically conductive capping material 28 formed directly on an upper surface of chalcogenide material 24.

[0048] Referring to FIG. 10, one or more ions (i.e., dopants) are implanted through the electrically conductive capping material and to an interface of the capping material and the chalcogenide material. The ions cause intermixing across such interface to form a thermal sink 62 comprising one or more components of the chalcogenide material in combination with one or more components of the capping material. For instance, in some embodiments the electrically conductive capping material comprises

titanium nitride; the chalcogenide material comprises GST; and the thermal sink comprises titanium telluride.

[0049] The construction 10b of FIG. 10 maybe subsequently subjected to processing analogous to that described above with reference to FIGS. 3-5 to form an array of memory cells from such construction.

[0050] The embodiments described above show that the thermal sink material may be formed between an electrically conductive capping material and a chalcogenide material through any of numerous methods in various embodiments; and may be formed before, during, and/or after formation of the electrically conductive capping material.

[0051] The memory cells and arrays discussed above may be incorporated into electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

[0052] The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

[0053] The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections in order to simplify the drawings.

[0054] When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against" another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

[0055] Some embodiments include an integrated device comprising a chalcogenide material, a top electrode over the chalcogenide material, and an interlayer between the top electrode and the chalcogenide material. The interlayer lowers thermal resistance in the device relative to the thermal resistance which would occur across a top electrode/chalcogenide material interface of the device in the absence of the interlayer.

[0056] Some embodiments include an integrated device comprising a chalcogenide material, an electrically conductive material over the chalcogenide material, and a thermal sink between the electrically conductive material and the chalcogenide material. The thermal sink is directly against the conductive material and the chalcogenide material. The thermal sink comprises a composition that includes an element in common with the electrically conductive material and includes antimony as an element in common with the chalcogenide material.

[0057] Some embodiments include a memory cell comprising a heater material, a chalcogenide material over the heater material, an electrically conductive material over the chalcogenide material, and a thermal sink between the electrically conductive material and the chalcogenide material. The thermal sink is directly against both the electrically conductive material and the chalcogenide material. The thermal sink comprises a composition that includes an element in common with the electrically conductive material and includes antimony as an element in common with the chalcogenide material.

[0058] Some embodiments include a method of forming a memory cell. Chalcogenide material is formed over heater material. An electrically conductive material is formed over the chalcogenide material. A thermal sink is formed between the electrically conductive material and the chalcogenide material. The thermal sink is directly against the conductive material and the chalcogenide material. The thermal sink comprises a composition that includes an element in common with the electrically conductive material and includes an element in common with the chalcogenide material.

Claims

1. An integrated device, comprising:

chalcogenide material (24) comprising antimony, tellurium and germanium;
an electrically conductive material (28) over the chalcogenide material; and
a thermal sink (26) between the electrically conductive material (28) and the chalcogenide material (24), the thermal sink (26) being directly against the conductive material (28) and the chalcogenide material (24);
the thermal sink (26) comprising a composition that includes antimony and an element in common with the electrically conductive material (28).

2. The device of claim 1 wherein:

the electrically conductive material (28) comprises titanium; and
wherein the thermal sink (26) comprises titanium and the antimony.

3. The device of claim 1 wherein:

the conductive material (28) comprises titanium, aluminum and nitrogen; and
the thermal sink (26) comprises the antimony in combination with one or both of titanium and aluminum.

4. The device of claim 1 wherein:

the conductive material (28) comprises tantalum; and
the thermal sink (26) comprises tantalum in combination with the antimony.

5. The device of claim 1 wherein:

the conductive material (28) comprises tungsten; and
the thermal sink (26) comprises tungsten in combination with the antimony.

6. The device of claim 1 wherein the chalcogenide material (24) is over a heater material (22).

7. A method of forming a memory cell, comprising:

forming chalcogenide material (24) over heater material (22);
forming an electrically conductive material (28) over the chalcogenide material (24); and
forming a thermal sink (26) between the electrically conductive material (28) and the chalcogenide material (24), the thermal sink (26) being directly against the conductive material (28) and the chalcogenide material (24);
the thermal sink (26) comprising a composition that includes an element in common with the electrically conductive material (28) and includes an element in common with the chalcogenide material (24).

8. The method of claim 7 wherein the forming of the thermal sink (26) comprises:

depositing a precursor material (50) directly onto the chalcogenide material (24); and
thermally treating the precursor material (50) and the chalcogenide material (24) to cause reaction between the precursor material (50) and the chalcogenide material (24) and thereby form the thermal sink (26).

9. The method of claim 8 wherein:

the chalcogenide material (24) comprises germanium, antimony and tellurium;
the precursor material (50) comprises titanium;

and
the thermal sink (26) comprises titanium and tellurium.

10. The method of claim 8 wherein:

the chalcogenide material (24) comprises germanium, antimony and tellurium;
the precursor material (50) comprises tungsten; and
the thermal sink (26) comprises tungsten and tellurium.

11. The method of claim 7 wherein the thermal sink (26) is formed before forming the electrically conductive material (28).

12. The method of claim 11 wherein the forming of the thermal sink (26) comprises depositing thermal sink material directly onto the chalcogenide material (24).

13. The method of claim 7 wherein the thermal sink (26) is formed after forming the electrically conductive material (28).

14. The method of claim 13 wherein the forming of the thermal sink (26) comprises:

forming the electrically conductive material (28) directly against the chalcogenide material (24); and
implanting one or more ions through the electrically conductive material (28) to an interface of the electrically conductive material (28) with the chalcogenide material (24);
said implanting causing intermixing of one or more components of the chalcogenide material (24) with one or more components of the electrically conductive material (28) to thereby form the thermal sink (26).

15. The method of claim 14 wherein:

the electrically conductive material (28) comprises titanium nitride;
the chalcogenide material (24) comprises germanium, antimony and tellurium; and
the thermal sink (26) comprises titanium telluride.

16. The method of claim 15 wherein the one or more ions include one or more of germanium, arsenic and argon.

Patentansprüche

1. Integrierte Vorrichtung, umfassend:

- Chalkogenid-Material (24), umfassend Antimon, Tellur und Germanium;
ein elektrisch leitendes Material (28) über dem Chalkogenid-Material; und
eine Wärmesenke (26) zwischen dem elektrisch leitenden Material (28) und dem Chalkogenid-Material (24), wobei die Wärmesenke (26) direkt an dem leitenden Material (28) und dem Chalkogenid-Material (24) anliegt;
wobei die Wärmesenke (26) eine Zusammensetzung umfasst, die Antimon und ein mit dem elektrisch leitenden Material (28) gemeinsames Element einschließt.
2. Vorrichtung nach Anspruch 1, wobei:
das elektrisch leitende Material (28) Titan umfasst; und
wobei die Wärmesenke (26) Titan und das Antimon umfasst.
3. Vorrichtung nach Anspruch 1, wobei:
das leitende Material (28) Titan, Aluminium und Stickstoff umfasst; und
die Wärmesenke (26) das Antimon in Kombination mit einem oder beiden von Titan und Aluminium umfasst.
4. Vorrichtung nach Anspruch 1, wobei:
das leitende Material (28) Tantal umfasst; und
die Wärmesenke (26) Tantal in Kombination mit dem Antimon umfasst.
5. Vorrichtung nach Anspruch 1, wobei:
das leitende Material (28) Wolfram umfasst; und
die Wärmesenke (26) Wolfram in Kombination mit dem Antimon umfasst.
6. Vorrichtung nach Anspruch 1, wobei das Chalkogenid-Material (24) sich über einem Heizmaterial (22) befindet.
7. Verfahren zum Ausbilden einer Speicherzelle, umfassend:
Ausbilden von Chalkogenid-Material (24) über Heizmaterial (22);
Ausbilden eines elektrisch leitenden Materials (28) über dem Chalkogenid-Material (24); und
Ausbilden einer Wärmesenke (26) zwischen dem elektrisch leitenden Material (28) und dem Chalkogenid-Material (24), wobei die Wärmesenke (26) direkt an dem leitenden Material (28) und dem Chalkogenid-Material (24) anliegt;
wobei die Wärmesenke (26) eine Zusammensetzung umfasst, die ein mit dem elektrisch leitenden Material (28) gemeinsames Element einschließt und die ein mit dem Chalkogenid-Material (24) gemeinsames Element einschließt.
8. Verfahren nach Anspruch 7, wobei das Ausbilden der Wärmesenke (26) Folgendes umfasst:
Abscheiden eines Vorläufermaterials (50) direkt auf das Chalkogenid-Material (24); und
thermisches Behandeln des Vorläufermaterials (50) und des Chalkogenid-Materials (24), um eine Reaktion zwischen dem Vorläufermaterial (50) und dem Chalkogenid-Material (24) hervorzurufen und dadurch die Wärmesenke (26) auszubilden.
9. Verfahren nach Anspruch 8, wobei:
das Chalkogenid-Material (24) Germanium, Antimon und Tellur umfasst;
das Vorläufermaterial (50) Titan umfasst; und
die Wärmesenke (26) Titan und Tellur umfasst.
10. Verfahren nach Anspruch 8, wobei:
das Chalkogenid-Material (24) Germanium, Antimon und Tellur umfasst;
das Vorläufermaterial (50) Wolfram umfasst; und
die Wärmesenke (26) Wolfram und Tellur umfasst.
11. Verfahren nach Anspruch 7, wobei die Wärmesenke (26) ausgebildet wird, bevor das elektrisch leitende Material (28) ausgebildet wird.
12. Verfahren nach Anspruch 11, wobei das Ausbilden der Wärmesenke (26) das Abscheiden von Wärmesenkenmaterial direkt auf das Chalkogenid-Material (24) umfasst.
13. Verfahren nach Anspruch 7, wobei die Wärmesenke (26) ausgebildet wird, nachdem das elektrisch leitende Material (28) ausgebildet wird.
14. Verfahren nach Anspruch 13, wobei das Ausbilden der Wärmesenke (26) Folgendes umfasst:
Ausbilden des elektrisch leitenden Materials (28) direkt an dem Chalkogenid-Material (24); und
Implantieren von einem oder mehreren Ionen an einer Schnittstelle des elektrisch leitenden Materials (28) mit dem Chalkogenid-Material (24) durch das elektrisch leitende Material (28);
wobei das Implantieren das Vermischen von einer oder mehreren Komponenten des Chalko-

genid-Materials (24) mit einer oder mehreren Komponenten des elektrisch leitenden Materials (28) herbeiführt, um dadurch die Wärmesenke (26) auszubilden.

15. Verfahren nach Anspruch 14, wobei:

das elektrisch leitende Material (28) Titannitrid umfasst;
das Chalkogenid-Material (24) Germanium, Antimon und Tellur umfasst; und
die Wärmesenke (26) Titantellurid umfasst.

16. Verfahren nach Anspruch 15, wobei die einen oder mehreren Ionen eines oder mehrere von Germanium, Arsen und Argon einschließen.

Revendications

1. Dispositif intégré, comprenant :

un matériau chalcogénure (24) comprenant de l'antimoine, du tellure et du germanium ;
un matériau électriquement conducteur (28) sur le matériau chalcogénure ; et
un puits thermique (26) entre le matériau électriquement conducteur (28) et le matériau chalcogénure (24), le puits thermique (26) étant directement contre le matériau conducteur (28) et le matériau chalcogénure (24) ;
le puits thermique (26) comprenant une composition comportant de l'antimoine et un élément en commun avec le matériau électriquement conducteur (28).

2. Dispositif selon la revendication 1, dans lequel :

le matériau électriquement conducteur (28) comprend du titane ; et
le puits thermique (26) comprend du titane et de l'antimoine.

3. Dispositif selon la revendication 1, dans lequel :

le matériau conducteur (28) comprend du titane, de l'aluminium et de l'azote ; et
le puits thermique (26) comprend de l'antimoine en association avec du titane et/ou de l'aluminium.

4. Dispositif selon la revendication 1, dans lequel :

le matériau conducteur (28) comprend du tantale ; et
le puits thermique (26) comprend du tantale en association avec l'antimoine.

5. Dispositif selon la revendication 1, dans lequel :

le matériau conducteur (28) comprend du tungstène ; et
le puits thermique (26) comprend du tungstène en association avec l'antimoine.

6. Dispositif selon la revendication 1, dans lequel le matériau chalcogénure (24) se trouve sur un matériau chauffant (22).

7. Procédé permettant de former une cellule de mémoire, comprenant :

la formation de matériau chalcogénure (24) sur matériau chauffant (22) ;
la formation d'un matériau électriquement conducteur (28) sur le matériau chalcogénure (24) ; et
la formation d'un puits thermique (26) entre le matériau électriquement conducteur (28) et le matériau chalcogénure (24), le puits thermique (26) étant directement contre le matériau conducteur (28) et le matériau chalcogénure (24) ;
le puits thermique (26) comprenant une composition comportant un élément en commun avec le matériau électriquement conducteur (28) et comportant un élément en commun avec le matériau chalcogénure (24).

8. Procédé selon la revendication 7, dans lequel la formation du puits thermique (26) comprend :

le dépôt d'un matériau précurseur (50) directement sur le matériau chalcogénure (24) ; et
le traitement thermique du matériau précurseur (50) et du matériau chalcogénure (24) afin d'entraîner une réaction entre le matériau précurseur (50) et le matériau chalcogénure (24) et ainsi former le puits thermique (26).

9. Procédé selon la revendication 8, dans lequel :

le matériau chalcogénure (24) comprend du germanium, de l'antimoine et du tellure ;
le matériau précurseur (50) comprend du titane ; et
le puits thermique (26) comprend du titane et du tellure.

10. Procédé selon la revendication 8, dans lequel :

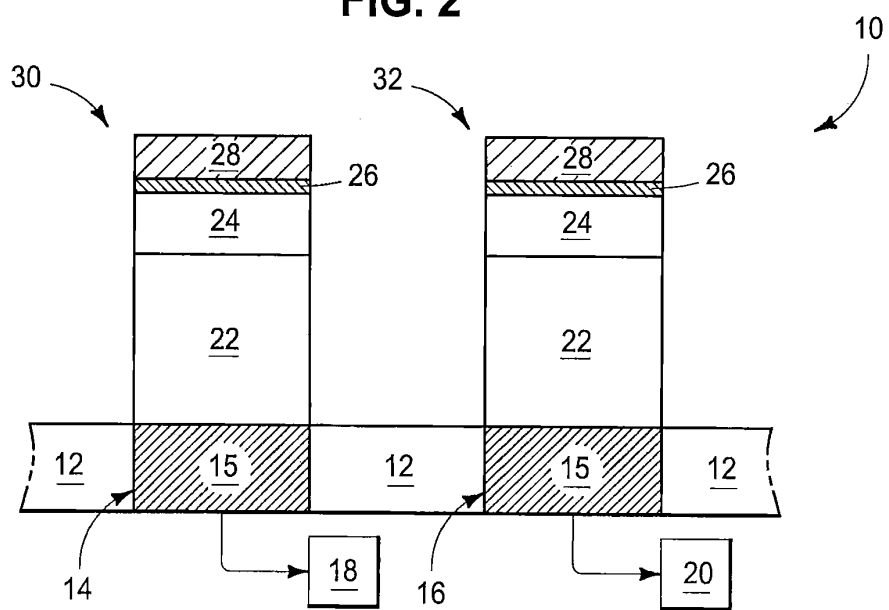
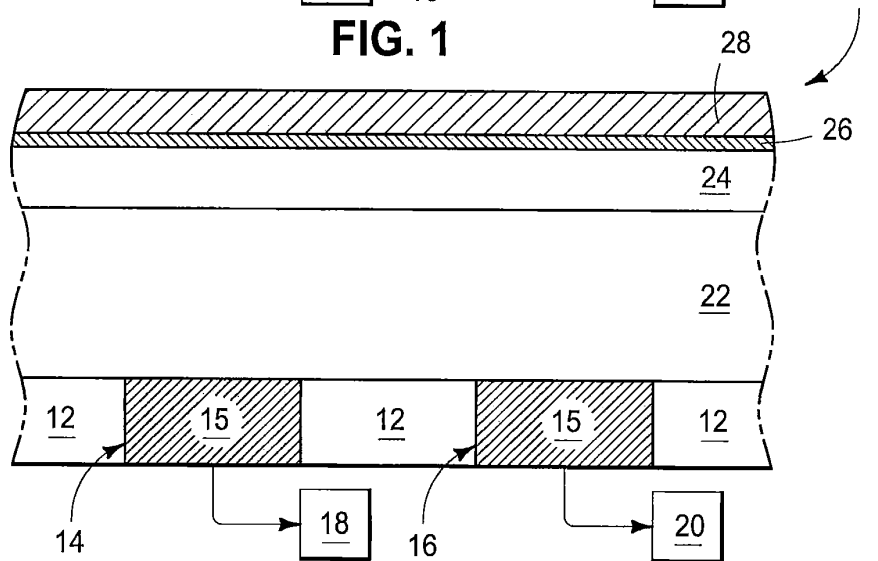
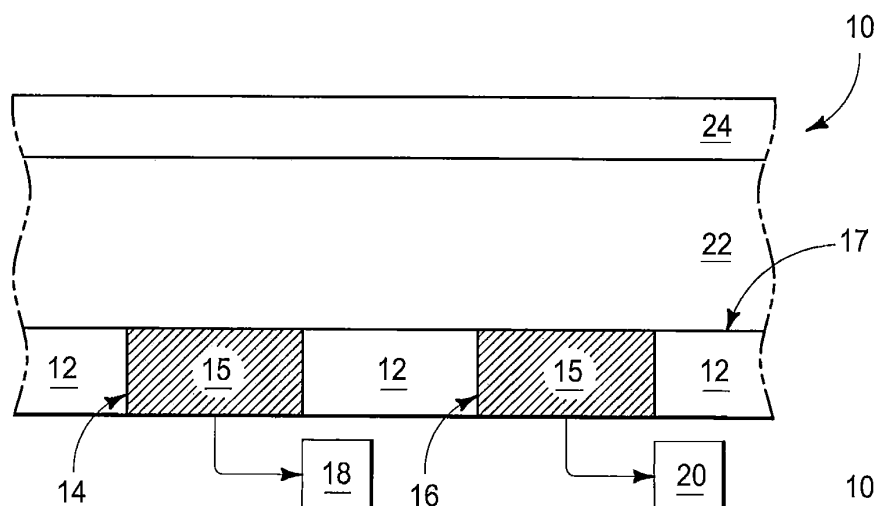
le matériau chalcogénure (24) comprend du germanium, de l'antimoine et du tellure ;
le matériau précurseur (50) comprend du tungstène ; et
le puits thermique (26) comprend du tungstène et du tellure.

11. Procédé selon la revendication 7, dans lequel le puits thermique (26) est formé avant la formation du matériau électriquement conducteur (28).
12. Procédé selon la revendication 11, dans lequel la formation du puits thermique (26) comprend le dépôt du matériau du puits thermique directement sur le matériau chalcogénure (24). 5
13. Procédé selon la revendication 7, dans lequel le puits thermique (26) est formé après la formation du matériau électriquement conducteur (28). 10
14. Procédé selon la revendication 13, dans lequel la formation du puits thermique (26) comprend : 15
- la formation du matériau électriquement conducteur (28) directement contre le matériau chalcogénure (24) ; et
- l'implantation d'un ou plusieurs ions à travers le matériau électriquement conducteur (28) vers une interface du matériau électriquement conducteur (28) avec le matériau chalcogénure (24) ; 20
- ladite implantation entraînant un mélange d'un ou plusieurs composants du matériau chalcogénure (24) avec un ou plusieurs composants du matériau électriquement conducteur (28) pour ainsi former le puits thermique (26). 25
- 30
15. Procédé selon la revendication 14, dans lequel :
- le matériau électriquement conducteur (28) comprend du nitrure de titane ;
- le matériau chalcogénure (24) comprend du germanium, de l'antimoine et du tellure ; et 35
- le puits thermique (26) comprend du tellure de titane.
16. Procédé selon la revendication 15, dans lequel les uns ou plusieurs ions comprennent un ou plusieurs parmi le germanium, l'arsenic et l'argon. 40

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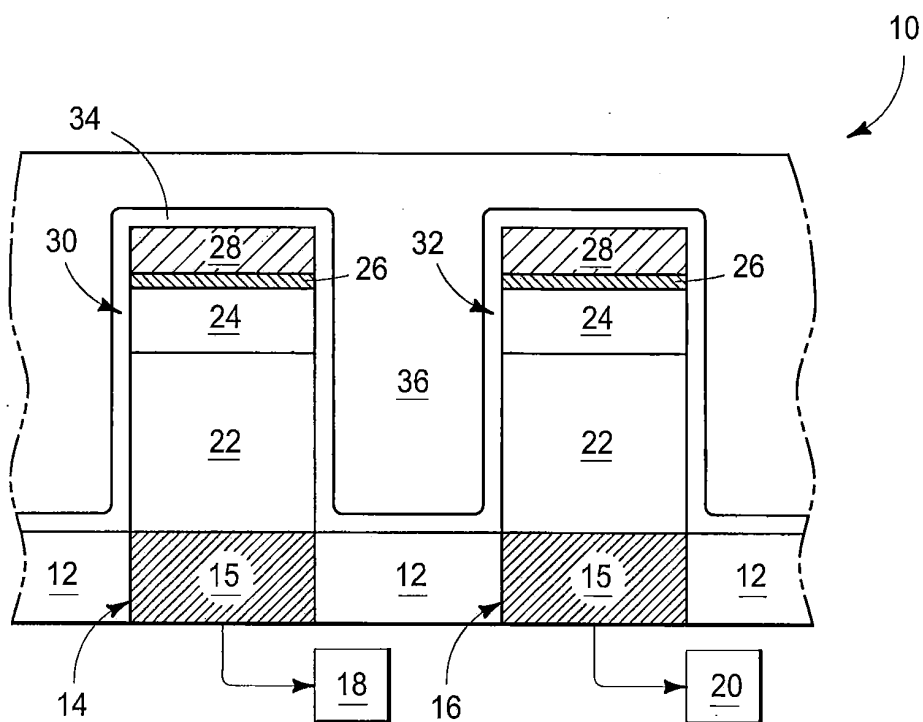


FIG. 4

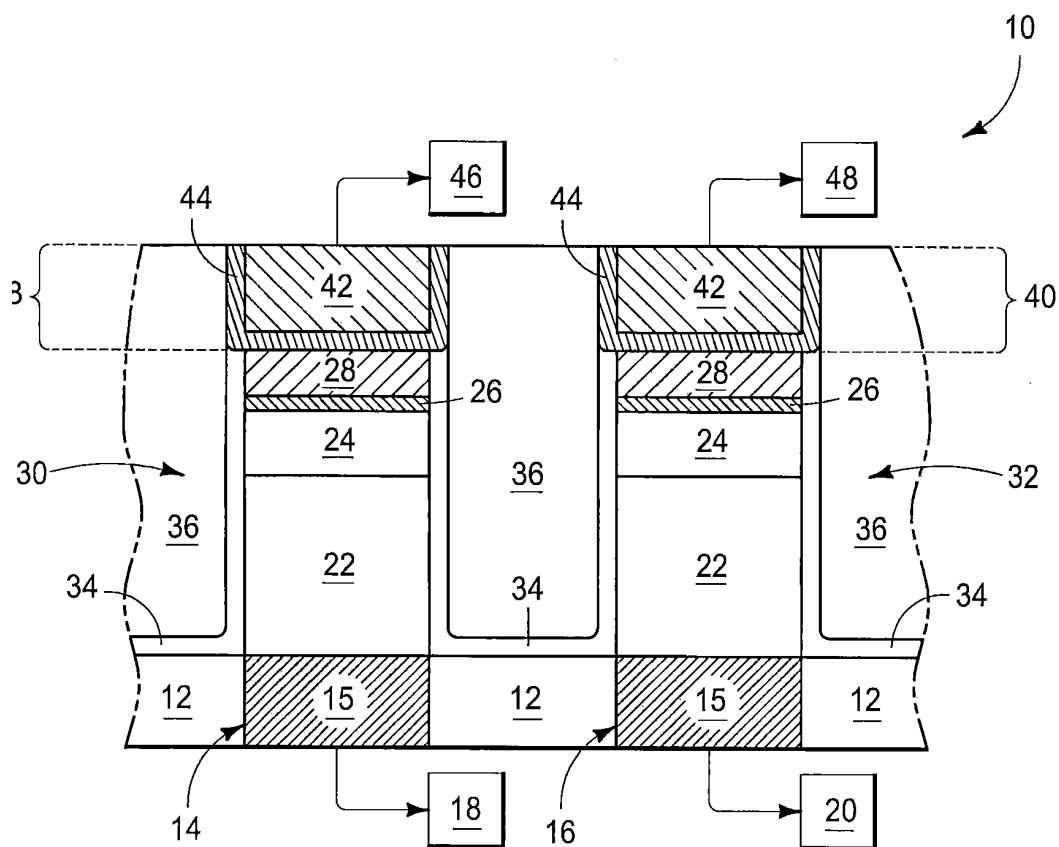


FIG. 5

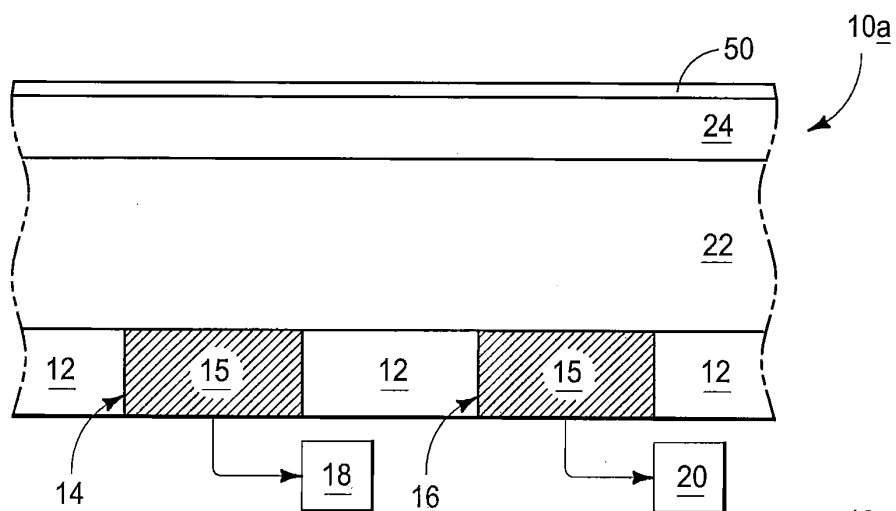


FIG. 6

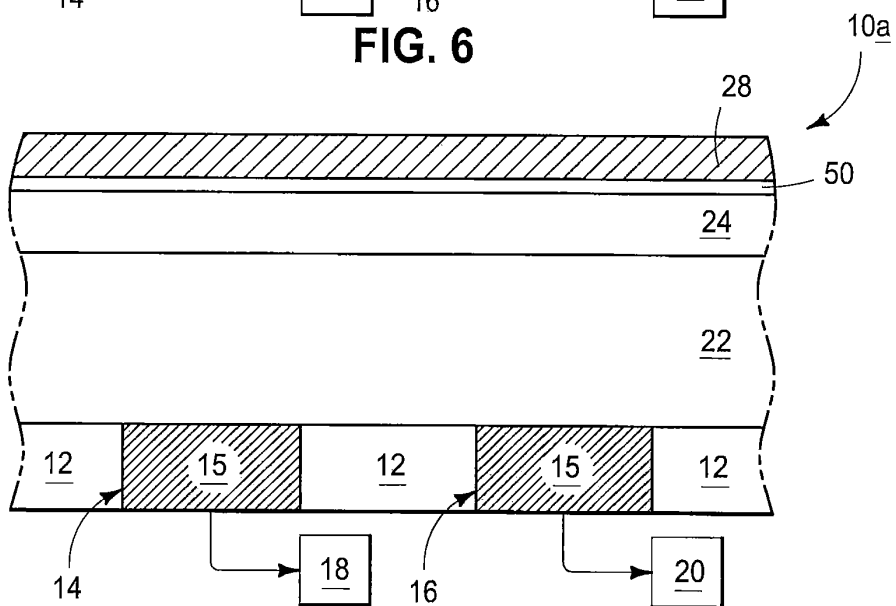


FIG. 7

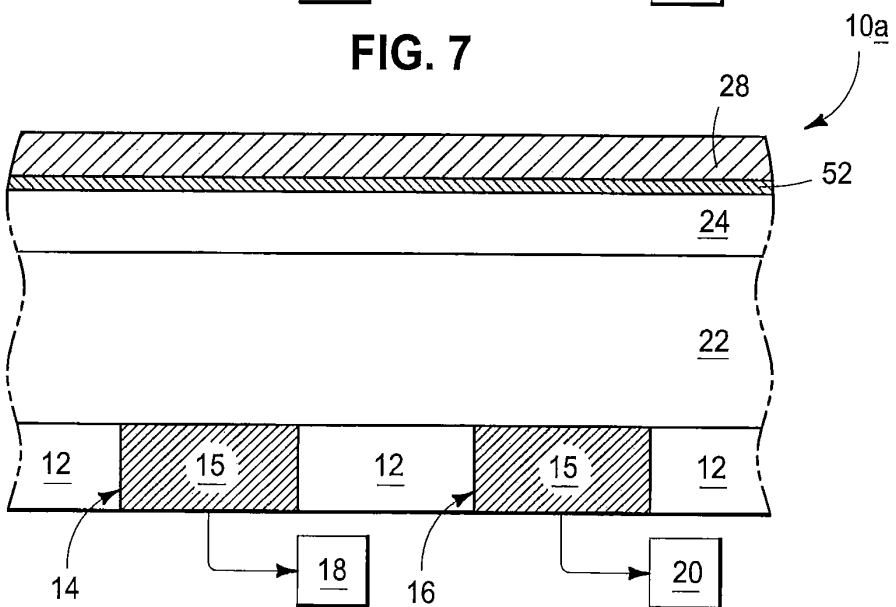


FIG. 8

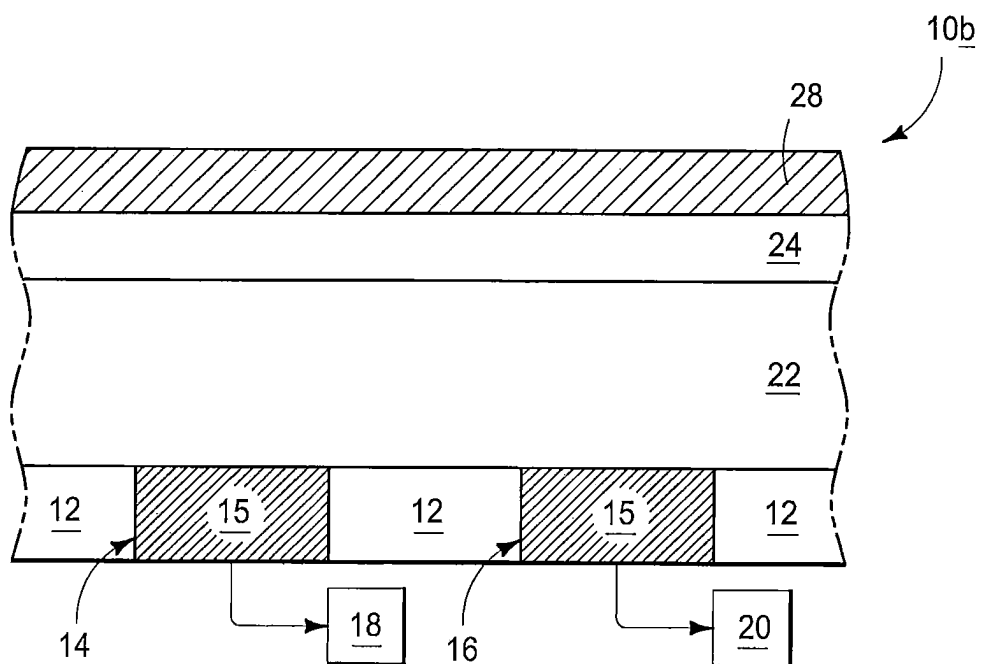


FIG. 9

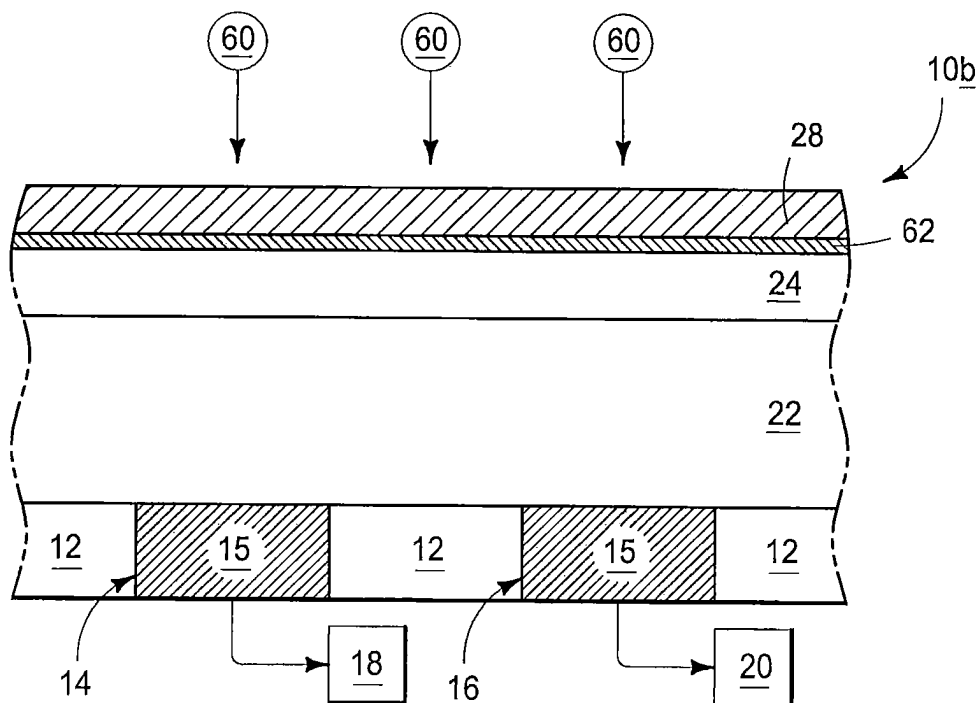


FIG. 10

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2009166601 A1 [0007]
- US 2004188668 A1 [0007]
- WO 2005041196 A1 [0007]
- US 2007075347 A1 [0007]