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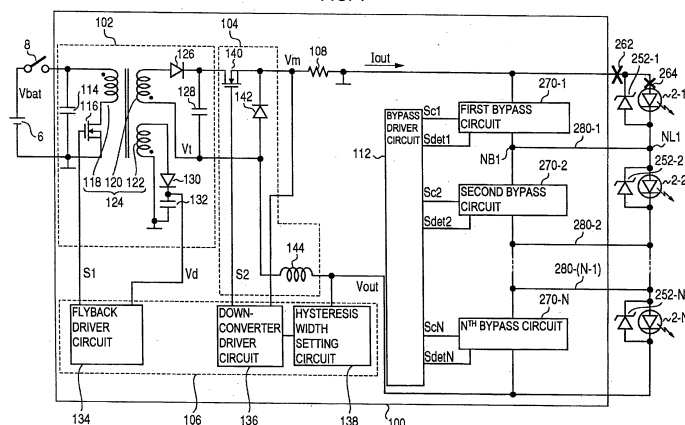
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(54) **Light source control device**

(57) A light source control device comprises a first bypass switch connected in parallel to one part of semiconductor light sources, and a second bypass switch connected in series to the first bypass switch and in parallel to another part of the semiconductor light sources. In a connection line connecting a connection node between the first and the second bypass switches and a connection node between the one part and the another

part of the semiconductor light sources, a polarity of a current flowing in the connection line when the first bypass switch is off and the second bypass switch is on is opposite to a polarity of the current flowing in the connection line when the first bypass switch is on and the second bypass switch is off. When a poor continuity is generated in the connection line, the first and the second bypass switches are forcedly turned on.

FIG. 1



Description

FIELD

5 **[0001]** The present invention relates to a light source control device that controls a light source.

BACKGROUND

10 **[0002]** In recent years, for a vehicle lighting device such as headlights, a semiconductor light source such as LEDs (light emitting diodes) which are longer in lifetime and lower in power consumption is used instead of a halogen lamp having a filament in a related art. The degree of light emission, that is, the brightness of the LED depends on the magnitude of a current that is made to flow in the LED. For that reason, when the LED is used as a light source, there is a need to provide a lighting circuit for adjusting the current flowing in the LED.

15 **[0003]** The present inventors have proposed, in Patent Literature 1, a technique in which in order to conduct fine light distribution control while making the light distribution of the headlight variable, an array of the LEDs is applied as the light source, and the respective LEDs are switched on or off, individually. In the lighting circuit disclosed in Patent Literature 1, a bypass switch is disposed in parallel to each of the LEDs, and the bypass switch is turned on/off to realize the individual switch-on/off of the LED.

20 [Citation List]

[Patent Literature]

[0004]

25 [Patent Literature 1] JP-A-2011-192865

30 **[0005]** When a bypass system disclosed in Patent Literature 1 is applied to the lighting circuit, lines around the LEDs become relatively complicated. When the lines become complicated, a possibility that a poor continuity such as a contact failure or disconnection is generated may become high.

SUMMARY

35 **[0006]** Exemplary embodiments of the invention provide a light source control device that can appropriately cope with the poor continuity which is generated in the line around the light sources or the bypass switches.

[0007] A light source control device (100,700) according to an exemplary embodiment, comprises:

a driver circuit (102,702) adapted to generate a drive current (Iout) that flows in a plurality of semiconductor light sources connected in series;

40 a first bypass switch (110-1) connected in parallel to one part of the plurality of semiconductor light sources; and a second bypass switch (110-2) connected in series to the first bypass switch (110-1), and connected in parallel to another part of the plurality of semiconductor light sources,

45 wherein in a connection line (280-1) that connects a connection node (NB1) between the first bypass switch (110-1) and the second bypass switch (110-2), and a connection node (NL1) between the one part of the plurality of semiconductor light sources and the another part of the plurality of semiconductor light sources, a polarity of a current that flows in the connection line (280-1) when the first bypass switch (110-1) is off and the second bypass switch (110-2) is on is opposite to a polarity of the current that flows in the connection line (280-1) when the first bypass switch (110-1) is on and the second bypass switch (110-2) is off, and

50 wherein when a poor continuity is generated in the connection line (280-1), both of the first bypass switch (110-1) and the second bypass switch (110-2) are forcedly turned on.

[0008] According to this aspect, if the poor continuity is generated in the connection line, both of the first bypass switch and the second bypass switch can be forcedly turned on.

[0009] A light source control device (100,700) according to an exemplary embodiment, comprises:

55 a driver circuit (102,702) adapted to generate a drive current (Iout) that flows in a plurality of semiconductor light sources connected in series;

a bypass switch (110) connected in parallel to at least one part of the plurality of semiconductor light sources;

a main control circuit (112) adapted to cyclically turn on/off the bypass switch (110) in a normal light-up state; and an abnormality detection auxiliary circuit (272,274) adapted to change the amount of charge held by a capacitor (282) to a first direction by a first time constant when the bypass switch (110) is off and a voltage between both ends of the bypass switch (110) is lower than a first voltage, or higher than a second voltage higher than the first voltage, and to change the amount of charge held by the capacitor (282) to a second direction opposite to the first direction by a second time constant longer than the first time constant when the amount of charge held by the capacitor is not changed to the first direction by the first time constant, wherein the main control circuit (112) determines whether an abnormality is generated, or not, on the basis of the voltage between both ends of the capacitor (282), and forcedly turns on the bypass switch (110) if it is determined that the abnormality is generated.

[0010] According to this aspect, it can be determined whether the abnormality is generated, or not, with the use of a difference between the first time constant and the second time constant.

[0011] An arbitrary combination of the above elements, and the components or expressions of the present invention which are displaced mutually among a device, a method, and a system are also effective as the aspect of the present invention.

[0012] According to the present invention, there can be provided the light source control device that can appropriately cope with the poor continuity which is generated in the line around the light sources or the bypass switches.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

FIG. 1 is a circuit diagram illustrating a configuration of a semiconductor light source control device and members connected to the semiconductor light source control device according to an embodiment.

FIG. 2 is a circuit diagram illustrating a configuration of a hysteresis width setting circuit of FIG. 1.

FIG. 3 is a graph illustrating a relationship between an absolute value of a drive voltage V_{out} and an offset voltage V_{offset} .

FIG. 4 is a circuit diagram illustrating a configuration of a downconverter driver circuit of FIG. 1.

FIG. 5 is a circuit diagram illustrating configurations of a second bypass circuit and a third bypass circuit of FIG. 1. FIGS. 6A to 6C illustrate a time variation of a drive current.

FIG. 7 is a timing chart illustrating a change in a second bypass switch drive signal and a second abnormality detection signal in a PWM dimming state.

FIG. 8 is a circuit diagram illustrating a configuration of a semiconductor light source lighting circuit according to a comparative example.

FIGS. 9A to 9C illustrate configurations of semiconductor light source control devices according to a first to third modified examples.

FIG. 10 is a circuit diagram illustrating a configuration of a semiconductor light source control device according to a fourth modified example.

FIG. 11 is a circuit diagram illustrating a configuration of a second bypass circuit in a semiconductor light source control device according to a fifth modified example.

FIG. 12 is a timing chart illustrating a change in the second lighting on/off control signals when the disconnection is generated in a second LED.

DETAILED DESCRIPTION

[0014] Hereinafter, identical or equivalent elements, members, and signals illustrated in the respective drawings are indicated by the same numerals or symbols, and their repetitive description will be appropriately omitted. Also, parts of members which are not important in description in the respective drawings will be omitted in illustration. Also, symbols affixed to voltages, currents, or resistances can be used as indications of respective voltage values, current values, or resistance values as occasion demands.

[0015] In the present specification, "a state in which a member A is connected to a member B" includes a case in which the member A and the member B are physically directly connected to each other, as well as a case in which the member A and the member B are connected indirectly to each other through another member that does not affect an electric connection state therebetween. Likewise, "a state in which a member C is disposed between the member A and the member B" includes a case in which the member A and the member C, or the member B and the member C are connected directly to each other, as well as a case in which those members are connected indirectly to each other through another member that does not affect an electric connection state therebetween.

[0016] A semiconductor light source control device according to an embodiment generates a drive current that flows in a plurality of semiconductor light sources connected in series, that is, LEDs. A bypass switch is disposed in parallel to each of the LEDs. When the bypass switch turns on (off), a corresponding LED turns on (off). A bypass connection line is disposed between a connection node between two adjacent LEDs, and a connection node between two corresponding bypass switches. The semiconductor light source control device is configured such that when a disconnection or contact failure is generated in the bypass connection line, the two bypass switches connected by the bypass connection line are forcedly turned on. With this configuration, when the poor continuity is thus generated, the associated LEDs can be turned off.

[0017] FIG. 1 is a circuit diagram illustrating a configuration of a semiconductor light source control device 100 and members connected to the semiconductor light source control device 100 according to the embodiment. The semiconductor light source control device 100 supplies a drive current Iout to a plurality (N) of in-vehicle LEDs 2-1 to 2-N which is connected in series with each other, and turns on those LEDs 2-1 to 2-N. N is a natural number of 2 or larger. The semiconductor light source control device 100 and the N LEDs 2-1 to 2-N are mounted in a vehicle lighting device such as headlights. The semiconductor light source control device 100 is connected to an in-vehicle battery 6 and a power switch 8.

[0018] The in-vehicle battery 6 generates a battery voltage (supply voltage) Vbat of 12V (or 24V) DC. The power switch 8 is a relay switch configured to control the on/off operation of the overall N LEDs 2-1 to 2-N, and connected in series with the in-vehicle battery 6. When the power switch 8 turns on, the battery voltage Vbat is applied to the semiconductor light source control device 100 from a positive terminal of the in-vehicle battery 6 as an input voltage. A negative terminal of the in-vehicle battery 6 is connected to a fixed voltage terminal, that is, grounded.

[0019] The LEDs 2-1 to 2-N are connected in parallel to electrostatic protection zener diodes 252-1 to 252-N in an opposite direction, respectively. That is, a cathode of the first electrostatic protection zener diode 252-1 is connected to an anode of the first LED 2-1, and an anode of the first electrostatic protection zener diode 252-1 is connected to a cathode of the first LED 2-1. The same is applied to the second electrostatic protection zener diodes 252-2 to the Nth electrostatic protection zener diodes 252-N. The electrostatic protection zener diodes 252-1 to 252-N protect the corresponding LEDs 2-1 to 2-N from being broken down by static electricity.

[0020] The semiconductor light source control device 100 includes a switching regulator, that is, a flyback regulator 102, a downconverter 104, a control circuit 106, a current detection resistor 108, N bypass circuits 270-1 to 270-N, and a bypass driver circuit 112. The control circuit 106 controls the flyback regulator 102 and the downconverter 104, and includes a flyback driver circuit 134, a downconverter driver circuit 136, and a hysteresis width setting circuit 138. The bypass driver circuit 112 is realized by a microcomputer.

[0021] The flyback regulator 102 is formed of a voltage regulator, and converts the input battery voltage Vbat into a target voltage Vt, and outputs the target voltage Vt. Since an output terminal on a high potential side of the flyback regulator 102 is on a ground side, the target voltage Vt is a voltage to be applied to the output terminal on a low potential side of the flyback regulator 102, and has a negative polarity. The flyback regulator 102 includes an input capacitor 114, a first switching element 116, an input transformer 124, an output diode 126, an output capacitor 128, a voltage detection diode 130, and a voltage detection capacitor 132.

[0022] The input capacitor 114 is disposed in parallel to the in-vehicle battery 6, and smooths the battery voltage Vbat. More specifically, the input capacitor 114 is disposed in the vicinity of the input transformer 124, and performs a function of smoothing a voltage in the switching operation of the flyback regulator 102.

[0023] A primary winding 118 of the input transformer 124 and the first switching element 116 are connected in series, and the series circuit is connected in parallel to the input capacitor 114 with respect to the in-vehicle battery 6. For example, the first switching element 116 is formed of an N-channel MOSFET (metal oxide semiconductor field effect transistor). One end of a secondary winding 120 of the input transformer 124 is connected to one end of the output capacitor 128, and the other end of the secondary winding 120 is connected to an anode of the output diode 126. The other end of the output capacitor 128 is connected to a cathode of the output diode 126. One end of the output capacitor 128 is connected to the output terminal on a low potential side of the flyback regulator 102, and is applied with the target voltage Vt. The other end of the output capacitor 128 is connected to the output terminal on the high potential side of the flyback regulator 102.

[0024] A control terminal (gate) of the first switching element 116 is supplied with an upstream control signal S1 having a rectangular waveform which is generated by the flyback driver circuit 134. The first switching element 116 turns on when the upstream control signal S1 is asserted, that is, high level, and turns off when the upstream control signal S1 is negated, that is, low level.

[0025] A voltage detection winding 122 of the input transformer 124, the voltage detection diode 130, and the voltage detection capacitor 132 configure a positive voltage detector circuit for detecting a magnitude of the target voltage Vt as a positive voltage. One end of the voltage detection winding 122 is grounded, and the other end thereof is connected to an anode of the voltage detection diode 130. A cathode of the voltage detection diode 130 is connected to one end of the voltage detection capacitor 132. The other end of the voltage detection capacitor 132 is grounded. One end of

the voltage detection capacitor 132 is applied with a positive voltage corresponding to an absolute value of the target voltage V_t . This voltage is applied to the flyback driver circuit 134 as a detected voltage V_d .

[0026] The flyback driver circuit 134 conducts a voltage feedback control for keeping a substantially constant target voltage V_t on the basis of the detected voltage V_d . The flyback driver circuit 134 adjusts a frequency or a duty ratio of the upstream control signal S_1 so that the target voltage V_t comes close to a set voltage of, for example, about -100V.

[0027] The downconverter 104 is disposed downstream of the flyback regulator 102, and includes a second switching element 140, a flywheel diode 142, and an inductor 144, but does not include an output voltage smoothing capacitor.

[0028] The second switching element 140 is formed of, for example, an N-channel MOSFET. A control terminal of the second switching element 140 is supplied with a downstream control signal S_2 of a rectangular waveform which is generated by the downconverter driver circuit 136. The second switching element 140 turns on when the downstream control signal S_2 is high level, and turns off when the downstream control signal S_2 is low level. A drain of the second switching element 140 is connected to the output terminal on a high potential side of the output capacitor 128, that is, the high potential side of the flyback regulator 102. A source of the second switching element 140 is connected to a cathode of the flywheel diode 142.

[0029] An anode of the flywheel diode 142 is connected to one end of the inductor 144. A connection node between the anode of the flywheel diode 142 and one end of the inductor 144 is connected to the output terminal on the low potential side of the output capacitor 128, that is, on the low potential side of the flyback regulator 102. The other end of the inductor 144 is connected to the cathode sides of the N LEDs 2-1 to 2-N.

[0030] The current detection resistor 108 is disposed on a route of the drive current I_{out} . One end of the current detection resistor 108 is connected to a connection node between the source of the second switching element 140 and the cathode of the flywheel diode 142. The other end of the current detection resistor 108 is grounded, and also connected to the anode side of the N LEDs 2-1 to 2-N. A voltage drop V_m proportional to the drive current I_{out} is generated in the current detection resistor 108.

[0031] Since the anode side of the N LEDs 2-1 to 2-N is grounded, the cathode side of the N LEDs 2-1 to 2-N, that is, the other end of the inductor 144 is applied with a drive voltage V_{out} of a negative polarity. In the normal light-up state, the drive voltage V_{out} becomes a negative voltage having a magnitude corresponding to (the number of LEDs that are in a light emitting state (= a state in which corresponding bypass switches are off)) $\times$ (forward drop voltage V_f of one LED).

[0032] The downconverter driver circuit 136 conducts a current feedback control for allowing the drive current I_{out} to fall within a given current range on the basis of the voltage drop V_m . The downconverter driver circuit 136 turns off the second switching element 140 if the magnitude of the drive current I_{out} exceeds a given current upper limit value I_{th1} . The downconverter driver circuit 136 turns on the second switching element 140 if the magnitude of the drive current I_{out} falls below a current lower limit value I_{th2} smaller than the current upper limit value I_{th1} . The downconverter driver circuit 136 sets the downstream control signal S_2 to the low level if the magnitude of the drive current I_{out} exceeds the current upper limit value I_{th1} . The downconverter driver circuit 136 sets the downstream control signal S_2 to the high level if the magnitude of the drive current I_{out} falls below the current lower limit value I_{th2} .

[0033] The hysteresis width setting circuit 138 sets a hysteresis width ΔI which is a difference between the current upper limit value I_{th1} and the current lower limit value I_{th2} , on the basis of the drive voltage V_{out} . The hysteresis width setting circuit 138 increases the hysteresis width ΔI more as an absolute value of the drive voltage V_{out} becomes larger if the absolute value of the drive voltage V_{out} falls below a voltage threshold value V_{th} smaller than the absolute value of the target voltage V_t . The hysteresis width setting circuit 138 decreases the hysteresis width ΔI more as the absolute value of the drive voltage V_{out} becomes larger if the absolute value of the drive voltage V_{out} exceeds the voltage threshold value V_{th} .

[0034] FIG. 2 is a circuit diagram illustrating a configuration of the hysteresis width setting circuit 138. The hysteresis width setting circuit 138 includes a first operational amplifier 146, a first diode 148, a first resistor 150, a second resistor 152, a third resistor 154, a fourth resistor 156, a fifth resistor 158, and a reference voltage source 160. One end of the third resistor 154 is applied with a positive control supply voltage V_{cc} . The other end of the third resistor 154 is connected with one end of the second resistor 152, one end of the fifth resistor 158, and one end of the fourth resistor 156. The other end of the fourth resistor 156 is grounded. The other end of the fifth resistor 158 is applied with the drive voltage V_{out} . The other end of the second resistor 152 is connected to an inverting input terminal of the first operational amplifier 146. The inverting input terminal of the first operational amplifier 146 is connected to an anode of the first diode 148 through the first resistor 150. A cathode of the first diode 148 is connected with an output terminal of the first operational amplifier 146. A non-inverting input terminal of the first operational amplifier 146 is applied with a reference voltage V_{ref} which is generated by the reference voltage source 160. A voltage applied to the anode of the first diode 148 is called "offset voltage V_{offset} ". As will be described later, the offset voltage V_{offset} corresponds to the hysteresis width ΔI , and the hysteresis width ΔI becomes larger as the offset voltage V_{offset} is higher.

[0035] In resistance values around the first operational amplifier 146, values of the first resistor 150 and the second resistor 152 which determine a gain are set to be sufficiently larger than values of the third resistor 154, the fourth resistor

156, and the fifth resistor 158 which are differentials from the reference voltage V_{ref} so that a feedback current does not affect the differentials from the reference voltage V_{ref} .

[0036] FIG. 3 is a graph illustrating a relationship between the absolute value of the drive voltage V_{out} and the offset voltage V_{offset} . When the absolute value of the drive voltage V_{out} having the negative polarity is small, because a voltage across a common connection node of the third resistor 154, the fourth resistor 156, and the fifth resistor 158 is larger than the reference voltage V_{ref} , the first operational amplifier 146 conducts a current sink, and the offset voltage V_{offset} becomes small. The offset voltage V_{offset} becomes maximum when the voltage across the common connection node becomes equal to the reference voltage V_{ref} .

[0037] In order to realize a control that the hysteresis width ΔI , that is, the offset voltage V_{offset} becomes maximum when the absolute value of the drive voltage V_{out} becomes the voltage threshold value V_{th} , the reference voltage V_{ref} is set to the voltage across the common connection node when the absolute value of the drive voltage V_{out} is equal to the voltage threshold value V_{th} . In particular, when the set value of the flyback regulator 102 is -100V, the reference voltage V_{ref} is set to the voltage across the common connection node when the drive voltage $V_{out} = -V_{th} = -50V$ is satisfied.

[0038] When the absolute value of the drive voltage V_{out} becomes larger than the voltage threshold value V_{th} , the action of the first operational amplifier 146 is disabled, and the voltage across the common connection node becomes the offset voltage V_{offset} as it is. The hysteresis width setting circuit 138 transmits the offset voltage V_{offset} that is changed into an inverted V-shape responsive to the absolute value of the drive voltage V_{out} to the downconverter driver circuit 136 to control the hysteresis width ΔI , and allows a switching frequency of the downconverter 104 to fall within a given range.

[0039] FIG. 4 is a circuit diagram illustrating a configuration of the downconverter driver circuit 136. The downconverter driver circuit 136 includes a second operational amplifier 162, a comparator 164, a gate driver 166, a first current mirror circuit 170, a seventh resistor 172, an eighth resistor 174, a tenth resistor 178, a twelfth resistor 182, a thirteenth resistor 184, a first npn bipolar transistor 190, a third switching element 202, a fourth switching element 204, and a second current mirror circuit 206.

[0040] A non-inverting input terminal of the second operational amplifier 162 is applied with the offset voltage V_{offset} . An output terminal of the second operational amplifier 162 is connected to a base of the first npn bipolar transistor 190, and an inverting input terminal of the second operational amplifier 162 is connected with an emitter of the first npn bipolar transistor 190. One end of the eighth resistor 174 is connected to the emitter of the first npn bipolar transistor 190, and the other end of the eighth resistor 174 is grounded. A collector of the first npn bipolar transistor 190 is connected to the first current mirror circuit 170 through the seventh resistor 172.

[0041] The first current mirror circuit 170 includes a sixth resistor 168, a ninth resistor 176, an eleventh resistor 180, a first pnp bipolar transistor 192, a second pnp bipolar transistor 194, and a third pnp bipolar transistor 196. Those circuit elements are connected to each other to configure a known current mirror circuit. The first current mirror circuit 170 receives a current that flows in the seventh resistor 172, and outputs a current that flows in the tenth resistor 178, and a current that flows in the third switching element 202, and makes a magnitude of the input current substantially equal to a magnitude of the output current.

[0042] The second current mirror circuit 206 includes a fourteenth resistor 186, a fifteenth resistor 188, a second npn bipolar transistor 198, and a third npn bipolar transistor 200. Those circuit elements are connected to each other to configure a known current mirror circuit. The second current mirror circuit 206 receives a current that flows in the tenth resistor 178, and outputs a current that flows in the fourth switching element 204, and makes a magnitude of the input current substantially equal to a magnitude of the output current.

[0043] The third switching element 202 is formed of, for example, a p-channel MOSFET. The fourth switching element 204 is formed of, for example, an n-channel MOSFET. A source of the third switching element 202 is connected to the first current mirror circuit 170. A gate of the third switching element 202 is connected to an inverting output terminal of the comparator 164. A drain of the third switching element 202 is connected to a drain of the fourth switching element 204. A gate of the fourth switching element 204 is connected to the inverting output terminal of the comparator 164. A source of the fourth switching element 204 is connected to the second current mirror circuit 206.

[0044] The twelfth resistor 182 and the thirteenth resistor 184 are connected in series between the control supply voltage V_{cc} and the ground potential in the stated order. A connection node between the twelfth resistor 182 and the thirteenth resistor 184 is connected to a connection node between a drain of the third switching element 202 and a drain of the fourth switching element 204. The connection node between the drain of the third switching element 202 and the drain of the fourth switching element 204 is connected to the non-inverting input terminal of the comparator 164. The inverting input terminal of the comparator 164 is applied with a voltage drop V_m .

[0045] A non-inverting output terminal of the comparator 164 is connected to the gate driver 166. The gate driver 166 matches a phase of the downstream control signal S_2 with a phase of a signal that appears in the non-inverting output terminal of the comparator 164. That is, the gate driver 166 sets the downstream control signal S_2 to high level (low level) when the signal appearing in the non-inverting output terminal of the comparator 164 become high level (low level).

[0046] The second operational amplifier 162 and the first npn bipolar transistor 190 which receive the offset voltage

Voffset output a current of $V_{offset}/(\text{resistance value of the eighth resistor } 174)$. This current is sunk or sourced into a voltage division node between the twelfth resistor 182 and the thirteenth resistor 184 by a phase of an output of the comparator 164 that receives the voltage drop V_m . In the third switching element 202 and the fourth switching element 204 configuring a bridge, at timing when a gate of the second switching element 140 is high level (second switching element 140 is on), the third switching element 202 turns on, and a voltage at the voltage division node between the twelfth resistor 182 and the thirteenth resistor 184 is raised to set the current upper limit value I_{th1} . When the drive current I_{out} is raised, and reaches the current upper limit value I_{th1} , the fourth switching element 204 turns on at substantially the same time when the gate of the second switching element 140 becomes low level (the second switching element 140 is off). The voltage at the voltage division node between the twelfth resistor 182 and the thirteenth resistor 184 is lowered to set the current lower limit value I_{th2} .

[0047] A mean value of the drive current I_{out} is set by a divided voltage between the twelfth resistor 182 and the thirteenth resistor 184. Also, because the sink/source current becomes larger as the absolute value of the drive voltage V_{out} is closer to the voltage threshold value V_{th} due to the action of the hysteresis width setting circuit 138, the current upper limit value I_{th1} - the current lower limit value I_{th2} = the hysteresis width ΔI becomes larger. The hysteresis width ΔI is smaller as the absolute value of the drive voltage V_{out} is farther from the voltage threshold value V_{th} . As will be described later, this acts so that the switching frequency of the downconverter 104 falls within a given range.

[0048] Returning to FIG. 1, the semiconductor light source control device 100 is configured to control the N LEDs 2-1 to 2-N to turn on/off, individually. The bypass driver circuit 112 generates N lighting on/off control signals Sc_1 to Sc_N for controlling the on/off operation of the respective LEDs 2-1 to 2-N. The bypass driver circuit 112 controls the levels of the respective N lighting on/off control signals Sc_1 to Sc_N so as to obtain a desired brightness or light distribution pattern, individually. Specifically, the bypass driver circuit 112 sets the first lighting on/off control signal Sc_1 to low level when the first LED 2-1 is turned on, and sets the first lighting on/off control signal Sc_1 to high level when the first LED 2-1 is turned off. The same is applied to the second lighting on/off control signal Sc_2 to the N^{th} lighting on/off control signal Sc_N . The bypass driver circuit 112 outputs the respective lighting on/off control signals Sc_1 to Sc_N to the corresponding bypass circuits 270-1 to 270-N.

[0049] The first bypass circuit 270-1 to the N^{th} bypass circuit 270-N are connected in parallel to the first LED 2-1 to the N^{th} LED 2-N, respectively. The first bypass circuit 270-1 to the N^{th} bypass circuit 270-N are connected in series between a high potential side output terminal and a low potential side output terminal of the downconverter 104 in the stated order.

[0050] The first bypass circuit 270-1 performs electric continuity between both ends of the first LED 2-1, that is, connects both ends of the first LED 2-1 to each other by an impedance lower than that of the first LED 2-1 when the first lighting on/off control signal Sc_1 is high level. With this configuration, the first LED 2-1 is turned off. Hereinafter, a state of the bypass circuits that turn off the LEDs is called "bypass-on state". The first bypass circuit 270-1 connects both ends of the first LED 2-1 to each other by an impedance higher than that of the first LED 2-1 when the first lighting on/off control signal Sc_1 is low level. With this configuration, the first LED 2-1 turns on. Hereinafter, a state of the bypass circuits that turn on the LEDs is called "bypass-off state".

[0051] The first bypass circuit 270-1 generates a first abnormality detection signal S_{det1} for detecting the abnormality of the first LED 2-1 and lines around the first LED 2-1, and supplies the first abnormality detection signal S_{det1} to the bypass driver circuit 112. If the first abnormality detection signal S_{det1} is high level, a voltage to be applied to the first bypass circuit 270-1 when the first bypass circuit 270-1 is in the bypass-off state is lower than a short-circuit detection voltage, or higher than a disconnection detection voltage higher than the short-circuit detection voltage. The short-circuit detection voltage is set to be lower than the forward drop voltage V_f of one LED. The disconnection detection voltage is set to be higher than the forward drop voltage V_f of the LED, and lower than a sum $2V_f$ of the forward drop voltages of two LEDs.

[0052] Similarly, the second bypass circuit 270-2 to the N^{th} bypass circuit 270-N control the on/off state of the second LEDs 2-2 to the N^{th} LED 2-N on the basis of the second lighting on/off control signals Sc_2 to the N^{th} lighting on/off control signal Sc_N , respectively. Also, the second bypass circuit 270-2 to the N^{th} bypass circuit 270-N generate second abnormality detection signal S_{det2} to N^{th} abnormality detection signal S_{detN} , respectively, and supply those abnormality detection signals to the bypass driver circuit 112.

[0053] When the brightness of the first LED 2-1 is dimmed in the normal light-up state, the bypass driver circuit 112 changes the first lighting on/off control signal Sc_1 at a dimming frequency f_1 of several hundred Hz to several kHz cyclically, that is, in a rectangular waveform. The first LED 2-1 blinks at the dimming frequency f_1 by the pulse modulation of the first lighting on/off control signal Sc_1 , and the brightness visible by human's eyes is dimmed. A duty ratio of the first lighting on/off control signal Sc_1 is set to obtain a desired degree of light mission. In this case, since a variation in a magnitude of the driver circuit that flows in the first LED 2-1 when the turning on the first LED 2-1 is suppressed, color shift is suppressed. Similarly, the bypass driver circuit 112 has a PWM (pulse width modulation) dimming function for the respective second LED 2-2 to N^{th} LED 2-N.

[0054] The bypass driver circuit 112 determines whether an abnormality is generated in the first LED 2-1 and the lines

around the first LED 2-1, or not, on the basis of the first abnormality detection signal Sdet1. The bypass driver circuit 112 determines that the abnormality is generated when the first abnormality detection signal Sdet1 becomes high level, and forcibly sets the first lighting on/off control signal Sc1 to the high level. For example, the bypass driver circuit 112 keeps the first lighting on/off control signal Sc1 in the high level, even in a period when the first lighting on/off control signal Sc1 is to be set to the low level according to the PWM dimming function. Alternatively, the bypass driver circuit 112 sets the first lighting on/off control signal Sc1 to the high level, even in a period when the first lighting on/off control signal Sc1 is to be set to the low level if it is not determined that the abnormality is generated. The bypass driver circuit 112 also has the same abnormality detection function for the respective second LED 2-2 to Nth LED 2-N.

[0055] A first bypass connection line 280-1 connects a first bypass side connection node NB1 between the first bypass circuit 270-1 and the second bypass circuit 270-2, and a first load side connection node NL1 between the first LED 2-1 and the second LED 2-2. When the first bypass circuit 270-1 is in the bypass-off state, and the second bypass circuit 270-2 is in the bypass-on state, the polarity of the drive current Iout flowing in the first bypass connection line 280-1 trends from a load side toward a bypass side. When the first bypass circuit 270-1 is in the bypass-on state, and the second bypass circuit 270-2 is in the bypass-off state, the polarity of the drive current Iout flowing in the first bypass connection line 280-1 trends from the bypass side toward the load side. Therefore, the polarity of the drive current Iout flowing in the first bypass connection line 280-1 in the former case is opposite to the polarity of the drive current Iout flowing in the first bypass connection line 280-1 in the latter case.

[0056] The same is applied to the second bypass connection line 280-2 to (N-1)th bypass connection line 280-(N-1).

[0057] If the poor continuity is generated in the bypass connection line, the bypass driver circuit 112, and the first bypass circuit 270-1 to the Nth bypass circuit 270-N are configured so that both of the two bypass circuits connected to the bypass connection lines are forcibly brought into the bypass-on state.

[0058] FIG. 5 is a circuit diagram illustrating configurations of the second bypass circuit 270-2 and the third bypass circuit 270-3. The second bypass circuit 270-2 includes a second switch level shift circuit 254-2, a second bypass/limiter circuit 250-2, a second disconnection detector circuit 272-2, a second short-circuiting detector circuit 274-2, a second detection signal level shift circuit 276-2, and a second integrating circuit 278-2.

[0059] The second switch level shift circuit 254-2 receives the second lighting on/off control signal Sc2 from the bypass driver circuit 112, and converts the second lighting on/off control signal Sc2 into a second bypass switch drive signal Sd2 with a voltage across the cathode of the second LED 2-2 as a standard, that is, a low level. A phase of the second bypass switch drive signal Sd2 matches a phase of the second lighting on/off control signal Sc2, and the low level of the second bypass switch drive signal Sd2 becomes the voltage of the cathode of the second LED 2-2. Thus, the second switch level shift circuit 254-2 shifts the level of the second lighting on/off control signal Sc2, and supplies the signal to the corresponding second bypass/limiter circuit 250-2.

[0060] The second bypass/limiter circuit 250-2 includes a second bypass switch 110-2 which is connected in parallel to the second LED 2-2. If the second bypass switch drive signal Sd2 is high level (low level), the second bypass/limiter circuit 250-2 turns on (off) the second bypass switch 110-2 to turn on (off) the second LED 2-2. Further, when the second bypass switch drive signal Sd2 is low level, the second bypass/limiter circuit 250-2 is configured to limit an upper limit of a voltage between both ends of the second bypass switch 110-2 with the use of the second bypass switch 110-2.

[0061] The second bypass/limiter circuit 250-2 includes a limiter zener diode 256, a backflow prevention diode 258, a sixteenth resistor 260, and the second bypass switch 110-2. The second bypass switch 110-2 is formed of, for example, an N-channel MOSFET.

[0062] A cathode of the limiter zener diode 256 is connected to a drain of the second bypass switch 110-2. A connection node therebetween is connected to the first bypass connection line 280-1. An anode of the limiter zener diode 256 is connected to an anode of the backflow prevention diode 258. The second bypass switch drive signal Sd2 is input to a gate of the second bypass switch 110-2 through the sixteenth resistor 260. A source of the second bypass switch 110-2 is connected to the second bypass connection line 280-2.

[0063] A series circuit of the limiter zener diode 256 and the backflow prevention diode 258 is connected to the gate side of the second bypass switch 110-2 with respect to the second bypass switch drive signal Sd2 that turns on/off the second bypass switch 110-2. That is, a cathode of the backflow prevention diode 258 is connected between the sixteenth resistor 260 and the gate of the second bypass switch 110-2.

[0064] If it is assumed that a zener voltage of the limiter zener diode 256 is 6V, the forward drop voltage Vf of the backflow prevention diode 258 is 0.5V, and a gate threshold voltage of the second bypass switch 110-2 is 2.5V, when the voltage between both ends of the second bypass switch 110-2, that is, a drain-source voltage reaches 9V, the second bypass switch 110-2 starts to turn on. Therefore, an upper limit value of the voltage between both ends of the second bypass switch 110-2, that is, the disconnection detection voltage becomes 9V.

[0065] The zener voltage of the limiter zener diode 256 is set so that the disconnection detection voltage becomes higher than a maximum value of the forward drop voltage Vf of the second LED 2-2, becomes lower than the zener voltage defined by the second electrostatic protection zener diodes 252-2, and becomes lower than a sum of the forward drop voltage Vf of the second LED 2-2, and the forward drop voltage Vf of the third LED 2-3. For example, if the respective

LEDs have substantially the same characteristics, when the maximum of the forward drop voltage V_f of the LEDs is 6V, and the zener voltage of the second electrostatic protection zener diodes 252-2 is 20V, the zener voltage of the limiter zener diode 256 is set to range from 3V to 9V.

[0066] The backflow prevention diode 258 is configured to prevent the second bypass switch drive signal S_d2 from inhibiting the on/off operation of the second bypass switch 110-2. For example, when the second LED 2-2 that is connected in parallel to the backflow prevention diode 258 is turned off, or the second bypass switch 110-2 is forcedly turned on as measures against the disconnection or the contact failure which will be described later, if there is no backflow prevention diode 258, the gate voltage of the second bypass switch 110-2 is reduced through the second bypass switch 110-2 which is in the on-state from a forward direction of the limiter zener diode 256. The backflow prevention diode 258 prevents this status from occurring.

[0067] The second disconnection detector circuit 272-2 determines whether the poor continuity is generated on a route of the drive current I_{out} that passes through the second LED 2-2, or not, when the second bypass switch 110-2 is off (that is, non-conduction state). The second short-circuiting detector circuit 274-2 determines whether a short-circuiting abnormality is generated in the second LED 2-2 or between the lines when the second bypass switch 110-2 is off, or not. If the abnormality is detected in the second disconnection detector circuit 272-2 or the second short-circuiting detector circuit 274-2, an integration capacitor 282 of the second integrating circuit 278-2 is charged by a first time constant through the second detection signal level shift circuit 276-2. This charging operation is continued in a period when the second bypass switch drive signal S_d2 is low level, and the abnormality is detected in the second disconnection detector circuit 272-2 or the second short-circuiting detector circuit 274-2. In other periods, the integration capacitor 282 is discharged by a second time constant longer than the first time constant.

[0068] The second detection signal level shift circuit 276-2 includes a seventeenth resistor 284, an eighteenth resistor 286, and a fourth pnp bipolar transistor 288. One end of the seventeenth resistor 284 is connected to an emitter of the fourth pnp bipolar transistor 288. A connection node therebetween is applied with the control supply voltage V_{cc} . The other end of the seventeenth resistor 284 is connected to one end of the eighteenth resistor 286. A connection node therebetween is connected to a base of the fourth pnp bipolar transistor 288.

[0069] The second disconnection detector circuit 272-2 includes a 23rd resistor 210, and a sixth npn bipolar transistor 212. A collector of the sixth npn bipolar transistor 212 is connected to the other end of the eighteenth resistor 286. A base of the sixth npn bipolar transistor 212 is connected to the connection node between the anode of the limiter zener diode 256 and the anode of the backflow prevention diode 258 through the 23rd resistor 210. An emitter of the sixth npn bipolar transistor 212 is connected to the second bypass connection line 280-2.

[0070] The second short-circuiting detector circuit 274-2 includes a nineteenth resistor 290, a twenty resistor 292, a 21st resistor 294, a 22nd resistor 296, a fourth npn bipolar transistor 298, and a fifth npn bipolar transistor 208. The twenty resistor 292 and the 22nd resistor 296 are connected in series between the first bypass connection line 280-1 and the second bypass connection line 280-2 in the stated order. A connection node between the twenty resistor 292 and the 22nd resistor 296 is connected to one end of the 21st resistor 294 and a base of the fourth npn bipolar transistor 298. The other end of the 21st resistor 294 is connected to the cathode of the backflow prevention diode 258. An emitter of the fourth npn bipolar transistor 298 is connected to the second bypass connection line 280-2. A collector of the fourth npn bipolar transistor 298 is connected to one end of the nineteenth resistor 290. The other end of the nineteenth resistor 290 is applied with the control supply voltage V_{cc} . A connection node between the collector of the fourth npn bipolar transistor 298 and the nineteenth resistor 290 is connected to the base of the fifth npn bipolar transistor 208. The emitter of the fifth npn bipolar transistor 208 is connected to the second bypass connection line 280-2, and a collector of the fifth npn bipolar transistor 208 is connected to the other end of the eighteenth resistor 286.

[0071] The second integrating circuit 278-2 includes the integration capacitor 282, a 24th resistor 214, and a 25th resistor 216. One end of the 24th resistor 214 is grounded to a ground potential which is substantially equal to a ground potential of a microcomputer, and the other end of the 24th resistor 214 is connected to one end of the 25th resistor 216. A connection node between the 24th resistor 214 and the 25th resistor 216 is connected to a collector of the fourth pnp bipolar transistor 288. The other end of the 25th resistor 216 is connected to one end of the integration capacitor 282. The other end of the integration capacitor 282 is grounded to a ground potential which is substantially equal to the ground potential of the microcomputer. A voltage across one end of the integration capacitor 282 is applied to the bypass driver circuit 112 as the second abnormality detection signal S_{det2} .

[0072] If the poor continuity is generated on the route of the drive current I_{out} , the voltage between both ends of the second bypass switch 110-2 is raised over the forward drop voltage V_f during the off-period of the second bypass switch 110-2. If the voltage between both ends thereof exceeds the disconnection detection voltage, a current flows into the limiter zener diode 256. Then, the sixth npn bipolar transistor 212 of the second disconnection detector circuit 272-2 turns on.

[0073] Also, if the second LED 2-2 is short-circuited, the voltage between both ends of the second bypass switch 110-2 becomes lower than the forward drop voltage V_f during the off-period of the second bypass switch 110-2. If the voltage between both ends thereof becomes lower than a short-circuit detection voltage, the fourth npn bipolar transistor

298 of the second short-circuiting detector circuit 274-2 turns off, and the fifth npn bipolar transistor 208 turns on. The respective resistance values of the twenty resistor 292, the 21st resistor 294, and the 22nd resistor 296 are set to satisfy the following three conditions.

- (1) When the other end of the 21st resistor 294 is supplied with the signal of the high level, the fourth npn bipolar transistor 298 turns on.
- (2) When the other end of the 21st resistor 294 is supplied with the signal of the low level, and the voltage between both ends of the second bypass switch 110-2 is the short-circuit detection voltage or higher, the fourth npn bipolar transistor 298 turns on.
- (3) When the other end of the 21st resistor 294 is supplied with the signal of the low level, and the voltage between both ends of the second bypass switch 110-2 is lower than the short-circuit detection voltage, the fourth npn bipolar transistor 298 turns off.

[0074] When any one of the sixth npn bipolar transistor 212 and the fifth npn bipolar transistor 208 turns on, the fourth npn bipolar transistor 288 of the second detection signal level shift circuit 276-2 turns on. The control supply voltage Vcc is a positive voltage with the ground potential of the microcomputer as a standard. If an abnormality is detected in the second disconnection detector circuit 272-2 or the second short-circuiting detector circuit 274-2, the control supply voltage Vcc is applied to the second integrating circuit 278-2. The integration capacitor 282 is charged through the 25th resistor 216, and discharged through the 24th resistor 214 and the 25th resistor 216. When a resistance value of the 24th resistor 214 is set to be larger than a resistance value of the 25th resistor 216, the abnormality can be detected even in a dimming state where a period (that is, off-period of the second bypass switch 110-2) for abnormality detection is short such as a mean current 10% light-up (on state of the second bypass switch 110-2 is 90%, off state thereof is 10%).

[0075] The third bypass circuit 270-3 is configured in the same manner as that of the second bypass circuit 270-2. The third bypass circuit 270-3 includes a third switch level shift circuit 254-3 corresponding to the second switch level shift circuit 254-2, a third bypass/limiter circuit 250-3 corresponding to the second bypass/limiter circuit 250-2, a third disconnection detector circuit 272-3 corresponding to the second disconnection detector circuit 272-2, a third short-circuiting detector circuit 274-3 corresponding to the second short-circuiting detector circuit 274-2, a third detection signal level shift circuit 276-3 corresponding to the second detection signal level shift circuit 276-2, and a third integrating circuit 278-3 corresponding to the second integrating circuit 278-2.

[0076] The first bypass circuit 270-1, the fourth bypass circuit 270-4 to the Nth bypass circuit 270-N are configured in the same manner as that of the second bypass circuit 270-2.

[0077] The operation of the semiconductor light source control device 100 configured as described above will be described.

FIGS. 6A to 6C are graphs illustrating a time variation of the drive current Iout. Let us consider a status in which only one LED is first turned on, about half of the LEDs are then turned on, and all of the LEDs are thereafter turned on. In this case, the PWM dimming is not considered. FIG. 6A illustrates a time variation of the drive current Iout when only one LED is turned on, and the remaining (N-1) LEDs are turned off by turning on the corresponding bypass switches. FIG. 6B illustrates a time variation of the drive current Iout when about half of the LEDs, that is N/2 LEDs are turned on, and the remaining LEDs are turned off. FIG. 6C illustrates a time variation of the drive current Iout when all of the LEDs are turned on.

[0078] FIGS. 6A to 6C illustrate a case in which the hysteresis width ΔI is adjusted so that the switching frequency, that is, a switching cycle Ts of the second switching element 140 is kept substantially constant, without depending on the number of lighting of the LEDs and the number of extinction of the LEDs. However, an ordinary skilled person that reads the present invention would understand that, in this embodiment, the hysteresis width ΔI is so controlled as to suppress a change in the switching cycle Ts caused by a change in the number of lighting of the LEDs and the number of extinction of the LEDs.

[0079] Referring to FIG. 6A, if the number of lighting of the LEDs is small, the drive current Iout is relatively quickly raised in an on-time Ton of the second switching element 140, and the drive current Iout is relatively slowly lowered in an off-time Toff of the second switching element 140. The hysteresis width in this case is expressed as " $\Delta I1$ ". An absolute value of the drive voltage Vout is relatively low, and the offset voltage Voffset generated by the hysteresis width setting circuit 138 is also relatively low.

[0080] Referring to FIG. 6B, when the number of lighting of the LEDs and the number of extinction of the LEDs are substantially equal to each other, the drive voltage Vout is about half of the setting voltage of the flyback regulator 102, and the on-time Ton and the off-time Toff of the second switching element 140 balance with each other. A speed of the overall change in the drive current Iout is larger than that when the number of lighting of the LEDs is small.

[0081] The hysteresis width setting circuit 138 allows the higher offset voltage Voffset to be generated as illustrated in FIG. 3. The downconverter driver circuit 136 receives the high offset voltage Voffset, and makes a hysteresis width $\Delta I2$ larger than a hysteresis width $\Delta I1$ when the number of lighting of the LEDs is 1. As a result, an increment in the

speed of the overall change of the drive current I_{out} is offset, and the switching cycle T_s is kept substantially constant.

[0082] Referring to FIG. 6C, when the number of extinction of the LEDs is small or null, the drive current I_{out} is relatively slowly raised in the on-time T_{on} of the second switching element 140, and the drive current I_{out} is relatively quickly lowered in the off-time T_{off} of the second switching element 140. The speed of the overall change of the drive current I_{out} becomes smaller than that when the number of lighting of the LEDs and the number of extinction of the LEDs balance with each other. The absolute value of the drive voltage V_{out} is relatively high, and the offset voltage V_{offset} generated by the hysteresis width setting circuit 138 is also relatively low.

[0083] The downconverter driver circuit 136 receives the low offset voltage V_{offset} , and makes a hysteresis width ΔI_3 smaller than the hysteresis width ΔI_2 when the number of lighting of the LEDs and the number of extinction of the LEDs balance with each other. As a result, a decrement in the speed of the overall change of the drive current I_{out} is offset, and the switching cycle T_s is kept substantially constant.

[0084] FIG. 7 is a timing chart illustrating a change in the second bypass switch drive signal S_{d2} and the second abnormality detection signal S_{det2} in a PWM dimming state. In this example, the second bypass switch drive signal S_{d2} corresponds to the mean current 20% lighting. That is, the off-time T_{off} of a period during which the second bypass switch drive signal S_{d2} is low level is about 1/4 of the on-time T_{on} of a period during which the second bypass switch drive signal S_{d2} is high level.

[0085] If no abnormality is generated, the second abnormality detection signal S_{det2} is kept constant in the vicinity of the ground potential of the microcomputer, that is, 0V, without depending on a change in the second bypass switch drive signal S_{d2} . In this case, it is assumed that the poor continuity or the disconnection is generated at a time t_1 during the period when the second bypass switch drive signal S_{d2} is high level. At the time t_1 , since the second bypass switch drive signal S_{d2} is high level, that is, the second bypass switch 110-2 is on (that is, conduction state), both of the sixth npn bipolar transistor 212 and the fifth npn bipolar transistor 208 are kept off as they are. Therefore, the potential of the second abnormality detection signal S_{det2} is not substantially changed.

[0086] At a time t_2 when the second bypass switch drive signal S_{d2} transitions from the high level to the low level, any one of the sixth npn bipolar transistor 212 and the fifth npn bipolar transistor 208 is turned on due to the generated abnormality, and the integration capacitor 282 starts to be charged.

[0087] At a time t_3 during a period when the second bypass switch drive signal S_{d2} is low level, the integration capacitor 282 is fully charged. A voltage of the second abnormality detection signal S_{det2} when the integration capacitor 282 is fully charged is higher than a level threshold value V_g for determining a level of the second abnormality detection signal S_{det2} in the bypass driver circuit 112.

[0088] At a time t_4 when the second bypass switch drive signal S_{d2} transitions from the low level to the high level, both of the sixth npn bipolar transistor 212 and the fifth npn bipolar transistor 208 turn off, and the integration capacitor 282 starts to be discharged.

[0089] After the time t_3 , although the second abnormality detection signal S_{det2} is higher than the level threshold value V_g , an operating speed of the bypass driver circuit 112 which is the microcomputer is relatively low. Therefore, the level transition of the second bypass switch drive signal S_{d2} is continued for a while.

[0090] At a t_5 when the second bypass switch drive signal S_{d2} then transitions from the high level to the low level, if the generated abnormality is continued, the integration capacitor 282 starts to be again charged. Therefore, the integration capacitor 282 is again fully charged.

[0091] The second time constant for the discharge of the integration capacitor 282 is set to be longer than the first time constant for the charge of the integration capacitor 282. Therefore, even in a period between the time t_4 when the second bypass switch drive signal S_{d2} is high level, and the time t_5 , the voltage of the second abnormality detection signal S_{det2} is kept higher than the level threshold value V_g . Thus, after the second bypass switch drive signal S_{d2} has repeated the level transition several times, the bypass driver circuit 112 determines that the second abnormality detection signal S_{det2} has transitioned from the low level to the high level.

[0092] Also, referring to FIG. 7, a case in which the integration capacitor 282 reaches a fully charged state in one off-period of the second bypass switch 110-2 has been described. However, the present invention is not limited to this configuration, but the integration capacitor 282 may come close to the fully charged state every time the off-period is repeated.

[0093] A description will be given of the operation of the semiconductor light source control device 100 when the poor continuity is generated in any one of the first bypass connection line 280-1 to the $(N-1)^{th}$ bypass connection line 280- $(N-1)$. As an example, let us consider a case in which the poor continuity is generated in the second bypass connection line 280-2, that is, a case in which the poor continuity is generated at a portion of a mark "X" indicated by reference numeral 218 shown in FIG. 5.

[0094] If the poor continuity is generated in the second bypass connection line 280-2, the potential of the connection node between the source of the second bypass switch 110-2 and the drain of the third bypass switch 110-3 floats. When both of the second bypass switch 110-2 and the third bypass switch 110-3 are off, the potential of the connection node comes closer to the potential of the source of the second bypass switch 110-2 or the potential of the drain of the third

bypass switch 110-3 due to a difference in a characteristic between the second bypass switch 110-2 and the third bypass switch 110-3. Then, for example, when the potential of the connection node comes sufficiently closer to the potential of the drain of the third bypass switch 110-3, it is determined that short-circuit failure is generated by the third short-circuiting detector circuit 274-3. A third abnormality detection signal Sdet3 becomes high level, and the bypass driver circuit 112

fixes a third lighting on/off control signals Sc3 to the high level.
[0095] Then, the third bypass switch 110-3 turns on, and a voltage between both ends of the second bypass switch 110-2 becomes substantially 2Vf. Since the disconnection detection voltage is lower than 2Vf, the second disconnection detector circuit 272-2 detects that the poor continuity is generated. The second abnormality detection signal Sdet2 becomes high level, and the bypass driver circuit 112 fixes the second lighting on/off control signal Sc2 to the high level.

[0096] As a result of the above, both of the second bypass switch 110-2 and the third bypass switch 110-3 are forcedly turned on to maintain both of the second LED 2-2 and the third LED 2-3 in an extinction state.

[0097] When the potential of the connection node between the source of the second bypass switch 110-2 and the drain of the third bypass switch 110-3 comes close to the potential of the source of the second bypass switch 110-2, the second short-circuiting detector circuit 274-2 detects the short-circuit abnormality, the third disconnection detector circuit 272-3 detects the disconnection abnormality, and both of the second bypass switch 110-2 and the third bypass switch 110-3 are forcedly turned on.

[0098] If the second bypass switch drive signal Sd2 is set to the low level to turn on the second LED 2-2, and the third bypass switch drive signal Sd3 is set to the high level to turn off the third LED 2-3 without forcedly turning on both of those two bypass switches, the third bypass switch 110-3 turns on, and the drive current Iout does not flow into the third bypass switch 110-3, but flows in the third LED 2-3. That is, the third LED 2-3 cannot be turned off. If the second bypass switch drive signal Sd2 is set to the high level, and the third bypass switch drive signal Sd3 is set to the low level, the second bypass switch 110-2 turns on, and the drive current Iout does not flow in the second bypass switch 110-2, but flows in the second LED 2-2. That is, the second LED 2-2 cannot be turned off.

[0099] Thus, if the poor continuity is generated in the second bypass connection line 280-2, it is difficult to control the respective lighting on/off states of the second LED 2-2 and the third LED 2-3, individually.

[0100] In the semiconductor light source control device 100 according to this embodiment, if the poor continuity is generated in any one of the first bypass connection line 280-1 to the (N-1)th bypass connection line 280-(N-1), both of the two bypass switches connected to the bypass connection line in which the poor continuity is generated are forcedly turned on. As a result, both of the two LEDs connected to the bypass connection line are turned off.

[0101] If the poor continuity is generated in the bypass connection line, it is difficult to control the respective lighting on/off states of the two LEDs connected to the bypass connection line, individually, as described above. For example, let us consider a case in which the semiconductor light source control device 100 is intended for the high beam of the vehicle headlights, and the semiconductor light source control device 100 has a function of turning off the appropriate LED so as not to give a preceding vehicle and an oncoming vehicle glare. In this case, if the poor continuity is generated in the bypass connection line connected to the appropriate LED, the appropriate LED cannot be turned off, and the preceding vehicle and the oncoming vehicle may be given glare. Under the circumstances, in this embodiment, if the poor continuity is generated in the bypass connection line, both of the two bypass switches connected to the bypass connection line are forcedly turned on. As a result, the bypass connection line in which the poor continuity is generated becomes irrelevant to a bypass route of the drive current Iout, and the appropriate LED can be maintained in the extinction state. As a result, glaring can be avoided.

[0102] Also, the semiconductor light source control device 100 according to this embodiment has a PWM dimming function of turning on/off the bypass switch at a relative high speed to adjust the brightness of the corresponding LED. When the bypass switch is on, the voltage between both ends of the bypass switch comes close to 0V. However, this is not abnormal, and therefore should not be determined as the short-circuit abnormality. Under the circumstance, the semiconductor light source control device 100 does not conduct the short-circuit abnormality detection and the disconnection abnormality detection when the bypass switch is on, and detects the short-circuit and the disconnection abnormality when the bypass switch is off.

[0103] Therefore, if the abnormality is detected in the PWM dimming LED or the lines, there is a need to determine the abnormality while a state in which the abnormality appears when the bypass switch is off, and a state in which the bypass switch turns on regardless of whether the abnormality is present, or not, are repeated at a high speed. A microcomputer is frequently used as a main device that controls the on/off operation of the LEDs, and the PWM dimming function. Since the microcomputer usually operates at relatively long time intervals such as about several tens msec, the microcomputer is not suited for picking up only the respective abnormalities of a large number of LEDs at a high speed for determination. For example, if the dimming frequency f1 is several kHz, and the LEDs are turned on with the mean current 10%, a length of the off-period of the bypass switch is several hundred micro second order. Thus, in order to determine the abnormality/normality in the relatively short period, there is a need to employ an expensive microcomputer which is relatively high in operating speed.

[0104] Under the circumstance, in the semiconductor light source control device 100 according to this embodiment,

an abnormality detection signal that becomes high level in an abnormal state, and low level in a normal state is generated without depending on the PWM dimming, due to the action of the integrating circuit. The bypass driver circuit 112 that is the microcomputer determines the normality or abnormality on the basis of the abnormality detection signal. As a result, when the PWM dimming function using the bypass switch is employed, the abnormality of the LEDs or the lines can be detected even if the expensive microcomputer is not used.

[0105] Also, according to the semiconductor light source control device 100 of this embodiment, even if the poor continuity such as the contact failure or the disconnection is generated on the route of the drive current Iout, the voltage to be applied to the bypass switch can be prevented from being raised. For example, let us consider a case in which when, for example, the first LED 2-1 is in the lighting state, that is, the first bypass switch 110-1 is off, the contact failure or the disconnection is generated in a line upstream of the connection node between the anode of the first LED 2-1 and the cathode of the first electrostatic protection zener diode 252-1, that is, the line of a mark "X" indicated by reference numeral 262 in the circuit illustrated in FIG. 1.

[0106] When the above contact failure or disconnection is generated, the voltage between both ends of the first bypass switch is raised, and the first abnormality detection signal Sdet1 transitions from the low level to the high level. When the bypass driver circuit 112 detects the above transition of the first abnormality detection signal Sdet1, the bypass driver circuit 112 determines that the abnormality is generated in the first LED 2-1, and the circuit illustrated in FIG. 1 takes a countermeasure to turn on the first bypass switch 110-1 so that the other LEDs can be turned on.

[0107] However, since the operating speed of the bypass driver circuit 112 which is the microcomputer is relatively low as described above, a time of several tens msec to several hundred msec is required for the above countermeasure. In this example, if the semiconductor light source control device has no limiter function of this embodiment, because no output voltage smoothing capacitor is present, a relatively high voltage such as several kV (absolute value) determined according to an energy accumulated in the inductor 144, and a parasitic capacitor of the first bypass switch is output immediately after the above contact failure or disconnection is generated. This high voltage is applied to the first bypass switch before the first bypass switch turns on. Therefore, there is a need to select an element having a withstand voltage of several kV as the first bypass switch, taking the contact failure or the disconnection into account, although only a voltage of several V is normally applied in the lighting state.

[0108] On the contrary, in the semiconductor light source control device 100 having the limiter function according to this embodiment, when the disconnection or the contact failure is generated as described above, the drain-source voltage of the first bypass switch 110-1 is raised. However, a rising of that voltage is limited by the action of the limiter zener diode 256 and the first bypass switch 110-1 per se. Therefore, the element having the lower withstand voltage can be selected as the first bypass switch 110-1 even taking the contact failure or the disconnection into account.

[0109] In this case, when the disconnection or the contact failure is generated, for example, $10\text{V} \times 1\text{A} = \text{about } 10\text{ W}$ is applied to the first bypass switch 110-1 for several ten seconds to several hundred seconds. However, because a device which is small in on-resistance and large in size to some degree originally needs to be used, an influence on the device size and the costs is small.

[0110] For example, let us consider a case in which when, for example, the first LED 2-1 is in the lighting state, that is, the first bypass switch 110-1 is off, the contact failure or the disconnection is generated in a line downstream of the connection node between the anode of the first LED 2-1 and the cathode of the first electrostatic protection zener diode 252-1, that is, the line of a mark "X" indicated by reference numeral 264 in the circuit illustrated in FIG. 1. When the semiconductor light source control device is equipped with no limiter function of this embodiment, most of an energy accumulated in the inductor 144 is consumed by the first electrostatic protection zener diode. As a result, there is a need to select the element that withstands such a large power consumption as the first electrostatic protection zener diode. Also, it is conceivable to employ an element having a zener diode higher than a voltage of several kV which can be generated when the contact failure or the disconnection is generated as the first electrostatic protection zener diode. However, in general, if the element has such a high zener voltage, the element cannot perform an original function of the electrostatic protection.

[0111] On the contrary, in the semiconductor light source control device 100 having the limiter function of this embodiment, the upper limit value of the voltage between both ends of the first bypass switch 110-1 is set to be lower than the zener voltage defined by the first electrostatic protection zener diode 252-1. Therefore, the relatively small zener diode can be selected as the first electrostatic protection zener diode 252-1.

[0112] Similarly, when the same contact failure or disconnection is generated in any one of the second LED 2-2 to the Nth LED 2-N, the upper limit of the voltage to be applied to the corresponding bypass switch or electrostatic protection zener diode is limited. Therefore, the element having the lower withstand voltage can be employed as the corresponding bypass switch, and the relatively small zener diode can be employed as the corresponding electrostatic protection zener diode.

[0113] Also, in the semiconductor light source control device 100 according to this embodiment, the bypass switches for controlling the on/off operation of the LEDs are also used as switches for realizing the limiter function for the voltage between both ends of the LEDs. That is, the bypass switches are shared by the lighting on/off control signal and the

limiter function. As a result, an increase in the number of elements can be suppressed while realizing the lighting on/off control function and the limiter function.

[0114] In the semiconductor light source control device 100 according to this embodiment, since no smoothing capacitor is installed on an output stage of the N LEDs 2-1 to 2-N, the following property of the drive current Iout to the second switching element 140 becomes excellent. In particular, when the second switching element 140 turns off, the drive current Iout becomes small whereas when the second switching element 140 turns on, the drive current Iout becomes large. Then, in order to stabilize the drive current Iout in the vicinity of a target value, the hysteresis control of the drive current Iout is employed instead of smoothing. As a result, a response to a current feedback can be speeded up. For example, when the number of lighting of the LEDs is changed by the action of the bypass driver circuit 112 and the bypass switches, the drive current Iout can more rapidly follow a change in the load. In particular, undershoot of the drive current Iout when the number of lighting of the LEDs is increased, and overshoot of the drive current Iout when the number of lighting of the LEDs is decreased can be suppressed.

[0115] Also, in the semiconductor light source control device 100 according to this embodiment, the upstream flyback regulator 102 is set as a negative output, and the downstream downconverter 104 is also set as the negative output. As a result, the N-channel MOSFET having the more excellent characteristic can be employed as the bypass switch.

[0116] In addition to the above negative outputs, since the inductor 144 is not disposed between the cathode of the flywheel diode 142 and the output, but disposed between the anode thereof and the output, the N-channel MOSFET having the more excellent characteristic can be employed as the second switching element 140 of the downconverter 104. Also, the drive voltage Vout can be stably detected.

[0117] Also, when the semiconductor light source control device has the positive output, the drive current is frequently detected on the high side taking a case in which the LEDs are grounded into account. When the load is changed, since the potential of the detected portion is also changed, it is difficult to precisely detect the drive current. Also, the configuration of the detector circuit may be more complicated. Under the circumstance, in the semiconductor light source control device 100 according to this embodiment, the negative output is employed, and output on the positive side, that is, the ground side is equipped with the current detection resistor 108. As a result, even if the load (drive voltage Vout) is changed, an influence of that change on the potential of the detected portion of the drive current Iout is small, and the drive current Iout can be stably detected. Also, the configuration of the detector circuit can be simplified.

[0118] In conducting the hysteresis control on the drive current Iout, if the input voltage to the downconverter 104, the drive voltage Vout, or both of those voltages are changed, since an inclination of the rising or falling of the drive current Iout is changed, the switching frequency of the second switching element 140 can be changed. Under the circumstance, in the semiconductor light source control device 100 according to this embodiment, the hysteresis width ΔI is adjusted so that a change in the switching frequency is suppressed. In particular, a target switching frequency is so set as to avoid a frequency band of a known radio noise, thereby making it possible to suppress an adverse effect of the radio noise on the semiconductor light source control device 100.

[0119] Also, in the semiconductor light source control device 100 according to this embodiment, a variation in the input voltage to the downconverter 104 due to a variation in the battery voltage Vbat is suppressed by the action of the flyback regulator 102. Therefore, a change in the switching frequency due to the fluctuation of the input voltage to the downconverter 104 is suppressed. In other words, there is no need to select the hysteresis width ΔI by the combination of the input voltage to the downconverter 104 with the drive voltage Vout, and the hysteresis width ΔI can be selected mainly on the basis of the drive voltage Vout. Therefore, a control for adjusting the hysteresis width ΔI is simplified. This contributes to a reduction in the scale of the control signal, and an increase in the processing speed thereof.

[0120] Also, in the semiconductor light source control device 100 according to this embodiment, the output capacitor 128 is disposed on an output stage of the flyback regulator 102. If the second switching element 140 is on when the bypass switch turns on, charge stored in the output capacitor 128 is going to flow in the LEDs at once. However, since the inductor 144 is disposed on the route of the drive current Iout in the semiconductor light source control device 100, a flow of the charge is smoothed to suppress the overshoot of the drive current Iout. Similarly, when the bypass switch turns off, the undershoot of the drive current Iout is suppressed.

[0121] Let us consider a semiconductor light source lighting circuit 300 according to the following comparative example which is uniquely created for the purpose of suppressing the overshoot or the undershoot of the drive current Iout at the time of changing over the bypass switch.

FIG. 8 is a circuit diagram illustrating a configuration of the semiconductor light source lighting circuit 300 according to the comparative example. The semiconductor light source lighting circuit 300 is a forward converter that basically uses no smoothing capacitor. The semiconductor light source lighting circuit 300 includes a control circuit 302, an input capacitor 306, a reset circuit 308, a transformer 310, a fifth switching element 312, a second diode 314, a third diode 316, an inductor 318, and a current detection resistor 320.

[0122] The control circuit 302 turns off the fifth switching element 312 if a magnitude of the drive current exceeds a given current upper limit value, and turns on the fifth switching element 312 if the magnitude of the driver circuit falls below a current lower limit value.

[0123] In the semiconductor light source lighting circuit 300, when it is assumed that a winding ratio of the transformer 310 is $N_{s/p}$, an inductance of the inductor 318 is Ls' , the hysteresis width of the driver circuit is $\Delta I'$, the input voltage is V_{in} , the output voltage V_{out} (<0), an on-time of the fifth switching element 312 is T_{on}' , an off-time of the fifth switching element 312 is T_{off}' , the switching frequency is F' , and the forward drop voltage of a rectifier diode is small and therefore ignored, F' can be obtained by the following expression.

$$\left. \begin{aligned} F' &= \frac{1}{T'}, \quad T' = T'_{on} + T'_{off} \\ T'_{on} &= \frac{\Delta I' \times Ls'}{V_{in} \times N_{s/p} - |V_{out}|}, \quad T'_{off} = \frac{\Delta I' \times Ls'}{|V_{out}|} \end{aligned} \right\} \dots \text{Ex. 1}$$

[0124] In the semiconductor light source lighting circuit 300, when it is assumed that the winding ratio of the transformer 310 is set to 16.7 (convert input = 6V into output = 100V), the inductance of the inductor 318 is set to 500 μH , the hysteresis width is set to 0.1A, a relationship between V_{in} , V_{out} , and F' obtained from Expression 1 are represented by the following Table 1. In Table 1, it is assumed that an input voltage variation is 6V to 20V, and an output (load) voltage variation is -4V to -88V (22 LEDs having $V_f = 4V$ are connected in series).

Table 1

	F'(kHz)	Vout(V)						
		-4	-12	-28	-44	-60	-72	-88
Vin(V)	6	76.8	211.2	403.2	492.8	480.0	403.2	211.2
	9	77.9	220.8	455.5	621.9	720.0	748.8	727.5
	14	78.6	227.7	492.8	714.1	891.4	995.7	1096.2
	16	78.8	229.2	501.2	734.8	930.0	1051.2	1179.2
	20	79.0	231.4	513.0	763.8	984.0	1129.0	1295.4

[0125] In this case, the switching frequency F' is varied between maximum/minimum by about 17 times. Although this variation range can be suppressed by making the inductance larger, the circuit is upsized. Also, when a function of suppressing a large variation of the switching frequency F' within a given range by calculating the input voltage and the output voltage is realized, the control circuit scale becomes large.

[0126] The same calculation is conducted in the semiconductor light source control device 100 according to this embodiment. In the semiconductor light source lighting circuit 100, when it is assumed that an inductance of the inductor 144 is Ls , the switching frequency is F , and the forward drop voltage of the flywheel diode 142 is small and therefore ignored, F can be obtained by the following expression.

$$\left. \begin{aligned} F &= \frac{1}{T}, \quad T = T_{on} + T_{off} \\ T_{on} &= \frac{\Delta I \times Ls}{|V_t| - |V_{out}|}, \quad T_{off} = \frac{\Delta I \times Ls}{|V_{out}|} \end{aligned} \right\} \dots \text{Ex. 2}$$

[0127] In the semiconductor light source lighting circuit 100, when it is assumed that a target voltage V_t is set to -100V, the inductance of the inductor 144 is set to 500 μH , and the hysteresis width is set to 0.1A, a relationship between V_t , V_{out} , and F obtained from Expression 2 are represented by the following Table 2.

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Table 2

Vin(V)	F'(kHz)	Vout(V)						
		-4	-12	-28	-44	-60	-72	-88
-100		76.8	211.2	403.2	492.8	480.0	403.2	211.2

[0128] In this case, a variation in the switching frequency F is suppressed to about 6.5 times. Also, since a main parameter that causes this variation is the drive voltage V_{out} , and the target voltage V_t is substantially fixed, the scale of the control circuit for adjusting the hysteresis width ΔI so as to suppress the variation in the switching frequency F can be relatively reduced.

[0129] When theoretical calculated values of the switching frequency F in Table 2 are viewed, the switching frequency F increases as the drive voltage V_{out} decreases from -4V to -44V, and the switching frequency F decreases as the drive voltage V_{out} decreases from -44V to -88V. A boundary between the increase and the decrease of the switching frequency F is -50V which is about half of the output voltage (input voltage of the downconverter 104 at a second stage (post stage)) of the flyback regulator 102 at a first stage (previous stage). Therefore, the control is conducted to increase the hysteresis width ΔI more as the drive voltage V_{out} is lower if $V_{out} > -50V$, and to decrease the hysteresis width ΔI if $V_{out} < -50V$, thereby making it possible that the switching frequency F easily falls within a given range.

[0130] Also, in this embodiment, it is found that the boundary between the increase and the decrease of the switching frequency F is about half of the output voltage of the flyback regulator 102. However, in another embodiment having another circuit arrangement, it is conceivable that this boundary is 1/3 or 1/4 of the output voltage. The common element between those embodiments resides that the drive voltage V_{out} that gives the maximum value of the switching frequency F when the hysteresis width is kept constant can be present between the maximum value and the minimum value of the drive voltage V_{out} . Therefore, when such a drive voltage V_{out} is found out by experiments or simulations, and the circuit is configured so that the hysteresis width ΔI becomes minimum at the drive voltage V_{out} , the variation in the switching frequency F can be more preferably suppressed.

[0131] A setting example of the parameters in the semiconductor light source control device 100 according to this embodiment is represented by the following Table 3.

Table 3

Vout (V)	Voffset	Lower limit voltage	Upper limit voltage	Ith2	Ith1	Mean Current	Switching frequency
-4	0.25	0.2356	0.2456	1.178	1.228	1.203	382.2 kHz
-8	0.37	0.2332	0.2480	1.166	1.240	1.203	498.7 kHz
-12	0.48	0.2309	0.2503	1.154	1.252	1.203	542.3 kHz
-16	0.60	0.2285	0.2527	1.143	1.264	1.203	555.8 kHz
-20	0.72	0.2262	0.2551	1.131	1.275	1.203	553.7 kHz
-24	0.83	0.2238	0.2574	1.119	1.287	1.203	542.8 kHz
-28	0.95	0.2215	0.2598	1.107	1.299	1.203	526.1 kHz
-32	1.07	0.2191	0.2621	1.095	1.311	1.203	505.7 kHz
-36	1.18	0.2167	0.2645	1.084	1.322	1.203	482.6 kHz
-40	1.30	0.2144	0.2668	1.072	1.334	1.203	457.6 kHz
-44	1.42	0.2120	0.2692	1.060	1.346	1.203	431.0 kHz
-48	1.54	0.2097	0.2716	1.048	1.358	1.203	403.4 kHz
-52	1.56	0.2093	0.2720	1.046	1.360	1.203	398.2 kHz
-56	1.46	0.2113	0.2700	1.056	1.350	1.203	419.6 kHz
-60	1.36	0.2132	0.2680	1.066	1.340	1.203	438.2 kHz
-64	1.26	0.2152	0.2660	1.076	1.330	1.203	453.4 kHz
-68	1.16	0.2172	0.2640	1.086	1.320	1.203	464.4 kHz
-72	1.06	0.2192	0.2621	1.096	1.310	1.203	469.9 kHz

(continued)

Vout (V)	Voffset	Lower limit voltage	Upper limit voltage	Ith2	Ith1	Mean Current	Switching frequency
-76	0.97	0.2211	0.2601	1.106	1.300	1.203	468.4 kHz
-80	0.87	0.2231	0.2581	1.116	1.291	1.203	457.3 kHz
-84	0.77	0.2251	0.2561	1.125	1.281	1.203	433.1 Hz
-88	0.67	0.2271	0.2542	1.135	1.271	1.203	390.0 kHz

[0132] The offset voltage Voffset is set so that the voltage value becomes high in the vicinity of Vout=-50V as illustrated by the graph of FIG. 3, by adjusting a circuit constant of the hysteresis width setting circuit 138 illustrated in FIG. 2. The lower limit voltage and the upper limit voltage are voltages of the voltage division node between the twelfth resistor 182 and the thirteenth resistor 184 of the downconverter driver circuit 136 illustrated in FIG. 4, which correspond to the current lower limit value Ith2 and the current upper limit value Ith1, respectively. The lower limit voltage and the upper limit voltage are calculated from the offset voltage Voffset by setting the respective resistance values of the eighth resistor 174, the twelfth resistor 182, and the thirteenth resistor 184, and the positive control supply voltage Vcc. The mean current is a mean value of the current upper limit value Ith1 and the current lower limit value Ith2. The switching frequency is obtained as $\Delta I = Ith1 - Ith2$, $V_t = -100V$, and $L_s = 200\mu H$ in the same calculation expression as Expression 2.

[0133] It is found that even if L_s decreases from $500\mu H$ to $200\mu H$, the switching frequency can fall within a range of from 550 kHz or higher to 500 kHz or lower. That is, in the semiconductor light source control device 100 according to this embodiment, the inductance for smoothing the drive current Iout can be downsized.

[0134] Also, when the semiconductor light source lighting circuit 300 according to the comparative example is compared with the semiconductor light source control device 100 according to this embodiment, in the semiconductor light source control device 100, the output capacitor 128 of the flyback regulator 102 and the second switching element 140 of the downconverter 104 are increased, but the reset circuit 308 can be reduced from the semiconductor light source lighting circuit 300. As a result, the circuit scale is substantially equal to each other.

[0135] The configuration and the operation of the semiconductor light source control device according to this embodiment have been described above. This embodiment is exemplary, and it would be understood by an ordinary skilled person that the combinations of the respective elements and the respective processing can be variously modified, and such modifications also fall within the scope of the present invention.

[0136] In this embodiment, as the element arrangement of the downconverter 104, a case in which the second switching element 140 is arranged on the cathode side of the flywheel diode 142, and the inductor 144 is arranged on the anode side of the flywheel diode 142 has been described. However, the present invention is not limited to this configuration. The flywheel diode may be connected in parallel to the output capacitor 128 of the flyback regulator 102. The second switching element is disposed on the route of the drive current Iout which leads to the LED from one end of the output capacitor 128, and returns to the other end of the output capacitor 128 from the LED. The second switching element may be also disposed between the output capacitor 128 and the flywheel diode. The on/off operation of the second switching element may be controlled on the basis of the drive current. The inductor 144 may be disposed on the route of the drive current Iout, and disposed between the flywheel diode and the LED.

[0137] FIGS. 9A to 9C are circuit diagrams illustrating the configurations of semiconductor light source control devices 400, 500, and 600 according to first, second, and third modified examples. FIG. 9A illustrates the configuration of the semiconductor light source control device 400 according to the first modified example. One end of a second switching element 440 is connected to a high potential side output of the flyback regulator 102, and the other end of the second switching element 440 is connected to a cathode of a flywheel diode 442. One end of an inductor 444 is connected to a connection node between the other end of the second switching element 440 and the cathode of the flywheel diode 442. The other end of the inductor 444 is grounded, and forms a high potential side output terminal to the LEDs. An anode of the flywheel diode 442 is connected to a low potential side output of the flyback regulator 102, and forms a low potential side output terminal to the LEDs.

[0138] FIG. 9B illustrates the configuration of the semiconductor light source control device 500 according to the second modified example. A cathode of a flywheel diode 542 is connected to a high potential side output of the flyback regulator 102, and grounded, and forms a high potential side output to the LEDs. One end of a second switching element 540 is connected to a low potential side output of the flyback regulator 102, and the other end of the second switching element 540 is connected to an anode of the flywheel diode 542. One end of an inductor 544 is connected to a connection node between the other end of the second switching element 540 and the anode of the flywheel diode 542. The other end of the inductor 544 forms a low potential side output terminal to the LEDs.

[0139] FIG. 9C illustrates the configuration of the semiconductor light source control device 600 according to the third modified example. One end of a second switching element 640 is connected to a low potential side output of the flyback

regulator 102, and the other end of the second switching element 640 is connected to an anode of a flywheel diode 642. A connection node between the other end of the second switching element 640 and the anode of the flywheel diode 642 forms a low potential side output to the LEDs. A cathode of the flywheel diode 642 is connected to one end of an inductor 644. A connection node between the cathode of the flywheel diode 642 and one end of the inductor 644 is connected to a high potential side output of the flyback regulator 102. The other end of the inductor 644 is grounded, and forms a high potential side output terminal to the LEDs.

[0140] According to the respective semiconductor light source control devices 400, 500, and 600 of the first, second, and third modified examples, the overshoot and the undershoot of the drive current Iout can be reduced as in the semiconductor light source control device 100 according to the embodiment.

[0141] In the embodiment, there has been described a case in which the high potential side of the output, that is, the anode side of the plurality of LEDs is grounded to realize the negative output. However, the present invention is not limited to this configuration, but, for example, the anode side of the plurality of LEDs may be connected to a terminal to which a DC voltage such as the battery voltage Vbat is applied.

[0142] In the embodiment, there has been described a case in which the switching frequency is not measured in real time, but, the relationship between the drive voltage Vout and the hysteresis width ΔI is determined on the basis of the known relationship between the drive voltage Vout and the switching frequency instead, and the circuit is configured so that the hysteresis width ΔI is changed according to the determined relationship. However, the present invention is not limited to this configuration. For example, the semiconductor light source control device may include a circuit for measuring the switching frequency of the second switching element 140, and adjust the hysteresis width so that the measured switching frequency falls within a target frequency range.

[0143] In the embodiment, there has been described a case in which the semiconductor light source control device 100 includes the N bypass switches 110-1 to 110-N. However, the present invention is not limited to this configuration, but the bypass switches may be disposed separately from the semiconductor light source control device.

[0144] In the embodiment, there has been described a case in which the hysteresis control of the driver circuit is conducted. However, the present invention is not limited to this configuration, but, for example, a duty ratio of the second switching element 140 may be controlled so that a voltage obtained by appropriately filtering the voltage drop Vm comes closer to a reference voltage corresponding to a target current.

[0145] In the embodiment, there has been described a case in which the driver circuit is configured to generate the drive current Iout by the combination of the flyback regulator 102 and the downconverter 104, and control the magnitude of the drive current Iout to come closer to the target value. However, the present invention is not limited to this configuration, but, for example, a circuit illustrated in FIG. 8 may be employed as the above driver circuit, or a flyback regulator that is subjected to a current feedback control may be employed.

[0146] FIG. 10 is a circuit diagram illustrating a configuration of a semiconductor light source control device 700 according to a fourth modified example, and members connected to the semiconductor light source control device 700. The semiconductor light source control device 700 includes a flyback regulator 702, a current detection resistor 708, the N bypass circuits 270-1 to 270-N, and the bypass driver circuit 112.

[0147] In the semiconductor light source control device 700 according to this modified example, when a poor continuity is generated in a portion of a mark "X" indicated by reference numeral 718 in the second bypass connection line 280-2, as in the semiconductor light source control device 100 according to this embodiment, both of the second bypass switch and the third bypass switch are forcedly turned on by the actions of the second bypass circuit 270-2, the third bypass circuit 270-3, and the bypass driver circuit 112.

[0148] Also, a limit value of the maximum voltage output by the flyback regulator 702 is set to a sum of the forward drop voltages Vf or more, taking a case in which all of the N LEDs connected in series are turned on into account. For example, when the maximum value of the forward drop voltage Vf of one LED is set to 6V, and the 30 LEDs are connected in series to each other, the limit value is set to 180V or higher. In this example, because the drive current Iout does not flow in the LED at the moment when the contact failure or the disconnection is generated in the line of the mark "X" indicated by reference numeral 762 in FIG. 10, the output voltage of the flyback regulator 702 is raised toward 180V. When the control circuit (not shown) detects that the drive current Iout is stopped from flowing in the LEDs, the control circuit takes a countermeasure to inspect in which line or LED the disconnection is generated, and turn on the first bypass switch 110-1 in the circuit of FIG. 10 so as to turn on the other LEDs. Normally, a time of several ten msec to several hundred msec is required for this countermeasure.

[0149] In this case, if the semiconductor light source control device does not include the limiter zener diode 256 and the backflow prevention diode 258, the output voltage of the flyback regulator 702 reaches 180V before the first bypass switch turns on. In this situation, when it is assumed that a mean value (at room temperature) of the forward drop voltages Vf of the used LEDs is 4V, and 3V when a current hardly flows, a voltage of $180V - 3V \times 30 = 90V$ is applied to the first bypass switch. Therefore, although only a voltage of several V is usually applied to each of 30 bypass switches, an element having the withstand voltage of 100V must be selected taking the disconnection or the contact failure into account.

[0150] Then, when the disconnection or the contact failure is generated in the line of a mark "X" indicated by reference

numeral 764 in FIG. 10, the first electrostatic protection zener diode is applied with the above 90V when a current hardly flows in the LEDs, and $180V - 4V \times 30 = 60V$ when a control current flows in the LEDs. In this example, when it is assumed that the zener voltage of the first electrostatic protection zener diode is 20V, since the above voltages 90V and 60V are higher than 20V, $20V \times 1A = 20W$ is applied to the first electrostatic protection zener diode for several ten msec to several hundred msec when the control current is 1A, and the element that withstands 20W needs to be selected. In order to avoid this, the zener voltage of the first electrostatic protection zener diode needs to be set to 90V or higher, which makes it difficult to perform the original function of the electrostatic protection.

[0151] Under the circumstance, the semiconductor light source control device 700 according to this modified example is equipped with a first bypass/limiter circuit 250-1 whereby even if the contact failure or the disconnection is generated, an upper limit of the voltage to be applied to the first bypass switch 110-1 is suppressed. Therefore, the element having the high withstand voltage of 100V or higher may not be selected as the first bypass switch 110-1. Also, if the limit voltage by the first bypass/limiter circuit 250-1 is set to the zener voltage or lower of the first electrostatic protection zener diode 252-1, a small zener diode can be selected.

[0152] In the semiconductor light source control device 100 according to the embodiment, the withstand voltage of kV order is required for the bypass switch when there is no limiter function. Therefore, the withstand voltage suppression effect obtained by provision of the limiter function is more remarkable in the embodiment.

[0153] In this embodiment, a case in which the LEDs and the bypass switches correspond to each other on a one-to-one basis has been described. However, the present invention is not limited to this configuration, but the on/off operation of the plurality of LEDs may be controlled by one bypass switch. For example, when one bypass switch is connected to two LEDs connected in series, a total maximum value of the forward drop voltages V_f of the LEDs is 12V, and the zener diode of the electrostatic protection zener diode is 40V. Therefore, the zener voltage of the limiter zener diode may fall within a range of from 9V to 21V. When the zener voltage of the limiter zener diode is set to 20V, the limit value of the voltage between both ends thereof becomes 23V. Therefore, the element having the withstand voltage of 30V may be selected as the bypass switch.

[0154] In the embodiment, when the poor continuity is generated not only in the second bypass connection line 280-2, but also in the portion of the mark "X" indicated by the reference numeral 220 (refer to FIG. 5) of the third bypass connection line 280-3, all of the second bypass switch, the third bypass switch, and the fourth bypass switch are forcedly turned on by the actions of the second bypass circuit 270-2, the third bypass circuit 270-3, the fourth bypass circuit 270-4, and the bypass driver circuit 112.

[0155] In the embodiment, the description has been given of a case in which when the poor continuity is generated in the bypass connection line, any one of the two bypass switches connected to the bypass connection line is forcedly turned on by the disconnection abnormality, and which of the bypass switches is forcedly turned on by the short-circuit abnormality depends on the characteristic of the bypass switch. However, the present invention is not limited to this configuration. For example, resistors may be disposed in parallel to the respective odd-numbered bypass circuits (the first bypass circuit 270-1, the third bypass circuit 270-3, ...). Also, resistors may be disposed in parallel to the respective even-numbered bypass circuits. In those cases, when the poor continuity is generated in the bypass connection line, the bypass switch on a side where the above resistor is provided is forcedly turned on by the short-circuit abnormality, and the bypass switch on a side where the above resistor is not provided is forcedly turned on by the disconnection abnormality.

[0156] In the embodiment, a description has been given of a case in which the poor continuity of the bypass connection line is treated by the disconnection detection function and the short-circuit detection function of the bypass circuit and the bypass driver circuit. However, the present invention is not limited to this configuration. For example, a unit for detecting the poor continuity of the bypass connection line such as a current measurement unit may be disposed in the bypass connection line, and the unit may be used to determine whether the poor continuity is generated in the bypass connection line, or not. If it is determined that the poor continuity is generated, the bypass driver circuit may forcedly turn on the corresponding two bypass switches.

[0157] In the embodiment, a description has been given of a case in which the integration capacitor is charged in a case where the poor continuity or the short-circuit abnormality is detected when the bypass switch is off, and the integrating capacitor is discharged in the other cases. However, the present invention is not limited to this configuration. For example, the integration capacitor may be discharged by the first time constant if the poor continuity or the short-circuit abnormality is detected when the bypass switch is off, and the integration capacitor may be charged by the second time constant in the other cases.

[0158] In the semiconductor light source control device 100 according to the embodiment, the PWM dimming function is employed. During the PWM dimming operation, the bypass driver circuit 112 cyclically changes the voltage level of the lighting on/off control signal at the dimming frequency f_1 . If no abnormality is generated, the corresponding bypass switch is turned off when the lighting on/off control signal is low level, and the corresponding bypass switch is turned on when the lighting on/off control signal is high level. Therefore, the low level of the lighting on/off control signal corresponds to an off state of the corresponding bypass switch, and the high level of the lighting on/off control signal corresponds to

an on state of the corresponding bypass switch.

[0159] Also, the bypass driver circuit 112 is a microcomputer, and operates at relatively long time intervals. In particular, the bypass driver circuit 112 monitors the abnormality detection signal over a given abnormality determination period for the respective LEDs to determine whether the abnormality is generated, or not. Then, if it is determined that the abnormality is generated in a certain LED, the bypass driver circuit 112 fixes the lighting on/off control signal corresponding to that LED to the high level. This will be described with a concept of certainty and uncertainty of the abnormality. When the bypass driver circuit 112 continuously detects the abnormal state for the abnormality determination period, the bypass driver circuit 112 decides the abnormal state as abnormality, and subjects the bypass switch to on-latch control.

[0160] In general, since the abnormality determination period is longer than a cycle ($=1/f_1$) of the PWM dimming, the semiconductor light source control device 100 according to the embodiment introduces the integrating circuit, to thereby enable more accurate short-circuit abnormality/disconnection abnormality detection which is little in misdetection even if the PWM dimming is conducted.

[0161] A case in which the disconnection abnormality is generated in the LED normally-on (bypass switch = normally-off) control where the PWM dimming is not conducted will be studied. In a period since the disconnection is generated in a certain LED until a bypass switch corresponding to the LED is subjected to the on-latch control, the bypass switch operates as a switch for realizing the limiter function by the action of, particularly, the limiter zener diode of the bypass/limiter circuit corresponding to the LED. As a result, routes of the current to the other LEDs can be maintained. However, in this case, since the bypass switch basically operates in a linear area, the bypass switch is continuously supplied with an electric power of "disconnection detection voltage x drive current I_{out} " with the result that a power loss becomes large in the bypass switch. In this case, the switching element large in size and large in tolerated dose is required as the bypass switch, resulting in an upsized circuit and an increase in the costs. If the on-latch control is conducted on the bypass switch immediately after the detection of the disconnection abnormality, the power loss is reduced. However, in this case, the number of determinations in the bypass driver circuit 112 is decreased (determination time is short), and in particular, a possibility of the misdetection (malfunction) of the disconnection abnormality in a PWM dimming mode becomes high.

[0162] Even if the disconnection is generated when the PWM dimming is conducted, the bypass switch operates as a switch for realizing the limiter function when the lighting on/off control signal is low level. For that reason, there is a risk that the power loss is increased in the bypass switch, likewise. A ratio of the on-period (=extinction period of the LED) of the bypass switch to one cycle ($=1/f_1$) of the PWM dimming is called "on-duty ratio". The power loss caused by the disconnection is increased more as the on-duty ratio is smaller.

[0163] Also, the power loss in the bypass switch when the bypass switch is turned on is mainly caused by the on-resistance of the bypass switch, and slight, and extremely smaller than the power loss particularly when the bypass switch basically operates in the linear area.

[0164] FIG. 11 is a circuit diagram illustrating a configuration of a second bypass circuit 870-2 in a semiconductor light source control device according to a fifth modified example. The other bypass circuits are configured in the same manner as that of the second bypass circuit 870-2.

[0165] A difference between the second bypass circuit 270-2 illustrated in FIG. 5 and the second bypass circuit 870-2 illustrated in FIG. 11 mainly resides in the configuration of the second switch level shift circuit. A second switch level shift circuit 854-2 of the second bypass circuit 870-2 receives a second lighting on/off control signal $Sc2'$ from a bypass driver circuit 812, and converts the second lighting on/off control signal $Sc2'$ into the second bypass switch drive signal $Sd2$. In particular, the second switch level shift circuit 854-2 sets the second bypass switch drive signal $Sd2$ to the low level if the second lighting on/off control signal $Sc2'$ is high level, and sets the second bypass switch drive signal $Sd2$ to the high level if the second lighting on/off control signal $Sc2'$ is low level.

[0166] A second bypass/limiter circuit 850-2 of the second bypass circuit 870-2 may not have a resistor corresponding to the sixteenth resistor 260.

[0167] The second switch level shift circuit 854-2 includes a 26th resistor 822, a 27th resistor 814, a 28th resistor 816, a 29th resistor 818, and a fifth pnp bipolar transistor 820. One end of the 26th resistor 822 is connected to a terminal of the bypass driver circuit 812. The second lighting on/off control signal $Sc2'$ is output from the terminal of the bypass driver circuit 812. The other end of the 26th resistor 822 is connected to a base of the fifth pnp bipolar transistor 820. One end of the 27th resistor 814 is connected to a connection node between the other end of the 26th resistor 822 and the base of the fifth pnp bipolar transistor 820. A positive control supply voltage V_{cc} is applied to the other end of the 27th resistor 814, and an emitter of the fifth pnp bipolar transistor 820. A collector of the fifth pnp bipolar transistor 820 is connected to one end of the 28th resistor 816. The other end of the 28th resistor 816 is connected to one end of the 29th resistor 818. The other end of the 29th resistor 818 is connected to the cathode of the second LED 2-2.

[0168] A connection node between the 28th resistor 816 and one end of the 29th resistor 818 is connected to the gate of the second bypass switch 110-2. A signal generated in the connection node forms the second bypass switch drive signal $Sd2$.

[0169] When the second lighting on/off control signal $Sc2'$ is high level, the second bypass switch drive signal $Sd2$

becomes low level, and the second bypass switch 110-2 turns off (the second LED 2-2 turns on). When the second lighting on/off control signal Sc2' is low level, the second bypass switch drive signal Sd2 becomes high level, and the second bypass switch 110-2 turns on (the second LED 2-2 turns off). When the PWM dimming is conducted, the bypass driver circuit 812 sets the second lighting on/off control signal Sc2' as a high level/low level repetitive signal having a cycle of several msec.

[0170] If the voltage between both ends of the integration capacitor 282 exceeds a given threshold voltage, the bypass driver circuit 812 increases the on-duty ratio and the cycle of a signal to be supplied to the control input terminal, that is, the gate of the second bypass switch 110-2 larger than those of the normal PWM dimming in synchronization with the second lighting on/off control signal Sc2'. In particular, if the voltage of the second abnormality detection signal Sdet2 exceeds the level threshold value V_g , the bypass driver circuit 812 starts the abnormality determination period for the second LED 2-2, and increases the ratio of a duration of the low level to one cycle of the second lighting on/off control signal Sc2'. In an example, the cycle of the second lighting on/off control signal Sc2' increases to several hundred msec, and the on-duty ratio increases to 90% or higher.

[0171] FIG. 12 is a timing chart illustrating a change in the second lighting on/off control signals Sc2 and Sc2' when the disconnection is generated in the second LED 2-2. A waveform represented on an upper stage of FIG. 12 represents the second lighting on/off control signal Sc2' when the semiconductor light source control device according to the fifth modified example conducts the PWM dimming in a first cycle PT1 of about several msec in the normal lighting state. A waveform represented in a middle stage of FIG. 12 represents the second lighting on/off control signal Sc2 when the semiconductor light source control device 100 according to the embodiment always conducts lighting in the normal lighting state. A waveform represented on a lower stage of FIG. 12 represents the second lighting on/off control signal Sc2 when the semiconductor light source control device 100 according to the embodiment conducts the PWM dimming in the first cycle PT1 in the normal lighting state.

[0172] When the disconnection is generated in the second LED 2-2 in the fifth modified example, a cycle of the second lighting on/off control signal Sc2' becomes a second cycle PT2 of about several hundred msec larger than the first cycle PT1. In particular, the bypass driver circuit 812 lengthens the duration of the low level while maintaining a length of the duration of the high level in one cycle of the second lighting on/off control signal Sc2', to thereby realize an increase in the cycle. The second cycle PT2 may be smaller than the second time constant for the discharge of the second integrating circuit 278-2.

[0173] In abnormality determination period PT3 of about several seconds, the bypass driver circuit 812 keeps the increased on-duty ratio and cycle of the signal to be supplied to the gate of the second bypass switch 110-2 in synchronization with the second lighting on/off control signal Sc2' if the voltage of the second abnormality detection signal Sdet2 when the second lighting on/off control signal Sc2' is set to the high level is higher than the level threshold value V_g . If the voltage of the second abnormality detection signal Sdet2 falls below the level threshold value V_g , the bypass driver circuit 812 returns the second lighting on/off control signal Sc2' to a state having the first cycle PT1. The bypass driver circuit 812 determines that the abnormality is generated (that is, abnormality certainty) if a state in which the voltage of the second abnormality detection signal Sdet2 is higher than the level threshold value V_g is continued until the abnormality determination period PT3 is expired. Then, the bypass driver circuit 812 fixes the second lighting on/off control signal Sc2' to the low level.

[0174] When the disconnection is generated in the second LED 2-2 in the embodiment, the state of the second lighting on/off control signal Sc2 remains in the same state as that before the abnormality is generated, during the abnormality determination period PT3. Then, if the abnormality determination period PT3 is expired, it is determined that the abnormality is generated, and the second lighting on/off control signal Sc2 is fixed to the high level.

[0175] Thus, according to the semiconductor light source control device of the fifth modified example, as compared with the semiconductor light source control device 100 according to the embodiment, a total length of the off-periods of the bypass switch in the abnormality determination period can be shortened even in the always-on state or even in the PWM dimming. Since the off-period corresponds to a period during which the bypass switch operates in the linear area when the disconnection is generated, the power loss in the bypass switch can be reduced in the fifth modified example. As a result, the switching element low in withstand can be employed as the bypass switch, so that the circuit can be downsized, and the costs can be reduced.

[0176] In particular, for the convenience of the PMW dimming, in a status where it is improper to determine that the abnormality is generated immediately with the level transition of the abnormality detection signal, according to the fifth modified example, it can be more precisely determined whether the abnormality is generated, or not, by monitoring the abnormality detection signal over the abnormality determination period, and the power loss of the bypass switch in the abnormality determination period can be reduced.

Claims

1. A light source control device (100,700), comprising:

5 a driver circuit (102,702) adapted to generate a drive current (I_{out}) that flows in a plurality of semiconductor light sources connected in series;
 a bypass switch (110) connected in parallel to at least one part of the plurality of semiconductor light sources;
 a main control circuit (112) adapted to cyclically turn on/off the bypass switch (110) in a normal light-up state; and
 10 an abnormality detection auxiliary circuit (272,274) adapted to change the amount of charge held by a capacitor (282) to a first direction by a first time constant when the bypass switch (110) is off and a voltage between both ends of the bypass switch (110) is lower than a first voltage, or higher than a second voltage higher than the first voltage, and to change the amount of charge held by the capacitor (282) to a second direction opposite to the first direction by a second time constant longer than the first time constant when the amount of charge held by the capacitor is not changed to the first direction by the first time constant,
 15 wherein the main control circuit (112) determines whether an abnormality is generated, or not, on the basis of the voltage between both ends of the capacitor (282), and forcedly turns on the bypass switch (110) if it is determined that the abnormality is generated.

2. The light source control device according to claim 1,

20 wherein the bypass switch (110) is controlled in on/off operation by a control signal (Sc'), wherein the control signal (Sc') cyclically repeats a state in which the bypass switch (110) is on, and a state in which the bypass switch (110) is off, in a normal light-up state;
 the device further comprising a limiter circuit (850) adapted to limit an upper limit of a voltage between both ends of at least one part of the plurality of semiconductor light sources with the use of the bypass switch (110) when the control signal (Sc') is in the state where the bypass switch (110) is off;
 25 wherein the abnormality detection auxiliary circuit (272,274) is adapted to change the amount of charge held by a capacitor (282) to a first direction by a first time constant when the limiter circuit (850) limits the upper limit of the voltage between both ends of the one part of the plurality of semiconductor light sources, and to change the amount of charge held by the capacitor (282) to a second direction opposite to the first direction by a second time constant longer than the first time constant when the amount of charge held by the capacitor (282) is not changed to the first direction by the first time constant; and
 30 the main control circuit (112) is adapted to increase an on-duty ratio of the control signal (Sc') when the voltage between both ends of the capacitor (282) intersects with a given threshold voltage (V_g) if a ratio of a duration of the state in which the bypass switch (110) is on to one cycle of the control signal (Sc') is called the on-duty ratio, and
 35 the main control circuit (112) monitors the voltage between both ends of the capacitor (282) over an abnormality determination period ($PT3$) longer than the cycle of the control signal (Sc') to determine whether an abnormality is generated, or not, and fixes the state of the control signal (Sc') to the state in which the bypass switch (110) is on if it is determined that the abnormality is generated.

3. The light source control device according to claim 2,

40 wherein the main control circuit (112) increases the cycle of the control signal (Sc') when the voltage between both ends of the capacitor (282) intersects with the threshold voltage (V_g).

FIG. 1

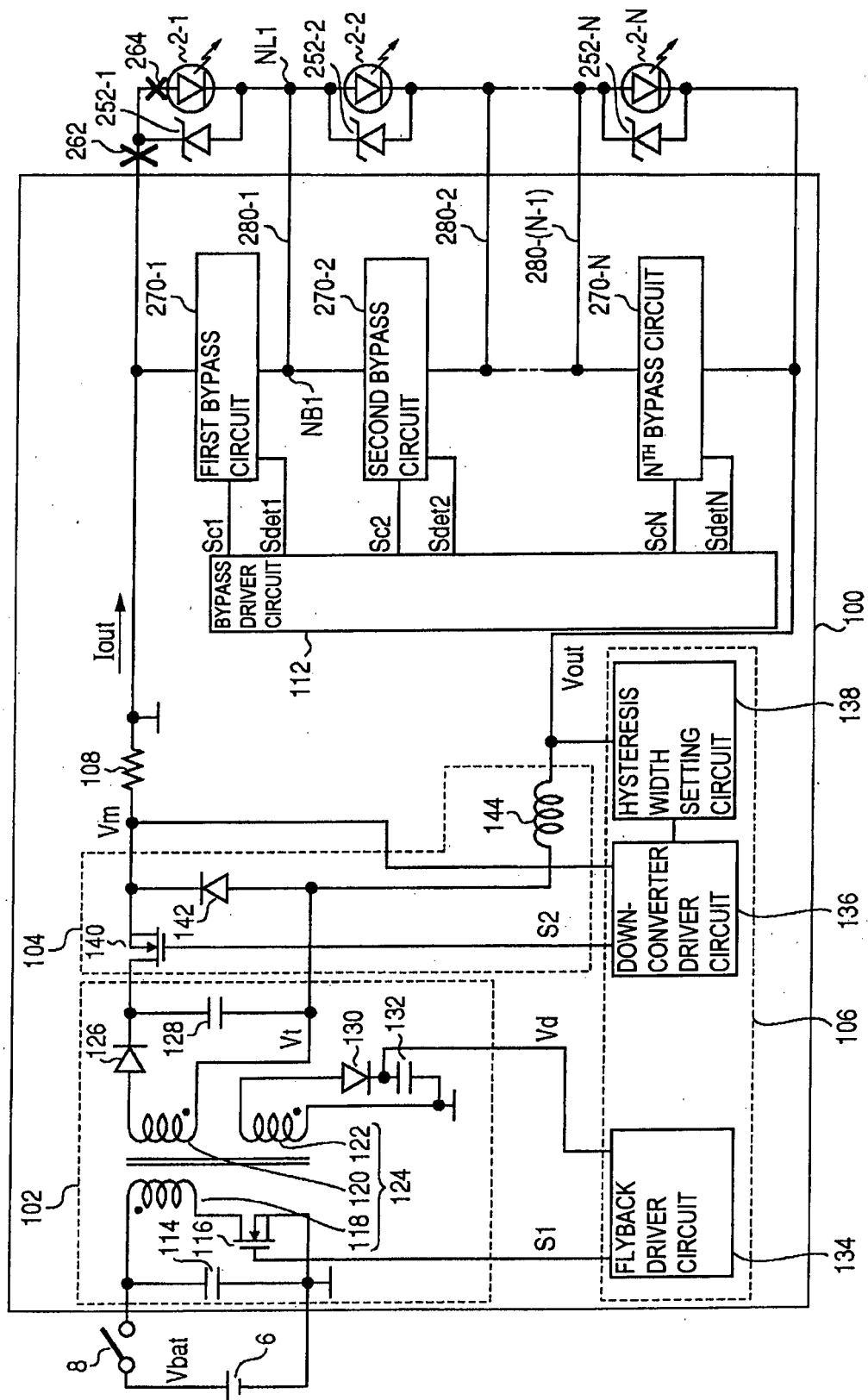


FIG. 2

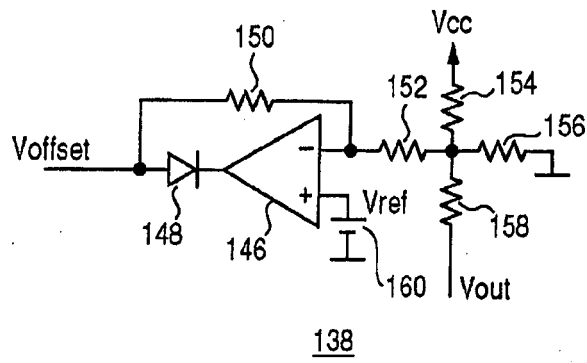


FIG. 3

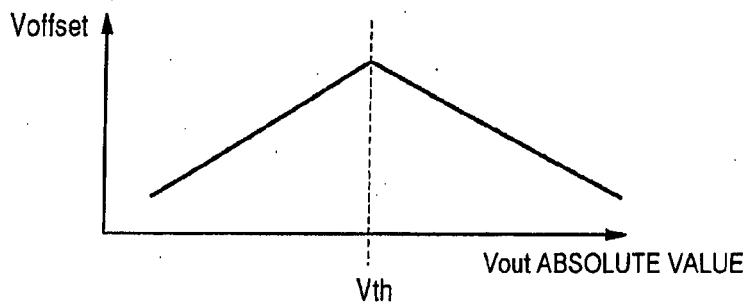
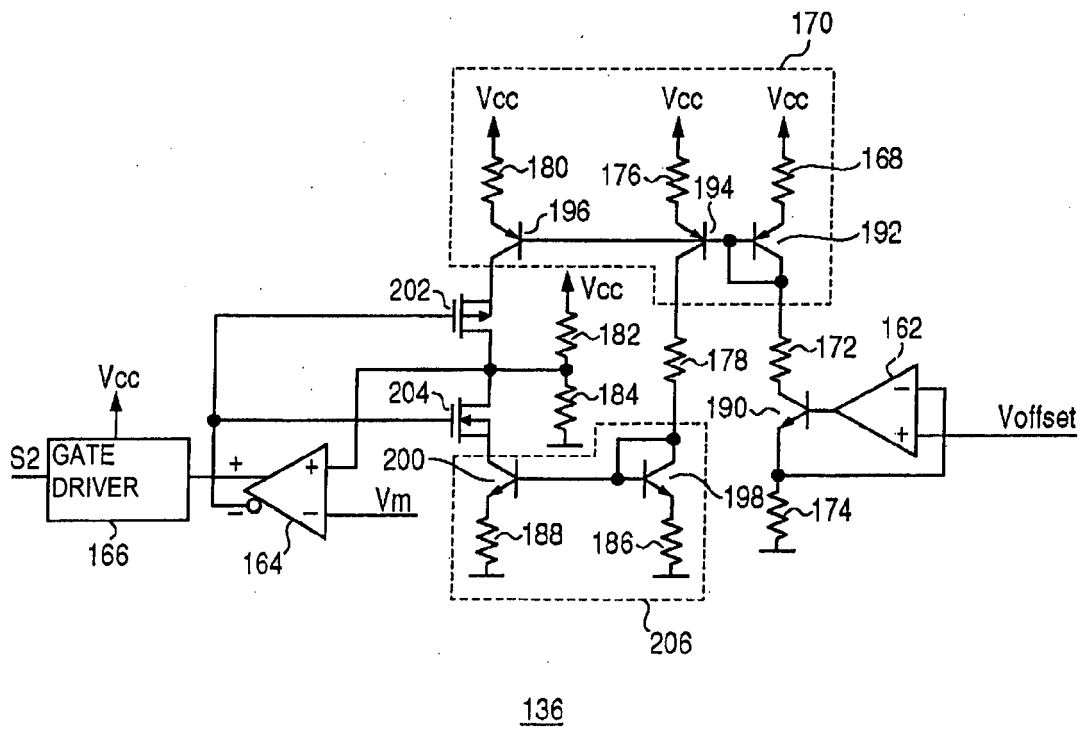


FIG. 4



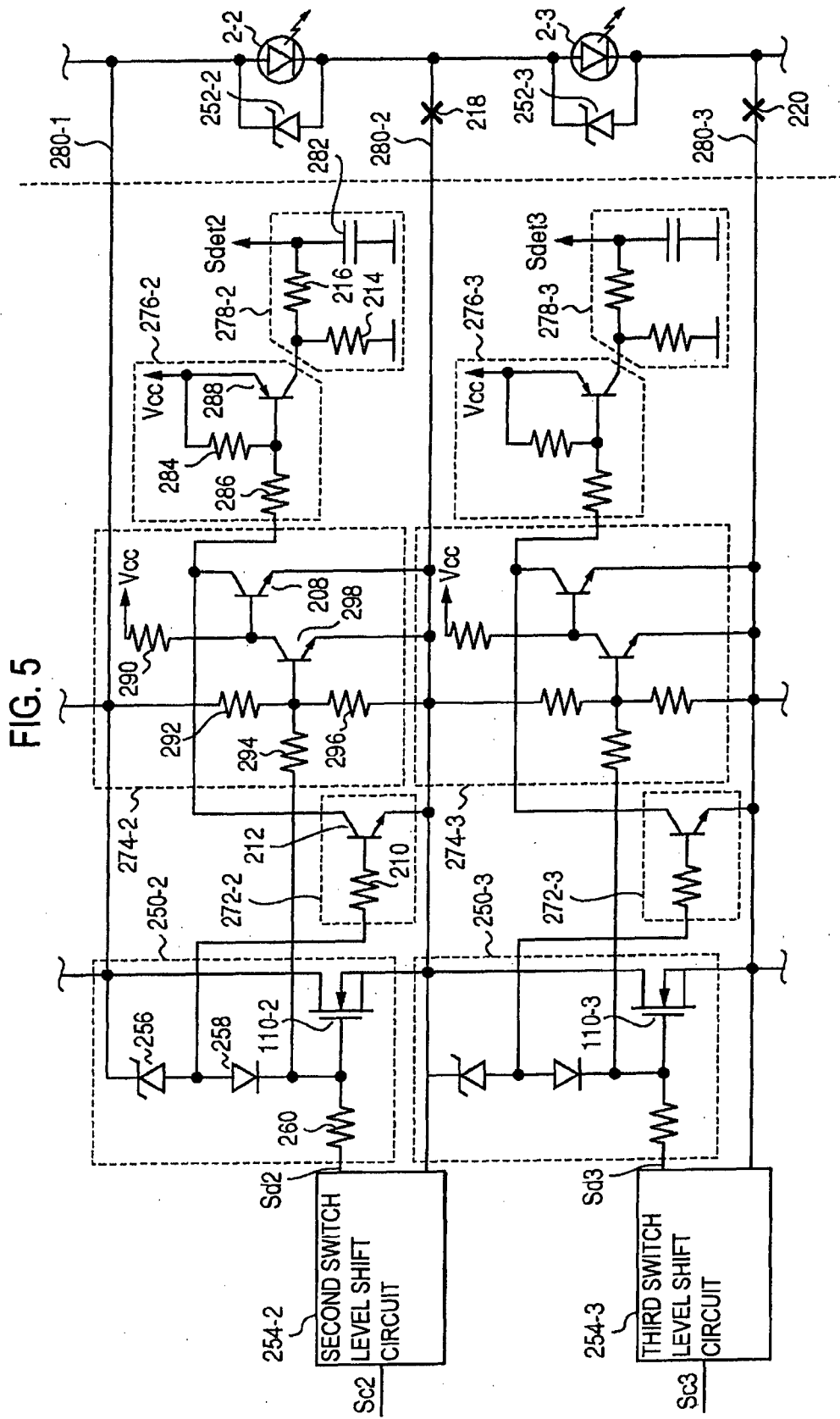


FIG. 6A

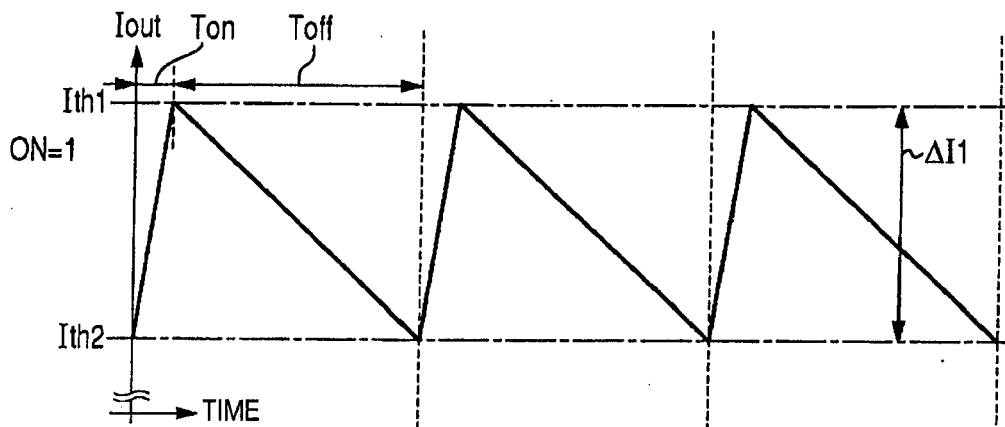


FIG. 6B

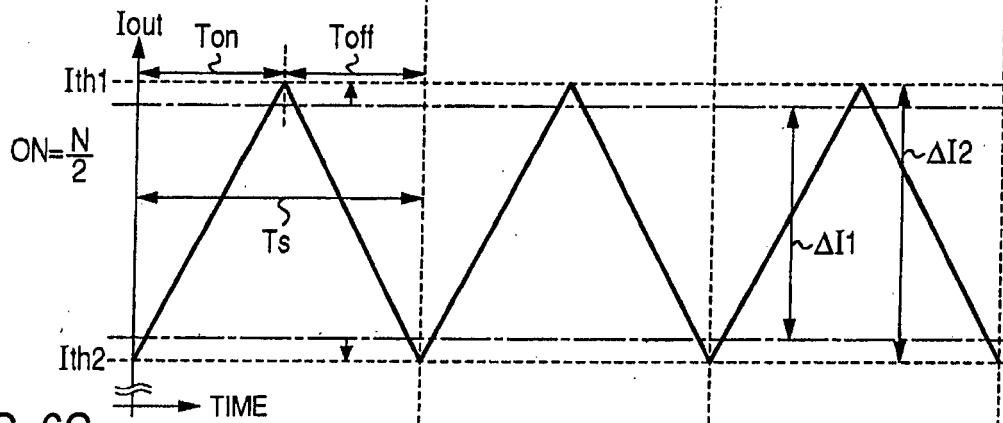
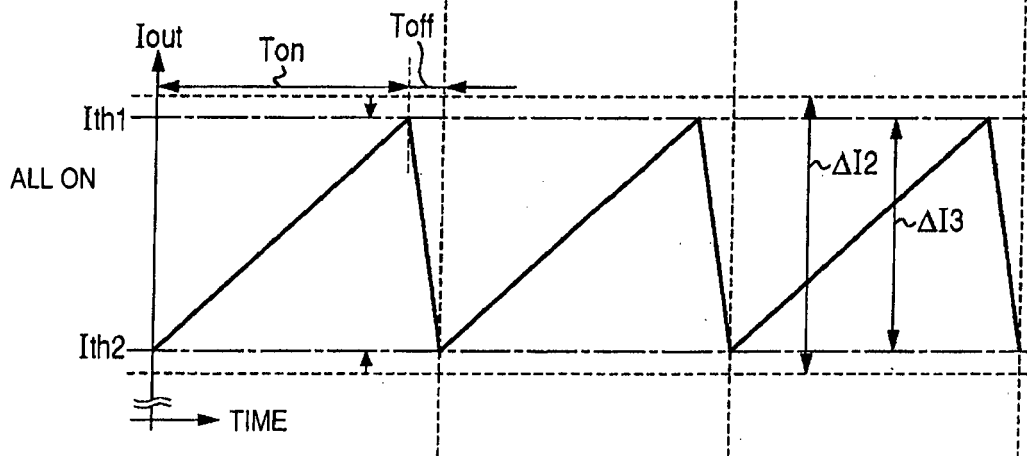


FIG. 6C



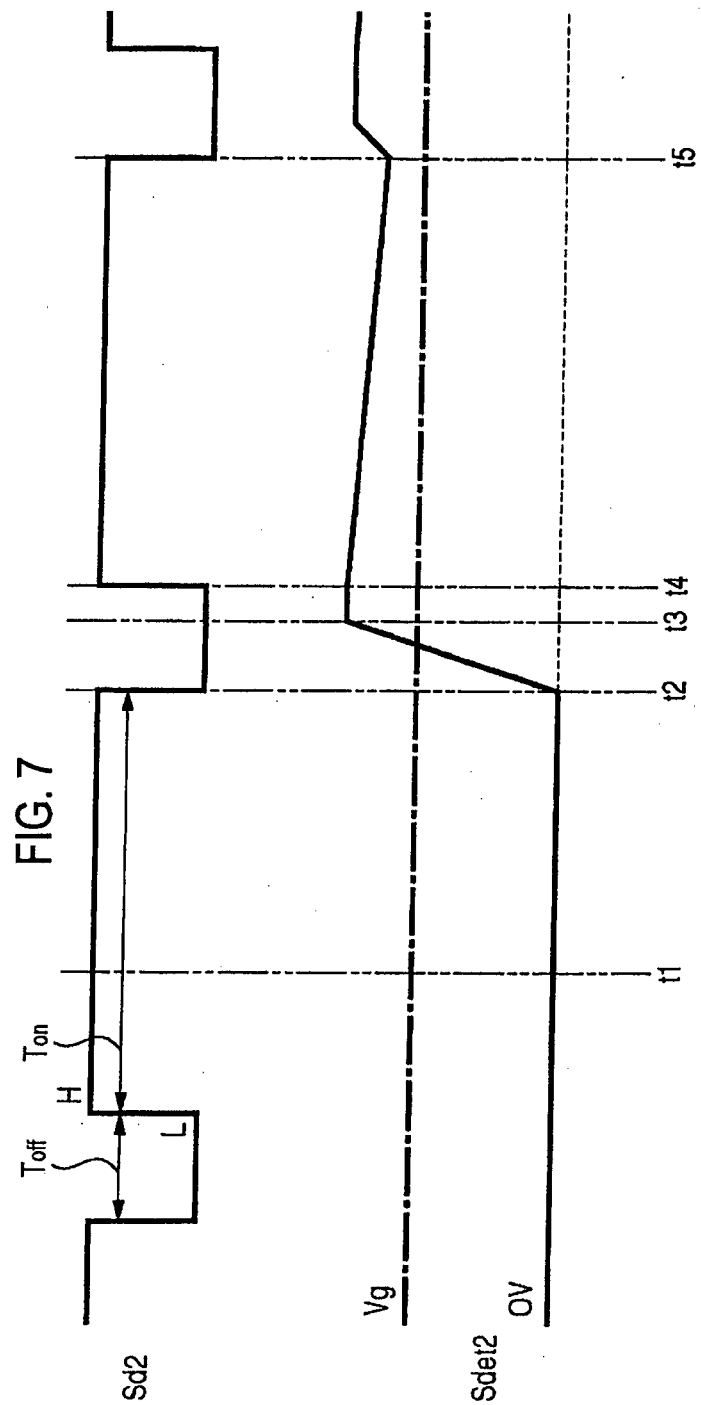


FIG. 8

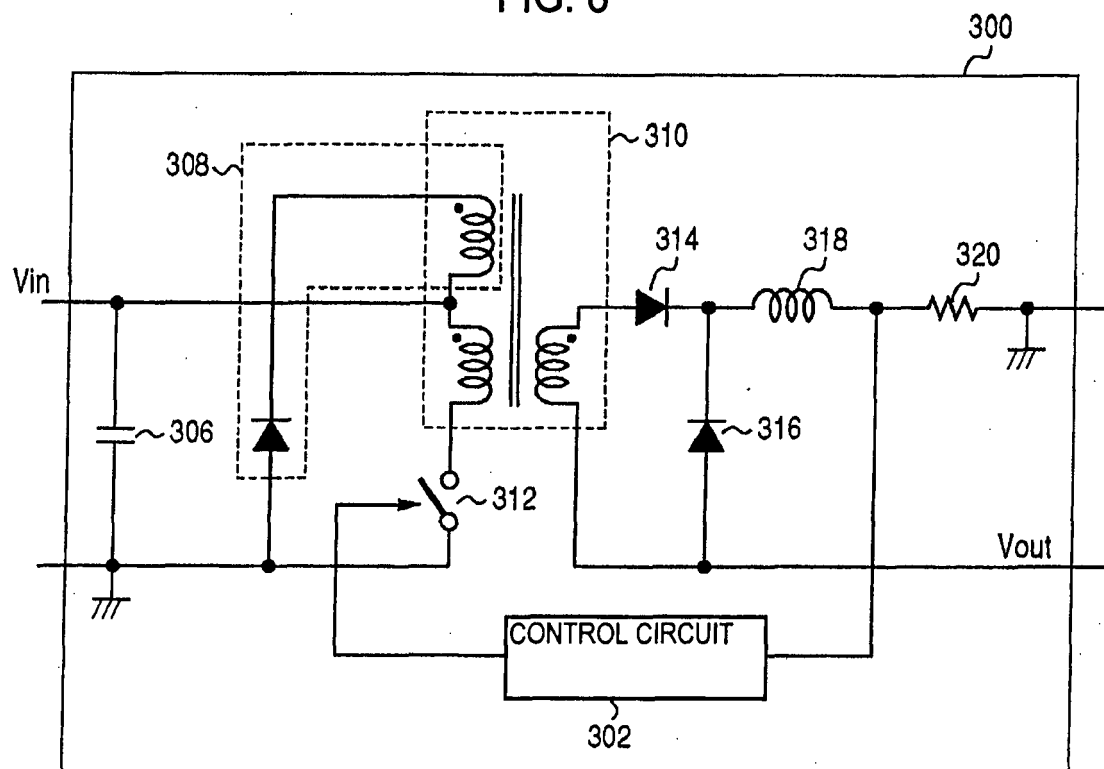


FIG. 9A

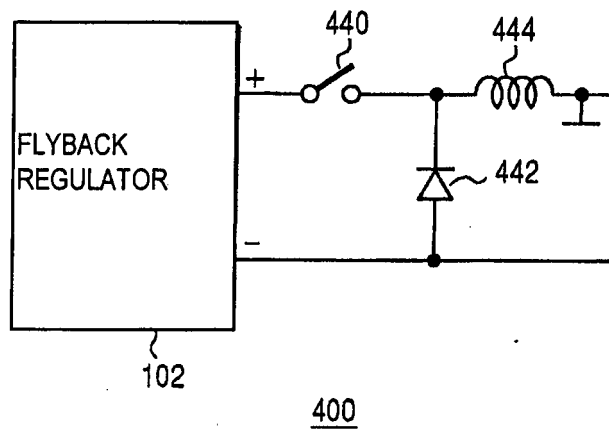


FIG. 9B

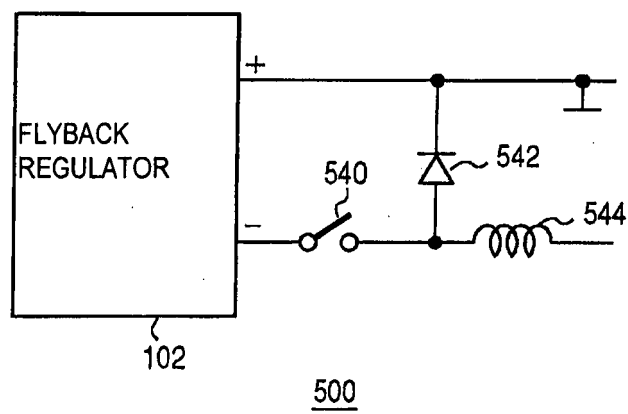


FIG. 9C

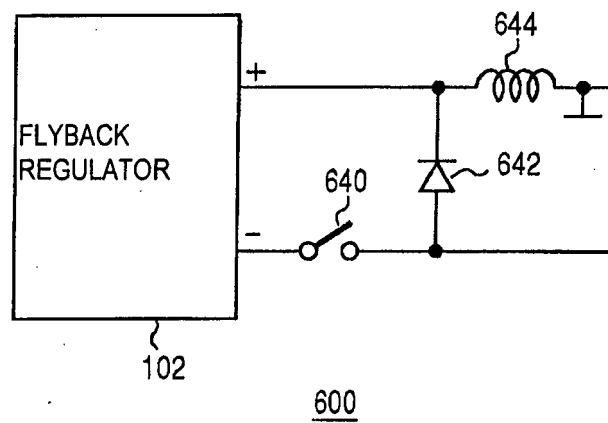


FIG. 10

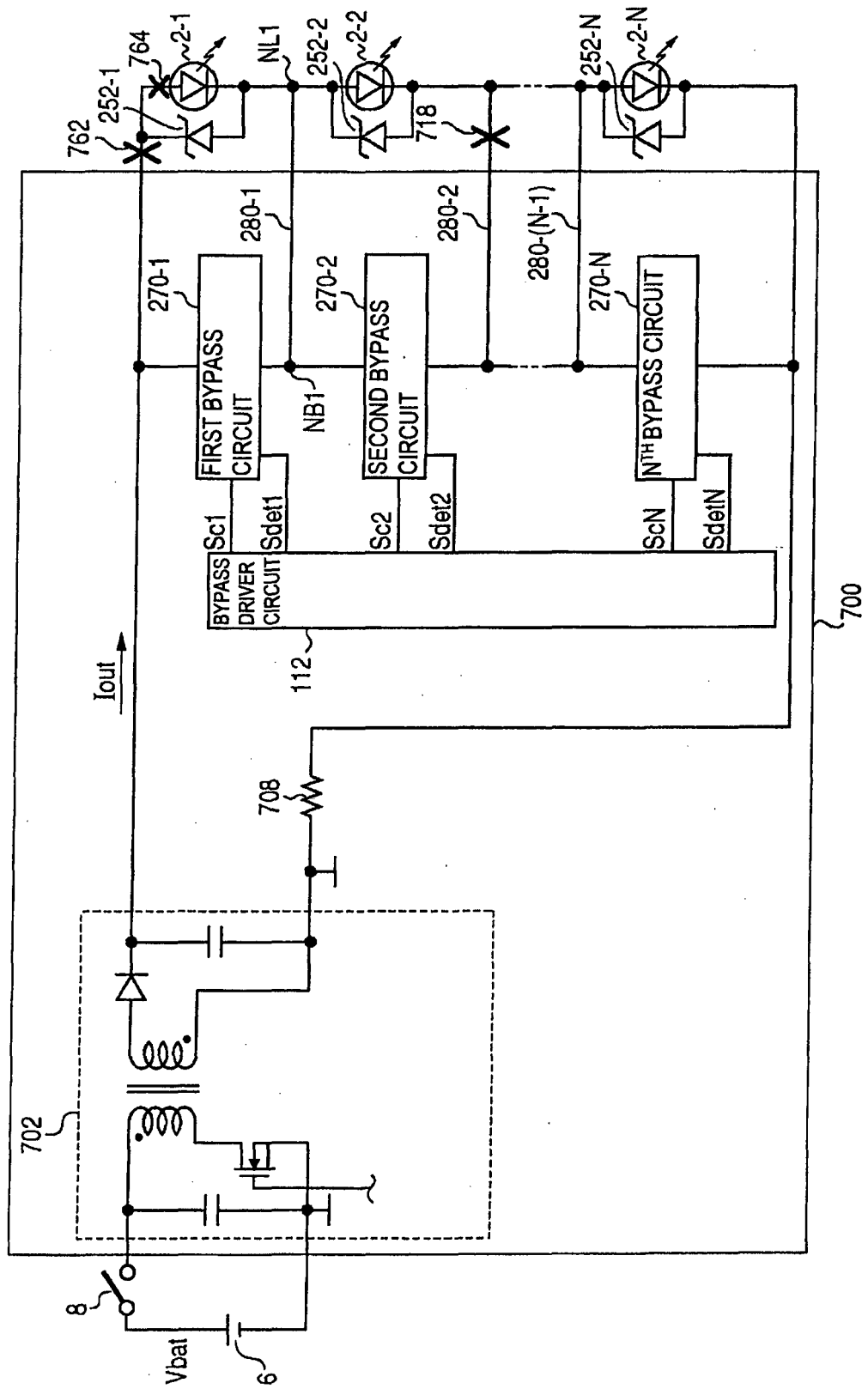
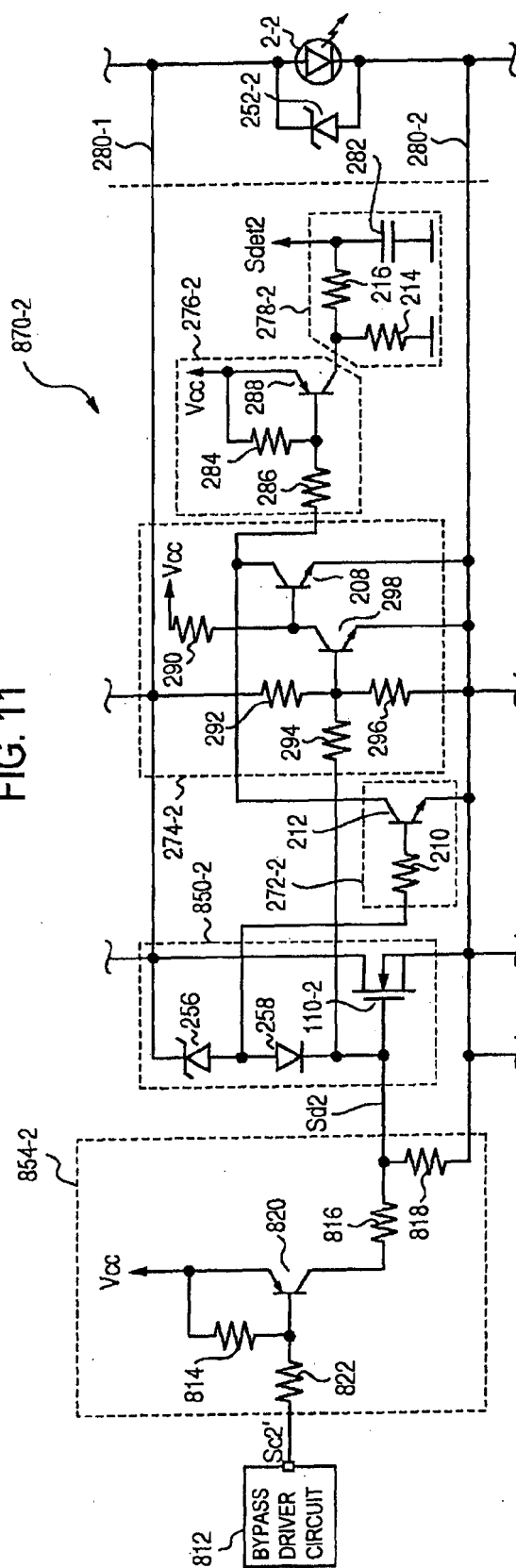
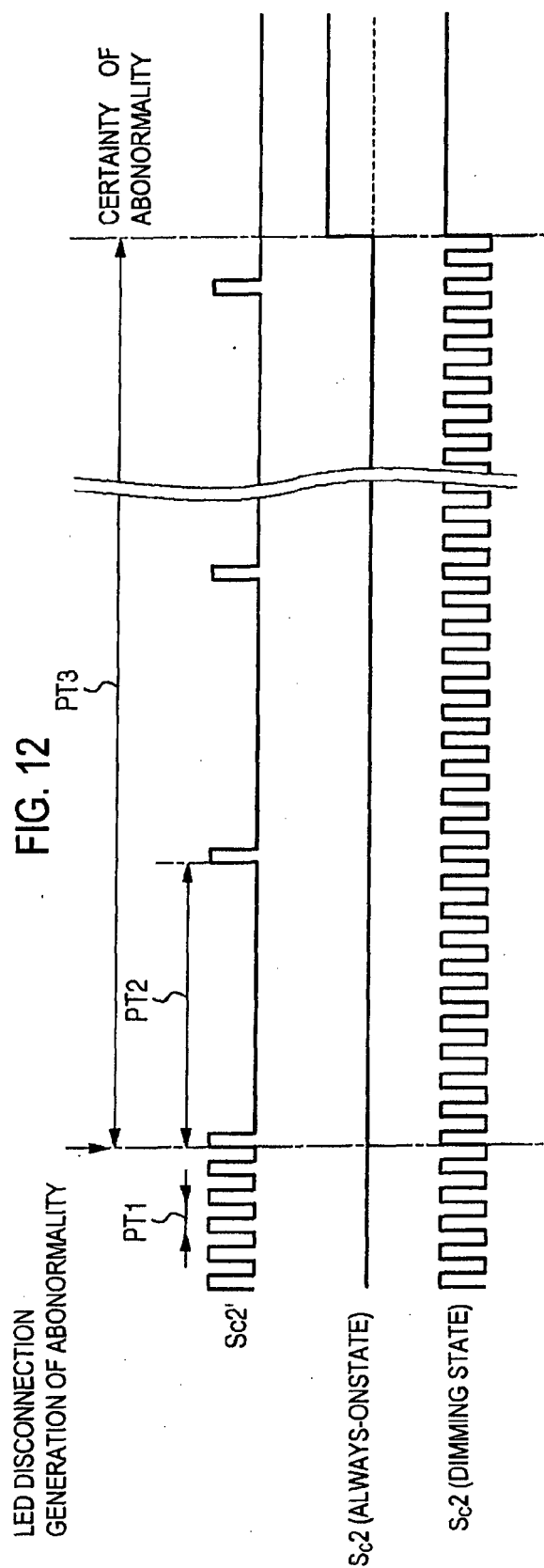


FIG. 11





REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2011192865 A [0004]