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(54) A driver for a light source

(57) A driver apparatus for driving one or more light emitting diodes is provided. The apparatus comprises one or more power source portions for providing two or more driving currents and a control portion for issuing two or more control signals for controlling the provision of two or more driving currents, each control signal exhibiting a respective duty cycle at a first cycle frequency, wherein the control portion is configured to issue the two or more control signals as synchronized control signals in predetermined time offsets with respect to each other for provision of the two or more driving currents in different phases.

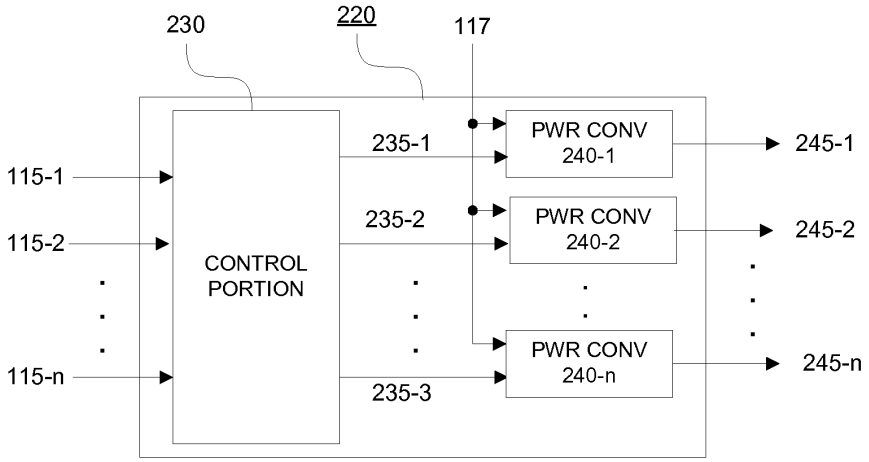

Figure 2

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Description

FIELD OF THE INVENTION

[0001] The invention relates to control of operation of one or more light sources. In particular, embodiments of the invention relate to a driver apparatus, use thereof, an arrangement and a computer program for driving one or more light emitting diodes (LEDs).

BACKGROUND

[0002] A driver for a light emitting diode (LED) light source may apply a control signal, such as a pulse-width modulation (PWM) signal, for controlling the light intensity provided by the LED light source. A periodic PWM signal with desired duty cycle and cycle frequency (PWM frequency) is typically applied in the driver to cause the driver to operate the LED light source at a light intensity determined by the duty cycle. In practice such control of the LED light source results in switching the light on and off in accordance with the PWM signal. With sufficiently high PWM frequency the off periods are unperceivable by a human eye but rather contribute to perceived reduced light intensity (compared to driving the LED light source without the off periods).

[0003] However, especially at low duty cycles, i.e. at low values of perceived light intensity, too low PWM frequency is likely to result in perceivable flickering of light due to too long off periods between the on periods, which may even be perceived as a disturbing stroboscopic effect. On the other hand, too high PWM frequency is likely to result in inaccurate control of light intensity or even variations in light level due to switching operation of power converters typically applied in such drivers.

SUMMARY

[0004] Consequently, it is an object of the present invention to provide a technique that enables driving the LED light source(s) at sufficient PWM cycle frequencies while avoiding disturbances caused by the power converter switching frequency.

[0005] The objects of the invention are reached by an apparatus, by arrangements and by a computer program as defined by the respective independent claims.

[0006] According to a first example embodiment, a driver apparatus for driving one or more LEDs is provided. The apparatus comprises one or more power source portions for providing two or more driving currents and a control portion for issuing two or more control signals for controlling the provision of two or more driving currents, each control signal exhibiting a respective duty cycle at a first cycle frequency, wherein the control portion is configured to issue the two or more control signals as synchronized control signals in predetermined time offsets with respect to each other for provision of the two or more driving currents in different phases.

[0007] According to a second example embodiment, a computer program for driving one or more LEDs is provided. The computer program comprises one or more sequences of one or more instructions which, when executed by one or more processors, cause an apparatus comprising one or more power source portions for providing two or more driving currents at least to issue two or more control signals for controlling the provision of two or more driving currents, each control signal exhibiting a respective duty cycle at a first cycle frequency, wherein the two or more control signals are synchronized control signals exhibiting predetermined time offsets with respect to each other for provision of the two or more driving currents in different phases.

[0008] The computer program may be embodied on a volatile or a non-volatile computer-readable record medium, for example as a computer program product comprising at least one computer readable non-transitory medium having program code stored thereon, the program code, which when executed by an apparatus, causes the apparatus at least to perform the operations described hereinbefore for the computer program in accordance with an example embodiment.

[0009] According to a third example embodiment, an arrangement comprising the driver apparatus according to the first example embodiment and one or more arrays of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents as two or more separate output currents of the driver apparatus and wherein each of the two or more separate output currents is coupled to a respective one of the two or more arrays of light emitting diodes.

[0010] According to a fourth example embodiment, an arrangement comprising the driver apparatus according to the first example embodiment and a single array of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents as two or more separate output currents of the driver apparatus and wherein the two or more separate output currents are coupled to the single array of light emitting diodes.

[0011] According to a fifth example embodiment, an arrangement comprising the driver apparatus according to the first example embodiment and a single array of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents combined into a single output current of the driver apparatus and wherein the single output current is coupled to the single array of light emitting diodes.

[0012] According to a sixth example embodiment, use of the driver apparatus according to the first example embodiment to drive one or more arrays of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents as two or more separate output currents of the driver apparatus and wherein each of the two or more output currents is applied to drive a respective one of the two or more arrays of light emitting diodes.

[0013] According to a seventh example embodiment, use of the driver apparatus according to the first example embodiment to drive a single array of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents as two or more separate output currents of the driver apparatus and wherein the two or more output currents are applied in parallel to drive the single array of light emitting diodes.

[0014] According to an eighth example embodiment, use of the driver apparatus according to the first example embodiment to drive a single array of light emitting diodes is provided, wherein the driver apparatus is configured to provide the two or more driving currents combined into a single output current of the driver apparatus and wherein the single output current is applied to drive the single array of light emitting diodes.

[0015] The exemplifying embodiments of the invention presented in this patent application are not to be interpreted to pose limitations to the applicability of the appended claims. The verb "to comprise" and its derivatives are used in this patent application as an open limitation that does not exclude the existence of also unrecited features. The features described hereinafter are mutually freely combinable unless explicitly stated otherwise.

[0016] The novel features which are considered as characteristic of the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following detailed description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Some embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

Figure 1a schematically illustrates an exemplifying arrangement in accordance with an example embodiment.

Figure 1b schematically illustrates an exemplifying arrangement in accordance with an example embodiment.

Figure 2 schematically illustrates some components of a driver in accordance with an example embodiment.

Figure 3 illustrates an example of a Pulse-Width Modulation (PWM) signal.

Figure 4 schematically illustrates some components of an exemplifying buck converter.

Figure 5a illustrates an example of control signals in different phases.

Figure 5b illustrates an example of control signals in different phases.

Figure 6a illustrates an example of control signals in different phases.

Figure 6b illustrates an example of control signals in different phases.

Figure 7 illustrates an example of control signals in different phases.

Figure 8 schematically illustrates some components of a driver in accordance with an example embodiment.

Figure 9 schematically illustrates an exemplifying arrangement in accordance with an example embodiment.

Figure 10 schematically illustrates an exemplifying arrangement in accordance with an example embodiment.

Figure 11 schematically illustrates an apparatus in accordance with an example embodiment.

Figure 12 schematically illustrates a circuit in accordance with an example embodiment.

Figure 13 schematically illustrates some components of a driver in accordance with an example embodiment.

DESCRIPTION OF SOME EMBODIMENTS

[0018] Figure 1a schematically illustrates an exemplifying arrangement 100 for providing light at a selectable light level. The arrangement 100 comprises a controller entity 110 for issuing input control signals 115-1, 115-2, ..., 115-n indicating desired characteristics of output currents 125-1, 125-2, ..., 125-3 to a driver 120. The driver 120 is arranged to derive each output current 125-1, 125-2, ..., 125-n on basis of operating power provided 117 thereto in accordance with the characteristics of the respective input control signal 115-1, 115-2, ..., 115-n. The output currents 125-1, 125-2, ..., 125-n are provided to a single array of light emitting diodes (LEDs) 170'. An array of LEDs, in other words a LED array, comprises either a single LED light source or two or more light sources connected in series. Hence, the driver 120 may be used to drive the single LED array 170'

[0019] In the following, the input control signals 115-1, 115-2, ..., 115-n may be referred to as input control signals 115 when referring jointly to all input control signals 115-1, 115-2, ..., 115-n or when referring to any single

one of the input control signals 115-1, 115-2, ..., 115-n. Moreover, the reference number 115-i may be applied to refer to the i:th input control signal. Similar practice may be applied to any numbered element comprising multiple sub-elements, i.e. to reference number having the format xxx-i.

[0020] Figure 1b schematically illustrates a second exemplifying arrangement 100' as a variation of the first arrangement 100. In the arrangement 100' each of the output currents 125-1, 125-2, ..., 125-n is coupled to one of separate LED arrays 170-1, 170-2, ..., 170-3, while the other components of the arrangement 100' are similar to those of the arrangement 100. The separate LED arrays 170-1, 170-2, ..., 170-3 are, preferably, arranged into a single luminaire or light fixture. The LED arrays 170, 170' may be identical or they may have different light emission spectra. Moreover, the LEDs within a LED array 170-i, 170' may be identical or they may have different light emission spectra.

[0021] In context of the arrangements 100 and 100' a dedicated input control signal 115-i is provided for each output current 125-i, i.e. the number of input control signals 115 is the same as the number of output currents 125. However, the number of input control signals 115 may be smaller than the number of output currents 125 e.g. such that each of the input control signals 115 is arranged to indicate desired characteristics for two or more output currents.

[0022] The number n indicating the number of input control signals and output currents in the arrangements 100 and 100' and the number of LED arrays for the arrangement 100' may be any number greater than or equal to two. In other words, the driver 120 is configured to receive two or more input control signals 115 and to provide respective two or more output currents 125. Similarly, in the arrangement 100' the two or more output currents 125 are coupled to respective two or more LED arrays 170. Hence, the driver 120 may be used to drive the two or more LED arrays 170.

[0023] Further exemplifying arrangements are schematically illustrated in Figures 9 and 10. An arrangement 400 depicted in Figure 9 employs a single input control signal 115' and a single output current 125', whereas an arrangement 500 depicted in Figure 10 employs a single input control signal 125' and a plurality of output currents 125-i. These arrangements and operation of the driver therein are described in more detail later in this document.

[0024] The controller entity 110 may be provided as a single control entity providing the input control signals 115. Alternatively, although depicted as a single entity in Figures 1a and 1b, the controller entity 110 may comprise a number of control entities that are configured to operate independently of each other, each control entity providing at least one of the input control signals 115-1, 115-2, ..., 115-n. The controller entity 110 may be arranged to issue the control signals 115 in response to a user input via a user interface and/or in response to a further control signal received at the controller entity 120 from a further entity. The controller entity 110 may also be a sensor, such as a PIR sensor or a light sensor, and it may be arranged to issue the control signals 115 in response to sensor measurements.

[0025] Hence, the controller entity 110 may be applied e.g. to control operation of an arrangement comprising the driver 120 and the single LED array 170' or to control operation of an arrangement comprising the driver 120 and the two or more LED arrays 170. Moreover, the controller entity 110 may be applied to control e.g. a plurality of drivers 120, each driver arranged to drive one or more LED arrays.

[0026] The input control signals 115 may be provided in a number of ways and/or in a number of formats. Typically, however, the input control signal 115 is provided as a command or request in accordance with a lighting control protocol. As an example in this regard, the input control signal 115 may be provided as a control signal providing one or more commands according to the Digital Addressable Lighting Interface (DALI) protocol specified in Appendix E.4 of the International Electrotechnical Commission (IEC) standard 60929, in other words as one or more DALI commands. A DALI command provided in an input control signal 115-i may e.g. specify a desired or requested light intensity level associated with the respective output current 125-i, thereby implying a request for a certain average current for the respective output current 125-i, which may be converted into a corresponding duty cycle in the driver 220, as will be described in more detail hereinafter.

[0027] As a further example, an input control signal 115-1, 115-2, ..., 115-n may be provided as a control signal comprising one or more commands according to the 1-10 V lighting control signaling, as described/specified in Appendix E.2 of the International Electrotechnical Commission (IEC) standard 60929. In such a signal the voltage of the input control signal 115-i may serve as an indication or as a request of the desired light intensity level associated with the respective output current 125-i implying a request for a certain average current for the respective output current 125-i, as will be described in more detail hereinafter. Figure 2 schematically illustrates some components of a driver 220. The driver 220 comprises a control portion 230 for issuing control signals 235-1, 235-2, ..., 235-n to control provision of respective driving currents 245-1, 245-2, ..., 245-n. The driver 220 further comprises power converter portions 240-1, 240-2, ..., 240-n for converting the operating power 117 supplied thereto into said respective driving currents 245-1, 245-2, ..., 245-n. The power converter portions 240-i serve as power source portions for providing the respective driving currents 245-i. The driving currents 245 may be provided as separate output currents of the driver 220, possibly via an output current portion (not shown) arranged to derive the output currents 125 on basis of the driving currents 245. The driver 220 may operate e.g. as the driver 120 of the arrangement 100 or 100', and hence

the driving currents 245 may be provided e.g. as output currents 125 of the arrangement 100 or 100'.

[0028] The control portion 230 is, preferably, configured to issue the control signals 235-i as suitable signals exhibiting a duty cycle D_i at the cycle frequency f_{ctrl}. An example of such a signal is a PWM signal exhibiting the duty cycle D_i at the cycle frequency f_{ctrl}. Figure 3 provides an example of a PWM signal, i.e. a square wave signal consisting of a sequence of cycles, each cycle having an active period (active state, 'high' state) of duration t_{on}, a non-active period (non-active state, 'low' state) of duration t_{off}, and overall duration t_c. The cycle duration t_c can be, alternatively, expressed as respective cycle frequency $f_c = 1 / t_c$ indicating the number of cycles per second. The duty cycle D may hence be expressed as $D = t_{on} / t_c = t_{on} * f_c$. The 'high' state may be provided e.g. as a voltage/current that is greater than or equal to a predetermined high threshold current while the 'low' state may be provided e.g. as a voltage/current that is smaller than or equal to a predetermined low threshold. As a specific example, assuming positive value of the high threshold, the low threshold may be set to zero.

[0029] Instead of a PWM signal, a signal of other type exhibiting the desired duty cycle D_i may be employed as the control signal 235, e.g. a square wave signal that does not exhibit strictly constant cycle duration t_c and therefore may not qualify as a PWM signal according a strict interpretation of the term PWM signal. As another alternative, the control signal 235 may be provided as a PWM-type signal consisting pulses (i.e. active periods exhibiting the 'high' state) having shape different from square waves at the desired duty cycle D_i.

[0030] The duty cycle D_i is, preferably, set in accordance with the respective input control signal 115-i. The duty cycles D_i may be the same across all control signals 235 or the duty cycles D_i may vary from one control signal 235 to another. In case the input control signal 115-i is provided or received as one or more DALI commands specifying or requesting a certain light intensity level for the output current 125-i, the control portion 230 may be configured to apply a predetermined mapping function to convert the specified/requested light intensity level into the duty cycle D_i for the corresponding control signal 235-i. Along similar lines, in case the input control signal 115-i is provided or received as one or more commands according to the 1-10 V lighting control signaling specifying or requesting a certain light intensity level or a certain average current for the output current 125-i, the control portion 230 may be configured to apply a(nother) predetermined mapping function to convert the specified/requested light intensity level into the duty cycle D_i for the corresponding control signal 235-i.

[0031] The control signals 235 may employ a fixed predetermined cycle frequency f_{ctrl}. The applied cycle frequency f_{ctrl} may be e.g. in the range 150 to 1000 Hz. The applied cycle frequency f_{ctrl} may be determined in accordance with the number of driving currents 245 employed by the driver 220. Alternatively, the control signals 235 may employ cycle frequency f_{ctrl} that is selected in accordance with the desired duty cycle, e.g. such that a lower duty cycle implies lower cycle frequency and vice versa. In case the applied cycle frequency f_{ctrl} is changed during operation of the driver, it is preferably changed simultaneously or essentially simultaneously for all control signals 245. As an example regarding dependence between the cycle frequency f_{ctrl} and the duty cycle(s) D_i applied in the control signals 235, the driver 220 may be configured to apply a first cycle f_{ctrl_H} frequency if the duty cycles D_i are greater than or equal to a predetermined threshold duty cycle D_{TH} and to apply otherwise a second cycle frequency f_{ctrl_L} that is lower than the first cycle frequency f_{ctrl_H}. As another example, the driver 220 may be configured to apply a mapping function for determining the cycle frequency f_{ctrl} on basis of the duty cycles D_i such that a lower duty cycle implies lower cycle frequency. In case different duty cycles D_i are applied for the control signals 235, the lowest duty cycle D_i among the control signals 235 may determine the cycle frequency applied in all control signals 235.

[0032] The control portion 230 is configured to issue the control signals 235-1, 235-2, ..., 235-n in predetermined time offsets with respect to each other. Providing the control signals 235-1, 235-2, ..., 235-n in suitably selected predetermined time offsets contributes to providing the respective output currents 125-1, 125-2, ..., 125-n in respective time offsets (or, broadly, in respective phase differences) in relation to each other. In this regard, the control signals 235 may be considered as synchronized control signals in the sense of employing the same or essentially similar cycle frequency f_{ctrl}. On the other hand, the control signals 235 are not time-aligned but exhibit said predetermined time offsets with respect to each other, such that the starting times of corresponding cycles of the control signals 235 are separated in time by the amount defined by the respective time offsets.

[0033] A purpose of such provision of the control signals 235 is to reduce or even eliminate the time periods during which none of the respective output currents 125 is in active state. Consequently, when the output currents 125 are coupled to drive the single LED array 170', the periods during which the LED array 170' is not providing light (i.e. the periods when none of the output currents 125 is in active state or, conversely, when all output currents 125 are in non-active state) are made shorter. Along similar lines, when the output currents 125 are coupled to drive the plurality of LED arrays 170 arranged in a single light fixture or luminaire, the periods during which the light fixture or luminaire is not providing light are made shorter. In particular, setting the control signals 235-i to employ suitable duty cycles D_i, suitable cycle frequency f_{ctrl} and suitable time offsets with respect to each other enables jointly employing the output currents 125-1, 125-2, ..., 125-n to drive the LED array(s) 170, 170' according to an effective duty cycle D_{out} at an effective cycle frequency f_{out} that is higher than the cycle frequency f_{ctrl} of the control signals 235 e.g. to cause the LED array(s)

170, 170' to provide light at desired light intensity level (corresponding to the effective duty cycle D_{out}), e.g. to provide desired dimming of light provided by the LED array(s) 170, 170'. A particular advantage arising from such an approach is that the LED arrays 170, 170' can be effectively driven according to a high cycle frequency while still employing a low cycle frequency for deriving each of the individual output currents 125-i.

[0034] The time offsets may be expressed directly as time (e.g. in milliseconds or nanoseconds) or e.g. in relation to the overall cycle duration t_c as a percentage of cycle duration. The time offset between the control signals 235 may be also referred to as phase differences between the control signals 235. In this regard, the terms phase and phase difference are used in a broad sense, indicating the degree of time difference t_{diff} between two control signals 235 in relation to the overall cycle duration t_c as 'angle' φ in the range 0 ... 360° such that the time difference $t_{diff} = (\varphi / 360°) * t_c$.

[0035] Provision of the control signals 235-1, 235-2, ..., 235-n in advantageous time offsets (or time differences, phase differences) with respect to each other and the relationship between the duty cycles D_i and the cycle frequency f_{ctrl} applied in the controls signals 235-i and the resulting effective duty cycle D_{out} and the effective cycle frequency f_{out} is discussed in detail hereinafter.

[0036] The control portion 230 may be configured to issue the control signals 235 independently of each other, thereby directly providing two or more control signals 235 exhibiting desired time offsets with respect to each other.

[0037] As another example, the control portion 230 may be configured to issue a single source control signal and to apply time-shifting to the single source control signal to generate the two or more control signals 235 exhibiting the desired time offsets with respect to each other, i.e. two or more synchronized control signals 235 exhibiting desired time offsets between each other. In particular the single source control signal may constitute as such one of the control signals 235, whereas the other control signals 235 are generated by time-shifting. As a variation of this example, instead of a single source control signal there may be a number of source control signals that are time-shifted to generate the two or more control signals 235 exhibiting the desired time offsets with respect to each other.

[0038] As a further example in this regard, the control portion 230 may be configured to issue two or more synchronized and time-aligned source control signals where the corresponding cycles of the control signals 235 coincide in time, and to apply time-shifting to at least one of these synchronized source control signals in order to provide the two or more control signals 235 exhibiting predetermined time offset with respect to each other. In practice, this may include providing one of the synchronized source control signals as such as the respective control signal 235 while the other one or more synchronized source control signals are time-shifted to introduce the desired time offsets with respect to the non-shifted synchronized source control signal.

[0039] Quite obviously, in case of the desired duty cycle D_i for all control signals 235 being 100 %, issuing the control signals in different phases is likely not to make any difference in characteristics of light provided by the LED array 170' or by the plurality of LED arrays 170. The same applies also for the case where there is only a single control signal 235 for which the desired duty cycle D_i that is less than 100 %, Hence, the control portion 230 may be configured to issue the control signals 235 in different phases (only) in response to the desired duty cycles D_i being less than 100 % for more than two control signals 235.

[0040] The power converter portions 240-i may be provided as switched-mode converters configured to convert the operating power 117 provided as input thereto at a first voltage into respective driving currents 245-i. A switched mode converter may be embodied as a buck converter or another suitable converter for converting a first DC voltage into a second DC voltage according to desired voltage conversion characteristics. Such power converters are known in the art. Each of the power converter portions 240-i is preferably configured to provide, when enabled, the respective driving current 245-i at constant or essentially constant predetermined level. Moreover, each of the power converter portions 240-i is typically arranged to provide the driving current at the same or at similar level. Alternatively, the power converter portions 240-i may be configured to provide, when enabled, constant or essentially constant output voltage.

[0041] As an example in this regard, each power converter portion 240 may be embodied as a buck converter. Figure 4 schematically illustrates a buck converter arranged to drive the LED array 170-i. This exemplifying buck converter receives the operating power via the input V_{in} and comprises a switch S, a diode D, an inductor L and a capacitor C. The driving circuitry DRV is arranged to operate, i.e. to periodically open and close at a frequency significantly higher than the cycle frequency f_{ctrl}, the switch S in a suitable manner in order to result in a desired output current to be provided via the inductor L to the LED array 170-i exemplifying a load coupled to the exemplifying buck converter. Suitable driving circuits DRV are known in the art, and further details regarding the operation logic of the driving circuit DRV are outside the scope of the present invention.

[0042] The control signal 235-i may be provided as an input to the driving circuitry DRV of the buck converter serving as the power converter portion 240-i, and the driving circuitry DRV is configured to operate the switch S to provide the respective driving current 245-i during active periods of the control signal 235-i, while on the other hand the driving circuitry DRV is configured to keep the switch S in open state during non-active periods of the control signal 235-i, thereby providing the driving current 245-i as zero current or current that is essentially zero. In other words, the control signal 235-i causes the power converter portion 240-i to enable and disable pro-

vision of the driving current 245-i in accordance with the control signal 235-i. Consequently, the driving current 245-i exhibits alternating active and non-active periods following or at least approximating the duty cycle D_i and the cycle frequency f_{ctrl} of the control signal 235-i. Moreover, also the phase of the driving current 245-i follows that of the control signal 235-i in relation to the phases of the driving currents 245 derived in control of the other control signals 235. Hence, during active periods the driving currents 245-i exhibit the constant (predetermined) current, whereas during non-active periods the driving currents 245-i exhibit zero current or current that is essentially zero, resulting in an average current corresponding to the requested light intensity level.

[0043] As pointed out hereinbefore, the control portion 230 is configured to issue the control signals 235 such that they exhibit predetermined time offset with respect to each other. In particular, the control portion may be configured to issue the control signals 235 in evenly distributed time offsets. In other words, the time offsets for the control signals 235 are preferably set such that they are evenly distributed over the total cycle duration t_c. In other words, assuming that the driver 220 is arranged to provide N driving currents 245, the control portion 230 may be configured to issue the control signals 235-i, where i = 1 ... N in phases (i - 1) * (360° / N). Timing-wise, the even distribution of phases among the N control signals 235-i results in respective cycles to commence at temporal intervals of $t_{diff} = t_c / N$. Consequently, assuming a cycle in the control signal 235-1 commencing at time t_0, the corresponding cycle commences in control signals 235-i at $t_i = t_0 + (i\text{-}1) * t_{diff}$.

[0044] As an example, in case of N=2 the time offset between the two control signals 235-1 and 235 is 50 % (or t_c / 2), the two controls signals 235-1 and 235-2 may be considered to be in opposite phases. This also implies time offsets evenly distributed over the overall duration of the cycle t_c. If using the phase shift (or phase difference) as the measure in this regard, the two control signals 235-1 and 235-2 exhibit phase difference of 180°, thereby setting the two controls signals 235-1 and 235-2 in opposite phases. As another example, in case of N=4 the phases of the four control signals 235-1 to 235-4 may be issued in time offsets of 25 % (i.e. t_c / 4) to provide even distribution over the overall cycle duration t_c, thereby corresponding to phases set into 90° intervals.

[0045] The effect of evenly distributed phases is illustrated in Figure 5a by using N=2 as an example. The curve (a) of Figure 5a indicates a first control signal employing a first duty cycle $D_1 = t_{on1} / t_c$ and a cycle frequency f_{ctrl} corresponding to cycle duration t_c, the curve (b) indicates a second control signal employing a second duty cycle $D_2 = D_1$ (with $t_{on2} = t_{on1}$) at the cycle frequency f_{ctrl}, which in this example is approximately 16.7 %. The first and second control signals 'take turns' in providing active periods, the curve (c) indicates the combined effect of the first and second control signals. Applying the time offset of t_c / 2 for these two exemplifying control signals results in the combined effect of the first and second controls signals resulting in duty cycle $D_{sum} = D_1 + D_2 = 2 * D_1$ and the cycle duration $t_{c\text{-}sum} = t_c / 2$ hence implying the cycle frequency $f_{sum} = 2 * f_{ctrl}$, as also comparison of the curves (a) and (b) to the curve (c) of Figure 5a indicates. Consequently, the resulting duty cycle D_{sum} is approximately 33.3 %. This also generalizes into any number of N control signals employing the same duty cycle D at the same cycle frequency f_{ctrl}, resulting in a combined effect amounting to the duty cycle $D_{sum} = N * D$ and the cycle frequency $f_{sum} = N * f_{ctrl}$.

[0046] Since, as described hereinbefore, the driving currents 245-i follow the duty cycle D_i, the cycle frequency f_{ctrl}, and the phase of the respective control signals 235-i, the output currents 125-i derived on basis of the driving currents 245 and coupled to the single LED array 170' (as illustrated in context of the arrangement 100) may be employed to drive the LED array 170' at an effective duty cycle D_{out} approximating the duty cycle D_{sum} and at an effective cycle frequency f_{out} that approximate the cycle frequency f_{sum}. Along similar lines, the output currents 125-i coupled to the LED arrays 170-i, respectively (as illustrated in context of the arrangement 100') may be employed to drive a luminaire comprising the LED arrays 170-i at the effective duty cycle D_{out} approximating the duty cycle D_{sum} and at an effective cycle frequency f_{out} that approximates the cycle frequency f_{sum}. A benefit of such an approach is that it allows increasing the effective cycle frequency provided in the output currents 125-i without the need to increase the cycle frequency applied in the control signals 235-i. Thus, any flicker in the resultant light is at a higher frequency, while the accuracy of the light intensity control is not compromised. To further illustrate the effective duty cycle D_{out} and the effective cycle frequency f_{out} in the output currents 125-i, the curve (d) of Figure 5a schematically illustrates the variations in the level of the sum of output currents 125 (denoted as I_{125} in Figure 5a) provided to the single LED array 170' or to the LED arrays 170-i on basis of the first and second control signals.

[0047] Figure 5b provides another example of evenly distributed phases, again by using N=2 as an example. This example corresponds to the example of Figure 5a with the difference that the duty cycle $D_2 = D_1$ is approximately 67.7 %, as illustrated by curves (a) and (b). Consequently, as the resulting variation in the level of sum of the output currents 125 illustrated in curve (c) indicates, the effect for the cycle frequency is actually the same as in the example of Figure 5a, i.e. the cycle frequency is doubled to $f_{sum} = 2 * f_{ctrl}$. On the other hand, the combined signal is continuously in the active state, although there signal level varies periodically at the cycle frequency $f_{sum} = 2 * f_{ctrl}$. Consequently, the duty cycle D_{sum} in the combined signal may be considered to be 100 %. This generalizes into any number of N control signals employing the same duty cycle D at the same cycle frequency f_{ctrl}, resulting in a combined effect amounting to the duty cycle $D_{sum} = \max(100\ \%, N * D)$ and the cycle frequency f_{sum}

= $N * f_{ctrl}$. If arranged to drive the single LED array 170', the sum of output currents 125, as indicated by the curve (c) of Figure 5b, exhibits periodic variation, which may, consequently, result in corresponding variation in the color or color temperature of the light provided by the single LED array 170'. Along similar lines, if arranged to drive the plurality of LED arrays 170 in a luminaire, the momentary lighting level provided by the luminaire may exhibit variation in intensity of light provided by the LED arrays 170 in accordance with the variation in the sum of the output currents 125.

[0048] Figure 6a provides a further example. Also in this case N=2 and the phases are evenly distributed by setting the time offsets such that the beginnings of the non-active periods in the two control signals are offset by t_c / 2. In other words, in this example the beginning of a non-active period of a cycle serves as a reference point in determination of the time offsets between the control signals. The difference to the example of Figures 5a and 5b is that the first control signal employs the first duty cycle D_1 and the cycle frequency f_{ctrl} (curve (a)) while the second control signal employs a second duty cycle $D_2 \neq D_1$ (with $t_{on2} \neq t_{on1}$) at the cycle frequency f_{ctrl} (curve (b)). The combined effect of the first and second control signals now exhibits cycles of fixed duration $t_{c\text{-sum1}} = t_{c\text{-sum2}} = t_c / 2$ implying the cycle frequency $f_{sum} = 2 * f_{ctrl}$, while the duty cycle alternates between $D_{sum1} = t_{on1} / t_{c\text{-sum1}}$ and $D_{sum2} = t_{on2} / t_{c\text{-sum1}}$, and the corresponding effect can be seen in the sum of the output currents schematically illustrated in curve (c). However, over a pair of such cycles - and in general over a plurality of pairs of such cycles - the (effective) duty cycle D_{sum} of the combined effect becomes $D_{sum} = D_1 + D_2$ as in case illustrated in context of Figure 5a despite the different duty cycles D_1 and D_2 employed in the first and second control signals. This generalizes into any number of N control signals employing the different duty cycles D_i at the same cycle frequency f_{ctrl}, resulting in a combined effect that amounts to the duty cycle $D_{sum} = D_1 + D_2 + ... + D_N$ and the cycle frequency $f_{sum} = N * f_{ctrl}$.

[0049] Figure 6b provides yet another example in this regard. Also in this case N=2 and the phases are evenly distributed by setting the time offsets such that the beginnings of the active periods in the two control signals are offset by t_c / 2. Hence, the difference to the example of Figure 6a is that the reference point for determining time offset is in the beginning of an active period instead of in the beginning of a non-active period. Also in this case the combined effect of the first and second control signals now exhibits cycles of fixed duration $t_{c\text{-sum1}} = t_{c\text{-sum2}} = t_c / 2$ implying the cycle frequency $f_{sum} = 2 * f_{ctrl}$, while the duty cycle alternates between $D_{sum1} = t_{on1} / t_{c\text{-sum1}}$ and $D_{sum2} = t_{on2} / t_{c\text{-sum1}}$, and the corresponding effect can be seen in the sum of the resulting output currents schematically illustrated in curve (c). Consequently, the (effective) duty cycle D_{sum} of the combined effect becomes $D_{sum} = D_1 + D_2$ as in case illustrated in context of Figures 5a and 6a despite the different duty cycles D_1 and D_2 employed in the first and second control signals. This generalizes into any number of N control signals employing the different duty cycles D_i at the same cycle frequency f_{ctrl}, resulting in a combined effect causing the duty cycle $D_{sum} = D_1 + D_2 + ... + D_N$ and the cycle frequency $f_{sum} = N * f_{ctrl}$.

[0050] Figure 7 provides yet another example in this regard by using N=2. As in the example of Figure 6, the first control signal employs the first duty cycle D_1 and the cycle frequency f_{ctrl} (curve (a)) while the second control signal employs a second duty cycle $D_2 \neq D_1$ (with $t_{on2} \neq t_{on1}$) at the cycle frequency f_{ctrl} (curve (b)). The phases of the first and second control signals are in this example evenly distributed by using the mid-points of an active period of a cycle as the reference point for determining the time offsets and by setting the time offsets such that the mid-points of the active-periods in the two control signals are offset by t_c / 2. The combined effect of the first and second control signals now exhibits cycles having duration that alternates between $t_{c\text{-sum1}}$ and $t_{c\text{-sum2}}$ where $t_{c\text{-sum1}} \neq t_{c\text{-sum2}}$ as can be seen in the sum of the resulting output currents schematically illustrated in curve (c). Regardless, the cycle frequency over the pair of cycles - and in general over a plurality of pairs of such cycles - is $f_{sum} = 2 * f_{ctrl}$ while the duty cycle alternates between $D_{sum1} = t_{on1} / t_{c\text{-sum1}}$ and $D_{sum2} = t_{on2} / t_{c\text{-sum1}}$. The duty cycle over a pair of such cycles and/or over a plurality of pairs of such cycles is again $D_{sum} = D_1 + D_2$ as in case illustrated in context of Figures 5a, 5b, 6a and 6b despite different duty cycles D_1 and D_2 and different phase alignment between the control signals. Hence, also this generalizes into any number of N control signals employing the different duty cycles D_i at the same cycle frequency f_{ctrl}, resulting in a combined effect amounting to the duty cycle $D_{sum} = D_1 + D_2 + ... + D_N$ and the cycle frequency $f_{sum} = N * f_{ctrl}$.

[0051] While the above examples employ even distribution of the time offsets over the duration of the cycle at of the controls signals 235, distribution different from the even one may be applied. As an example in this regard, small variation or ripple in time offsets between the control signals 235 may be allowed. As another example, the time offsets between the control signals 235 may be set to differ from each other according a predetermined rule such that the resulting distribution of phases over the total duration of the cycle t_c is not even.

[0052] Therefore, the controller entity 110 may be arranged to provide the control signals 115 to cause the control portion 230 to set the duty cycles D_i to values whose sum is equal to or approximates the desired effective duty cycle D_{out}. As an example, the input control signals 115 may be arranged to request the driver 220 to provide the same duty cycle D_i, determined by dividing the desired effective duty cycle D_{out} by the number of power converter portions 240 applied in the driver 220.

[0053] As already pointed out in context of Figure 5b, the above considerations regarding the sum of the duty cycles D_{sum} serving as an indication of the effective duty

cycle D_{sum} that can be obtained as combination of the output currents 125-i fully applies for the scenario where the active periods of the control signals 235 (and hence the active periods of the driving currents 245) do not overlap in time. On the other hand, in case there is temporal overlap between the active periods of the control signals 235, the resulting effective duty cycle D_{out} may be smaller than the sum of the duty cycles D_{sum}. In particular, in case the input control signals 115 causing the control portion 230 to set the duty cycles D_i to values whose sum is greater than 100 %, the resulting effective duty cycle will be 100 %. Regardless, even in case of partial temporal overlap between the active periods of the output currents 125 the periods during which none of the respective output currents 125 is in active state are shortened and/or made less frequent, and hence the periods during which the LED array 170' is or the plurality of LED arrays 170 are not providing any light are likewise shortened and/or made less frequent.

[0054] As indicated by the examples provided hereinbefore, with suitable phase differences between the control signals 235, *N* power converter portions 240 may be employed to provide *N* driving currents 245 in order to enable increasing the cycle frequency f_{ctrl} applied within the driver 220 to provide the individual driving currents 245 by the factor *N* into the effective cycle frequency $f_{sum} = N * f_{ctrl}$ Hence, using *N*=2 already enables doubling the cycle frequency from that applied within the driver to provide the individual driving currents 245, thereby providing a significant advantage over a conventional approach. Hence, the appropriate number of the power converter portions may be selected e.g. in view of the applied or applicable cycle frequency f_{ctrl} in relation to the desired or required effective cycle frequency f_{sum}. This selection may be made (further) in view of limitations with respect to the physical size of the driver 220, standards or regulations prohibiting the light provided by the LED light sources from flickering at a certain frequency or within a certain range of frequencies, etc.

[0055] Figure 8 schematically illustrates some components of a driver 320. A number of components of the driver 320 are similar to the corresponding components of the driver 220. In particular, the control portion 230 and the power converter portions 240 are configured to operate in a manner described in context of the driver 220. Like the driver 220, also the driver 320 may operate e.g. as the driver 120 of the arrangement 100 or 100', and hence the driving currents 245 of the driver 320 may be provided e.g. as output currents 125 of the arrangement 100 or 100'.

[0056] A difference to the driver 220 is that in the driver 320 the control signals 235-1, 235-2, ..., 235-n issued by the control portion 240 are provided to control respective switches 350-1, 350-2, ..., 350-n arranged to control provision of the respective driving currents 245-1, 245-2, ..., 245-n for the output of the driver 320. In particular, the control signal 245-i is arranged to control the respective switch 350-i such that the switch 350-i is kept closed during active periods of the control signal 235-i while the switch 350-i is kept in open state during non-active periods of the control signal 235-i. In other words, the switches 350-i are controlled to enable or disable provision of the respective driving current 245-i as the output current 115-i of the driver 320. Consequently, the respective driving current 245-i, as provided to the output of the driver 320, is caused to exhibit alternating active and non-active periods following or at least approximating the duty cycle D_i and the cycle frequency f_{ctrl} of the control signal 235-i. Moreover, also the phase of the driving current 245-i follows that of the control signal 235-i in relation to the phases of the driving currents 245 derived in control of the other control signals 235. Therefore, during active periods the driving currents 245-i exhibit the constant (predetermined) current, whereas during non-active periods the driving currents 245-i exhibit zero current or current that is essentially zero, resulting in an average current corresponding to the requested light intensity level,

[0057] Figure 13 schematically illustrates some components of a driver 620. A number of components of the driver 620 are similar to the corresponding components of the drivers 220 and 320. In particular, the control portion 230 is configured to operate in a manner described hereinbefore in context of the driver 220 and/or, 320. Like the drivers 220 and 320, also the driver 620 may operate e.g. as the driver 120 of the arrangement 100 or 100', and hence the driving currents 245 of the driver 620 may be provided e.g. as output currents 125 of the arrangement 100 or 100'.

[0058] Instead applying the power converter portions 240, the driver 620 comprises a voltage source portion 640 serving as a power source portion for providing the driving currents 245-i. The voltage source portion 640 is configured to provide constant or essentially constant driving voltage for provision of the driving currents 245-i. On the other hand, like the driver 320, also the driver 620 comprises the switches 350-i arranged to control provision of the respective driving currents 245-i in control of the respective control signal 245-i: along the lines described for the driver 320, also in the driver 620 the control signal 245-i is arranged to control the respective switch 350-i such that the switch 350-i is kept closed during active periods of the control signal 235-i while the switch 350-i is kept in open state during non-active periods of the control signal 235-i, thereby resulting in the respective driving currents 245-i exhibiting alternating active and non-active periods following or at least approximating the duty cycle D_i, the cycle frequency f_{ctrl} and phase of the control signal 235-i. Hence, during active periods the driving currents 245-i exhibit the driving voltage, while during non-active periods the driving currents 245-i exhibit voltage that is zero or essentially zero, thereby resulting in an average voltage corresponding to the requested light intensity level. The driving currents 245-i are provided as respective output currents 125-i of the driver 620.

[0059] The voltage source portion 640 may comprise a single power converter portion arranged to provide the constant driving voltage for provision of the driving currents 245-i on basis of the operating power 117 supplied to the driver 620. The single power converter portion may be provided e.g. as a switched-mode converters configured to convert the operating power 117 provided at a first voltage into the predetermined (constant) driving voltage. Also in this context, the switched mode converter may be embodied as a buck converter or another suitable converter for converting a first DC voltage into a second DC voltage according to desired voltage conversion characteristics. General operation of a buck converter is well known for a person skilled in the art - and also briefly described in context of the power converter portions 240. However, in context of the driver 620 the buck converter may be operated independently of the control signal 235-i, i.e. the driving circuit DRV is arranged to continuously operate the switch S to cause the buck converter to provide the driving voltage.

[0060] Instead of applying the power converter portion, the operating power 117 supplied to the driver 620 may be provided directly at the desired driving voltage. Consequently, the voltage source portion 640 may be arranged to pass the input voltage as the driving voltage for provision of the driving currents 245-i and the voltage source portion 640 may hence be provided without power converter portion.

[0061] Figure 9 schematically illustrates a third exemplifying arrangement 400 as a variation of the first arrangement 100. The difference to the arrangement 100 is that a controller entity is arranged to issue a single input control signal 115' instead of the input control signals 115-i applied in the arrangement 100, while a driver 420 of the arrangement 400 is arranged to receive the single input control signal 115' and to provide a single output current 125' instead of the output currents 125-i applied in the arrangement 100.

[0062] Figure 10 schematically illustrates a fourth exemplifying arrangement 500 as another variation of the first arrangement 100. As in the arrangement 400, the difference to the arrangement 100 is that the controller entity 410 is arranged to issue the single input control signal 115'. While illustrated in Figure 10 as variation of the arrangement 100, respective variations may be provided on basis of the arrangement 100' as well.

[0063] The drivers 420 and 520 may be provided e.g. as a variation of any of the drivers 220, 320 and 620 described hereinbefore. The difference to the drivers 220, 320 and 620 is that due to receiving the single input control signal 115' (instead of the plurality of control signals 115), the control portion 230 is configured to derive the duty cycles D_i to be applied in the respective control signals 235-i on basis of the characteristics of the single input control signal 125'. For the driver 420 a further difference to the drivers 220, 320 and 620 is that the driver 420 comprises an output portion configured to combine the driving currents 245 into a single output current 125', thereby providing the single output current 125' as a combined signal employing the effective duty cycle D_{out} at the effective cycle frequency f_{out} in accordance with the duty cycles D_i, the cycle frequency f_{ctrl} and the time offsets introduced to the control signals 245-i.

[0064] The drivers 420 and 520 are advantageous in that they may be provided as entities employing a smaller number of input lines for provision the input control signal(s) compared to drivers 220, 320 and 620.

[0065] As described hereinbefore in context of the plurality of input control signals 115, as an example, the single input control signal 115' may provide one or more DALI commands or one or more commands according to the 1-10 V lighting control signaling specifying or requesting a desired light intensity level to be provided by (the combination of) the output currents 125 or by the single output current 125'. The control portion 230 may be configured to apply respective predetermined mapping function to determine the corresponding desired duty cycle D_{in} on basis of the specified/requested light intensity level. The control portion 230 may be configured to derive the duty cycles D_i for the respective control signals 235-i on basis of the value D_{in}. Some examples of mapping a command or request received in the single input control signal 115' are described in the following.

[0066] As an example, the single input control signal 115' may provide a DALI command or a command according the 1-10 V lighting control signaling addressed to the driver 420 or 520 as a whole, the command indicating a request to provide a desired light intensity level by the single output current 125' or the desired light intensity level by (the sum of) the plurality of output currents 125. In such an arrangement the control portion 230 may be configured to apply a (respective) predetermined mapping function to determine the duty cycle D_{in} corresponding to the requested light intensity level, to select the duty cycles D_i for the respective control signals 235-i on basis of the value D_{in} e.g. such that the sum of the duty cycles D_i equals to D_{in}, and to issue the control signals 235-i at respective duty cycles. Hence, in such a scenario the driver 420 or 520 is provided with an indication of the desired light intensity level, while the control logic required to determine the actually applied duty cycles D_i in the individual control signals 245-i is located in the control portion 230. The operation of the driver 420 or 520 otherwise follows that of the driver 220 or 320 e.g. within framework of the arrangement 100 or the arrangement 100'. The control portion 230 may be configured to set duty cycles D_i such that their sum equals to the duty cycle D_{in}, e.g. such that $D_i = D_{in} / N$, where N denotes the number of driving currents 245 applied in the driver 420 or 520. If the driver 420 or 520 is configured to distribute the time offsets evenly or essentially evenly over the overall cycle duration t_c, this serves to ensure that only one of the output currents 125-i is active at any given moment of time, thereby contributing to the resulting color or color temperature of light provided by the single LED array 170' being perceived by a human observer as con-

stant or essentially constant.

[0067] Alternatively, for the driver 520, the single input control signal 115' providing a DALI command or a command according the 1-10 V lighting control signaling addressed to the driver 420 or 520 as a whole may indicate a request to provide the desired light intensity level in each of the output current 125-i. Consequently, the determined duty cycle D_{in} corresponding to the requested light intensity level may be applied as the duty cycle D_i for each of the control signals 235-i. Since in such a scenario the light intensity levels provided by the output currents 125-i are individually controlled outside the driver 520, the entity providing the requests (e.g. the control entity 110) is responsible for requesting the light intensity levels for the output currents 125-i such that their combined contribution results in desired overall light intensity level.

[0068] As another example, in the driver 520 a separate DALI address may have been assigned to each output current 125-i, and the single input control signal 115' may provide a DALI command addressed to a certain output current 125-i or two or more DALI command addressed to respective two or more output currents 125-i, each command indicating a request to provide a desired light intensity level by the respective driving current 245-i. In such an arrangement the control portion 230 may be configured to apply a (respective) predetermined mapping function to determine the duty cycle D_i corresponding to the requested light intensity level for the driving current 245-i, and to issue the control signals 235-i at respective duty cycles. In such a scenario the control logic for selecting the desired light intensity levels is located outside the driver 520 (e.g. in the controller entity 110), whereas the control logic required to determine the actually applied respective duty cycles D_i is located in the control portion 230 of the driver 520. As in the previous example, also in this scenario the output currents of the driver 520 follow the commands/requests received in the input control signal 115', and hence the requesting entity (e.g. the control entity 110) is responsible for requesting the light intensity levels for the output currents 125-i such that their combined contribution results in desired overall light intensity level.

[0069] The operations, procedures and/or functions assigned to the structural units described in the context of the driver 220, 320, 420, 520, 620 may be provided as steps of a method. As an example, such a method for driving one or more light emitting diodes 170, 170' may be carried out by a driver apparatus, the driver apparatus comprising one or more power source portions for providing two or more driving currents 245, the method comprising issuing two or more control signals 235 for controlling the provision of two or more driving currents 245, each control signal 235 exhibiting a respective duty cycle D_i at a first cycle frequency f_{ctrl}, wherein the two or more control signals 235 are synchronized control signals exhibiting predetermined time offsets with respect to each other for provision of the two or more driving currents 245 in different phases.

[0070] The control portion 230 of the driver apparatus 220, 320, 420, 520, 620 may be provided by hardware means, by software means, or by combination of hardware and software means. As a particular example, the control portion 230 may be provided as an integrated circuit (IC) or as a processor carrying out instructions stored in a memory, which instructions control provision of the control signals 235 as described hereinbefore. The IC or the processor may be provided with output lines (e.g. output pins) via which the control signals 235 are provided.

[0071] Figure 11 schematically illustrates an exemplifying apparatus 700 that may be employed for embodying at least the control portion 220 of the driver 220, 320, 420, 520, 620. The apparatus 700 comprises a processor 710 and a memory 720, the processor 710 being configured to read from and write to the memory 720. The apparatus 700 may further comprise further structural units or portions. Although the processor 710 is illustrated as a single component, the processor 710 may be implemented as one or more separate components. Although the memory 720 is illustrated as a single component, the memory 720 may be implemented as one or more separate components.

[0072] The memory 720 may store a computer program 750 comprising computer-executable instructions that control the operation of the apparatus 700 when loaded into the processor 710 and executed by the processor 710. As an example, the computer program 750 may include one or more sequences of one or more instructions. The computer program 750 may be provided as a computer program code. The processor 710 is able to load and execute the computer program 750 by reading the one or more sequences of one or more instructions included therein from the memory 720. The one or more sequences of one or more instructions may be configured to, when executed by one or more processors, cause the apparatus 700 to implement the operations, procedures and/or functions described hereinbefore in context of the control portion 220.

[0073] Hence, the apparatus 700 may comprise at least one processor 710 and at least one memory 720 including computer program code for one or more programs, the at least one memory 720 and the computer program code configured to, with the at least one processor 710, cause the apparatus 700 to perform the operations, procedures and/or functions described hereinbefore in context of the control portion 220.

[0074] Figure 12 schematically illustrates an example circuit 800 that may be employed for embodying the control portion 220 of the driver 220, 320, 420, 520, 620. The circuit 800 comprises three 'stages', arranged to derive the control signals $CTRL_1$, $CTRL_2$ and $CTRL_3$, respectively. Each of the control signals $CTRL_i$ is based on a source control signal $CTRL_{in}$ and the reference signal REF_i of the respective stage. The source control signal $CTRL_{in}$ may a control signal derived on basis of a com-

mand or request received in the single input control signal 115' or on basis of command(s) or request(s) received in the plurality of control signals 115, exhibiting duty cycle corresponding the command(s)/request(s) at selected cycle frequency. The control signals $CTRL_1$, $CTRL_2$ and $CTRL_3$ may be provided as the control signals 235.

[0075] The first two stages comprise an amplifier AMP_i, a resistor R_i and a capacitor C_i while the last stage comprises the AMP_i, where the index i denotes the stage number. In other words, the stages except the last one comprise the respective amplifier AMP_i, the respective resistor R_i and the respective capacitor C_i while the last 'stage' comprises the AMP_i. The resistor R_i and the capacitor C_i at each stage implement the so-called RC circuit known in the art. At each stage, the components corresponding to the resistor R_i and the capacitor Ci are selected to provide a desired delay in passing the input control signal $CTRL_{in}$ to the next stage, as described in more detail in the following.

[0076] Assuming the cycle frequency f_{ctrl} and hence the cycle duration $t_{ctrl} = 1 / f_{ctrl}$ the cycle duration can be divided by the number N of control signals to be provided from the circuit 800, i.e. in this example N=3, to determine the time shift that evenly distributes the phases of controls signals $CTRL_i$, i.e. as $t_{diff} = 1 / (f_{ctrl} * N)$. As known in the art, the capacitor of the RC circuit is fully charged after being connected to a voltage source for a period of $t_{RC} = 5 * \tau = 5 * R * C$. In contrast, the capacitor of the RC circuit is fully discharged after being disconnected from the voltage source for the period of t_{RC}. Therefore, in order to provide the even distribution of the phases of the control signals $CTRL_i$, the time shift t_{diff} should be equal to t_{RC}. This can be accomplished e.g. by selecting the resistors R_i and the capacitors C_i according to $C_i = 1 / (5 * R_i * f_{ctrl} * N)$ or by adjusting the f_{ctrl} to correspond to the resistors R_i and the capacitors C_i of predetermined values.

[0077] Consequently, when providing a control signal consisting of alternating active and non-active periods, such as a PWM signal or a variation thereof as described hereinbefore, the RC circuit in each stage i of the circuit 800 provides an intermediate signal corresponding to the shape of the input control signal $CTRL_{in}$, delayed by $(i-1) * t_{diff}$ to the amplifier AMP_i of the respective stage and to the next stage i+1 of the circuit 800. The amplifiers AMP_i, in turn, are arranged to generate the respective control signals $CTRL_i$ in accordance with the respective intermediate signal and the reference signal REFi.

[0078] As an example, assuming the cycle frequency 500 Hz and three stages as in the circuit 800, the relationship between the resistors R_i and the capacitors C_i becomes $C_i = 1 / (5 * R_i * f_{ctrl} * N) = 1 / (7500 * R_i)$. Consequently, if selecting e.g. $R_i = 100\ \Omega$, the capacitor C_i should be selected to have the capacitance $C_i = 1 / (7500 * 100) \approx 1.33\ \mu F$.

[0079] Although described above by employing equal time shift between two consecutive stages, thereby providing even distribution of phases, the above example generalizes into an arrangement where the time shift between two consecutive stages is not the same across stages. In such an arrangement the sum of time shifts over all stages is preferably the cycle duration $t_{ctrl} = 1 / f_{ctrl}$.

[0080] Moreover, the circuit 800 is illustrated hereinbefore with three stages, hence providing three control signals. However, the circuit 800 generalizes to any number of stages (two or more stages) and hence to any number (two or more) control signals $CTRL_i$. Moreover, with suitable selection of components for each of the stages, such a circuit may be arranged to provide desired number of control signals 235 exhibiting desired phase differences with respect to each other.

Claims

1. A driver apparatus for driving one or more light emitting diodes, the driver apparatus comprising
one or more power source portions for providing two or more driving currents, and
a control portion for issuing two or more control signals for controlling the provision of two or more driving currents, each control signal exhibiting a respective duty cycle at a first cycle frequency,
wherein the control portion is configured to issue the two or more control signals as synchronized control signals in predetermined time offsets with respect to each other for provision of the two or more driving currents in different phases.

2. A driver apparatus according to claim 1, wherein the control portion is configured to
issue at least one source control signal, and
apply time-shifting to said at least one source control signal to generate the two more control signals exhibiting said predetermined time offsets with respect to each other.

3. A driver apparatus according to claim 1 or 2, wherein the control portion is configured to issue the two or more control signals in evenly distributed time offsets.

4. A driver apparatus according to claim 3, wherein the driver apparatus is configured to provide a predetermined number N of driving currents and wherein the control portion is configured to issue the respective two or more control signals i = 1 ... N in time offsets of 1/N of the total cycle duration.

5. A driver apparatus according to any of claims 1 to 4, wherein the control portion is further configured to receive two or more commands or requests indicative of the requested light intensity levels for the respective driving currents derive duty cycles for the two or more control signals corresponding to the respective requested light intensity levels, and

issue the two or more control signals at respective derived duty cycles.

6. A driver apparatus according to any of claims 1 to 4, wherein the control portion is further configured to receive a single command or request indicative of the requested light intensity level for the two or more driving currents,
derive the duty cycles for the two or more control signals such that the sum of the duty cycles corresponds to the requested light intensity level, and issue the two or more control signals at respective derived duty cycles.

7. A driver apparatus according to any of claims 1 to 6, wherein said one or more power source portions comprise two or more power converter portions configured to convert operating power supplied to the driver apparatus into respective two or more driving currents, and wherein the control portion is configured to issue the two or more control signals to control respective two or more power converter portions to cause the respective power converter portion to enable and disable the provision of the driving current in accordance with the respective control signal.

8. A driver apparatus according to any of claims 1 to 6, wherein said one or more power source portions comprise two or more power converter portions configured to convert operating power supplied to the driver apparatus into respective two or more driving currents, and wherein the control portion is configured to issue the two or more control signals to control respective two or more switches arranged to enable and disable provision of the respective driving currents from the respective power converter portion in accordance with the respective control signal.

9. A driver apparatus according to any of claims 1 to 6, wherein said one or more power source portions comprises a voltage source portion configured to provide a constant driving voltage for provision of the two or more driving currents, and
wherein the control portion is configured to issue the two or more control signals to control respective two or more switches arranged to control provision of the driving voltage to provide the respective driving currents in accordance with the respective control signal.

10. A driver apparatus according to claim 9, wherein said voltage source portion comprises a power converter portion for converting an input voltage supplied to the driver apparatus into said driving voltage.

11. A driver apparatus according to any of claims 1 to 10, wherein the two or more control signals comprise a series of cycles, each cycle consisting of an active period and a non-active period in accordance with the respective duty cycle and the first cycle frequency.

12. A driver apparatus according to claim 11, wherein the two or more control signals are provided as pulse-width modulation signals.

13. A driver apparatus according to any of claims 1 to 12, wherein the apparatus is arranged to provide the two or more driving currents as two or more separate output currents of the driver apparatus.

14. A driver apparatus according to any of claims 1 to 11, wherein the apparatus further comprises an output current portion configured to combine the two or more driving currents into a single output current of the driver apparatus.

15. An arrangement comprising a driver apparatus according to claim 13 and two or more arrays of light emitting diodes, wherein each of the two or more separate output currents is coupled to a respective one of the two or more arrays of light emitting diodes.

16. An arrangement comprising a driver apparatus according to claim 13 and a single array of light emitting diodes, wherein the two or more separate output currents are coupled to the single array of light emitting diodes.

17. An arrangement comprising a driver apparatus according to claim 14 and a single array of light emitting diodes, wherein the single output current is coupled to the single array of light emitting diodes.

18. Use of a driver apparatus according to claim 13 to drive two or more arrays of light emitting diodes, wherein each of the two or more output currents is applied to drive a respective one of the two or more arrays of light emitting diodes.

19. Use of a driver apparatus according to claim 13 to drive a single array of light emitting diodes, wherein the two or more output currents are applied in parallel to drive the single array of light emitting diodes.

20. Use of a driver apparatus according to claim 14 to drive a single array of light emitting diodes, wherein the single output current is applied to drive the single array of light emitting diodes.

21. A computer program for driving one or more light emitting diodes, the computer program including one or more sequences of one or more instructions which, when executed by one or more processors, cause a driver apparatus comprising one or more power source portions for providing two or more driv-

ing currents to at least issue two or more control signals for controlling the provision of two or more driving currents, each control signal exhibiting a respective duty cycle at a first cycle frequency, wherein the two or more control signals are synchronized control signals exhibiting predetermined time offsets with respect to each other for provision of the two or more driving currents in different phases.

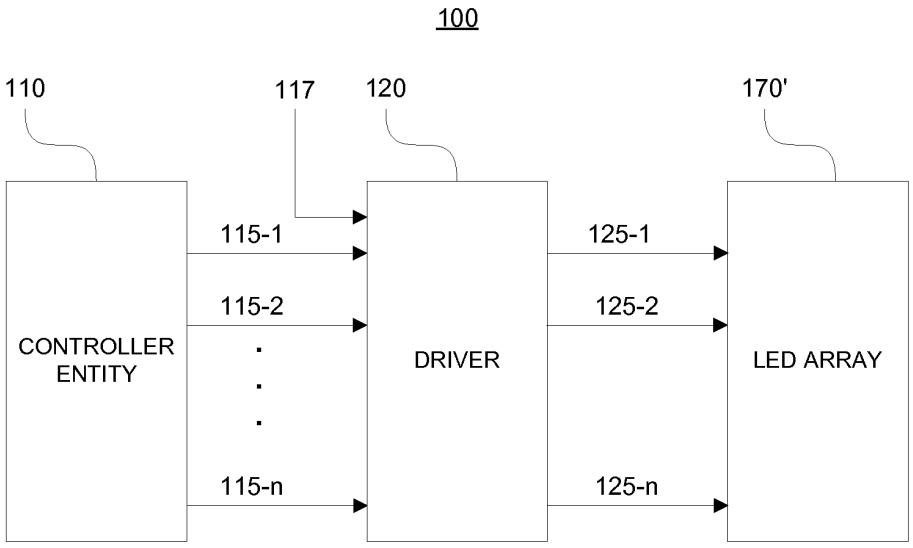


Figure 1a

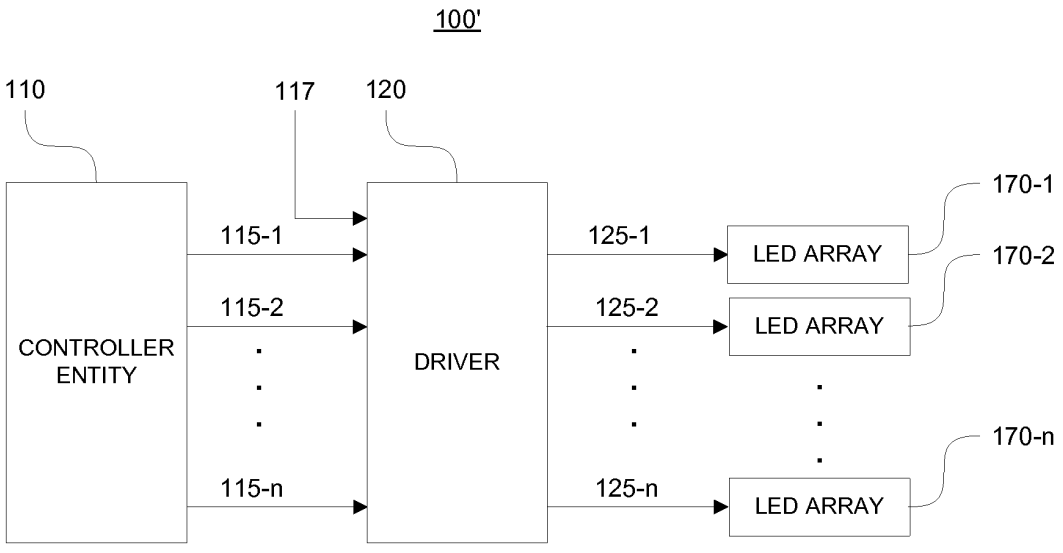


Figure 1b

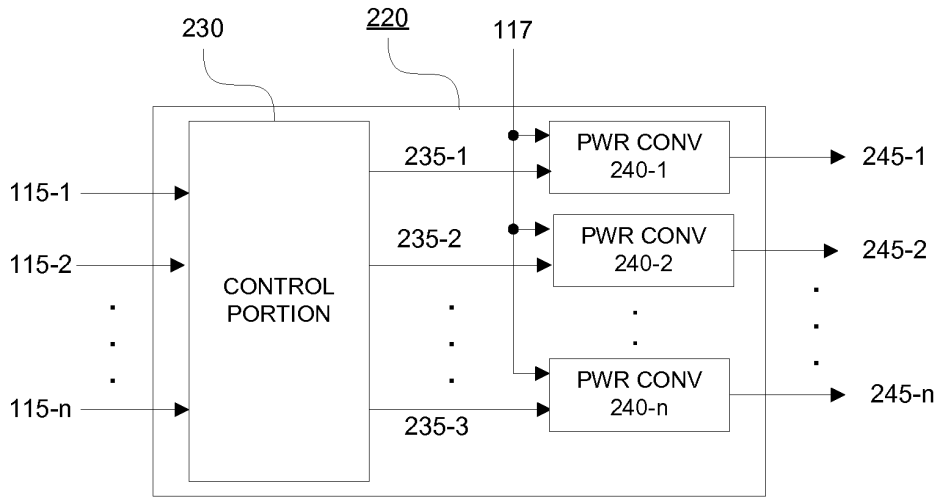


Figure 2

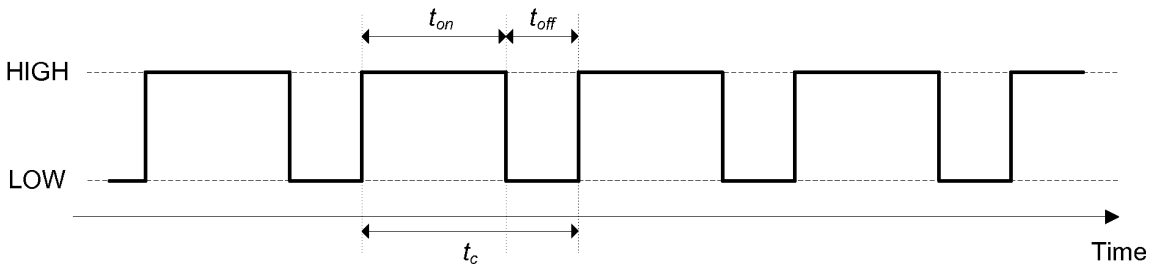
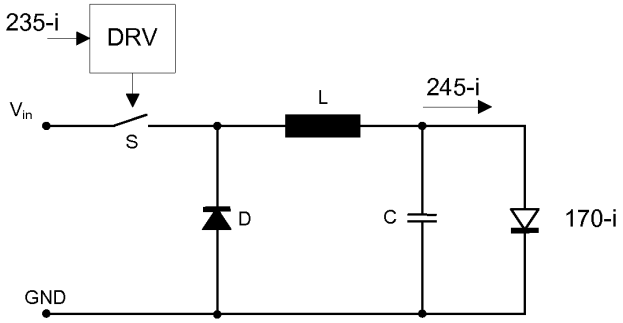


Figure 3



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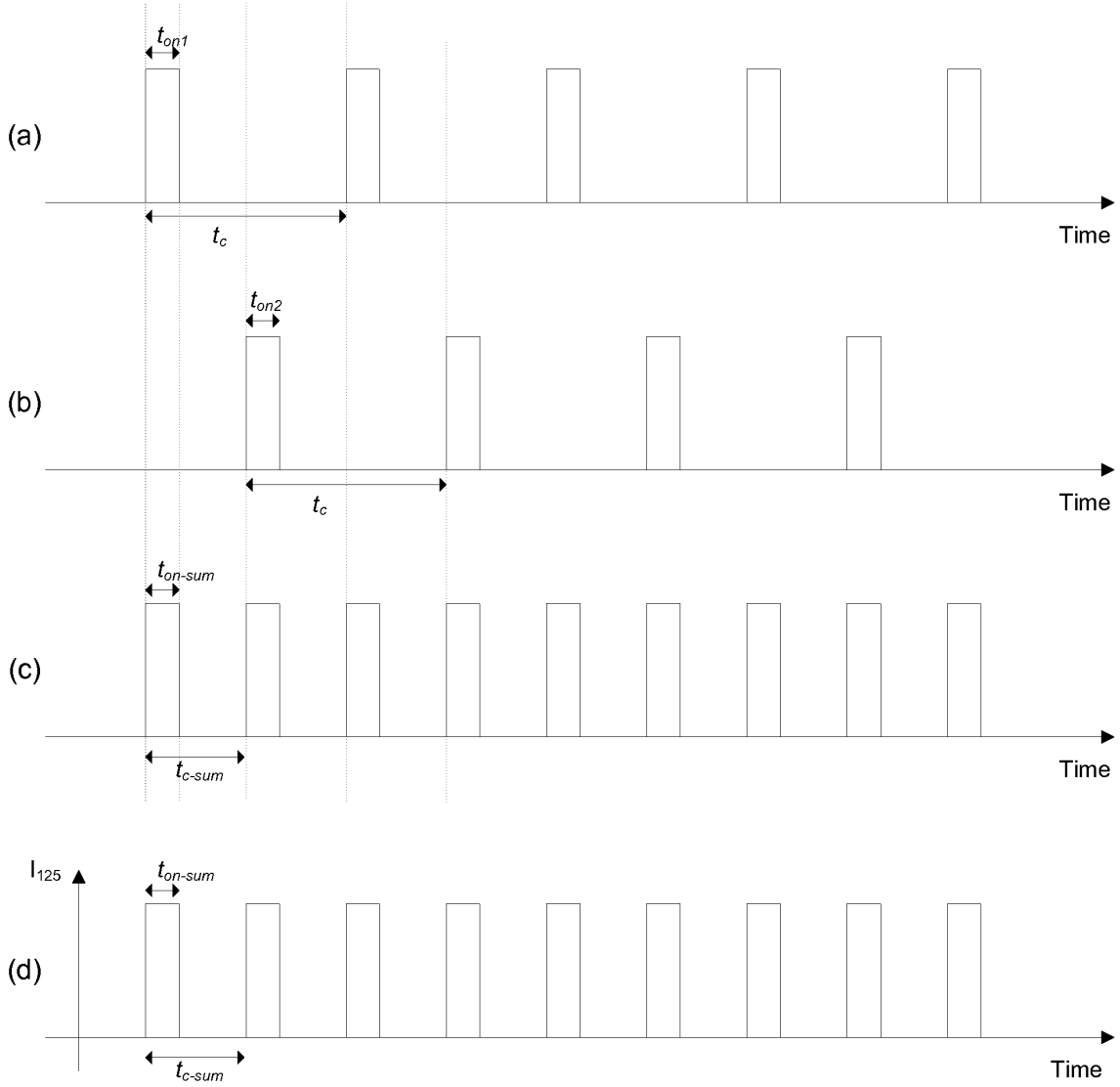


Figure 5a

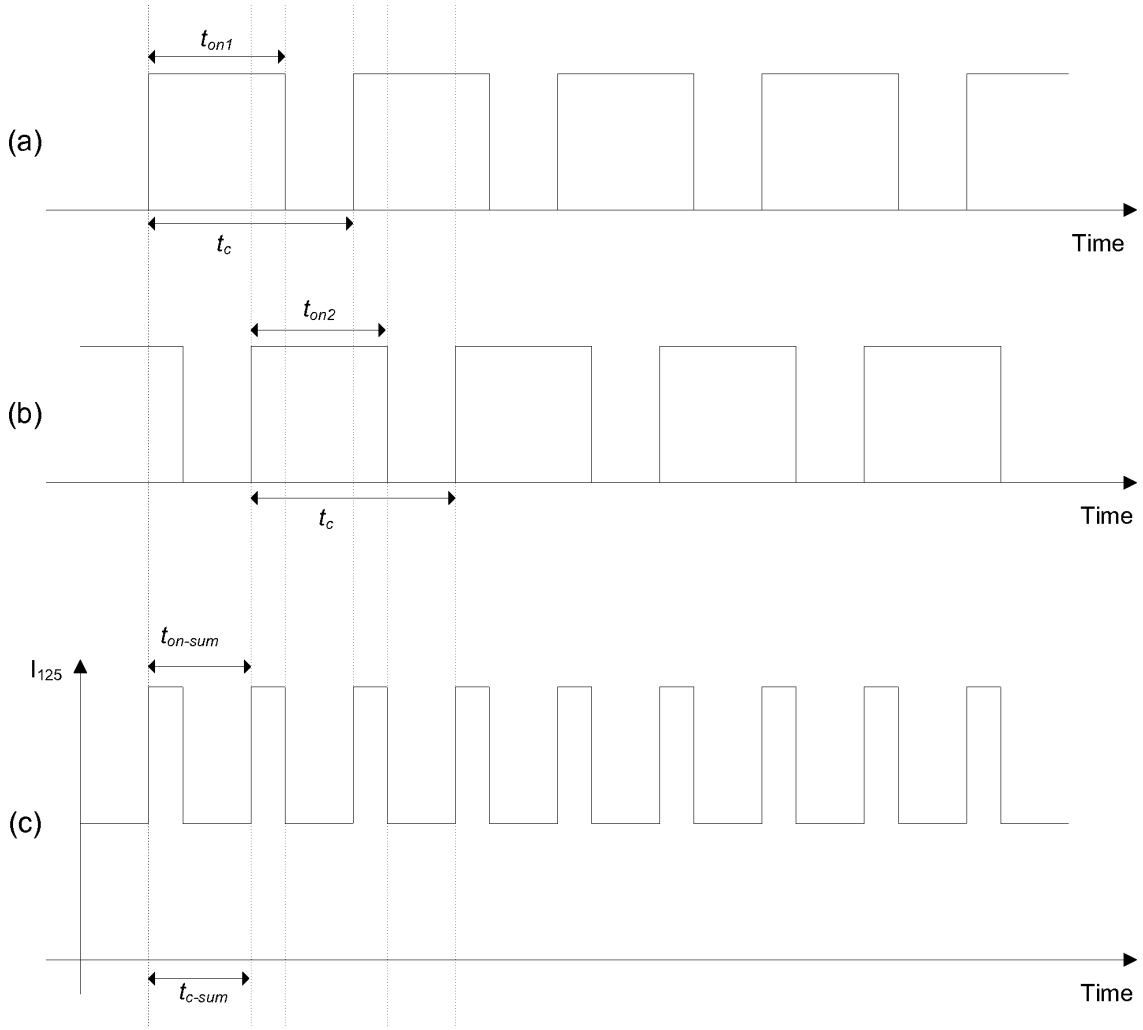
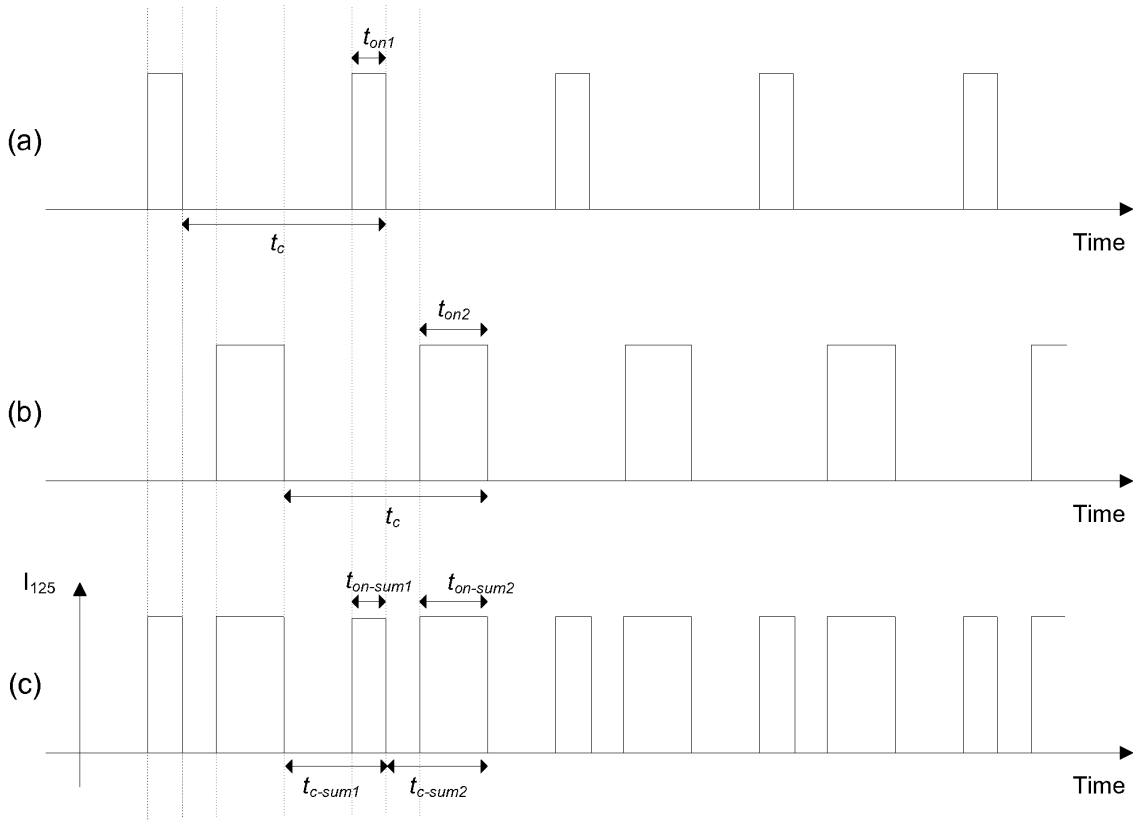


Figure 5b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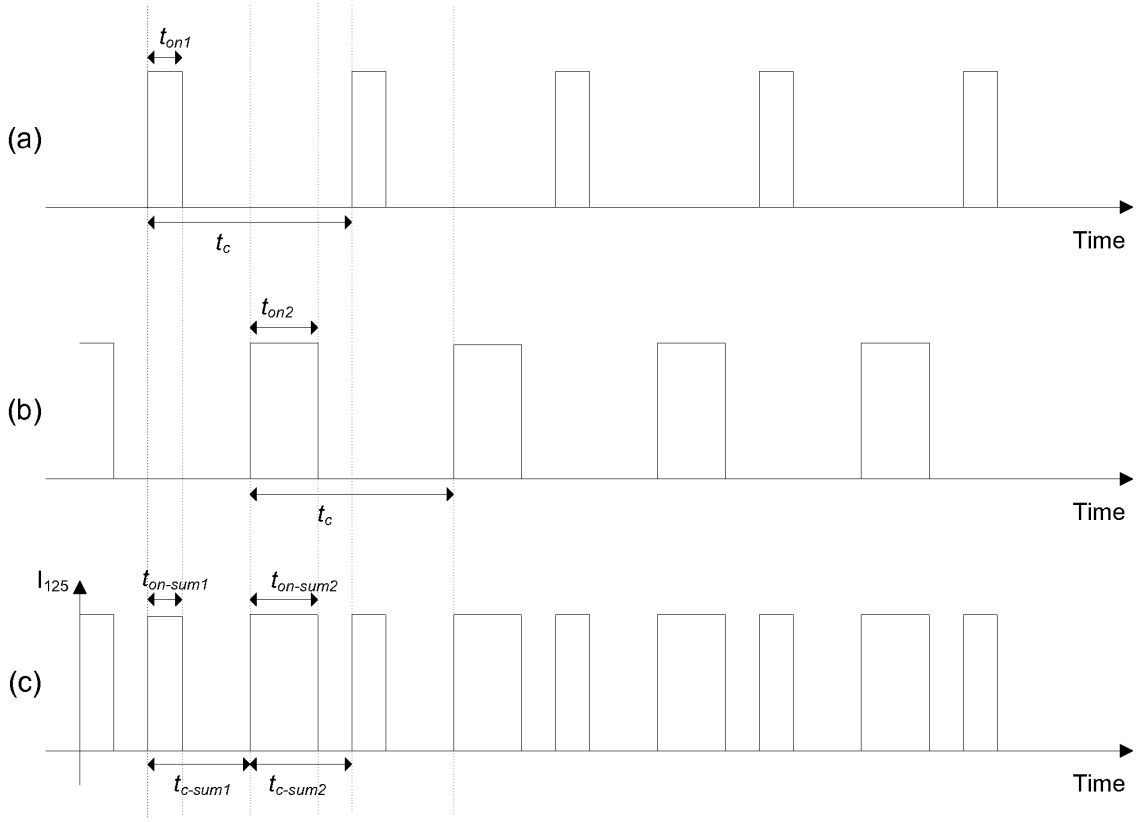
t_{c-sum2}
Time

Figure 6a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Time

Figure 6b

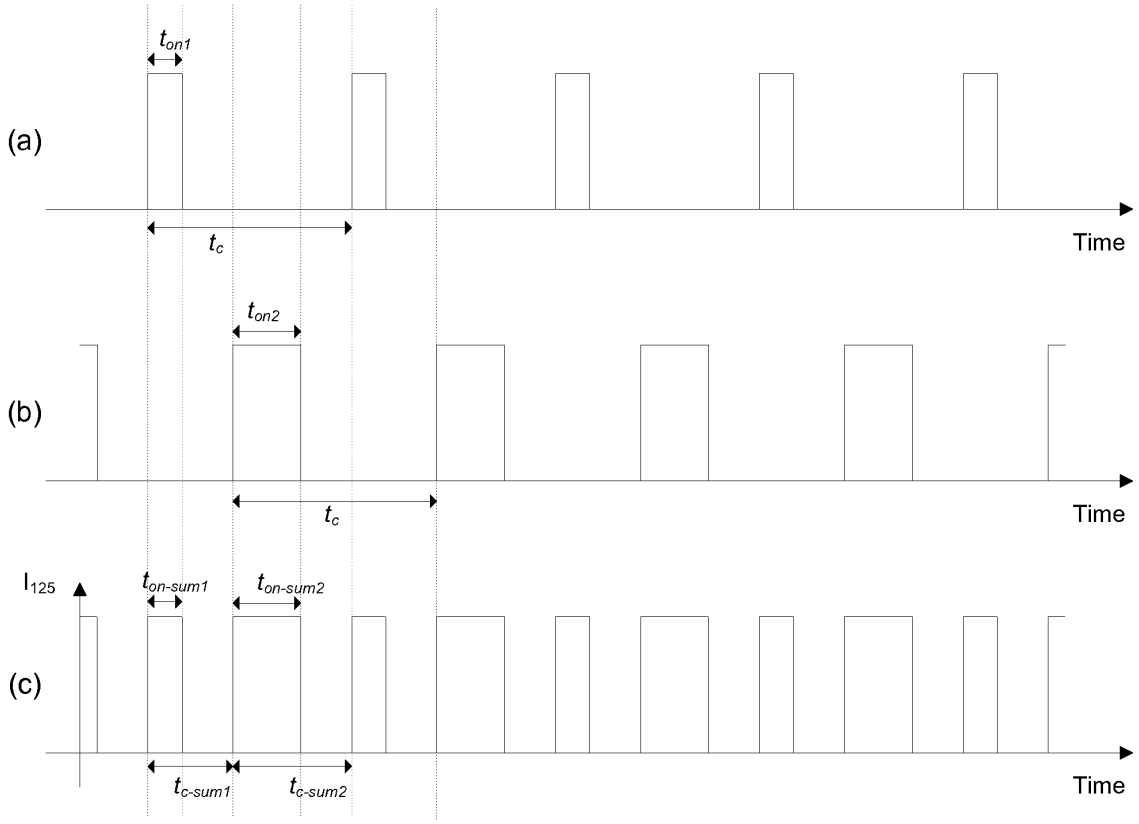
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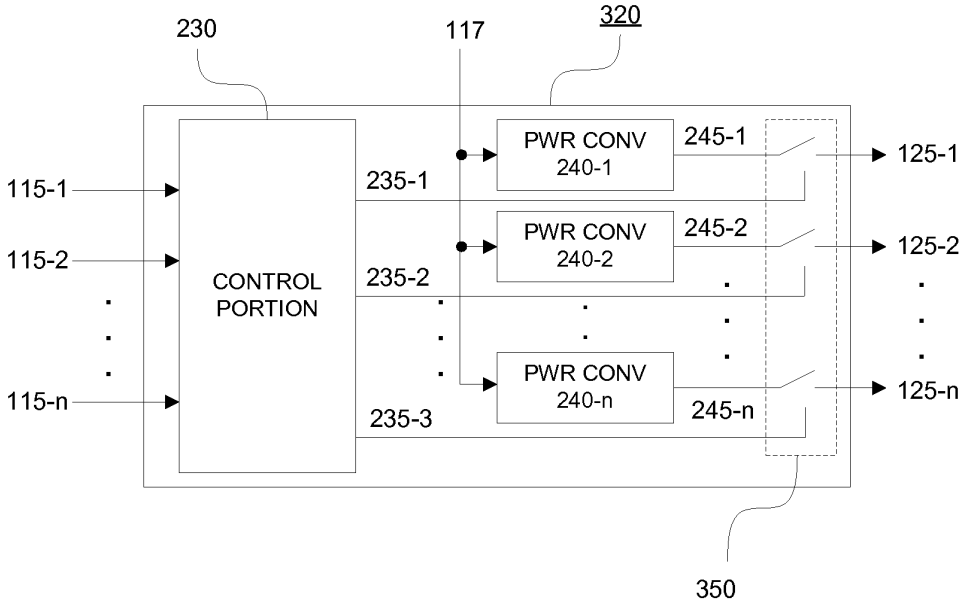
Figure 7



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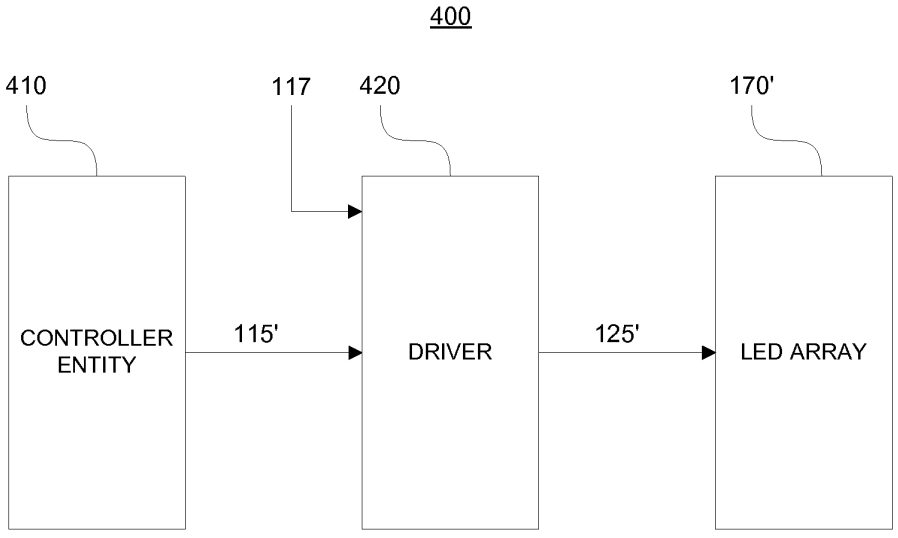

Figure 9

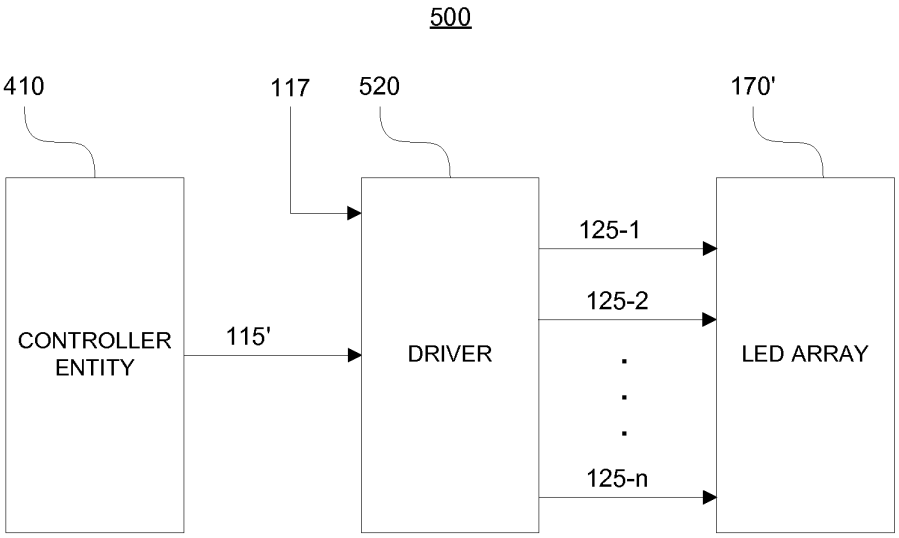

Figure 10

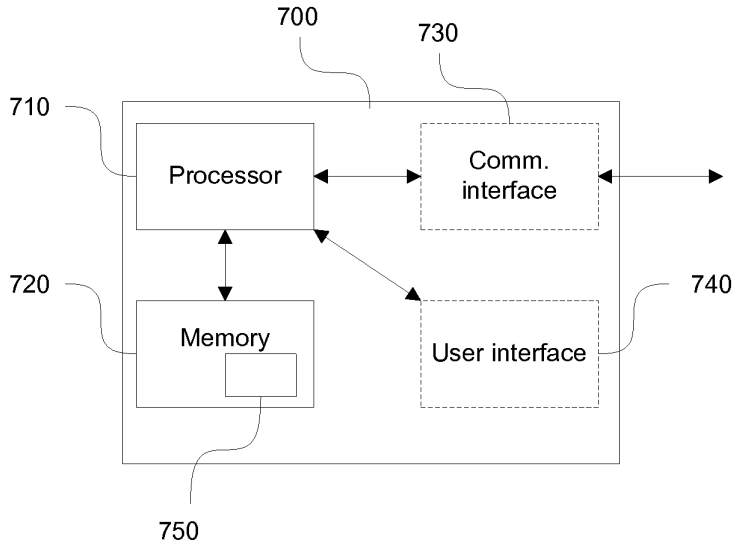

Figure 11

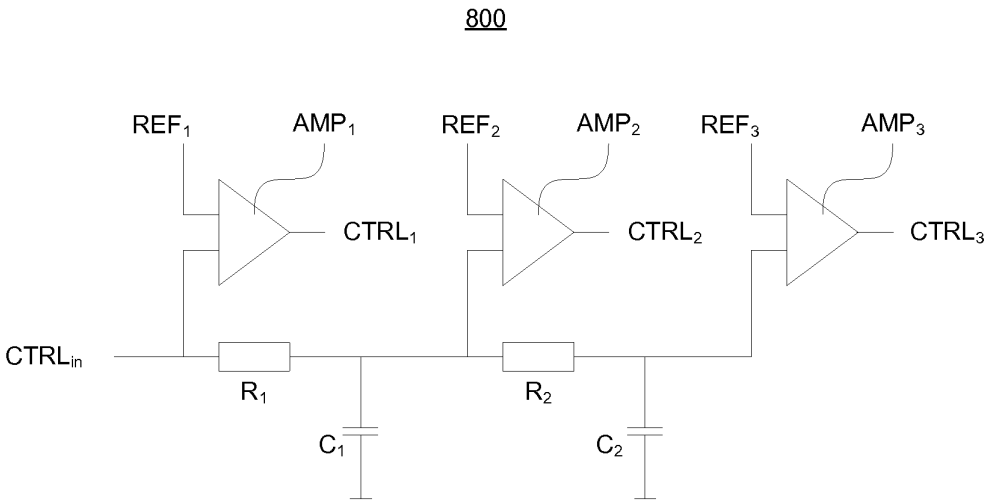

Figure 12

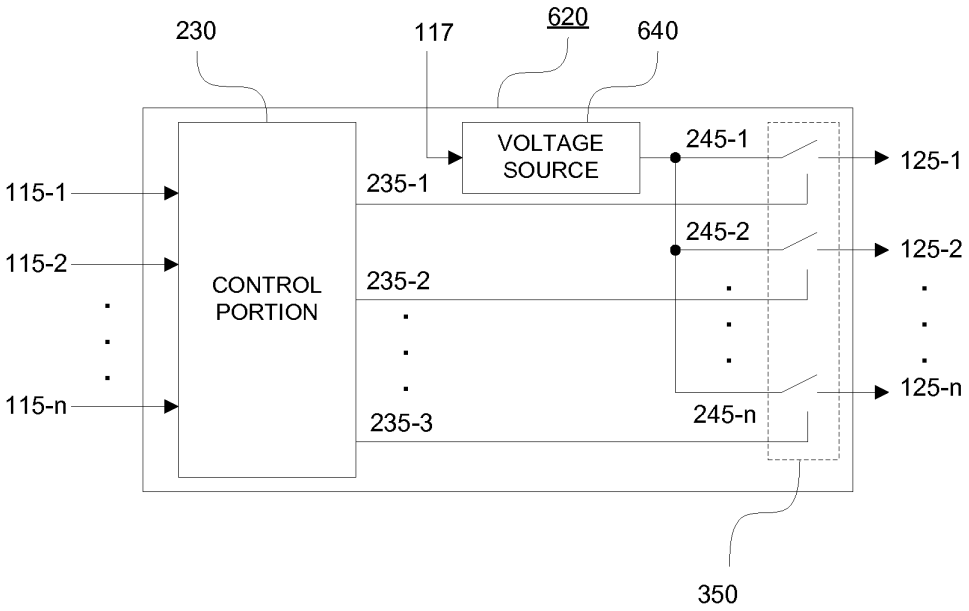

Figure 13

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EUROPEAN SEARCH REPORT

Application Number
EP 13 17 1212

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2012/098869 A1 (TSENG KUAN-JEN [TW]) 26 April 2012 (2012-04-26) * abstract; figures 3-8a *	1-6	INV. H05B33/08
X	US 2010/301764 A1 (LIU JING-MENG [TW]) 2 December 2010 (2010-12-02) * abstract; figures 3-8 *	1-6	
X	US 2010/220049 A1 (MURAKAMI SADAKAZU [JP]) 2 September 2010 (2010-09-02) * figure 71 *	1	
X	US 2009/225020 A1 (RAN KAIPING [US] ET AL) 10 September 2009 (2009-09-10) * abstract; figure 2b *	1	
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X	WO 02/056643 A1 (O2MICRO INT LTD [KY]; LIN YUNG-LIN [US]) 18 July 2002 (2002-07-18) * figures 1,2,4,6 *	1	TECHNICAL FIELDS SEARCHED (IPC) H05B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	18 March 2014	Maicas, Jesús

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