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(54) **Instruction and logic for machine checking communication**

(57) A processor includes a logic to determine an error condition reported in an error bank. The error bank is communicatively coupled to the processor and is associated with logical processors of the processor. The processor includes another logic to generate an interrupt indicating the error condition. The processor includes yet another logic to selectively send the interrupt to a single one of the logical processors associated with the error bank.

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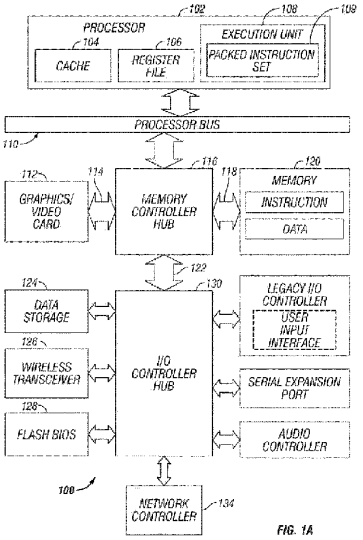

FIG. 1A

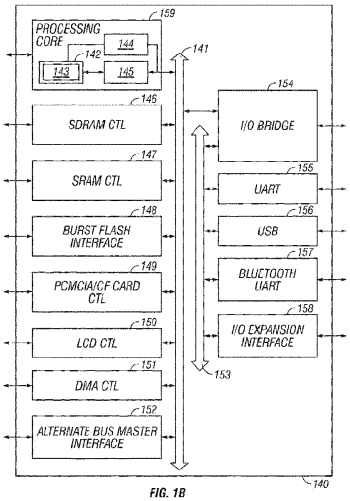

FIG. 1B

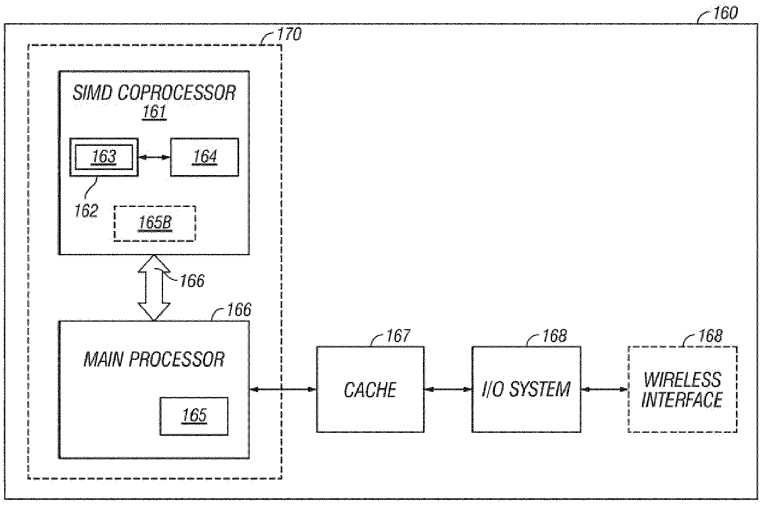

FIG. 1C