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(54) **Processor with architecturally-visible programmable on-die storage to store data that is accessible by instruction**

(57) A processor of an aspect includes an on-die programmable architecturally-visible storage. The processor also includes a decode unit to receive a data access instruction of an instruction set of the processor. The data access instruction to indicate a data address that is to be associated with data to be stored in the on-die programmable architecturally-visible storage, to indicate a data size associated with the data to be stored in the on-die programmable architecturally-visible storage, and to indicate a destination storage location of the processor. An execution unit is coupled with the decode unit and the on-die programmable architecturally-visible storage. The execution unit is on-die with the on-die programmable storage. The execution unit is operable, in response to the data access instruction, to store the data, which is associated with the data address and the data size, in the destination storage location that is to be indicated by the instruction.

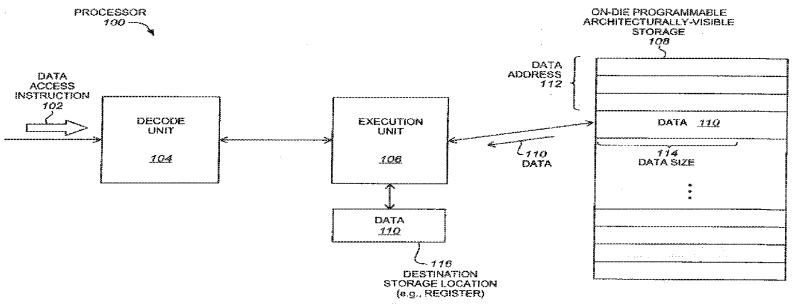

FIG. 1

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