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Remarks:

This application was filed on 03-02-2015 as a
divisional application to the application mentioned
under INID code 62.

(54) **Microelectronic package and method of manufacturing same**

(57) A microelectronic package comprising: a substrate (210); a first die (220) and a second die (260), both of which are embedded in the substrate, both of which have a front side (221, 261) and an opposing back side (222, 262), and both of which have at least one through-silicon-via (223, 263) therein; a plurality of build-up layers (230) adjacent to and built up over the front sides of the first and second dies; and an electrically conductive structure (240) adjacent to and in physical contact with the back sides of the first and second dies.

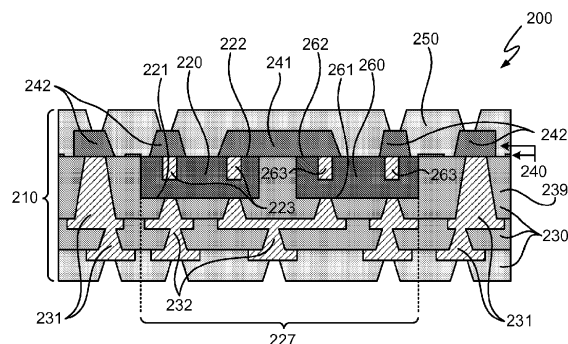


FIG. 2B