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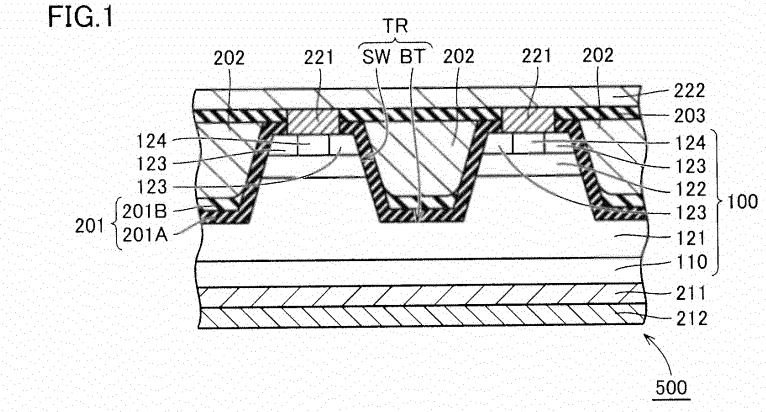
(54) METHOD FOR PRODUCING SILICON CARBIDE SEMICONDUCTOR DEVICE

(57) A silicon carbide substrate (100) including a first layer (121) having first conductivity type, a second layer (122) having second conductivity type, and a third layer (123) having the first conductivity type is formed. A trench (TR) provided with an inner surface having a side wall surface (SW) and a bottom surface (BT) is formed, the side wall surface extending through the third layer (123) and the second layer (122) and reaching the first layer (121), the bottom surface being formed of the first layer (121). A silicon film is formed to cover the bottom surface (BT). A gate oxide film (201) is formed on the inner surface by oxidation in the trench (TR). The gate oxide film (201) includes a first portion (201A) formed by oxidation of the silicon carbide substrate, and a second portion (201 B) formed by oxidation of the silicon film on the bottom surface (BT). Accordingly, a method for manufacturing a silicon carbide semiconductor device (500) having a high breakdown voltage is provided.

FIG.1



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Description

TECHNICAL FIELD

[0001] The present invention relates to methods for manufacturing silicon carbide semiconductor devices, and particularly to a silicon carbide semiconductor device having a trench and a method for manufacturing the same.

BACKGROUND ART

[0002] Japanese Patent Laying-Open No. 7-326755 (Patent Document 1) discloses a silicon carbide semiconductor device having a trench. This patent publication states that a gate thermal oxidation film has a larger film thickness on a bottom surface of a trench than the film thickness thereof on a side surface of the trench, so that a threshold voltage becomes low and breakdown voltage between the gate and the drain becomes high. It is also stated that the bottom surface of the trench corresponds to a carbon plane, which allows for fast oxidation rate, of hexagonal single-crystal silicon carbide, whereas the side surface of the trench corresponds to a plane perpendicular to this carbon plane and allowing for slow oxidation rate. Hence, by performing a thermal oxidation process once, a thermal oxidation film can be formed such that the thickness of the thermal oxidation film on the side surface of the trench is greatly different from the thickness of the thermal oxidation film on the bottom surface of the trench.

CITATION LIST

PATENT DOCUMENT

[0003] PTD 1: Japanese Patent Laying-Open No. 7-326755

SUMMARY OF INVENTION

TECHNICAL PROBLEM

[0004] According to a study conducted by the present inventors, however, it was difficult to selectively increase the film thickness of a gate oxide film to a sufficient degree on a bottom surface of a trench merely by using the difference in oxidation rate of silicon carbide dependent on the crystal orientation.

[0005] The present invention has been made to solve the problems as described above, and an object of the present invention is to provide a method for manufacturing a silicon carbide semiconductor device having a high breakdown voltage.

SOLUTION TO PROBLEM

[0006] A method for manufacturing a silicon carbide semiconductor device of the present invention includes the following steps. A silicon carbide substrate including a first layer having first conductivity type, a second layer provided on the first layer and having second conductivity type, and a third layer provided on the second layer, separated from the first layer by the second layer, and having the first conductivity type is formed. A trench provided with an inner surface having a side wall surface and a bottom surface is formed, the side wall surface extending through the third layer and the second layer and reaching the first layer, the bottom surface being formed of the first layer. A silicon film is formed to cover the bottom surface. A gate oxide film is formed on the inner surface by oxidation in the trench. The gate oxide film includes a first portion formed by oxidation of the silicon carbide substrate, and a second portion formed by oxidation of the silicon film on the bottom surface. A gate electrode is formed on the gate oxide film.

[0007] According to this manufacturing method, the gate oxide film includes the first portion formed by the oxidation of the silicon carbide substrate, as well as the second portion formed by the oxidation of the silicon film on the bottom surface of the trench. Thus, the thickness of the gate oxide film on the bottom surface of the trench can be increased for the thickness of the second portion. Accordingly, the silicon carbide semiconductor device can have a high breakdown voltage.

[0008] Preferably, the gate electrode is formed such that the gate electrode makes direct contact with the first portion on the second layer. Thus, the gate insulating film on the channel surface formed of the second layer can be formed only of the first portion higher in quality than the second portion.

[0009] The silicon film may be formed to cover the second layer on the side wall surface. Subsequently, a portion of the silicon film may be removed such that the silicon film remains on the bottom surface of the trench and the second layer is exposed at the side wall surface of the trench.

[0010] Thus, even if the second layer is covered with the silicon film when the silicon film is formed, the second portion is not formed on the second layer. Thus, the gate electrode can make direct contact with the first portion on the second layer.

[0011] Preferably, the silicon film is formed such that the silicon film has a first thickness on the bottom surface and has a second thickness on the side wall surface formed of the second layer. The first thickness is larger than the second thickness.

[0012] Thus, the second portion can be formed with a further sufficient thickness on the bottom surface.

[0013] Preferably, the step of removing a portion of the silicon film includes the following steps. The silicon film is oxidized for a thickness smaller than the first thickness and larger than the second thickness. A portion of the silicon film that has been oxidized in the step of oxidizing the silicon film is removed.

[0014] Thus, the second portion can be selectively

formed on the bottom surface rather than on the side wall surface.

[0015] Preferably, the step of forming a trench includes the following steps. A mask having an opening is formed on the third layer. The silicon carbide substrate is etched using the mask. The step of forming a silicon film is performed using the mask.

[0016] Thus, the formation of the silicon film on the portion covered with the mask can be prevented.

[0017] Preferably, the silicon carbide substrate is etched such that the silicon carbide substrate is side-etched from the opening of the mask.

[0018] Thus, the side wall surface of the trench is recessed by the side etching. As a result, the mask remains protruding from the side wall surface. During the formation of the silicon film using this mask, therefore, the silicon film is unlikely to be formed on the side wall surface since the side wall surface is located in the shadow of the mask.

[0019] Preferably, the step of etching the silicon carbide substrate includes the step of thermally etching the silicon carbide substrate.

[0020] Thus, the silicon carbide substrate can be side-etched.

ADVANTAGEOUS EFFECTS OF INVENTION

[0021] As described above, according to the present invention, the silicon carbide semiconductor device can have a high breakdown voltage.

BRIEF DESCRIPTION OF DRAWINGS

[0022]

Fig. 1 is a partial cross sectional view schematically showing the configuration of a silicon carbide semiconductor device in one embodiment of the present invention.

Fig. 2 is a perspective view schematically showing the shape of a silicon carbide substrate included in the silicon carbide semiconductor device of Fig. 1.

Fig. 3 shows the configuration of Fig. 2 in more detail.

Fig. 4 is an enlarged view of Fig. 1.

Fig. 5 is an enlarged view of a broken line CP of Fig. 4.

Fig. 6 is a partial cross sectional view schematically showing a first step of a method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 7 is a partial cross sectional view schematically showing a second step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 8 is a partial cross sectional view schematically showing a third step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 9 is a partial cross sectional view schematically showing a fourth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 10 is a partial cross sectional view schematically showing a fifth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 11 is a partial cross sectional view schematically showing a sixth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 12 is a partial cross sectional view schematically showing a seventh step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 13 is a partial cross sectional view schematically showing an eighth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 14 is a partial cross sectional view schematically showing a ninth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 15 is a partial cross sectional view schematically showing a tenth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 16 is a partial cross sectional view schematically showing an eleventh step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 17 is a partial cross sectional view schematically showing a twelfth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 18 is a partial cross sectional view schematically showing a thirteenth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 19 is a partial cross sectional view schematically showing a fourteenth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 20 is a partial cross sectional view schematically showing a fifteenth step of the method for manufacturing the silicon carbide semiconductor device of Fig. 1.

Fig. 21 is a partial cross sectional view schematically showing a fine structure in a surface of a silicon carbide substrate included in the silicon carbide semiconductor device.

Fig. 22 shows a crystal structure of a (000-1) plane in a hexagonal crystal of polytype 4H.

Fig. 23 shows a crystal structure of a (11-20) plane along a line XXIII-XXIII in Fig. 22.

Fig. 24 shows a crystal structure of a combined plane of Fig. 21 in the vicinity of the surface within the (11-20) plane.

Fig. 25 shows the combined plane of Fig. 21 when viewed from a (01-10) plane.

Fig. 26 is a graph showing an exemplary relation between channel mobility and an angle between a channel surface and the (000-1) plane when macroscopically viewed, in each of a case where thermal

etching is performed and a case where no thermal etching is performed.

Fig. 27 is a graph showing an exemplary relation between the channel mobility and an angle between a channel direction and a <0-11-2> direction.

Fig. 28 shows a modification of Fig. 21.

DESCRIPTION OF EMBODIMENTS

[0023] Embodiments of the present invention will be described hereinafter with reference to the drawings, in which the same or corresponding parts are designated by the same reference numbers and description thereof will not be repeated. Regarding crystallographic descriptions in the present specification, an individual orientation is represented by [], a group orientation is represented by <>, an individual plane is represented by (), and a group plane is represented by { }. In addition, although a negative crystallographic index is usually indicated by putting "-" (bar) above a numeral, it is indicated by putting a negative sign before the numeral in the present specification.

[0024] As shown in Fig. 1, a vertical type MOSFET 500 (silicon carbide semiconductor device) of the present embodiment includes an epitaxial substrate 100 (silicon carbide substrate), gate oxide films 201 (gate insulating films), gate electrodes 202, interlayer insulating films 203, source electrodes 221, a drain electrode 211, a source interconnection 222, and a protecting electrode 212.

[0025] Epitaxial substrate 100 has a single-crystal substrate 110 and an epitaxial layer provided thereon. The epitaxial layer includes an n^- layer 121 (first layer), p type body layers 122 (second layer), n regions 123 (third layer), and contact regions 124. Epitaxial substrate 100 is made of silicon carbide. This silicon carbide preferably has a hexagonal crystal structure, and more preferably has a polytype of 4H.

[0026] Single-crystal substrate 110 has n type conductivity (first conductivity type). The plane orientation (hklm) of one main surface (upper surface in Fig. 1) of single-crystal substrate 110 preferably has m of negative value, more preferably, corresponds to approximately a (000-1) plane.

[0027] N^- layer 121 has a donor added therein and therefore has n type conductivity. The donor is preferably added to n^- layer 121 during epitaxial growth of n^- layer 121, rather than by ion implantation. N^- layer 121 preferably has a donor concentration lower than that of single-crystal substrate 110. N^- layer 121 preferably has a donor concentration of not less than 1×10^{15} cm^{-3} and not more than 5×10^{16} cm^{-3}, for example, has a donor concentration of 8×10^{15} cm^{-3}.

[0028] Each of p type body layers 122 is provided on n^- layer 121, has an acceptor added therein, and therefore has p type conductivity (second conductivity type). P type body layer 122 has an acceptor concentration of, for example, 1×10^{18} cm^{-3}.

[0029] Each of n regions 123 has n type conductivity. N region 123 is provided on p type body layer 122, and is separated from n^- layer 121 by p type body layer 122. Contact region 124 has p type conductivity. Contact region 124 is formed on a portion of p type body layer 122 so as to be connected to p type body layer 122.

[0030] Further, referring to Fig. 2 and Fig. 3, epitaxial substrate 100 has a trench TR provided with an inner surface having side wall surfaces SW and a bottom surface BT. Each of side wall surfaces SW extends through n region 123 and p type body layer 122 and reaches n^- layer 121. Bottom surface BT is formed of n^- layer 121. Side wall surface SW has a channel surface CH (Fig. 3) on p type body layer 122. Preferably, side wall surface SW has a predetermined crystal plane (also referred to as "special plane") particularly on p type body layer 122. Details of the special plane will be described later.

[0031] The fact that epitaxial substrate 100 has trench TR corresponds to such a fact that the epitaxial layer is partially removed above the upper surface of single-crystal substrate 110. In the present embodiment, a multiplicity of mesa structures are formed on the upper surface of single-crystal substrate 110. Specifically, each of the mesa structures has an upper surface and a bottom surface both having a hexagonal shape, and has side walls inclined relative to the upper surface of single-crystal substrate 110. Thus, trench TR expands in a tapered shape toward the opening.

[0032] Gate oxide film 201 (Fig. 1) covers the inner surface of trench TR, namely, side wall surfaces SW and bottom surface BT. Gate oxide film 201 has a thickness TA (Fig. 4) on side wall surface SW formed of p type body layer 122. Gate oxide film 201 also has a thickness TB (Fig. 4) on bottom surface BT. Thickness TB is larger than thickness TA. Preferably, thickness TB is larger than thickness TA by 300 nm or more.

[0033] Gate oxide film 201 includes a first portion 201 A formed by thermal oxidation of silicon carbide, and a second portion 201B formed by thermal oxidation of silicon. At least a portion of second portion 201B is provided on bottom surface BT of trench TR with first portion 201 A interposed therebetween.

[0034] Second portion 201B has a carbon atom concentration lower than that of first portion 201 A. First portion 201 A may have a carbon atom concentration of more than 1×10^{15} cm^{-3} Second portion 201B preferably has a carbon atom concentration of less than 1×10^{15} cm^{-3}. It should be noted that in the case where the carbon atom concentrations are not uniform, an average value may be calculated.

[0035] A portion where bottom surface BT and side wall surface SW of trench TR are connected to each other forms a corner portion RS (Fig. 5). First portion 201 A provided on corner portion RS forms a corner portion RA having a radius of curvature approximately similar to that of corner portion RS. Second portion 201B provided on corner portion RA forms a corner portion RB having a radius of curvature greater than that of corner portion RA.

Thus, an electric field is relaxed in corner portion RB.

[0036] Gate electrode 202 is buried in trench TR with gate oxide film 201 interposed therebetween. Gate oxide film 201 separates epitaxial substrate 100 and gate electrode 202 from each other in trench TR. Gate electrode 202 faces the surface of p type body layer 122 with gate oxide film 201 interposed therebetween. Gate electrode 202 has an upper surface substantially as high as the upper surface of a portion of gate oxide film 201 on the upper surface of n region 123. Interlayer insulating film 203 is provided to cover gate electrode 202 as well as the extended portion of gate oxide film 201 on the upper surface of n region 123.

[0037] Source electrode 221 extends through interlayer insulating film 203 and makes contact with each of n region 123 and contact region 124. Source interconnection 222 is provided on source electrode 221 and interlayer insulating film 203 in contact with source electrode 221. Drain electrode 211 is provided on an opposite surface of epitaxial substrate 100 to its surface in which trench TR is provided. Protecting electrode 212 covers drain electrode 211.

[0038] A method for manufacturing MOSFET 500 (Fig. 1) is now described.

[0039] As shown in Fig. 6, on single-crystal substrate 110, n^- layer 121 is formed by means of epitaxial growth. This epitaxial growth can be performed by means of, for example, a CVD (Chemical Vapor Deposition) method in which a mixed gas of silane (SiH_4) and propane (C_3H_8) is used as a source material gas and hydrogen gas (H_2) is used as a carrier gas, for example. In doing so, it is preferable to introduce nitrogen (N) or phosphorus (P) as a donor, for example.

[0040] As shown in Fig. 7, p type body layer 122 is formed on n^- layer 121, and n region 123 is formed on p type body layer 122. Specifically, ion implantation is performed into the upper surface of n^- layer 121. In the ion implantation for forming p type body layer 122, ions of an acceptor such as aluminum (Al) are implanted. Meanwhile, in the ion implantation for forming n region 123, ions of a donor such as phosphorus (P) are implanted. Thus, epitaxial substrate 100 is formed which has n^-layer 121, p type body layer 122, and n region 123. It should be noted that instead of the ion implantation, epitaxial growth involving addition of impurities may be employed.

[0041] As shown in Fig. 8, contact regions 124 are formed by ion implantation. Next, activation heat treatment is performed to activate the impurities added by the ion implantation. This heat treatment is preferably performed at a temperature of not less than 1500°C and not more than 1900°C, for example, a temperature of approximately 1700°C. The heat treatment is performed for approximately 30 minutes, for example. The atmosphere of the heat treatment is preferably an inert gas atmosphere, such as Ar atmosphere.

[0042] Next, a mask 247 (Fig. 9) having an opening through which n region 123 is partially exposed is formed on epitaxial substrate 100. The opening is formed to correspond to the location of trench TR (Fig. 1). As mask 247, a silicon oxide film formed by thermal oxidation can be used, for example.

[0043] As shown in Fig. 10, in the opening of mask 247, n region 123, p type body layer 122, and a portion of n^- layer 121 are removed by etching. An exemplary, usable etching method is reactive ion etching (RIE), in particular, inductively coupled plasma (ICP) RIE. Specifically, ICP-RIE can be employed in which SF_6 or a mixed gas of SF_6 and O_2 is used as the reactive gas, for example. By means of such etching, in the region where trench TR (Fig. 1) is to be formed, a recess TQ can be formed which has a side wall having an inner surface SV substantially perpendicular to the main surface of single-crystal substrate 110.

[0044] Next, epitaxial substrate 100 is etched using mask 247. Specifically, inner surface SV of recess TQ of epitaxial substrate 100 is thermally etched. The thermal etching can be performed, for example, by heating epitaxial substrate 100 in an atmosphere including a reactive gas containing at least one or more types of halogen atom. The at least one or more types of halogen atom include at least one of chlorine (Cl) atom and fluorine (F) atom. This atmosphere is, for example, Cl_2, BCL_3, SF_6, or CF_4 For example, the thermal etching is performed using a mixed gas of chlorine gas and oxygen gas as a reactive gas, at a heat treatment temperature of, for example, not less than 700°C and not more than 1000°C.

[0045] As a result of the thermal etching, trench TR is formed as shown in Fig. 11. During the formation of trench TR, epitaxial substrate 100 is etched in a side etching manner from the opening of mask 247 as indicated by an arrow SE. Further, during this thermal etching, a special plane is spontaneously formed on side wall surface SW of trench TR, in particular, on its portion formed of p type body layer 122.

[0046] It should be noted that the reactive gas may contain a carrier gas in addition to the chlorine gas and the oxygen gas. An exemplary, usable carrier gas is nitrogen (N_2) gas, argon gas, helium gas, or the like. When the heat treatment temperature is set at not less than 700°C and not more than 1000°C as described above, a rate of etching SiC is, for example, approximately 70 μm/hour. Moreover, in this case, mask 247, which is made of silicon oxide and therefore has a very large selection ratio relative to SiC, is not substantially etched during the etching of SiC.

[0047] As shown in Fig. 12, a silicon film 90 is formed on epitaxial substrate 100 having mask 247 provided thereon. In other words, silicon film 90 is formed while using mask 247. Silicon film 90 covers bottom surface BT of trench TR. In the present embodiment, silicon film 90 also covers p type body layer 122 on side wall surface SW.

[0048] Silicon film 90 has a first thickness UB on bottom surface BT. Silicon film 90 has a second thickness UA on side wall surface SW formed of p type body layer 122. Side wall surface SW formed of p type body layer 122 is

not directly covered with mask 247, but is located in the shadow of mask 247 during the formation of silicon film 90. Therefore, second thickness UA is smaller than first thickness UB. Conversely, first thickness UB is larger than second thickness UA. The silicon film is preferably made substantially only of silicon, but may be made of silicon containing an impurity. Next, mask 247 is removed with an appropriate method such as etching (Fig. 13). In doing so, the portion of silicon film 90 on mask 247 is also removed.

[0049] Next, a portion of silicon film 90 is removed such that silicon film 90 remains on bottom surface BT of trench TR and p type body layer 122 is exposed at side wall surface SW of trench TR. Specifically, the following steps are performed.

[0050] First, silicon film 90 (Fig. 13) is thermally oxidized such that the oxidation progresses to a thickness smaller than first thickness UB (Fig. 12) and larger than second thickness UA (Fig. 12). This thermal oxidation is preferably performed at a temperature at which silicon is thermally oxidized and silicon carbide is not substantially thermally oxidized. Consequently, on side wall surface SW, silicon film 90 having second thickness UA is oxidized as shown in Fig. 14. On bottom surface BT, a portion corresponding to second thickness UA of silicon film 90 having first thickness UB (Fig. 13) is oxidized to become a silicon oxide film 90A, and the remaining portion remains as a silicon film 90B. The entire portion of silicon film 90 that was located on side wall surface SW formed of p type body layer 122 becomes silicon oxide film 90A. The portion of silicon film 90 that was located on bottom surface BT partially becomes silicon oxide film 90A on the surface side, and silicon film 90B remains between silicon oxide film 90A and bottom surface BT. This thermal oxidation is performed, for example, at not less than 800°C and not more than 950°C. Next, silicon oxide film 90A is removed by etching (Fig. 15). This removal can be performed, for example, by wet etching using hydrofluoric acid.

[0051] In the manner described above, a portion of silicon film 90 (Fig. 13) is removed such that silicon film 90 (i.e., silicon film 90B) remains on bottom surface BT of trench TR and p type body layer 122 is exposed at side wall surface SW of trench TR.

[0052] Next, oxidation is performed in trench TR, thereby forming gate oxide film 201 (Fig. 1) on the inner surface of trench TR. Specifically, the following steps are performed.

[0053] First, silicon film 90B (Fig. 15) is thermally oxidized. Thus, second portion 201B that forms a portion of gate oxide film 201 (Fig. 1) is formed (Fig. 16). Silicon film 90B is thermally oxidized, for example, at not less than 800°C and not more than 950°C. Next, as shown in Fig. 17, epitaxial substrate 100 made of silicon carbide is thermally oxidized, thereby forming first portion 201A of gate oxide film 201. Epitaxial substrate 100 is thermally oxidized preferably at a temperature higher than the temperature at which silicon film 90B is thermally oxidized, for example, is thermally oxidized at not less than 1300°C.

[0054] Gate oxide film 201 is formed in the manner described above.

[0055] As shown in Fig. 18, gate electrode 202 is formed on gate oxide film 201. In the present embodiment, gate electrode 202 is formed in direct contact with first portion 201A on p type body layer 122. A method for forming gate electrode 202 can be performed, for example, by forming a film of conductor or doped polysilicon and performing CMP (Chemical Mechanical Polishing).

[0056] As shown in Fig. 19, interlayer insulating film 203 is formed on gate electrode 202 and gate oxide film 201 so as to cover the exposed surface of gate electrode 202.

[0057] Referring to Fig. 20, etching is performed to form openings in interlayer insulating film 203 and gate oxide film 201. Through the opening, each of n region 123 and contact region 124 is exposed on the upper surface of the mesa structure. Next, on the upper surface of the mesa structure, source electrode 221 is formed in contact with each of n region 123 and contact region 124.

[0058] Referring to Fig. 1 again, source interconnection 222, drain electrode 211, and protecting electrode 212 are formed. In this way, MOSFET 500 is obtained.

[0059] According to MOSFET 500 (Fig. 1) of the present embodiment, gate oxide film 201 includes first portion 201 A formed by the oxidation of epitaxial substrate 100, as well as second portion 201B formed by the oxidation of silicon film 90 on bottom surface BT of trench TR. Thus, the thickness of gate oxide film 201 on bottom surface BT of trench TR can be increased for the thickness of second portion 201B. That is, the thickness of a portion of the gate oxide film where breakdown particularly tends to occur can be increased. Accordingly, MOSFET 500 can have a high breakdown voltage.

[0060] Moreover, epitaxial substrate 100 is etched in a side etching manner from the opening of mask 247 (arrow SE in Fig. 11). That is, side wall surface SW of trench TR is recessed by the side etching. As a result, mask 247 remains protruding from side wall surface SW. During the formation of silicon film 90 using mask 247, therefore, silicon film 90 is unlikely to be formed on side wall surface SW since side wall surface SW is located in the shadow of mask 247.

[0061] Moreover, the step of forming silicon film 90 is performed using mask 247 (Fig. 12). Thus, the formation of silicon film 90 on the portion covered with mask 247 can be prevented.

[0062] Furthermore, in the present embodiment, silicon film 90 is formed to cover p type body layer 122 on side wall surface SW (Fig. 12). Then, a portion of silicon film 90 is removed such that silicon film 90 remains on bottom surface BT of trench TR and p type body layer 122 is exposed at side wall surface SW of trench TR (Figs. 13 to 15). Thus, gate electrode 202 can make direct contact with first portion 201 A on p type body layer 122.

[0063] Furthermore, silicon film 90 is formed to have

first thickness UB on bottom surface BT and have second thickness UA on side wall surface SW formed of p type body layer 122 (Fig. 12). First thickness UB is larger than second thickness UA. Thus, second portion 201B can be formed with a further sufficient thickness on bottom surface BT.

[0064] Moreover, the step of removing a portion of silicon film 90 includes the following steps. Silicon film 90 is oxidized for a thickness smaller than first thickness UB and larger than second thickness UA (Fig. 14). A portion of silicon film 90 that has been oxidized in the step of oxidizing silicon film 90 is removed (Fig. 15). Thus, second portion 201B can be selectively formed on bottom surface BT rather than on side wall surface SW.

[0065] Furthermore, gate electrode 202 is formed in direct contact with first portion 201A on p type body layer 122 (Fig. 18). Thus, the gate insulating film on the channel surface formed of p body layer 122 can be formed only of first portion 201A higher in quality than second portion 201B.

[0066] Although the "first conductivity type" corresponds to n type conductivity and the "second conductivity type" corresponds to p type conductivity in the present embodiment, these conductivity types may be reversed. In this case, the donor and acceptor in the foregoing description are also reversed. It should be noted that in order to attain higher channel mobility, it is preferable that the "first conductivity type" corresponds to n type conductivity. In addition, the silicon carbide semiconductor device is not limited to the MOSFET, and may be a trench type IGBT (Insulated Gate Bipolar Transistor), for example.

(Surface Having Special Plane)

[0067] As described above, side wall surface SW (Fig. 1) of trench TR preferably has a predetermined crystal plane (also referred to as "special plane") on, in particular, p type body layer 122. Such a side wall surface SW includes a plane S1 (first plane) having a plane orientation of {0-33-8} as shown in Fig. 21. Plane S1 preferably has a plane orientation of (0-33-8).

[0068] More preferably, side wall surface SW microscopically includes plane S1, and side wall surface SW microscopically further includes a plane S2 (second plane) having a plane orientation of {0-11-1}. Here, the term "microscopically" refers to "minutely to such an extent that at least the size about twice as large as an interatomic spacing is considered". As a method for observing such a microscopic structure, for example, a TEM (Transmission Electron Microscope) can be used. Preferably, plane S2 has a plane orientation of (0-11-1).

[0069] Preferably, plane S1 and plane S2 of side wall surface SW form a combined plane SR having a plane orientation of {0-11-2}. Specifically, combined plane SR is formed of periodically repeated planes S1 and S2. Such a periodic structure can be observed, for example, by TEM or AFM (Atomic Force Microscopy). In this case, combined plane SR has an off angle of 62° relative to the {000-1} plane, macroscopically. Here, the term "macroscopically" refers to "disregarding a fine structure having a size of approximately interatomic spacing." For the measurement of such a macroscopic off angle, a method employing general X-ray diffraction can be used, for example. Preferably, combined plane SR has a plane orientation of (0-11-2). In this case, combined plane SR has an off angle of 62° relative to the (000-1) plane, macroscopically.

[0070] Preferably, in the channel surface, carriers flow in a channel direction CD, in which the above-described periodic repetition is done.

[0071] A detailed structure of combined plane SR is now described.

[0072] Generally, regarding Si atoms (or C atoms), when viewing a silicon carbide single crystal of polytype 4H from the (000-1) plane, atoms in a layer A (solid line in the figure), atoms in a layer B (broken line in the figure) disposed therebelow, and atoms in a layer C (chain-dotted line in the figure) disposed therebelow, and atoms in a layer B (not shown in the figure) disposed therebelow are repeatedly provided as shown in Fig. 22. In other words, with four layers ABCB being regarded as one period, a periodic stacking structure such as ABCBABCBABCB ... is provided.

[0073] As shown in Fig. 23, in the (11-20) plane (cross section taken along a line XXIII-XXIII of Fig. 22), atoms in each of four layers ABCB constituting the above-described one period are not aligned completely along the (0-11-2) plane. In Fig. 23, the (0-11-2) plane is illustrated to pass through the locations of the atoms in layers B. In this case, it is understood that each of atoms in layers A and C is deviated from the (0-11-2) plane. Hence, even when the macroscopic plane orientation of the surface of the silicon carbide single crystal, i.e., the plane orientation thereof with its atomic level structure being ignored is limited to (0-11-2), this surface can have various structures microscopically.

[0074] As shown in Fig. 24, combined plane SR is constructed by alternately providing planes S1 having a plane orientation of (0-33-8) and planes S2 connected to planes S1 and having a plane orientation different from that of each of planes S1. Each of planes S 1 and S2 has a length twice as large as the interatomic spacing of the Si atoms (or C atoms). It should be noted that a plane with plane S1 and plane S2 being averaged corresponds to the (0-11-2) plane (Fig. 23).

[0075] As shown in Fig. 25, when viewing combined plane SR from the (01-10) plane, the single-crystal structure has a portion periodically including a structure (plane S1 portion) equivalent to a cubic structure. Specifically, combined plane SR is constructed by alternately providing planes S1 having a plane orientation of (001) in the above-described structure equivalent to the cubic structure and planes S2 connected to planes S 1 and having a plane orientation different from that of each of planes S1. Also in a polytype other than 4H, the surface can be

formed of the planes (planes S1 in Fig. 25) having a plane orientation of (001) in the structure equivalent to the cubic structure and the planes (planes S2 in Fig. 25) connected to the foregoing planes and having a plane orientation different from that of each of the foregoing planes. The polytype may be, for example, 6H or 15R.

[0076] Referring to Fig. 26, a relation between the crystal plane of side wall surface SW and mobility MB of the channel surface is described. In the graph of Fig. 26, the horizontal axis represents an angle D1 formed by the (000-1) plane and the macroscopic plane orientation of side wall surface SW having the channel surface, whereas the vertical axis represents mobility MB A group of plots CM corresponds to a case where side wall surface SW is finished to correspond to a special plane by thermal etching, whereas a group of plots MC corresponds to a case where side wall surface SW is not thermally etched.

[0077] In group of plots MC, mobility MB is at maximum when the surface of the channel surface has a macroscopic plane orientation of (0-33-8). This is presumably due to the following reason. That is, in the case where the thermal etching is not performed, i.e., in the case where the microscopic structure of the channel surface is not particularly controlled, the macroscopic plane orientation thereof corresponds to (0-33-8), with the result that a ratio of the microscopic plane orientation of (0-33-8), i.e., the plane orientation of (0-33-8) in consideration of that in atomic level becomes statistically high.

[0078] On the other hand, mobility MB in group of plots CM is at maximum when the macroscopic plane orientation of the channel surface is (0-11-2) (arrow EX). This is presumably due to the following reason. That is, as shown in Fig. 24 and Fig. 25, the multiplicity of planes S1 each having a plane orientation of (0-33-8) are densely and regularly arranged with planes S2 interposed therebetween, whereby a ratio of the microscopic plane orientation of (0-33-8) becomes high in the surface of the channel surface.

[0079] It should be noted that mobility MB has orientation dependency on combined plane SR. In a graph shown in Fig. 27, the horizontal axis represents an angle D2 between the channel direction and the <0-11-2> direction, whereas the vertical axis represents mobility MB (in any unit) in the channel surface. A broken line is supplementarily provided therein for viewability of the graph. From this graph, it has been found that in order to increase channel mobility MB, channel direction CD (Fig. 21) preferably has an angle D2 of not less than 0° and not more than 60°, more preferably, substantially 0°.

[0080] As shown in Fig. 28, side wall surface SW may further include plane S3 (third plane) in addition to combined plane SR. More specifically, side wall surface SW may include a combined plane SQ formed of periodically repeated plane S3 and combined plane SR. In this case, the off angle of side wall surface SW relative to the {000-1} plane is deviated from the ideal off angle of combined plane SR, i.e., 62°. Preferably, this deviation is small, preferably, in a range of $\pm 10°$. Examples of a surface included in such an angle range include a surface having a macroscopic plane orientation of the {0-33-8} plane. More preferably, the off angle of side wall surface SW relative to the (000-1) plane is deviated from the ideal off angle of combined plane SR, i.e., 62°. Preferably, this deviation is small, preferably, in a range of $\pm$ 10°. Examples of a surface included in such an angle range include a surface having a macroscopic plane orientation of the (0-33-8) plane.

[0081] Such a periodic structure can be observed, for example, by TEM or AFM.

[0082] It should be understood that the embodiments disclosed herein are illustrative and non-restrictive in every respect. The scope of the present invention is defined by the terms of the claims, rather than the embodiments described above, and is intended to include any modifications within the scope and meaning equivalent to the terms of the claims.

REFERENCE SIGNS LIST

[0083] 90 silicon film; 90A silicon oxide film; 90B silicon film; 100 epitaxial substrate (silicon carbide substrate); 110 single-crystal substrate; 121 n^- layer (first layer); 122 p type body layer (second layer); 123 n region (third layer); 124 contact region; 201 gate oxide film; 201 A first portion; 201B second portion; 202 gate electrode; 203 interlayer insulating film; 211 drain electrode; 212 protecting electrode; 221 source electrode; 222 source interconnection; 247 mask; 500 MOSFET (silicon carbide semiconductor device); BT bottom surface; SW side wall surface; TR trench.

Claims

1. A method for manufacturing a silicon carbide semiconductor device, comprising the steps of:

   forming a silicon carbide substrate including a first layer having first conductivity type, a second layer provided on said first layer and having second conductivity type, and a third layer provided on said second layer, separated from said first layer by said second layer, and having said first conductivity type;
   forming a trench provided with an inner surface having a side wall surface and a bottom surface, said side wall surface extending through said third layer and said second layer and reaching said first layer, said bottom surface being formed of said first layer;
   forming a silicon film to cover said bottom surface;
   forming a gate oxide film on said inner surface by oxidation in said trench, said gate oxide film including a first portion formed by oxidation of said silicon carbide substrate, and a second por-

tion formed by oxidation of said silicon film on said bottom surface; and
forming a gate electrode on said gate oxide film.

2. The method for manufacturing a silicon carbide semiconductor device according to claim 1, wherein said step of forming a gate electrode is performed such that said gate electrode makes direct contact with said first portion on said second layer.

3. The method for manufacturing a silicon carbide semiconductor device according to claim 2, wherein said step of forming a silicon film is performed such that said silicon film covers said second layer on said side wall surface, and
said method for manufacturing a silicon carbide semiconductor device further comprises the step of removing a portion of said silicon film such that said silicon film remains on said bottom surface and said second layer is exposed at said side wall surface.

4. The method for manufacturing a silicon carbide semiconductor device according to claim 3, wherein said step of forming a silicon film is performed such that said silicon film has a first thickness on said bottom surface and has a second thickness on said side wall surface formed of said second layer, said first thickness being larger than said second thickness.

5. The method for manufacturing a silicon carbide semiconductor device according to claim 4, wherein said step of removing a portion of said silicon film includes the steps of oxidizing said silicon film for a thickness smaller than said first thickness and larger than said second thickness, and
removing a portion of said silicon film that has been oxidized in said step of oxidizing said silicon film.

6. The method for manufacturing a silicon carbide semiconductor device according to any one of claims 1 to 5, wherein
said step of forming a trench includes the steps of
forming a mask having an opening on said third layer, and
etching said silicon carbide substrate using said mask, and
said step of forming a silicon film is performed using said mask.

7. The method for manufacturing a silicon carbide semiconductor device according to claim 6, wherein said step of etching said silicon carbide substrate is performed such that said silicon carbide substrate is side-etched from said opening of said mask.

8. The method for manufacturing a silicon carbide semiconductor device according to claim 6 or 7, wherein said step of etching said silicon carbide substrate includes the step of thermally etching said silicon carbide substrate.

FIG.1

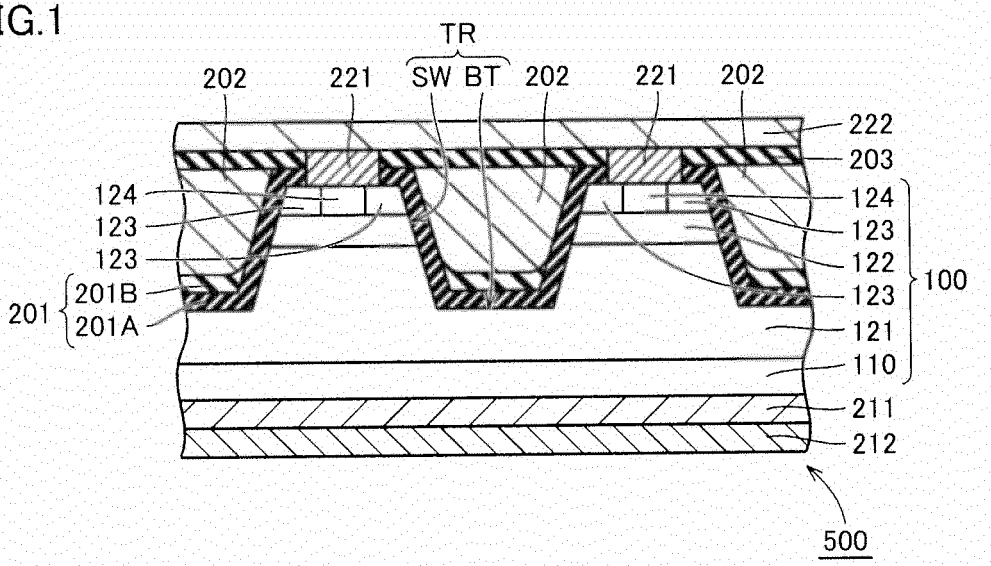

TR
202
221
SW BT
202
221
202
222
203
124
123
123
201
201B
201A
124
123
122
123
121
110
100
211
212
500

FIG.2

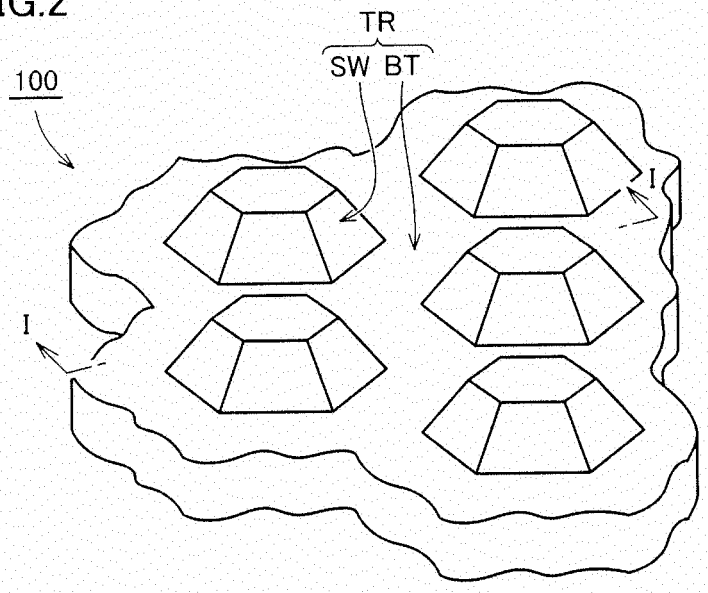

TR
SW BT
100
I
I

FIG.3

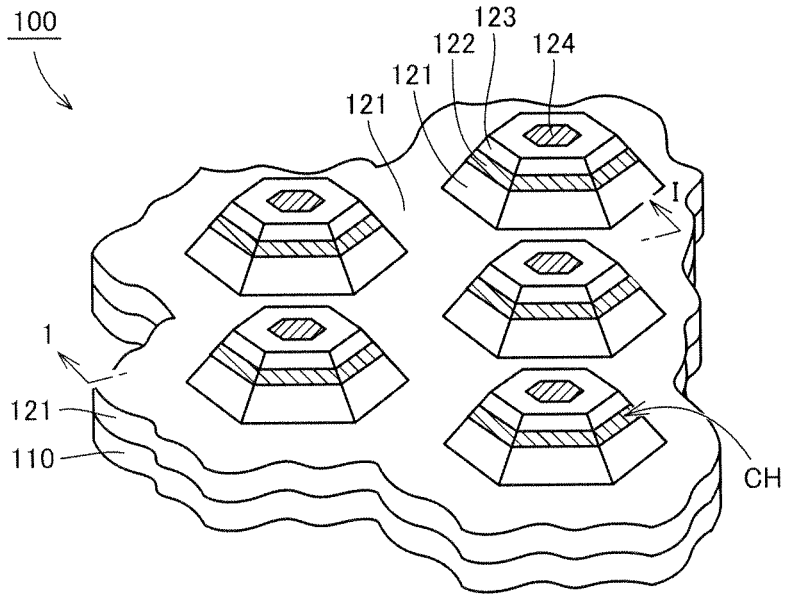


FIG.4

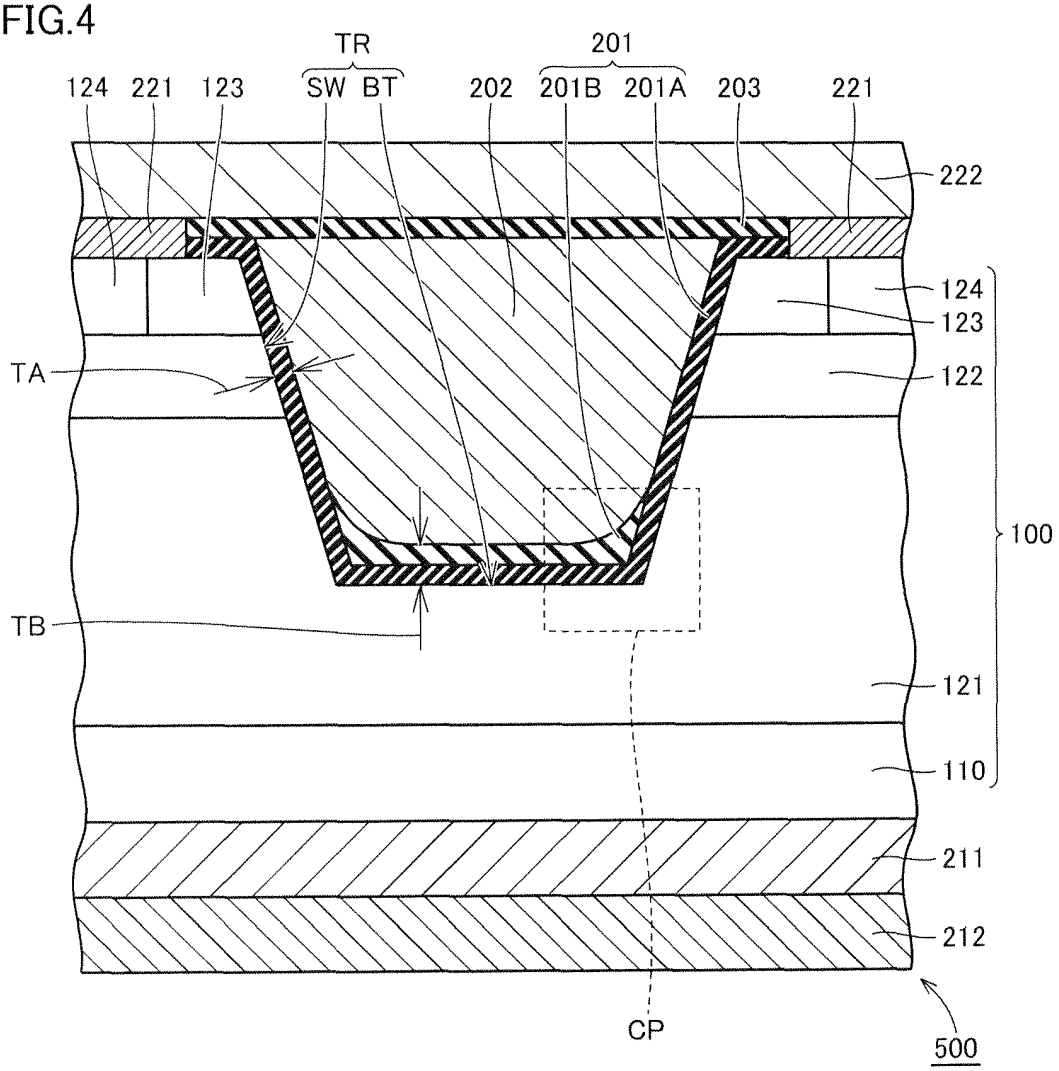

TR
201
124
221
123
SW
BT
202
201B
201A
203
221
222
124
123
TA
122
100
TB
121
110
211
212
CP
500

FIG.5

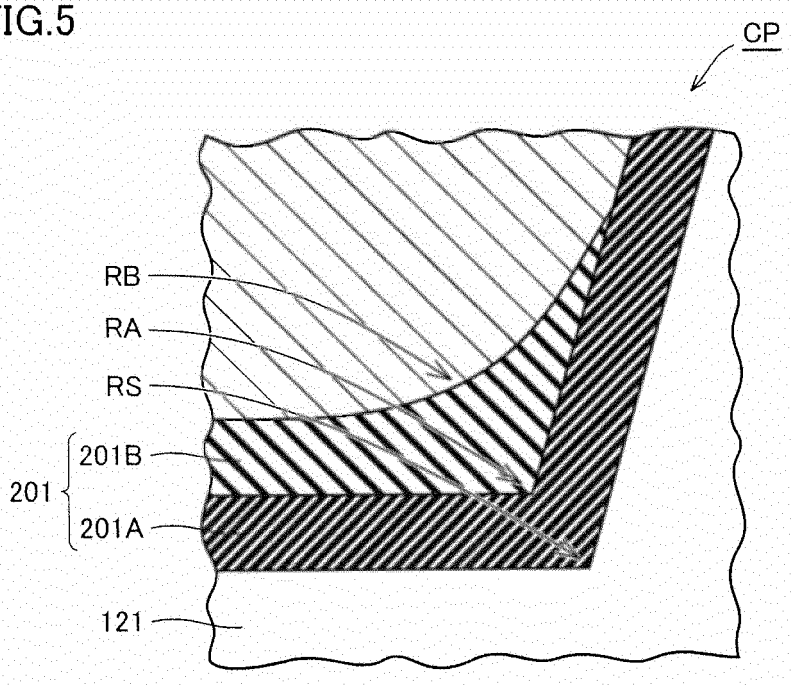


FIG.6

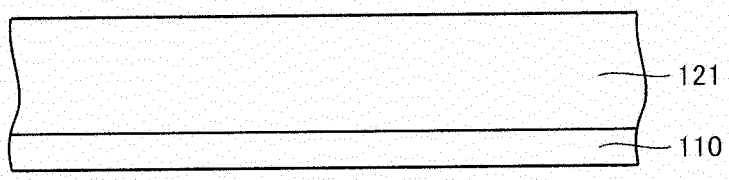


FIG.7

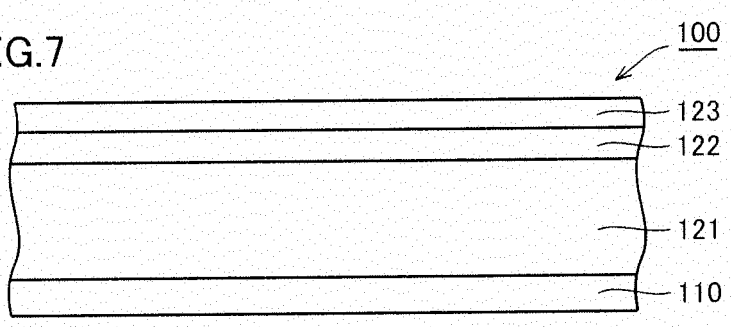


FIG.8

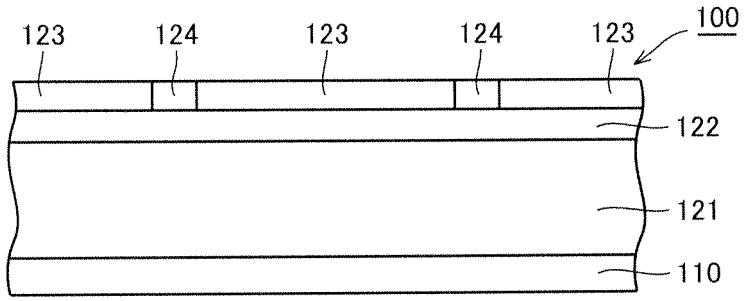


FIG.9

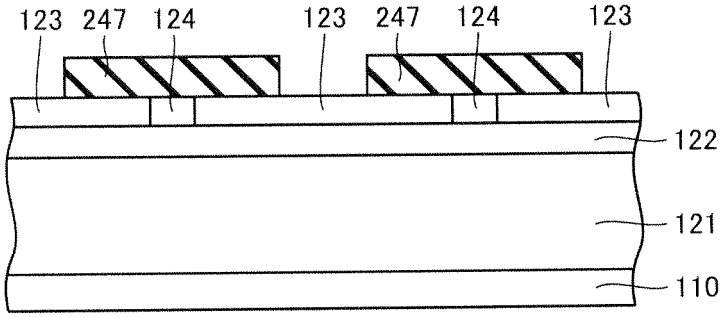


FIG.10

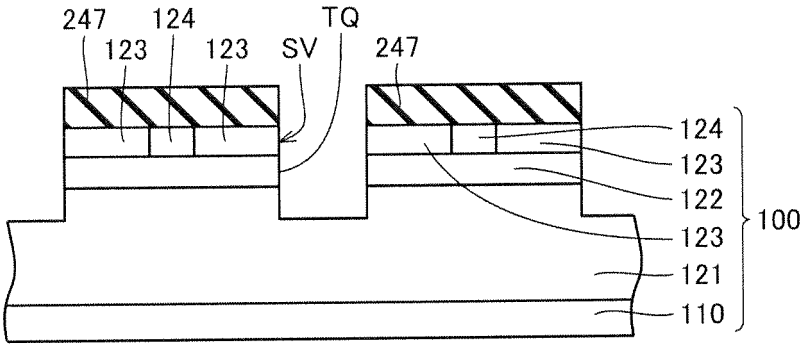


FIG.11

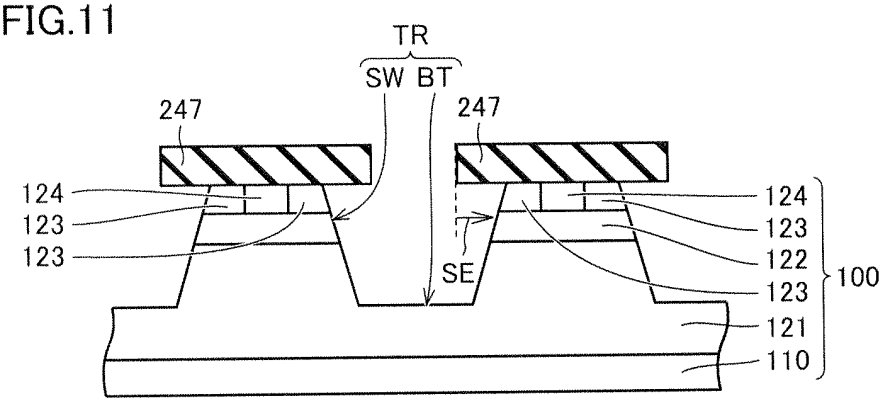


FIG.12

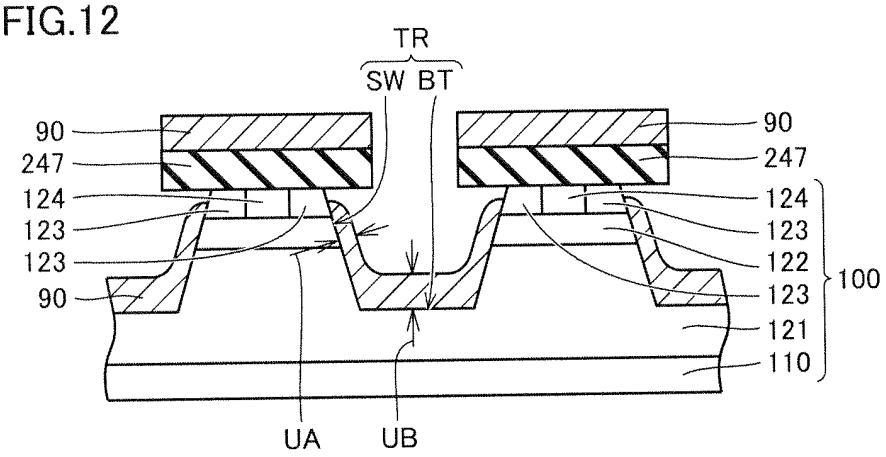


FIG.13

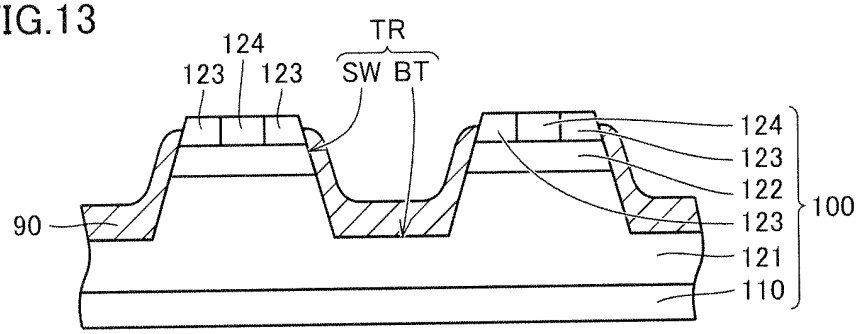


FIG.14

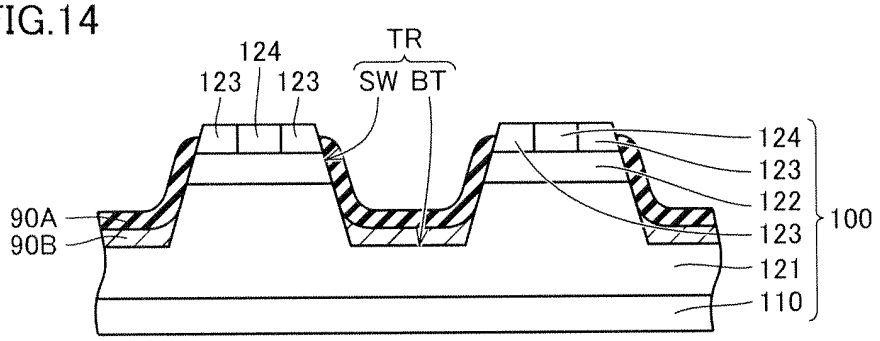


FIG.15

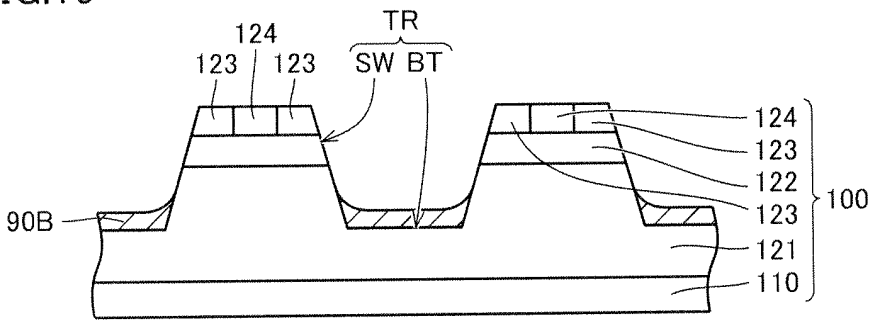


FIG.16

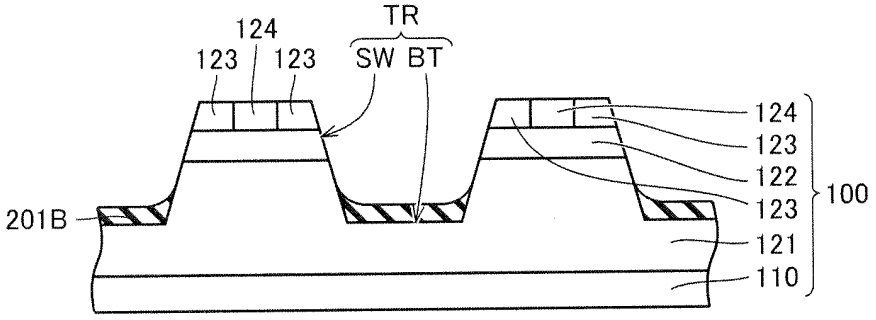


FIG.17

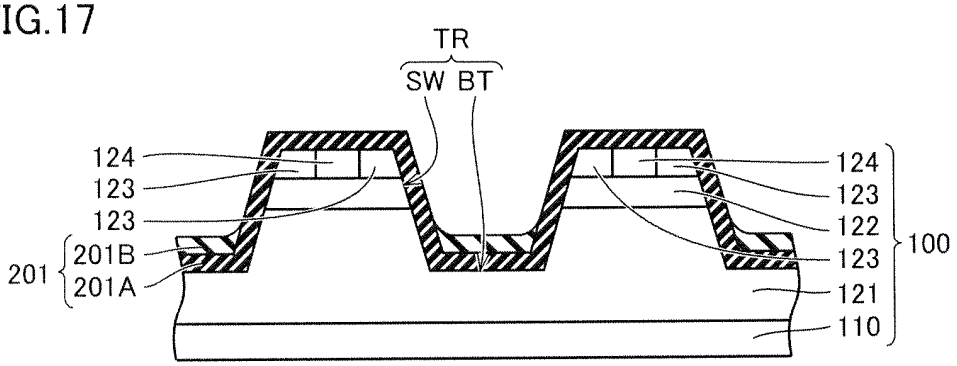


FIG.18

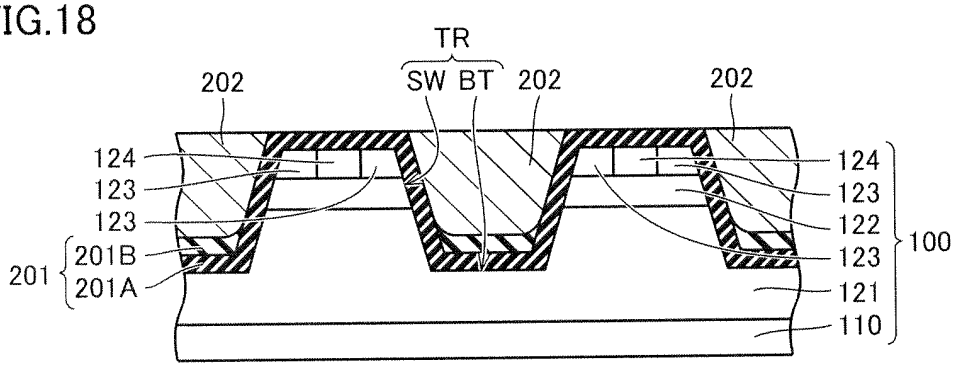


FIG.19

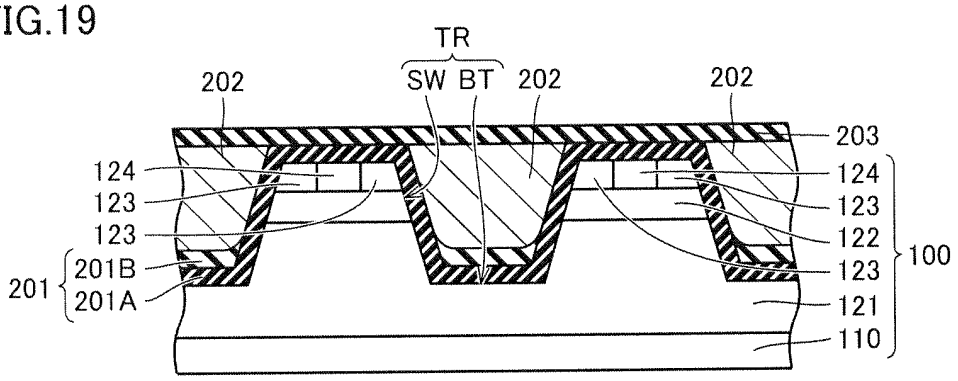


FIG.20

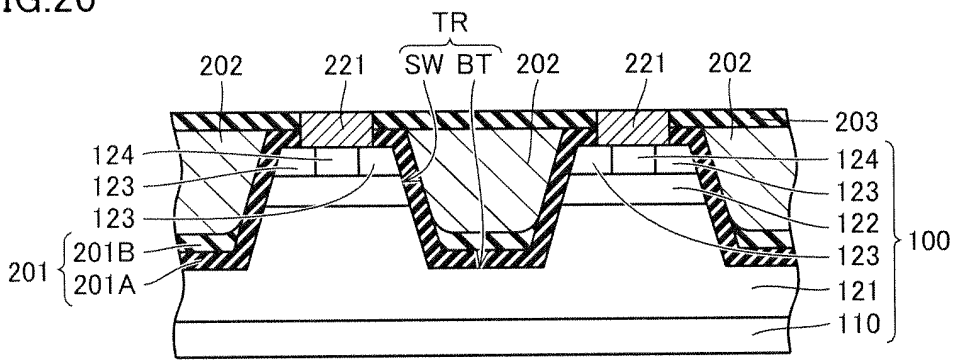

TR
202
221
SW
BT
202
221
202
203
124
123
123
201
201B
201A
124
123
122
123
100
121
110

FIG.21

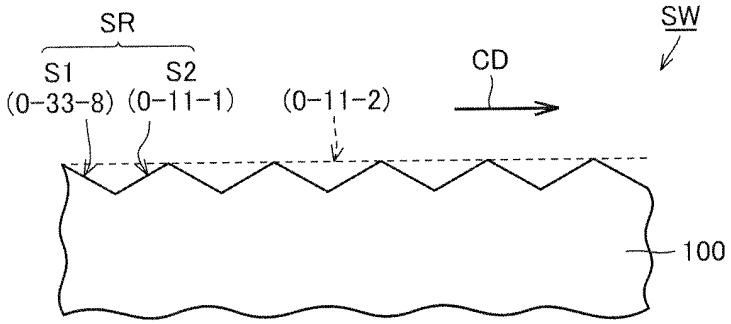

SR
S1
(0-33-8)
S2
(0-11-1)
(0-11-2)
CD
SW
100

FIG.22

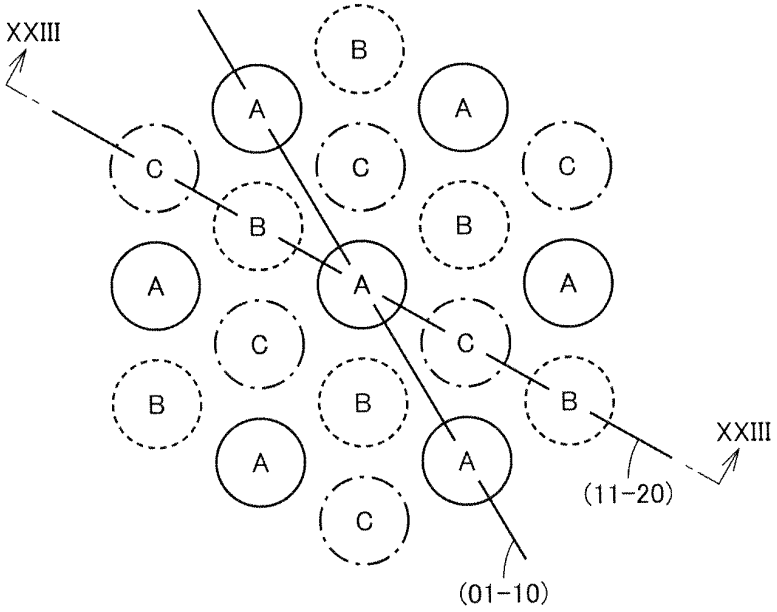


FIG.23

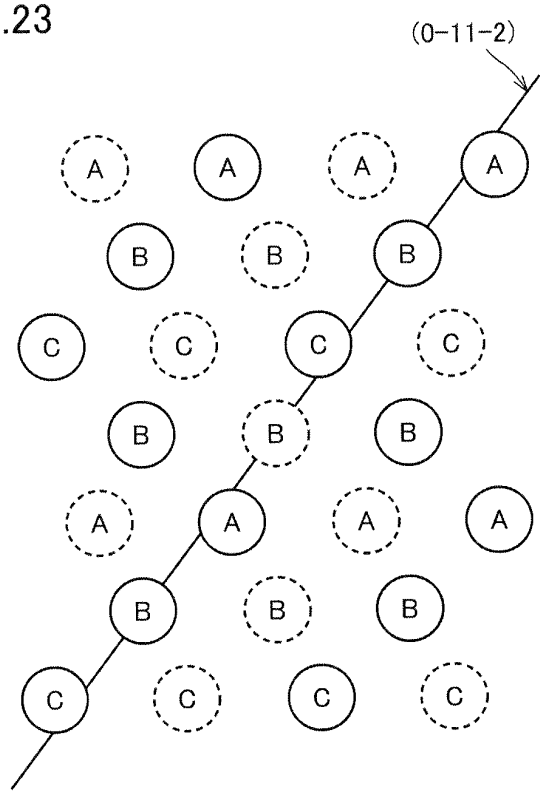


FIG.24

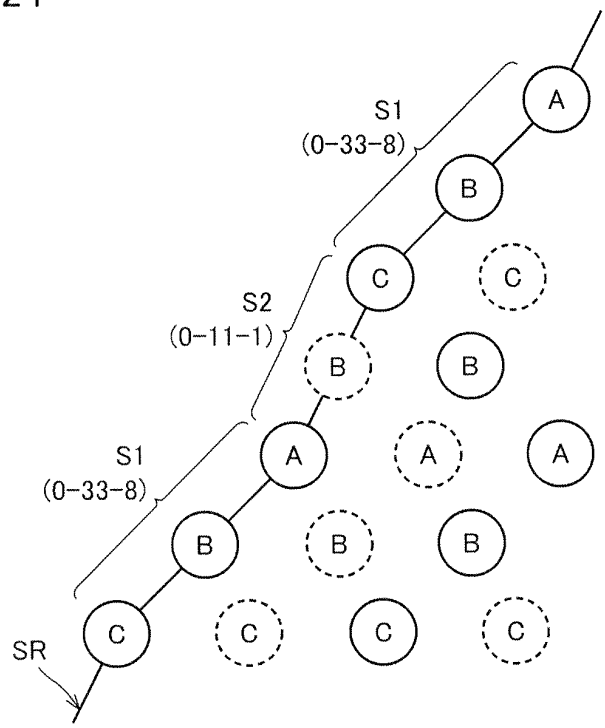

S1
(0-33-8)
S2
(0-11-1)
S1
(0-33-8)
SR
A
B
C

FIG.25

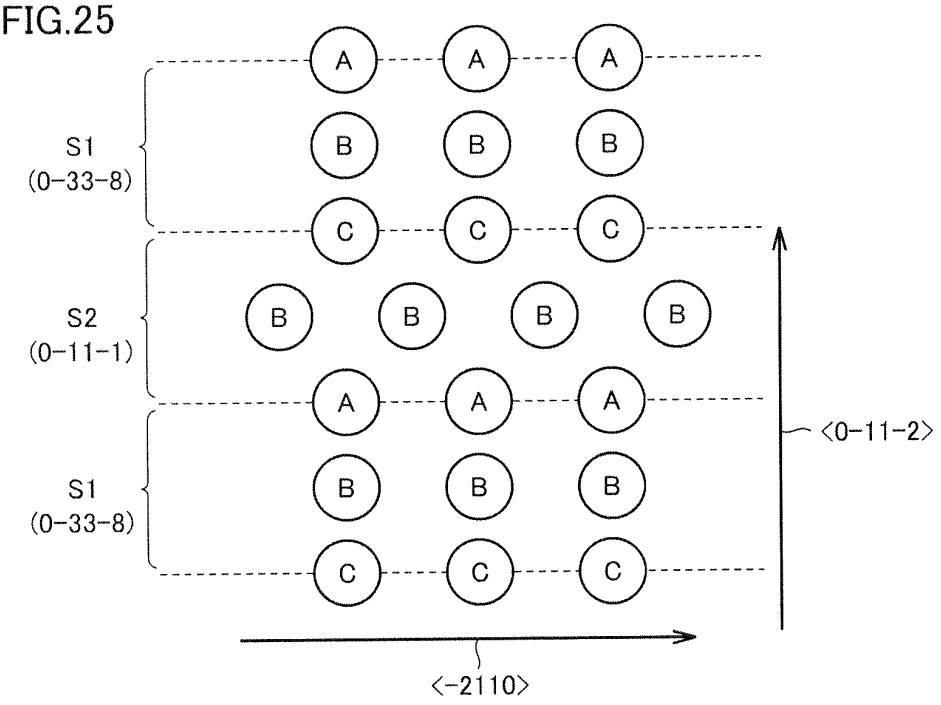

S1
(0-33-8)
S2
(0-11-1)
S1
(0-33-8)
<0-11-2>
<-2110>
A
B
C

FIG.26

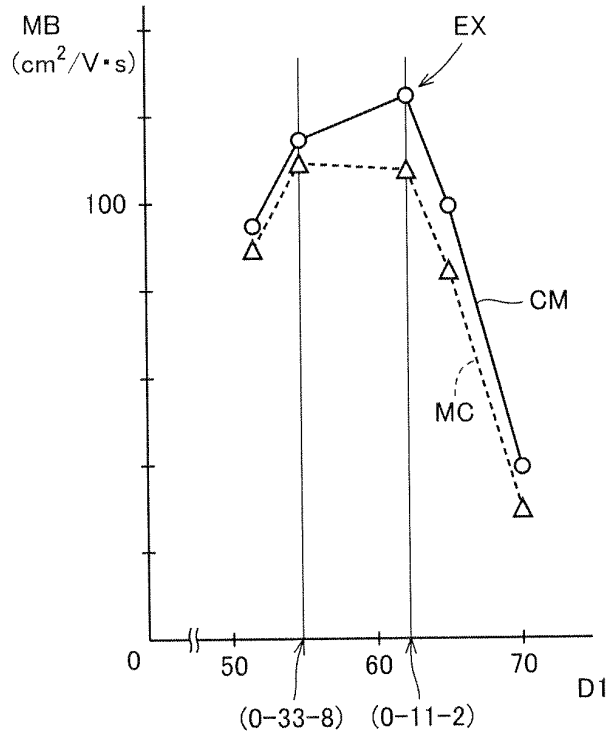

MB
(cm²/V·s)
EX
100
CM
MC
0
50
60
70
D1
(0-33-8)
(0-11-2)

FIG.27

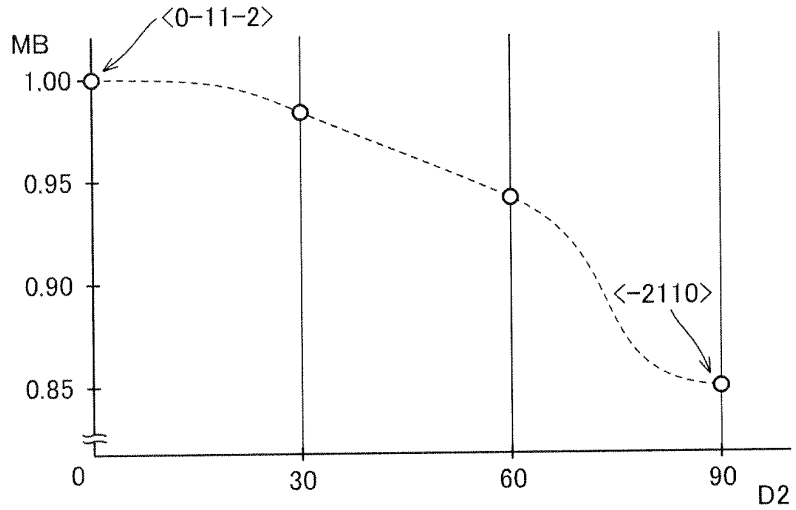
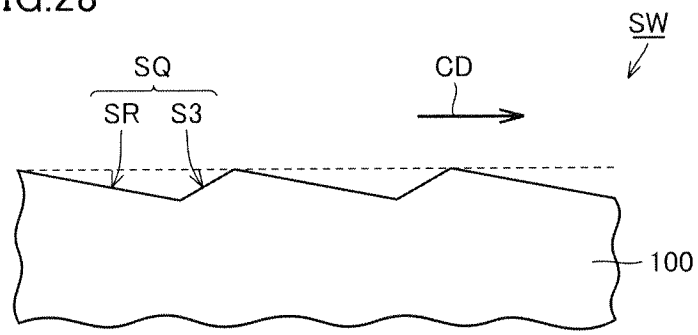

<0-11-2>
MB
1.00
0.95
0.90
0.85
<-2110>
0
30
60
90
D2

FIG.28



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2013/068399

A. CLASSIFICATION OF SUBJECT MATTER
H01L29/78(2006.01)i, *H01L21/336*(2006.01)i, *H01L29/12*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L29/78, H01L21/336, H01L29/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2013
Kokai Jitsuyo Shinan Koho	1971-2013	Toroku Jitsuyo Shinan Koho	1994-2013

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2009-224365 A (Rohm Co., Ltd.), 01 October 2009 (01.10.2009), paragraphs [0016] to [0031]; fig. 1 to 4 (Family: none)	1-8
Y	JP 2010-263104 A (Elpida Memory, Inc.), 18 November 2010 (18.11.2010), paragraphs [0018] to [0026]; fig. 1 to 7 (Family: none)	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 September, 2013 (27.09.13)	08 October, 2013 (08.10.13)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 7326755 A **[0002] [0003]**