(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 908 542 A1**

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
19.08.2015 Bulletin 2015/34

(21) Application number: **13845230.5**

(22) Date of filing: **08.10.2013**

(51) Int Cl.:
H04N 21/4385 *(2011.01)* ***H04N 21/418*** *(2011.01)*
H04N 21/434 *(2011.01)*

(86) International application number:
PCT/JP2013/077398

(87) International publication number:
WO 2014/057955 (17.04.2014 Gazette 2014/16)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **10.10.2012 JP 2012225563**

(71) Applicant: **Sony Corporation**
Tokyo 108-0075 (JP)

(72) Inventors:
- **HIRAYAMA, Yuichi**
  Tokyo 108-0075 (JP)
- **OKADA, Satoshi**
  Tokyo 108-0075 (JP)
- **MICHAEL, Lachlan, Bruce**
  Tokyo 108-0075 (JP)
- **IKEDA, Tamotsu**
  Tokyo 108-0075 (JP)

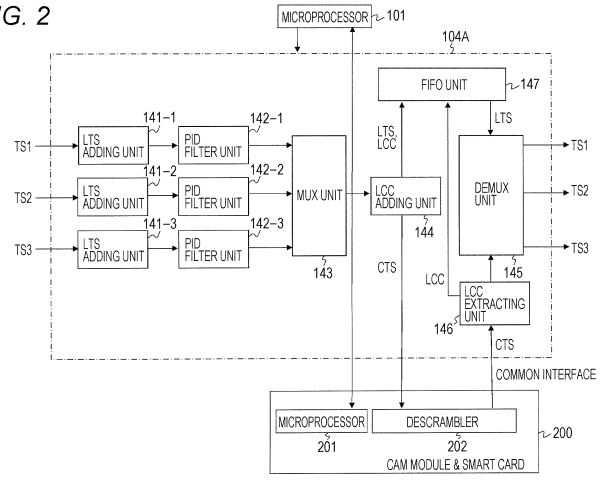
(74) Representative: **Witte, Weller & Partner**
Patentanwälte mbB
Postfach 10 54 62
70047 Stuttgart (DE)

(54) ELECTRONIC DEVICE, COMPOSITE-STREAM TRANSMISSION METHOD, AND PROGRAM

(57) Plural streams are synthesized into one stream, and preferable transmission and reception of the synthesized stream to and from an external device is realized.

Transport stream packets of plural transport streams are synthesized to create a synthesized stream, and the created synthesized stream is transmitted to an external device. In this transmission, a count information adding area provided in each of the transport stream packets is brought into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream. This configuration notifies the external device that a function for handling packet order switching based on count information is not provided, and receives from the external device a synthesized stream containing the respective transport stream packets arranged in the same order as the order of the transport stream packets at the time of transmission.

FIG. 2



EP 2 908 542 A1

Description

TECHNICAL FIELD

[0001] The present technology relates to an electronic device, a synthesized stream transmitting method, and a program, and more particularly to an electronic device and others for synthesizing plural streams into one stream and transmitting and receiving the synthesized stream to and from an external device.

BACKGROUND ART

[0002] CI_Plus standard v1. 3. 1 released in January, 2011 does not have a function of simultaneous descrambling of plural receiving channels, and therefore does not allow simultaneous recording of a program by a viewer who is viewing another program. Rather than CI_Plus, M-Card system meeting USA open cable (Open Cable) standards is known as a precedent having this function, and is currently in operation.

[0003] M-Card system realizes output from a host device (Host Device), such as a television receiver (TV Set) and a set-top box (Set-top Box), to a CAM module having the descrambling function without changing a conventional physical interface, by full-multiplexing MPEG-TS signals received by two tuners provided within the host device on a time axis.

[0004] For example, there is described in Patent Document 1, a method which creates a synthesized stream by multiplexing two transport streams, transmits and receives the synthesized stream to and from a security mechanism executing descrambling, and distributes transport packets of the received synthesized stream based on stream identification information.

CITATION LIST

PATENT DOCUMENT

[0005] Patent Document 1: US Patent No. 7,508,454

SUMMARY OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0006] An object of the present technology is to synthesize plural streams into one stream, and realize preferable transmission and reception of the synthesized stream to and from an external device.

SOLUTIONS TO PROBLEMS

[0007] A concept of the present technology is directed to an electronic device including:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;

a stream transmitting unit that transmits the created synthesized stream to an external device;

a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;

a count information adding unit that brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device;

a stream receiving unit that receives the synthesized stream from the external device; and

a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information corresponding to the respective transport stream packets and sequentially output from the processing information retaining unit.

[0008] According to the present technology, the synthesized stream creating unit synthesizes transport stream packets of plural transport streams to create a synthesized stream. Then, the stream transmitting unit transmits the synthesized stream to the external device. For example, the stream transmitting unit and the stream receiving unit may transmit and receive the synthesized stream to and from the external device via a DVB-CI common interface, or a CI+ common interface, and the external device may be a conditional access module (CAM module) that executes descrambling.

[0009] The processing information retaining unit retains processing information for a certain period, which information is output at the transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets. The processing information retaining unit is constituted by a FIFO (first in first out) memory, for example.

[0010] The count information adding unit brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device. For example, the count information adding area may be constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

[0011] In this case, the partial area may be a predetermined-number bit area having 1 as a bit value of a synchronous signal. In this case, bit values corresponding to a synchronous signal can be used without change when the particular count value is set to a value containing 1 for all the bit values. In this state, rewriting is not

required.

[0012] The stream receiving unit receives the synthesized stream from the external device. For example, the external device equalizes the order of the respective transport stream packets of the transmitted synthesized stream with the order of the respective transport stream packets of the received synthesized stream based on the fact that the count information added to the count information adding area provided in each of the transport stream packets is the particular count value. Then, the processing unit processes the respective transport stream packets of the received synthesized stream based on the processing information sequentially output from the processing information and corresponding to the respective transport stream packets.

[0013] According to the present technology, therefore, the count information adding area provided in each of the transport stream packets is brought into the state to which the particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device. Accordingly, this configuration notifies the external device that a function for handling the packet order switching based on count information is not provided, and receives the synthesized stream containing the respective transport stream packets arranged in the same order as the order of the transport stream packets at the time of transmission.

[0014] According to the present technology, the processing information for processing the respective transport stream packets may contain time information indicating time positions of the respective transport stream packets in original transport streams, and the processing unit may locate, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams, for example.

[0015] In this case, there may be further provided a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device, and a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream. The processing unit may distribute the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

[0016] Another concept of the present technology is directed to an electronic device including:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;

a stream transmitting unit that transmits the created synthesized stream to an external device;

a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;

a count information adding unit that adds count information sequentially counted while skipping a particular count value to both a count information adding area provided in each of the transport stream packets, and processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device;

a stream receiving unit that receives the synthesized stream from the external device; and

a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining unit and containing count information having the same value as the value of count information added to each of the transport stream packets.

[0017] According to the present technology, the synthesized stream creating unit synthesizes transport stream packets of plural transport streams to create a synthesized stream. Then, the stream transmitting unit transmits the synthesized stream to the external device. For example, the stream transmitting unit and the stream receiving unit may transmit and receive the synthesized stream to and from the external device via a DVB-CI common interface, or a CI+ common interface, and the external device may be a conditional access module (CAM module) that executes descrambling.

[0018] The processing information retaining unit retains the processing information for a certain period, which information is output at the transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets. The processing information retaining unit is constituted by a FIFO (first in first out) memory, for example.

[0019] The count information adding unit adds the count information sequentially counted while skipping a particular count value to both the count information adding area provided in each of the transport stream packets, and the processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device. For example, the count information adding area may be constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets. In this case, the partial area may be a low-order 4-bit area or a low-order 3-bit area, for example.

[0020] The stream receiving unit receives the synthesized stream from the external device. Then, the processing unit processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining unit and containing count information having the same count value as the count value of count information added to each of the transport stream packets.

[0021] According to the present technology, therefore, the count information sequentially counted while skipping a particular count value is added to both the count information adding area provided in each of the transport stream packets, and the processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device. Accordingly, this configuration notifies the external device that the function for handling packet order switching based on count information is provided. In this case, the respective transport stream packets of the received synthesized stream can be appropriately processed based on the corresponding processing information even when the respective transport stream packets received from the external device are arranged in an order different from the order of the transport stream packet at the time of transmission.

[0022] According to the present technology, for example, the processing information for processing the respective transport stream packets of the received synthesized stream may contain time information indicating time positions of the respective transport stream packets in original transport streams, and the processing unit may locate, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams.

[0023] In this case, there may be further provided a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device, and a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream. The processing unit may distribute the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

[0024] A further concept of the present technology is directed to an electronic device including:

a stream receiving unit that receives a synthesized stream created by synthesizing transport stream packets of plural transport streams from an external device;

a processing unit that separates the respective transport stream packets of the received synthesized stream, decrypts the respective separated transport stream packets, and synthesizes the respective decrypted transport stream packets to create a synthesized stream;

a stream transmitting unit that transmits the created synthesized stream to the external device; and

a control unit that controls the processing unit based on count information added to a count information adding area provided in each of the transport stream packets of the received synthesized stream.

[0025] According to the present technology, the stream receiving unit receives the synthesized stream created by synthesizing the transport stream packets of the plural transport streams from the external device. The processing unit separates the respective transport stream packets of the received synthesized stream, decrypts the respective separated transport stream packets, and synthesizes the respective decrypted transport stream packets to create a synthesized stream. Then, the stream transmitting unit transmits the created synthesized stream to the external device.

[0026] The control unit controls the processing unit based on count information added to the count information adding area provided in each of the transport stream packets of the received synthesized stream. For example, the count information adding area may be constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

[0027] For example, the control unit may control such that the order of the respective transport stream packets of the created synthesized stream becomes the same order as the order of the respective transport stream packets of the received synthesized stream when the count information has a particular count value. In this case, the control unit may raise the speed of decrypting operation. By raising the operation speed, the power consumption increases. However, reduction of the delay amount is achievable.

[0028] According to the present technology, therefore, the processing unit is controlled based on the count information added to the count information adding area provided in each of the transport stream packets of the received synthesized stream. This configuration easily notifies the external device that the function for handling packet order switching based on count information is not provided, and transmits to the external device a synthesized stream containing the respective transport stream packets arranged in the same order as the order of the transport stream packets at the time

[0029] of transmission.

EFFECTS OF THE INVENTION

[0030] According to the present technology, plural streams are synthesized into one stream, and preferable transmission and reception of the synthesized stream to and from an external device is realized.

BRIEF DESCRIPTION OF DRAWINGS

[0031]

Fig. 1 is a block diagram illustrating a configuration example of a digital broadcasting reception system according to an embodiment.

Fig. 2 is a block diagram illustrating a configuration example of a common interface controller which has a function for handling packet order switching based on count information, and allows switching of a packet order at a CAM module.

Fig. 3 is a figure illustrating a structure of a transport stream packet (TSP).

Fig. 4 is a block diagram illustrating a configuration example of a multiplexing unit constituting a common interface controller.

Figs. 5 (a) and 5 (b) are figures illustrating an example of information added to a PID packet, and an example of information retained at a FIFO unit only for a certain period.

Fig. 6 is a figure illustrating an example of bit allocation of LTSID and LCC in a synchronous byte area.

Figs. 7 (a) to 7 (c) are figures illustrating an example of bit arrangement and the like when 4 bits are allocated to both LTSID and LCC.

Figs. 8 (a) to 8 (c) are figures illustrating an example of bit arrangement and the like when 5 bits and 3 bits are allocated to LTSID and LCC, respectively.

Figs. 9(a) to 9(c) are figures illustrating another example of bit arrangement and the like when 4 bits are allocated to both LTSID and LCC.

Fig. 10 is a block diagram illustrating a configuration example of a demultiplexing unit constituting the common interface controller.

Fig. 11 is a block diagram illustrating a configuration example of a FIFO unit constituting the common interface controller.

Figs. 12(a) to 12(d) are figures schematically illustrating an operation example (1/2) of the FIFO unit.

Figs. 13(e) to 13(h) are figures schematically illustrating an operation example (2/2) of the FIFO unit.

Figs. 14(a) and 14(b) illustrate a configuration example of the PID packets of respective transport streams supplied to the LTS adding unit and an example of not unnecessary PID packets after removal of PID data packets of not selected (channel-selected) service channels.

Figs. 15(a) to 15(c) are figures for explaining processing by the multiplexing unit and an LCC adding unit.

Figs. 16(a) to 16(c) are figures for explaining processing by the demultiplexing unit and the FIFO unit.

Fig. 17 is a flowchart showing an example of processing procedures executed by the common interface controller for synthesizing PID packets of respective transport streams and transmitting the synthesized PID packets to the CAM module as one stream.

Fig. 18 is a figure illustrating an example of processing procedures executed by the common interface controller for receiving the synthesized PID packets of the respective transport streams from the CAM module.

Fig. 19 is a block diagram illustrating a configuration example of a common interface which does not have the function for handling packet order switching based on count information, and does not allow switching of a packet order at the CAM module.

Figs. 20(a) to 20(c) are figures schematically illustrating an operation example (1/2) of the FIFO unit.

Fig. 21(a) to 21(c) are figures schematically illustrating an operation example (2/2) of the FIFO unit.

Fig. 22 is a flowchart showing an example of processing procedures executed by the common interface controller for synthesizing PID packets of respective transport streams and transmitting the synthesized PID packets to the CAM module as one stream.

Fig. 23 is a figure illustrating an example of processing procedures executed by the common interface controller for receiving the synthesized PID packets of the respective transport streams from the CAM module.

Fig. 24 is a block diagram illustrating a configuration example of the CAM module.

Figs. 25(a) to 25(d) are timing charts when a synthesized stream CTS received by a TS separating unit is transmitted from a controller having the function for handling packet order switching based on count information.

Figs. 26(a) to 26(d) are timing charts when the synthesized stream CTS received by the TS separating unit is transmitted from a controller not having the function for handling packet order switching based on count information.

Fig. 27 is a flowchart showing an outline of an example of processing procedures executed by the CAM module.

Figs. 28(a) to 28(d) are timing charts when the synthesized stream CTS received by the TS separating unit is transmitted from a controller not having the function for handling packet order switching based on count information, at a raised speed of decryption.

Figs. 29 (a) and 29(b) are figures illustrating another example of information added to a PID packet, and information retained by the FIFO unit only for a certain period.

Fig. 30 is a figure illustrating an example of bit allocation of LTSID and LCC in a cyclic counter area.

MODE FOR CARRYING OUT THE INVENTION

[0032] A mode for carrying out the invention (hereinafter referred to as "embodiment") is now described. The description is presented in the following order.

1. Embodiment
2. Modified Example

<1. Embodiment>

[Configuration Example of Digital Broadcasting Reception System]

[0033] Fig. 1 is a configuration example of a digital broadcasting reception system 10 according to the embodiment. Discussed herein is an example handling three transport streams. However, the number of transport streams allowed to be handled by the present technology is not limited to this number. The reception system 10 is constituted by a host device (Host Device) 100, and a CAM module (CAM Module) 200. The host device 100 is an electronic device such as a television receiver (TV Set) and a set-top box (Set-top Box).

[0034] The host device 100 includes a microprocessor (Microprocessor) 101, tuners (Tuners) 102-1, 102-2, and 102-3, and demodulators (Demodulators) 103-1, 103-2, and 103-3. The host device 100 further includes a common interface controller (Common Interface Controller) 104, demultiplexers (Demultiplexers) 105-1, 105-2, and 105-3. The host device 100 further includes MPEG decoders (MPEG Decoders) 106-1, 106-2, and 106-3.

[0035] The microprocessor 101 controls operations of the respective units of the host device 100. The tuners 102-1, 102-2, and 102-3 receive RF modulation signals of transport streams TS1, TS2, and TS3, respectively, transmitted from broadcasting stations. The tuners 102-1, 102-2, and 102-3 subsequently down-convert the received RF modulation signals into signals at an intermediate frequency, and output the converted signals as input to the demodulators 103-1, 103-2, and 103-3. The demodulators 103-1, 103-2, and 103-3 demodulate IF modulation signals at the intermediate frequency after down-conversion to obtain the baseband transport streams TS1, TS2, and TS3, respectively.

[0036] The common interface controller 104 synthesizes the transport streams TS1, TS2, and TS3 obtained at the demodulators 103-1, 103-2, and 103-3 to create a synthesized stream, and exchanges the synthesized stream with the CAM module 200, i.e., transmits and receives the synthesized stream to and from the CAM module 200. The common interface controller 104 and the CAM module 200 are connected via a DVB-CI common interface (DVB-CI Common Interface), or a CI+ common interface (CI+ Common Interface).

[0037] Each of the transport streams contains PID packets (TSP: transport stream packets) of plural service channels on a time-sharing basis. The common interface controller 104 performs exchanges while removing PID data packets of service channels not selected (channel-selected) from each of the transport streams. This method is adopted for the purpose of reduction of the transmission bit rate. The detailed configuration of the common interface controller 104 will be described later.

[0038] The demultiplexers 105-1, 105-2, and 105-3 extract PID data packets of selected (channel-selected) service channels from the transport streams TS1, TS2, and TS3 obtained at the common interface controller 104. These PID data packets are video and audio PID data packets. The MPEG decoders 106-1, 106-2, and 106-3 decode elementary streams constituted by the PID data packets extracted by the demultiplexers 105-1, 105-2, and 105-3 to obtain video data and audio data.

[0039] The CAM module 200 is an attachment device which engages with a common interface connector (Common Interface Connector) of the host device 100 for executing descrambling. The CAM module 200 is used with insertion of cards (Smartcards) such as a magnetic card and an IC card where view subscriber information, contract term information and others are recorded.

[0040] The CAM module 200 includes a microprocessor 201 and a descrambler (De-scrambling) 202. The CAM module 200 receives PID packets transmitted from the common interface controller 104 of the host device 100 via a common interface, and descrambles the received PID packets. The CAM module 200 subsequently transmits the respective PID packets to the common interface controller 104 of the host device 100.

[0041] The operation of the reception system 10 illustrated in Fig. 1 is now briefly described. The RF modulation signals of the transport streams TS1, TS2, and TS3 transmitted from the broadcasting stations are received by the tuners 102-1, 102-2, and 102-3, respectively. The received RF modulation signals are down-converted into signals at an intermediate frequency by the tuners 102-1, 102-2, and 102-3, and supplied to the demodulators 103-1, 103-2, and 103-3. The demodulators 103-1, 103-2, and 103-3 demodulate the IF modulation signals down-converted into the intermediate frequency to obtain the baseband transport streams TS1, TS2, and TS3, respectively. The obtained transport streams TS1, TS2, and TS3 are supplied to the common interface controller 104.

[0042] The common interface controller 104 synthesizes the PID packets of the transport streams TS1, TS2, and TS3 supplied from the demodulators 103-1, 103-2, and 103-3 to create a synthesized stream. The respective PID packets constituting the synthesized stream are sequentially transmitted from the common interface controller 104 to the CAM module 200 via the common interface. At this time, PID data packets of service channels not selected (channel-selected) are removed from each of the transport streams.

[0043] The CAM module 200 receives the synthesized stream transmitted from the common interface controller

104 of the host device 100 via the common interface, and descrambles the respective PID packets. Thereafter, the synthesized stream is transmitted from the CAM module 200 to the common interface controller 104 of the host device 100 via the common interface.

[0044] The common interface controller 104 receives the synthesized stream transmitted from the CAM module 200 via the common interface. The common interface controller 104 distributes the respective PID packets contained in the synthesized stream to respective streams to reconstitute the transport streams TS1, TS2, and TS3. The reconstituted transport streams TS1, and TS2, and TS3 are supplied to the demultiplexers 105-1, 105-2, and 105-3, respectively.

[0045] The demultiplexers 105-1, 105-2, and 105-3 extract PID data packets of service channels selected (channel-selected) from the transport streams TS1, TS2, and TS3, respectively, to which the PID data packets have been distributed by the common interface controller 104. The video and audio PID data packets extracted at the demultiplexers 105-1, 105-2, and 105-3 are supplied to the MPEG decoders 106-1, 106-2, and 106-3.

[0046] Each of the MPEG decoders 106-1, 106-2, and 106-3 decodes video and audio elementary streams constituted by video and audio PID data packets. Thereafter, video data and audio data of the selected (channel-selected) service channels are output from the MPEG decoders 106-1, 106-2, and 106-3.

[Configuration Example of Common Interface Controller]

[0047] The detailed configuration of the common interface controller 104 is now described. Discussed herein are (1) a common interface controller 104A having a function for handling packet order switching based on count information, and (2) a common interface controller 104B not having a function for handling packet order switching based on count information.

"Example Having Function for Handling Packet Order Switching"

[0048] Initially discussed is the common interface controller 104A which has a function for handling packet order switching based on count information, and allows switching of the packet order at the CAM module 200. Fig. 2 illustrates a configuration example of the controller 104A. The controller 104A includes LTS (Local Time Stamp) adding units 141-1, 141-2, and 141-3, and PID filter (PID filter) units 142-1, 142-2, and 142-3. The controller 104A further includes a multiplexing (MUX) unit 143, an LCC (Local Continuity Counter) adding unit 144, a demultiplexing (DEMUX) unit 145, an LCC extracting unit 146, and a FIFO (First In First Out) unit 147.

[0049] The LTS adding units 141-1, 141-2, and 141-3 add an LTS (Local Time Stamp) corresponding to input time to each of the PID packets (TSP: transport stream packet) of the corresponding input transport streams TS1, TS2 and TS3. This LTS is obtained based on a clock generated by a self-advancing type clock generator or a PCR-recovered clock generator, for example.

[0050] The PID filter units 142-1, 142-2, and 142-3 execute filtering for removing PID data packets of channels not selected (channel-selected) from the transport streams TS1, TS2, and TS3. This filtering reduces the transmission bit rate of the synthesized stream obtained by synthesizing the respective PID data packets of the transport streams TS1, TS2, and TS3.

[0051] The multiplexing unit 143 synthesizes the respective PID packets of the transport streams TS1, TS2, and TS3 into one stream, i.e., creates a synthesized stream CTS, and outputs the synthesized stream CTS. The multiplexing unit 143 also adds an LTSID (Local TS Identifier) to a part of a synchronous byte (Sync byte) within a TS header of each of the PID packets of the synthesized stream CTS thus created. This LTSID is stream identification information for identifying the original transport stream of the corresponding PID packet, and created and used at the time of creation of the synthesized stream CTS.

[0052] Fig. 3 illustrates a structure of a TSP (PID packet). A TSP is configured to have a fixed length of 188 bytes. Initial 4 bytes of the TSP correspond to a TS header, and the following 184 bytes correspond to a PES packet payload. There exist in the TS header an 8-bit synchronous word (0×47) in the initial synchronous byte area, a subsequent 13-bit PID, and a final 4-bit cyclic counter (Continuity counter).

[0053] The multiplexing unit 143 also outputs LTSs (Local Time Stamps) corresponding to the respective PID packets in accordance with the output timing of the respective PID packets of the synthesized stream CTS. Each of the LTSs is time information indicating a time position of the corresponding PID packet in the original transport stream. For example, the LTSs added by the LTS adding units 141-1, 141-2, and 141-3 as discussed above are separated and utilized as the LTSs to be output from the multiplexing unit 143.

[0054] Fig. 4 illustrates a configuration example of the multiplexing unit 143. The multiplexing unit 143 includes LTS separating units 151-1, 151-2, and 151-3, and a TS multiplexing unit 152. The LTS separating units 151-1, 151-2, and 151-3 separate LTSs from the respective PID packets of the transport streams TS1, TS2, and TS3. The LTS separating units 151-1, 151-2, and 151-3 subsequently output the transport streams TS1, TS2, and TS3 constituted by respective PID packets not containing LTS, and also output LTSs corresponding to the LTSs which had been added to the respective PID packets.

[0055] The TS multiplexing unit 152 synthesizes the respective PID packets of the transport streams TS1, TS2, and TS3 output from the LTS separating units 151-1, 151-2, and 151-3 to create and output the synthesized stream CTS. For example, the respective PID packets of the transport streams TS1, TS2, and TS3 are temporarily accumulated in a not-shown dual port memory,

and sequentially extracted in the order from the earliest PID packet on a time basis for synthesis.

[0056] The TS multiplexing unit 152 also creates a predetermined-bit LTSID for identifying the original transport stream of each of the PID packets of the synthesized stream CTS, and inserts and adds the created LTSID to a part of the synchronous byte area within the TS header of each of the PID packets. Thereafter, the TS multiplexing unit 152 sequentially outputs the LTSs corresponding to the respective PID packets based on the LTSs output from the LTS separating units 151-1, 151-2, and 151-3 in accordance with the output timing of the respective PID packets of the synthesized stream CTS.

[0057] The LCC adding unit 144 inserts and adds count information sequentially counted while skipping a particular count value to a count information adding area of each of the PID packets as an LCC (Local continuity counter) for each of the PID packets of the synthesized stream CTS output from the multiplexing unit 143. The count information adding area herein is constituted by a part of the synchronous byte area within the TS header of each of the PID packets. According to this embodiment, the particular count value is a value containing "1" for all the bit values. The particular count values are used by the common interface controller 104B which does not have the function for handling packet order switching based on count information, as will be described later.

[0058] The LCC adding unit 144 sequentially outputs the respective PID packets of the synthesized stream CTS containing LCCs added thereto in this manner to the CAM module 200. Each of the LCCs is count information for handling packet order switching which occurs within the CAM module 200, and is created and used at the time of addition of LCCs. The LCC adding unit 144 also adds LCCs added to the respective PID packets of the synthesized stream CTS as discussed above to LTSs output in correspondence with the respective PID packets from the multiplexing unit 143. The LCC adding unit 144 sequentially outputs the LTSs containing the added LCCs to the FIFO unit 147.

[0059] Fig. 5(a) illustrates insertion of LTSID and LCC into a synchronous byte (Sync byte) area within a TS header of a PID packet transmitted from the host device 100 (controller 104A, 104B) to the CAM module 200. Either LTSID or LCC may be located at the head. The bit areas of LTSID and LCC may be mixed. Fig. 5(b) illustrates addition of LCC to LTS supplied to the FIFO unit 147 within the host device 100 (controller 104A) for each of the PID packets.

[0060] Fig. 6 illustrates an example of bit allocation of LTSID and LCC in a synchronous byte area. For example, when 6 bits and 2 bits are allocated to LTSID and LCC, respectively, identification of 64 transport streams is allowed, wherefore order change of 2 or fewer packets can be handled. On the other hand, when 5 bits and 3 bits are allocated to LTSID and LCC, respectively, for example, identification of 32 transport streams is allowed, wherefore order change of 6 or fewer packets can be handled. Furthermore, when 4 bits are allocated to both LTSID and LCC, for example, identification of 16 transport streams is allowed, wherefore order change of 14 or fewer packets can be handled.

[0061] Fig. 7(a) illustrates an example of bit arrangement when 4 bits are allocated to both LTSID and LCC. According to this example, 4 bits of LTSID are located in high-order 4 bits, while 4 bits of LCC are located in low-order 4 bits. Fig. 7(b) shows respective bit values of a synchronous word (0×47) originally located in a synchronous byte area. Each of the sixth bit, second bit, first bit, and zeroth bit is "1", while each of the seventh bit, fifth bit, fourth bit, and third bit is "0".

[0062] Fig. 8(a) illustrates an example of bit arrangement when 5 bits and 3 bits are allocated to LTSID and LCC, respectively. According to this example, 5 bits of LTSID are located in high-order 5 bits, while 3 bits of LCC are located in low-order 3 bits. Fig. 8(b) shows respective bit values of a synchronous word (0×47) originally located in a synchronous byte area similarly to Fig. 7 (b) discussed above.

[0063] According to the examples of bit arrangement illustrated in Fig. 7(a) and Fig. 8(a), the respective bits of LTSID are successively located in the high-order bit side, while the respective bits of LCC are successively located on the low-order bit side. On the contrary, the respective bits of LCC may be located on the high-order bit side, while the respective bits of LTSID may be located on the low-order bit side. In addition, the respective bits of LTSID and LCC are not required to be successively located.

[0064] Fig. 9(a) illustrates an example of bit arrangement when 4 bits are allocated to both LTSID and LCC. According to this example, the respective bits of LTSID are located in the seventh bit, fifth bit, fourth bit, and third bit, while the respective bits of LCC are located in the sixth bit, second bit, first bit, and zeroth bit. Fig. 9(b) shows the respective bit values of a synchronous word (0×47) originally located in a synchronous byte area similarly to Fig. 7(b) discussed above.

[0065] Returning to Fig. 2, the FIFO unit 147 retains LTSs sequentially output from the LCC adding unit 144 and containing added LCCs for a certain period. The certain period herein is required to be at least time corresponding to the maximum delay time from reception to transmission of the synthesized stream CTS by the CAM module 200.

[0066] The FIFO unit 147 also outputs LTSs corresponding to the respective PID packets for each of the PID packets of the synthesized stream CTS received from the CAM module 200 as will be described later. In this case, the FIFO unit 147 refers to LCC inserted and added to the synchronous byte area within the header of each of the PID packets, and selectively outputs LTS to which LCC having the same value is added. This selective output allows output of LTSs corresponding to the respective PID packets even when an order change of PID packets, i.e., packet order switching, occurs within

the CAM module 200.

[0067] The demultiplexing unit 145 receives the synthesized stream CTS from the CAM module 200. The demultiplexing unit 145 subsequently processes the respective PID packets of the received synthesized stream based on LTSs corresponding to the PID packets and output from the FIFO unit 147.

[0068] More specifically, the demultiplexing unit 145 distributes the respective PID packets of the received synthesized stream to respective streams based on LTSIDs inserted and added to the synchronous byte areas within the headers of the respective PID packets. The demultiplexing unit 145 subsequently locates the respective PID packets at time positions corresponding to LTSs in the respective streams to which the PID packets are distributed, so as to reconstitute the transport streams TS1, TS2, and TS3.

[0069] Fig. 10 illustrates a configuration example of the demultiplexing unit 145. The demultiplexing unit 145 includes a TS separating and Sync replacing unit 161, and output timing adjusting units 162-1, 162-2, and 162-3.

[0070] The TS separating and Sync replacing unit 161 distributes respective PID packets of a synthesized stream received from the CAM module 200 to respective streams based on LTSIDs added to the respective PID packets. The TS separating and Sync replacing unit 161 also replaces the bit values of the synchronous byte areas of the respective PID packets distributed to the corresponding streams with bit values of a synchronous word (0×47) at the FIFO unit 147.

[0071] The output timing adjusting units 162-1, 162-2, and 162-3 locate the respective PID packets at time positions in the respective streams in accordance with LTSs corresponding to the respective PID packets output from the FIFO unit 147. The output timing adjusting units 162-1, 162-2, and 162-3 subsequently output the reconstituted transport streams TS1, TS2, and TS3, respectively.

[0072] Returning to Fig. 2, the LCC extracting unit 146 extracts the LCC inserted into the synchronous byte area within the header of each of the PID packets from each of the PID packets of the received synthesized stream, and transmits the extracted LCC to the FIFO unit 147. As discussed above, the FIFO unit 147 refers to the received LCC, and selectively outputs LTS to which LCC having the same value is added.

[0073] Fig. 11 illustrates an example of a detailed configuration of the FIFO unit 147. Discussed in this example is a case when LCC is 2-bit count information. The FIFO unit 147 includes series circuits of six flip-flops (latched circuits) 171a, 171b, 171c, 171d, 171e, and 171f, a selection signal generating unit 172, and a switch unit 173.

[0074] The six flip-flop series circuits constitute a processing information retaining unit. TS sync signals (TS Sync) are input as latch signals from the multiplexing (MUX) unit 143 to the respective flip-flops. The LTS and LCC input from the LCC adding unit 144 are sequentially shifted to and retained by the following flip-flops every time a TS sync signal (TS Sync) is input.

[0075] The switch unit 173 selectively outputs one LTS from the respective LTSs retained by the flip-flops 171c, 171d, 171e, and 171f. The selection signal generating unit 172 compares the LCC extracted by the LCC extracting unit 146 with each of the LCCs retained by the flip-flops 171c, 171d, 171e, and 171f, and transmits a selection signal SWC to the switch unit 173 to allow the switch unit 173 to output LTS to which LCC having the same value is added.

[0076] By the function of the FIFO unit 147 having the configuration illustrated in Fig. 11, the LTSs corresponding to PID packets are extracted and output for each of the PID packets of the received synthesized stream even when the order of the PID packets (2 packet or fewer) changes within the CAM module 200.

[0077] Figs. 12 and 13 schematically illustrate an operation example of the FIFO unit 147 having the configuration illustrated in Fig. 11. According to this example, LCC to which 2 bits are allocated is added to each of the PID packets of the synthesized stream CTS, and changes in the manner as "0", "1", "2", "0", "1", and further in this order at the input to the CAM module 200. As discussed above, the count value containing "1" for all the bit values is skipped, wherefore the value following "2" ("10" in binary digits) is not "3" ("11" in binary digits), but "0" ("00" in binary digits).

[0078] In addition, according to this example, 6 bits are allocated to LTSID, wherefore identification of 64 transport streams is allowed. This example handles the synthesized stream CTS obtained by synthesizing the respective PID packets of three transport streams LTSID 0, LTSID 1, and LTSID 2.

[0079] Figs. 12 and 13 show input to the flip-flop 171a (FIFO in), output from the flip-flop 171c (C out), output from the flip-flop 171d (D out), output from the flip-flop 171e (E out), and output from the flip-flop 171f (F out) for the line of the FIFO unit 147. On the other hand, Figs. 12 and 13 show input (to CAM) and output (from CAM) for the line of the CAM module 200. "Numerals" indicate values of LCC added to LTS for the line of the FIFO unit 147, and indicate values of LCC added to a PID packet for the line of the CAM module 200.

[0080] The values of LCC added to the PID packet as input to the CAM module 200 (to CAM) agree with the values of LCC added to LTS as input to the flip-flop 171a (FIFO in). The state switches in the manner shown in Figs. 12(a), (b), (c), (d) and further in this order, in accordance with input of the TS sync signal (TS Sync).

[0081] The state in Fig. 12 (d) subsequently switches to a state in Fig. 13(e). In this case, the value of LCC added to the PID packet as output from the CAM module 200 (from CAM) is "1". This value agrees with the value of LCC added to LTS as output from the flip-flop 171e (E out). Accordingly, the switch unit 173 of the FIFO unit 147 outputs LTS of the flip-flop 171e at this time based on the selection signal SWC.

[0082] The state in Fig. 13 (e) subsequently shifts to a

state in Fig. 13(f). In this case, the value of LCC added to the PID packet as output from the CAM module 200 (from CAM) is "0" (order change). This value agrees with the value of LCC added to LTS as output from the flip-flop 171d (D out). Accordingly, the switch unit 173 of the FIFO unit 147 outputs LTS of the flip-flop 171d at this time based on the selection signal SWC.

[0083] The state in Fig. 13 (f) subsequently shifts to a state in Fig. 13(g). In this case, the value of LCC added to the PID packet as output from the CAM module 200 (from CAM) is "2". This value agrees with the value of LCC added to LTS as output from the flip-flop 171f (F out). Accordingly, the switch unit 173 of the FIFO unit 147 outputs LTS of the flip-flop 171f at this time based on the selection signal SWC.

[0084] The state in Fig. 13 (g) subsequently shifts to a state in Fig. 13(h). In this case, the value of LCC added to the PID packet as output from the CAM module 200 (from CAM) is "1". This value agrees with the value of LCC added to LTS as output from the flip-flop 171e (E out). Accordingly, the switch unit 173 of the FIFO unit 147 outputs LTS of the flip-flop 171e at this time based on the selection signal SWC. Thereafter, similar operations continue.

[0085] The operation of the common interface controller 104A illustrated in Fig. 2 is now described. The transport streams TS1, TS2, and TS3 supplied from the demodulators 103-1, 103-2, and 103-3 (see Fig. 1) are supplied to the LTS adding units 141-1, 141-2, and 141-3, respectively. The LTS adding units 141-1, 141-2, and 141-3 add LTSs (Local Time Stamps) corresponding to input time to the respective PID packets of the input transport streams TS1, TS2, and TS3 (TSP: transport stream packets), respectively.

[0086] The transport streams TS1, TS2, and TS3 containing the respective PID packets to each of which LTS is added are supplied to the PID filter units 142-1, 142-2, and 142-3, respectively. The PID filter units 142-1, 142-2, and 142-3 execute filtering for removing PID data packets of service channels not selected (channel-selected) from the transport streams TS1, TS2, and TS3.

[0087] Fig. 14(a) illustrates a configuration example of the PID packets of the transport streams TS1, TS2, and TS3 supplied to the LTS adding units 141-1, 141-2, and 141-3. Fig. 14 (b) illustrates an example of PID packets (not unnecessary PID packets) remaining after filtering of the input in Fig. 14(a) by the PID filter units 142-1, 142-2, and 142-3.

[0088] Returning to Fig. 2, the filtered transport streams TS1, TS2, and TS3 are supplied to the multiplexing unit 143. The multiplexing unit 143 synthesizes respective PID packets of the transport streams TS1, TS2, and TS3 after removal of LTS to create the synthesized stream CTS.

[0089] In addition, the multiplexing unit 143 inserts and adds LTSID to the synchronous byte area within the TS header of each of the PID packets of the synthesized stream CTS thus created (see Figs. 5 (a) and 5 (b)). The multiplexing unit 143 also outputs LTSs (Local Time Stamps) corresponding to the PID packets in accordance with output timing of the respective PID packets of the synthesized stream CTS.

[0090] The synthesized stream CTS created by the multiplexing unit 143 is supplied to the LCC adding unit 144. The LTSs output from the multiplexing unit 143 are supplied to the LCC adding unit 144. The LCC adding unit 144 inserts and adds count information, as the LCC, which indicates a count value sequentially counted while skipping a particular count value, to a count information adding area provided in the synchronous byte area within the TS header of each of the PID packets for each of the PID packets of the synthesized stream CTS.

[0091] As discussed above, this LCC is count information for handling an order change of PID packets, i.e., packet order switching within the CAM module 200, and is created and used at the time of addition of LCC. The respective PID packets of the synthesized stream CTS to which LCCs are added in this manner are sequentially transmitted from the LCC adding unit 144 to the CAM module 200 via a common interface.

[0092] The LCC adding unit 144 also adds LCCs added to the respective PID packets of the synthesized stream CTS as described above to LTSs output from the multiplexing unit 143 in correspondence with the respective PID packets. The LTSs to which the LCCs are added in this manner are sequentially supplied to the FIFO unit 147.

[0093] Fig. 15(a) illustrates an example of the PID packets of the respective transport streams TS1, TS2, and TS3 supplied from the PID filter units 142-1, 142-2, and 142-3 to the multiplexing unit 143. Each of the PID packets contains LTS added thereto.

[0094] Fig. 15 (b) illustrates an example of arrangement of the respective PID packets of the synthesized streams CTS sequentially output from the LCC adding unit 144 to the CAM module 200. Fig. 15 (c) illustrates an example of arrangement of LTSs containing LCCs added thereto and sequentially output from the LCC adding unit 144 to the FIFO unit 147.

[0095] LTSID and LCC are added to each of the PID packets of the synthesized stream CTS. LTSID (ID1) is LTSID indicating that the original transport stream is the transport stream TS1. LTSID (ID2) is LTSID indicating that the original transport stream is the transport stream TS2. LTSID (ID3) is LTSID indicating that the original transport stream is the transport stream TS3.

[0096] The respective PID packets of the synthesized streams sequentially received from the CAM module 200 via the common interface are transmitted to the demultiplexing unit 145 via the LCC extracting unit 146. The LCC extracting unit 146 extracts LCC inserted into the synchronous byte area within the header for each of the PID packets of the received synthesized stream, and transmits the extracted LCCs to the FIFO unit 147.

[0097] The FIFO unit 147 retains LTSs sequentially output from the LCC adding unit 144 and containing LCCs

added to the LTSs for a certain period. In this case, the LTSs are retained at least for a time corresponding to the maximum delay time from reception to transmission of the synthesized stream CTS by the CAM module 200.

[0098] The FIFO unit 147 subsequently outputs LTSs corresponding to the respective PID packets for each of the PID packets of the synthesized stream CTS received from the CAM module 200. More specifically, the FIFO unit 147 in this case refers to LCC extracted by the LCC extracting unit 146 and inserted and added to the synchronous byte area of the header of each of the PID packets, and selectively outputs LTS to which LCC having the same value is added (see FIGS. 11 through 13).

[0099] The respective LTSs sequentially output from the FIFO unit 147 are transmitted to the demultiplexing unit 145. The demultiplexing unit 145 processes the respective PID packets of the received synthesized stream based on the added LTSIDs, and LTSs output from the FIFO unit 147 and corresponding to the respective PID packets.

[0100] More specifically, the demultiplexing unit 145 distributes the respective PID packets of the received synthesized stream to respective streams in accordance with LTSIDs. The demultiplexing unit 145 also adjusts output timing such that the respective PID packets can be located at time positions in accordance with LTSs corresponding to the respective PID packets, and obtains the reconstituted transport streams TS1, TS2, and TS3.

[0101] Fig. 16 (a) illustrates an example of the respective PID packets of the synthesized streams CTS sequentially input to the demultiplexing unit 145 from the CAM module 200 via the common interface (Fig. 16(a) corresponds to Fig. 15(b), but is different therefrom in the parts to which marks "*" are added).

[0102] Fig. 16(b) illustrates an example of the LTSs sequentially transmitted from the FIFO unit 147 to the demultiplexing unit 145 at the input timing of the respective PID packets of the synthesized stream CTS (Fig. 16(b) corresponds to Fig. 15(c), but the order is changed in accordance with order switching of the PID packets). In practical situations, LCCs are not contained herein, but are shown in the figure for comparison with the LCCs added to the PID packets.

[0103] FIG. 16 (c) illustrates an example of the respective PID packets of the transport streams TS1, TS2, and TS3 reconstituted and output from the demultiplexing unit 145.

[0104] A flowchart shown in Fig. 17 shows an example of processing procedures executed by the common interface controller 104A for synthesizing the respective PID packets of the transport streams TS1, TS2, and TS3 to create the synthesized stream CTS, and transmitting the created synthesized stream CTS to the CAM module 200.

[0105] The controller 104A starts processing in step ST1, and then shifts to a process in step ST2. In this step ST2, the controller 104A inputs the transport streams TS1, TS2, and TS3. The controller 104A adds LTSs to the PID packets of each of the transport streams in step ST3.

[0106] Then, the controller 104A removes PID data packets of service channels not selected (channel-selected) in the respective transport streams in step ST4. The controller 104A subsequently arranges the remaining PID packets (PID packets after LTS removal) in the order from the earliest PID packet on a time basis to create a synthesized stream in step ST5. At this time, the controller 104A adds LTSID and LCC to each of the PID packets. The LCC in this case is count information sequentially counted while skipping a particular count value.

[0107] Then, the controller 104A sequentially transmits the respective PID packets of the synthesized stream CTS to the CAM module 200 at a clock rate necessary for successive transmission in step ST6. In this step ST6, the controller 104A also inputs LTSs to which LCCs are added to the FIFO unit 147 in accordance with transmission of the respective PID packets, and allows the FIFO unit 147 to retain the LTSs for a certain period. After the process in step ST6, the controller 104A ends the processing in step ST7.

[0108] A flowchart in Fig. 18 shows an example of processing procedures executed by the common interface controller 104A for receiving the synthesized stream CTS from the CAM module 200, and reconstituting the transport streams TS1, TS2, and TS3.

[0109] The controller 104A starts processing in step ST11, and then shifts to a process in step ST12. In this step ST12, the controller 104A sequentially receives the respective PID packets of the synthesized stream CTS from the CAM module 200. The controller 104A also obtains LTSs corresponding to the respective PID packets from the FIFO unit 147.

[0110] Then, the controller 104A executes Sync replacement of the respective PID packets of the synthesized stream CTS, and also distributes the respective PID packets to corresponding streams based on LTSIDs added to the respective PID packets in step ST13. The controller 104A subsequently outputs the respective PID packets for each stream while adjusting output timing based on LTSs selectively output from the FIFO unit 147 with reference to LCCs added to the respective PID packets in step ST14. By this method, the controller 104A outputs the reconstituted transport streams TS1, TS2, and TS3. After the process in step ST14, the controller 104A ends processing in step ST15.

[0111] The controller 104A executes the foregoing transmitting process shown in the flowchart in Fig. 17, and the foregoing receiving process shown in the flowchart in Fig. 18 in parallel, and repeats the respective processes cyclically.

[0112] As described above, the controller 104A illustrated in Fig. 2 executes addition of LCC corresponding to count information sequentially counted while skipping a particular count value, for each of the PID packets of the synthesized stream CTS transmitted to the CAM

module 200. In this case, LCC is added to both a part of the synchronous byte area as a count information adding area provided for each of the PID packets, and LTS output in accordance with the corresponding PID packet.

[0113] By adding LCC to each of the PID packets of the synthesized stream CTS transmitted to the CAM module 200, the controller 104A can notify the CAM module 200 that the controller 104A has a function for handling packet order switching based on count information, and that packet order switching is thus allowed.

[0114] In addition, the controller 104A can obtain LTS corresponding to each of the PID packets from the FIFO unit 147 based on LCC added to the synchronous byte area within the header of the corresponding PID packet of the received synthesized stream CTS. Accordingly, the respective PID packets can be appropriately processed based on the corresponding LTSs even in the case of receiving from the CAM module 200 the synthesized stream CTS containing PID packets arranged in a different order from the order at the time of transmission.

"Example of Not Having Function for Handling Packet Order Switching"

[0115] Discussed hereinafter is the common interface controller 104B which does not have a function for handling packet order switching based on count information, and does not allow packet order switching at the CAM module 200. Fig. 19 illustrates a configuration example of the controller 104B. Parts in Fig. 19 corresponding to the parts in Fig. 2 are given similar reference numbers, and the detailed explanation of these parts are not repeated when appropriate.

[0116] The controller 104B includes the LTS (Local Time Stamp) adding units 141-1, 141-2, and 141-3, and the PID filter (PID filter) units 142-1, 142-2, and 142-3. The controller 104B further includes the multiplexing (MUX) unit 143, a LCC (Local Continuity Counter) adding unit 144B, the demultiplexing (DEMUX) unit 145, and a FIFO (First In First Out) unit 147B.

[0117] The LCC adding unit 144B inserts and adds a particular count value to a count information addition area as LCC (Local continuity counter) for each of the PID packets of the synthesized stream CTS output from the multiplexing unit 143. As discussed in the description of the controller 104A (see Fig. 2), the count information adding area is constituted by a part of the synchronous byte area within the TS header of each of the PID packets. The particular count value is a value containing "1" for all the bit values.

[0118] Fig. 7(c) illustrates an example in which each bit of LCC is set to 1 in a state of high-order 4 bits of the synchronous byte area allocated to LTSID, and low-order 4 bits allocated to LCC. In this case, the low-order 4 bits of a synchronous word (0×47) are "0111" as illustrated in Fig. 7(b), wherefore the LCC adding unit 144B rewrites the third bit of the synchronous byte area from "0" to "1", and maintains the bits from the second to the zero at "1" without change.

[0119] Fig. 8(c) illustrates an example in which each bit of LCC is set to 1 in a state of high-order 5 bits of the synchronous byte area allocated to LTSID, and low-order 3 bits allocated to LCC. In this case, the low-order 3 bits of a synchronous word (0×47) are "111" as illustrated in Fig. 8(b), wherefore the LCC adding unit 144B maintains the bits from the second to the zero at "1" without change.

[0120] Fig. 9(c) illustrates an example in which each bit of LCC is set to 1 in a state of the seventh bit, fifth bit, fourth bit, and third bit of the synchronous byte area allocated to LTSID, and sixth bit, second bit, first bit, and zero bit allocated to LCC. In this case, each of the sixth bit, second bit, first bit, and zero bit of a synchronous word (0×47) is "1" as illustrated in Fig. 9(b), wherefore the LCC adding unit 144B maintains the sixth bit, second bit, first bit, and zeroth bit second bit at "1" without change.

[0121] The LCC adding unit 144B sequentially outputs the respective PID packets of the synthesized stream CTS containing LCCs added thereto to the CAM module 200. Each of the LCCs is information for notifying the CAM module 200 that the controller 104B does not have the function for handling packet order switching based on count information. Unlike the LCC adding unit 144 of the foregoing controller 104A (see Fig. 2), the LCC adding unit 144B does not add LCC to LTS output in accordance with each of the PID packets from the multiplexing unit 143. The LCC adding unit 144B sequentially transmits LTS corresponding to each of the PID packets and not containing LCC to the FIFO unit 147B in accordance with sequential transmission of the respective PID packets of the synthesized stream CTS to the CAM module 200.

[0122] The FIFO unit 147B retains LTSs sequentially output from the LCC adding unit 144B for a certain period, and outputs the LTSs after retention. The certain period herein is set to time corresponding to the delay time from reception to transmission of the synthesized stream CTS by the CAM module 200. The microprocessor 101 communicates with the CAM module 200 to obtain information on the delay time at the CAM module 200, and controls the retention time at the FIFO unit 147B based on this information. By this method, the FIFO unit 147B outputs LTSs corresponding to the PID packets for each of the PID packets of the synthesized stream CTS received from the CAM module 200.

[0123] The CAM module 200 recognizes that the controller 104B does not have the function for handling packet order switching based on count information from the fact that the LCC inserted and added to the synchronous byte area within the header of each of the PID packets of the synthesized stream CTS has a particular count value. In this case, the CAM module 200 operates such that packet order switching does not occur. Accordingly, the respective PID packets of the synthesized stream input to the CAM module 200 are sequentially output from the CAM module 200 with a certain delay time and in the packet order kept unchanged.

[0124] The demultiplexing unit 145 receives the synthesized stream CTS from the CAM module 200. The demultiplexing unit 145 subsequently processes each of the PID packets of the received synthesized stream based on LTSs corresponding to the respective PID packets output from the FIFO unit 147B. More specifically, the demultiplexing unit 145 distributes the respective PID packets of the received synthesized stream to respective streams based on LTSIDs inserted and added to the synchronous byte areas within the headers of the respective PID packets.

[0125] The demultiplexing unit 145 subsequently locates the respective PID packets at time positions corresponding to LTSs in the respective streams to which the PID packets are distributed, so as to reconstitute the transport streams TS1, TS2, and TS3. Other parts of the controller 104B illustrated in Fig. 19, which are not detailed herein, have configurations similar to the corresponding parts of the controller 104A illustrated in Fig. 2.

[0126] The operation of the common interface controller 104B illustrated in Fig. 19 is now described. The transport streams TS1, TS2, and TS3 supplied from the demodulators 103-1, 103-2, and 103-3 (see Fig. 1) are supplied to the LTS adding units 141-1, 141-2, and 141-3, respectively. The LTS adding units 141-1, 141-2, and 141-3 add LTSs (Local Time Stamps) corresponding to input time to the respective PID packets of the input transport streams TS1, TS2, and TS3 (TSP: transport stream packets), respectively.

[0127] The transport streams TS1, TS2, and TS3 containing the respective PID packets to each of which LTS is added are supplied to the PID filter units 142-1, 142-2, and 142-3, respectively. The PID filter units 142-1, 142-2, and 142-3 execute filtering for removing PID data packets of service channels not selected (channel-selected) from the transport streams TS1, TS2, and TS3.

[0128] Fig. 14(a) illustrates a configuration example of the PID packets of the transport streams TS1, TS2, and TS3 supplied to the LTS adding units 141-1, 141-2, and 141-3. Fig. 14 (b) illustrates an example of PID packets (not unnecessary PID packets) remaining after filtering of the input in Fig. 14(a) by the PID filter units 142-1, 142-2, and 142-3.

[0129] Returning to Fig. 19, the transport streams TS1, TS2, and TS3 after filtering are supplied to the multiplexing unit 143. The multiplexing unit 143 synthesizes respective PID packets of the transport streams TS1, TS2, and TS3 after removal of LTS to create the synthesized stream CTS.

[0130] In addition, the multiplexing unit 143 inserts and adds LTSID to the synchronous byte area within the TS header of each of the PID packets of the synthesized stream CTS thus created (see Figs. 5 (a) and 5 (b)). The multiplexing unit 143 also outputs LTSs (Local Time Stamps) corresponding to the PID packets in accordance with output timing of the respective PID packets of the synthesized stream CTS.

[0131] The synthesized stream CTS created by the multiplexing unit 143 is supplied to the LCC adding unit 144B. The LTSs output from the multiplexing unit 143 are supplied to the LCC adding unit 144B.

[0132] The LCC adding unit 144B inserts and adds, as the LCCs, a particular count value (such as value having "1" for all bits) to a count information adding area provided in the synchronous byte area within the TS header of each of the PID packets for each of the PID packets of the synthesized stream CTS. The respective PID packets of the synthesized stream CTS to which LCCs are added in this manner are sequentially transmitted from the LCC adding unit 144B to the CAM module 200 via a common interface.

[0133] The LTSs corresponding to the respective PID packets are sequentially transmitted from the LCC adding unit 144B to the FIFO unit 147B in accordance with sequential transmission of the respective PID packets of the synthesized stream CTS to the CAM module 200. Accordingly, LCCs are not added to the LTSs transmitted to the FIFO unit 147B.

[0134] Fig. 20 (a) illustrates an example of the respective PID packets of the respective transport streams TS1, TS2, and TS3 supplied from the PID filter units 142-1, 142-2, and 142-3 to the multiplexing unit 143. Each of the PID packets contains LTS added thereto.

[0135] Fig. 20 (b) illustrates an example of arrangement of the respective PID packets of the synthesized stream CTS sequentially output from the LCC adding unit 144B to the CAM module 200. Fig. 20 (c) illustrates an example of arrangement of LTSs sequentially output from the LCC adding unit 144B to the FIFO unit 147B.

[0136] LTSID and LCC (particular count value) are added to each of the PID packets of the synthesized stream CTS. LTSID (ID1) is LTSID indicating that the original transport stream is the transport stream TS1. LTSID (ID2) is LTSID indicating that the original transport stream is the transport stream TS2. LTSID (ID3) is LTSID indicating that the original transport stream is the transport stream TS3.

[0137] The respective PID packets of the synthesized stream sequentially received from the CAM module 200 via the common interface are transmitted to the demultiplexing unit 145. As discussed above, the CAM module 200 recognizes that the controller 104B does not have the function for handling packet order switching based on count information from the fact that each of the LCCs inserted and added to the respective PID packets of the synthesized stream CTS is a particular count value.

[0138] The CAM module 200 is operated such that packet order switching does not occur. Accordingly, the packet order of the respective PID packets of the synthesized stream CTS output from the CAM module 200 does not change from the packet order of the respective PID packets of the synthesized stream CTS input to the CAM module 200.

[0139] The LTSs sequentially output from the LCC adding unit 144B are transmitted from the FIFO unit 147B to the demultiplexing unit 145 with delay corresponding

to the time from reception to transmission of the synthesized stream CTS by the CAM module 200. By this method, the demultiplexing unit 145 receives supply of the respective LTSs corresponding to the PID packets in accordance with supply of the respective PID packets of the synthesized stream CTS received from the CAM module 200.

[0140] The demultiplexing unit 145 processes the respective PID packets of the received synthesized stream based on the added LTSIDs, and further on the LTSs corresponding to the PID packets and output from the FIFO unit 147B. More specifically, the demultiplexing unit 145 distributes the respective PID packets of the received synthesized stream to respective streams in accordance with LTSIDs. The demultiplexing unit 145 also adjusts output timing such that the respective PID packets can be located at time positions in accordance with LTSs corresponding to the respective PID packets, and obtains the reconstituted transport streams TS1, TS2, and TS3.

[0141] Fig. 21(a) illustrates an example of the respective PID packets of the synthesized stream CTS sequentially input from the CAM module 200 to the demultiplexing unit 145 via the common interface. Fig. 21(a) in this example corresponds to Fig. 20(b), but the packet order is maintained at the CAM module 200, wherefore packet order switching does not occur in this example.

[0142] Fig. 21(b) illustrates an example of the respective LTSs sequentially transmitted from the FIFO unit 147B to the demultiplexing unit 145 at the timing of input of the respective PID packets of the synthesized stream CTS (corresponds to Fig. 20(c)). Fig. 21(c) illustrates an example of the respective PID packets of the transport streams TS1, TS2, and TS3 reconstituted and output from the demultiplexing unit 145.

[0143] A flowchart in Fig. 22 shows an example of processing procedures executed by the common interface controller 104B for synthesizing the respective PID packets of the transport streams TS1, TS2, and TS3 to create the synthesized stream CTS, and transmitting the synthesized stream CTS to the CAM module 200.

[0144] The controller 104B starts processing in step ST21, and then shifts to a process in step ST22. In this step ST22, the controller 104B inputs the transport streams TS1, TS2, and TS3. The controller 104B adds LTSs to the PID packets of each of the transport streams in step ST23.

[0145] Then, the controller 104B removes PID data packets of service channels not selected (channel-selected) in the respective transport streams in step ST24. The controller 104B subsequently arranges the remaining PID packets (PID packets after LTS removal) in the order from the earliest PID packet on a time basis to create a synthesized stream in step ST25. At this time, the controller 104B adds LTSID and LCC to each of the PID packets. The LCC in this case is a particular count value (fixed value).

[0146] Then, the controller 104B sequentially transmits the respective PID packets of the synthesized stream CTS to the CAM module 200 at a clock rate necessary for successive transmission in step ST26. In this step ST26, the controller 104B also inputs LTSs corresponding to the PID packets to the FIFO unit 147B in accordance with transmission of the respective PID packets, and allows the FIFO unit 147B to retain the LTSs for a certain period. After the process in step ST26, the controller 104B ends the processing in step ST7.

[0147] A flowchart in Fig. 23 shows an example of processing procedures executed by the common interface controller 104B for receiving the synthesized stream CTS from the CAM module 200, and reconstituting the transport streams TS1, TS2, and TS3.

[0148] The controller 104B starts processing in step ST31, and then shifts to a process in step ST32. In this step ST32, the controller 104B sequentially receives the respective PID packets of the synthesized stream CTS from the CAM module 200. The controller 104B also obtains LTSs corresponding to the respective PID packets from the FIFO unit 147B.

[0149] Then, the controller 104B executes Sync replacement of the respective PID packets of the synthesized stream CTS, and also distributes the respective PID packets to corresponding streams based on LTSIDs added to the respective PID packets in step ST33. The controller 104B subsequently outputs the respective PID packets for each stream while adjusting output timing based on corresponding LTSs output from the FIFO unit 147B in step ST34. By this method, the controller 104B outputs the reconstituted transport streams TS1, TS2, and TS3. After the process in step ST34, the controller 104B ends processing in step ST35.

[0150] The controller 104B executes the foregoing transmitting process shown in the flowchart in Fig. 22, and the foregoing receiving process shown in the flowchart in Fig. 23 in parallel, and repeats the respective processes cyclically.

[0151] As described above, the controller 104B illustrated in Fig. 19 adds the particular count value to the count information adding area as LCC for each of the PID packets of the synthesized stream CTS transmitted to the CAM module 200. By this method, the controller 104B can notify the CAM module 200 that the controller 104B does not have the function for handling packet order switching based on count information, and that packet order switching is thus not allowed.

[0152] By notifying the CAM module 200 that packet order switching is not allowed as discussed above, the controller 104B receives from the CAM module 200 the synthesized stream CTS having the same packet order of PID packets as the packet order at the time of transmission. In addition, the FIFO unit 147B outputs the LTSs with delay of time corresponding to the time from reception to transmission of the synthesized stream CTS by the CAM module 200. Accordingly, the respective PID packets of the synthesized stream CTS can be appropriately processed based on the corresponding LTSs.

[Configuration Example of CAM Module]

[0153] The detailed configuration of the CAM module 200 is now described. Fig. 24 illustrates a configuration example of the CAM module 200. The CAM module 200 includes the microprocessor 201 and the descrambler 202 as discussed above (see Fig. 1).

[0154] The microprocessor 201 executes necessary communication with the microprocessor 101 of the host device 100, and controls operation of the descrambler 202. The descrambler 202 receives the synthesized stream CTS transmitted from the common interface controller 104 (104A, 104B) of the host device 100 via a common interface, and descrambles the synthesized stream CTS. The descrambler 202 subsequently transmits the descrambled synthesized stream CTS to the controller 104 of the host device 100.

[0155] The descrambler 202 includes a TS separating unit 211, N CA decryption units 212-1 through 212-N, N buffer units 213-1 through 213-N, and a TS synthesizing unit 214. The TS separating unit 211 receives the synthesized stream CTS transmitted from the controller 104 of the host device 100. The TS separating unit 211 subsequently distributes the respective PID packets of the synthesized stream CTS to respective streams TS1 through TSN based on LTSID inserted and added to the synchronous byte area within the header of each of the PID packets (see Figs. 5(a) and 5(b)).

[0156] The TS separating unit 211 also extracts LCC inserted and added to a count information area, i.e., a part of the synchronous byte area within the header (see Figs. 5(a) and 5(b)) in each of the PID packets of the synthesized stream CTS, and transmits the extracted LCC to the microprocessor 201. As discussed above, this LCC is count information sequentially counted while skipping a particular count value when the synthesized stream CTS is transmitted from the controller 104A having the function for handling packet order switching based on count information (see Fig. 2). In this case, the microprocessor 201 recognizes that the controller 104 to transmit the synthesized stream CTS is the controller 104A having the function for handling packet order switching based on count information, and that packet order switching is thus allowed.

[0157] On the other hand, when the synthesized stream CTS is transmitted from the controller 104B which does not have the function for handling packet order switching based on count information (see Fig. 19), the LCC has a particular count value. In this case, the microprocessor 201 recognizes that the controller 104 to transmit the synthesized stream CTS is the controller 104B not having the function for handling packet order switching based on count information, and that packet order switching is thus not allowed.

[0158] The microprocessor 201 controls operation of the descrambler 202, particularly operation of buffering and synthesis of the respective PID packets based on recognition of whether or not packet order switching by LCC as above is allowed. This control operation will be detailed later.

[0159] Each of the CA decryption units 212-1 through 212-N decrypts the PID packets of the corresponding streams. The CA decryption units used herein are not all the CA decryption units 212-1 through 212-N, but only a part of the CA description units corresponding to the number of streams contained in the synthesized stream CTS. The buffer units 213-1 through 213-N buffer the PID packets decrypted by the CA decryption units 212-1 through 212-N.

[0160] The TS synthesizing unit 214 synthesizes the PID packets of the respective streams buffered by the buffer units 213-1 through 213-N to create the synthesized stream CTS, and transmits the synthesized stream CTS to the controller 104 of the host device 100.

[0161] The operation control of buffering and synthesis of the respective PID packets executed by the microprocessor 201 is now described. When recognizing that the packet order switching is allowed based on LCCs as discussed above, the microprocessor 201 controls buffering and synthesis of the respective PID packets such that the PID packets of the respective decrypted streams can be synthesized in the decrypting order.

[0162] Figs. 25(a) to 25(d) are timing charts when the synthesized stream CTS received by the TS separating unit 211 is transmitted from the controller 104A having the function for handling packet order switching based on count information.

[0163] Fig. 25(a) shows the synthesized stream CTS received by the TS separating unit 211. In this figure, a0, a1, a2, and others represent PID packets of the transport stream TS1. Moreover, b0, b1, b2, and others represent PID packets of the transport stream TS2. Furthermore, c0, c1, c2, and others represent PID packets of the transport stream TS3.

[0164] Fig. 25(b) shows PID packets of the streams TS1, TS2, and TS3 separated by the TS separating unit 211. Fig. 25 (c) shows the PID packets of the streams TS1, TS2, and TS3 decrypted by the CA decryption units 212-1, 212-2, and 212-3.

[0165] Fig. 25(d) shows the synthesized stream CTS created by synthesizing the PID packets of the respective streams by the TS synthesizing unit 214, and transmitted to the controller 104A. The order of the respective PID packets of this synthesized stream CTS is different from the order of the PID packets of the received synthesized stream CTS, indicating that packet order switching has occurred. However, no problem arises in the controller 104A where packet order switching is allowed.

[0166] On the other hand, when recognizing that packet order switching is not allowed based on LCCs as discussed above, the microprocessor 201 controls buffering and synthesis of the respective PID packets such that the PID packets of the respective decrypted streams are synthesized in the order of the respective packets PID at the time of reception of the synthesized stream CTS.

[0167] Figs. 26(a) to 26(d) are timing charts when the

synthesized stream CTS received by the TS separating unit 211 is transmitted from the controller 104B not having the function for handling packet order switching based on count information.

[0168] Fig. 26(a) shows the synthesized stream CTS received by the TS separating unit 211. In this figure, a0, a1, a2, and others represent PID packets of the transport stream TS1. Moreover, b0, b1, b2, and others represent PID packets of the transport stream TS2. Furthermore, c0, c1, c2, and others represent PID packets of the transport stream TS3.

[0169] Fig. 26(b) shows PID packets of the streams TS1, TS2, and TS3 separated by the TS separating unit 211. Fig. 25 (c) shows the PID packets of the streams TS1, TS2, and TS3 decrypted by the CA decryption units 212-1, 212-2, and 212-3. Figs. 26 (a) through 26 (c) are identical to Figs. 25 (a) through 25(c).

[0170] Fig. 26 (d) shows the synthesized stream CTS created by synthesizing the PID packets of the respective streams by the TS synthesizing unit 214, and transmitted to the controller 104B. The order of the respective PID packets of this synthesized stream CTS is identical to the order of the PID packets of the received synthesized stream CTS. In this case, the buffer capacity required for queuing increases so as to maintain the order of the PID packets, wherefore delay time at the CAM module 200 becomes longer.

[0171] The operation of the CAM module 200 illustrated in Fig. 24 is now described. The TS separating unit 211 receives the synthesized stream CTS transmitted from the common interface controller 104 (104A, 104B) of the host device 100 via a common interface. The TS separating unit 211 subsequently distributes the respective PID packets of the synthesized stream CTS to the respective streams TS1 through TSN based on LTSID inserted and added to the synchronous byte area within the header of each of the PID packets of the synthesized stream CTS (see Figs. 5(a) and 5(b)).

[0172] The TS separating unit 211 extracts LCC inserted and added to the synchronous byte area within the header of each of the PID packets of the synthesized stream CTS, and transmits the LCC to the microprocessor 201. The microprocessor 201 recognizes whether or not packet order switching is allowed based on the extracted LCCs, and controls buffering and synthesis of the respective PID packets based on the recognition result.

[0173] The PID packets of the respective streams separated by the TS separating unit 211 are supplied to the CA decryption units 212-1 through 212-N. The CA decryption units 212-1 through 212-N decrypt the PID packets of the respective streams to which the PID packets are distributed. The decrypted PID packets of the respective streams are supplied to the buffer units 213-1 through 213-N to be temporarily accumulated therein.

[0174] The TS synthesizing unit 214 synthesizes the PID packets of the respective streams accumulated in the buffer units 213-1 through 213-N to create the synthesized stream CTS, and transmits the synthesized stream CTS to the controller 104 (104A, 104B) of the host device 100. In this case, the decrypted PID packets of the respective streams are synthesized in the order of decrypting (see Fig. 25(d)) when the controller 104 is the controller 104A which allows packet order switching (see Fig. 2). On the other hand, the decrypted PID packets of the respective streams are synthesized in the order of the respective PID packets of the received synthesized stream CTS (see Fig. 26(d)) when the controller 104 is the controller 104B which does not allows packet order switching (see Fig. 19).

[0175] A flowchart in Fig. 27 shows the outline of an example of processing procedures executed by the CAM module 200. The CAM module 200 initially starts processing in step ST41, and subsequently shifts to a process in step ST42. In this step ST42, the CAM module 200 receives the synthesized stream CTS.

[0176] Then, the CAM module 200 detects LCCs added to the respective PID packets of the received synthesized stream CTS in step ST43. The CAM module 200 also distributes the respective PID packets of the received synthesized stream CTS to respective streams based on LTSIDs added to the PID packets in step ST44. The CAM module 200 subsequently decrypts the PID packets of the respective streams in step ST45.

[0177] Thereafter, the CAM module 200 determines whether or not the LCCs detected in step ST43 are particular count values in step ST46. When the LCCs are particular count values, i. e. , when packet order switching is not allowed, the CAM module 200 executes buffering and queuing of the PID packets of the respective streams in step ST47, and then synthesizes the decrypted PID packets of the respective streams such that the order of the PID packets becomes identical to the order of the respective PID packets of the received synthesized stream CTS, so as to create the synthesized stream CTS in step ST48.

[0178] Subsequently, the CAM module 200 transmits the synthesized stream CTS obtained in step ST48 to the controller 104 of the host device 100 in step ST49. Thereafter, the CAM module 200 ends processing in step ST50.

[0179] On the other hand, when the LCCs are not particular count values in step ST46, i.e., when packet order switching is allowed, the CAM module 200 synthesizes the decrypted PID packets of the respective stream in the order of decrypting to create the synthesized stream CTS in step ST48. Then, the CAM module 200 transmits the synthesized stream CTS to the controller 104 of the host device 100 in step ST49. Thereafter, the CAM module 200 ends processing in step ST50.

[0180] As described above, the CAM module 200 illustrated in Fig. 24 controls buffering and synthesis of the respective PID packets at the descrambler 202 based on LCC added to the count information adding area provided in each of the PID packets of the received synthesized stream. Accordingly, the synthesized stream returns to the control 104 in the state corresponding to the controller

104 of the host device 100.

[0181] In the foregoing description of the CAM module 200, the operation for decrypting by the CA decryption units 212-1 through 212-N is not particularly touched upon. However, even when the decrypted PID packets of the respective streams are synthesized in the same order as the packet order of the received synthesized stream CTS based on recognition that packet order switching is not allowed, reduction of the delay amount is achievable by increasing the operation speed of the decrypting process.

[0182] Figs. 28(a) to 28(d) are timing charts for describing this method. Fig. 28(a) shows the synthesized stream CTS received by the TS separating unit 211. Fig. 28 (b) shows PID packets of the streams TS1, TS2, and TS3 separated by the TS separating unit 211. Figs. 28(a) and 28(b) are identical to Figs. 26(a) and 26(b).

[0183] Fig. 28(c) shows PID packets of the streams TS1, TS2, and TS3 decrypted by the CA decryption units 212-1, 212-2, and 212-3. By increasing the operation speed of the decrypting process, delays of the streams TS1, TS2, and TS3 produced by the decrypting process become 1/3 packet, 2/3 packet, and 1 packet, respectively. On the other hand, when the operation speed of the decrypting process is not raised, the delays of the streams TS1, TS2, and TS3 by the decrypting process become 1 packet, 2 packets, and 3 packets, respectively, as illustrated in Fig. 26(c).

[0184] Fig. 28(d) shows the synthesized stream CTS created by synthesizing the PID packets of the respective streams at the TS synthesizing unit 214, and transmitted to the controller 104B. The order of the respective PID packets of the synthesized stream CTS is identical to the order of the PID packets of the received synthesized stream CTS. In this case, the operation speed of the decrypting process is raised, wherefore the delay amount becomes smaller in comparison with the delay amount shown in Fig. 26(d).

<2. Modified Example>

[0185] According to the foregoing example, LTSID and LCC are inserted into a synchronous byte (Sync byte) area within a TS header of a PID packet (see Fig. 5(a)). However, the present technology is not limited to this example. For example, there is a method which inserts LTSID and LCC into a cyclic counter (continuity_counter) area within a TS header of a PID packet as illustrated in Fig. 29(a). In this case, processing information supplied to the FIFO unit 147 or 147B and retained for a certain period therein becomes LTS and CC to which LCC is added as illustrated in Fig. 29(b), or LTS and CC to which LCC is not added. The CC herein is an original value in the cyclic count area.

[0186] For the controller 104A which allows packet order switching at the CAM module 200, addition of LCC to LTS and CC in this manner is needed. However, for the controller 104B which does not allow packet order switching at the CAM module 200, addition of LCC to LTS and CC in this manner is not needed.

[0187] Fig. 30 illustrates an example of bit allocation of LTSID and LCC. When 2 bits are allocated to both LTSID and LCC, for example, identification of 4 transport streams is allowed. In this case, order switching of 2 packets or fewer can be handled. When 1 bit and 3 bits are allocated to LTSID and LCC, respectively, for example, identification of 2 transport streams is allowed. In this case, order switching of 6 packets or fewer can be handled.

[0188] According to the foregoing description, the host device 100 includes 3 tuners 102-1, 102-2, and 102-3 to handle the three transport streams TS1, TS2, and TS3. The present technology is applicable to situations handling two, four or more transport streams.

[0189] According to the foregoing description, the host device 100 transmits and receives synthesized streams to and from the CAM module 200 connected via a DVB-CI common interface, or a CI+ common interface. However, needless to say, the present technology is similarly applicable to wired or wireless transmission and reception of these synthesized streams between a host device and other external devices.

[0190] The present technology may have the following configurations.

(1) An electronic device including:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
a stream transmitting unit that transmits the created synthesized stream to an external device;
a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
a count information adding unit that brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device;
a stream receiving unit that receives the synthesized stream from the external device; and
a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information corresponding to the respective transport stream packets and sequentially output from the processing information retaining unit.

(2) The electronic device according (1) described above, wherein the count information adding area is

constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

(3) The electronic device according (2) described above, wherein the partial area is a predetermined-number bit area having 1 as a bit value of a synchronous signal.

(4) The electronic device according any of (1) through (3) described above, wherein

the processing information for processing the respective transport stream packets contains time information indicating time positions of the respective transport stream packets in original transport streams, and

the processing unit locates, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams.

(5) The electronic device according to (4) described above, further including:

a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device; and

a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream,

wherein the processing unit distributes the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

(6) The electronic device according to any of (1) through (5) described above, wherein

the stream transmitting unit transmits the synthesized stream to the external device via a DVB-CI common interface, or a CI+ common interface,

the stream receiving unit receives the synthesized stream from the external device via a DVB-CI common interface, or a CI+ common interface, and

the external device is a conditional access module that executes descrambling.

(7) A synthesized stream transmitting method including:

in transmitting a synthesized stream created by synthesizing transport stream packets of plural transport streams to an external device, bringing a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream.

(8) A program under which a computer provides the functions of:

synthesized stream creating means that synthesizes transport stream packets of plural transport streams to create a synthesized stream;

stream transmitting means that transmits the created synthesized stream to an external device;

processing information retaining means that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;

count information adding means that brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device;

stream receiving means that receives the synthesized stream from the external device; and

processing means that processes the respective transport stream packets of the received synthesized stream based on the processing information corresponding to the respective transport stream packets sequentially output from the processing information retaining means.

(9) An electronic device including:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;

a stream transmitting unit that transmits the created synthesized stream to an external device;

a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;

a count information adding unit that adds count information sequentially counted while skipping a particular count value to both a count information adding area provided in each of the transport stream packets, and processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted

to the external device;
a stream receiving unit that receives the synthesized stream from the external device; and
a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining unit and containing count information having the same value as the value of count information added to each of the transport stream packets.

(10) The electronic device according to (9) described above, wherein the count information adding area is constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.
(11) The electronic device according to (10) described above, wherein the partial area is a low-order 4-bit area or a low-order 3-bit area of the synchronous byte area.
(12) The electronic device according to any of (9) through (11) described above, wherein
the processing information for processing the respective transport stream packets of the received synthesized stream contains time information indicating time positions of the respective transport stream packets in original transport streams, and
the processing unit locates, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams.
(13) The electronic device according to (12) described above, further including:

a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device; and
a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream,
wherein the processing unit distributes the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

(14) The electronic device according to any of (9) through (13) described above, wherein
the stream transmitting unit transmits the synthesized stream to the external device via a DVB-CI common interface, or a CI+ common interface,
the stream receiving unit receives the synthesized stream from the external device via a DVB-CI common interface, or a CI+ common interface, and
the external device is a conditional access module that executes descrambling.
(15) A synthesized stream transmitting method including:

in transmitting a synthesized stream created by synthesizing transport stream packets of plural transport streams to an external device, adding predetermined-bit count information sequentially incremented except for a particular count value to a count information adding area provided in each of the transport stream packets for each of the transport stream packets of the synthesized stream.

(16) A program under which a computer provides the functions of:

synthesized stream creating means that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
stream transmitting means that transmits the created synthesized stream to an external device;
processing information retaining means that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
count information adding means that adds count information sequentially counted while skipping a particular count value to both a count information adding area provided in each of the transport stream packets, and processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device;
stream receiving means that receives the synthesized stream from the external device; and
processing means that processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining means and containing count information having the same value as the value of count information added to each of the transport stream packets.

(17) An electronic device including:

a stream receiving unit that receives a synthesized stream created by synthesizing transport stream packets of plural transport streams from an external device;
a processing unit that separates the respective transport stream packets of the received synthesized stream, decrypts the respective separated transport stream packets, and synthesizes the respective decrypted transport stream packets to create a synthesized stream;
a stream transmitting unit that transmits the created synthesized stream to the external device; and
a control unit that controls the processing unit based on count information added to a count information adding area provided in each of the transport stream packets of the received synthesized stream.

(18) The electronic device according to (17) described above, wherein the control unit controls such that the order of the respective transport stream packets of the created synthesized stream becomes the same order as the order of the respective transport stream packets of the received synthesized stream when the count information has a particular count value.
(19) The electronic device according to (18) described above, wherein the control unit raises the speed of decrypting operation when the count information has a particular count value.
(20) The electronic device according to any of (17) through (19) described above, wherein the count information adding area is constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

REFERENCE SIGNS LIST

[0191]

10	Reception system
100	Host device
101	Microprocessor
102-1 to 102-3	Tuner
103-1 to 103-3	Demodulator
104, 104A, 104B	Common interface controller
105-1 to 105-3	Demultiplexer
106-1 to 106-3	MPEG decoder
141-1 to 141-3	LTS adding unit
142-1 to 142-3	PID filter unit
143	Multiplexing (MUX) unit
144, 144B	LCC adding unit
145	Demultiplexing (DEMUX) unit
146	LCC extracting unit
147, 147B	FIFO unit
151-1 to 151-3	LTS separating unit
152	TS multiplexing unit
161	TS separating and Sync replacing unit
162-1 to 162-3	Output timing adjusting unit
171a to 171f	Flip-flop
172	Selection signal generating unit
173	Switch unit
200	CAM module
201	Microprocessor
202	Descrambler
211	TS separating unit
212-1 to 212-N	CA decryption unit
213-3 to 213-N	Buffer unit
214	TS synthesizing unit

Claims

1. An electronic device comprising:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
a stream transmitting unit that transmits the created synthesized stream to an external device;
a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
a count information adding unit that brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device;
a stream receiving unit that receives the synthesized stream from the external device; and
a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information corresponding to the respective transport stream packets and sequentially output from the processing information retaining unit.

2. The electronic device according to claim 1, wherein the count information adding area is constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

3. The electronic device according to claim 2, wherein the partial area is a predetermined-number bit area having 1 as a bit value of a synchronous signal.

4. The electronic device according to claim 1, wherein the processing information for processing the respective transport stream packets contains time in-

formation indicating time positions of the respective transport stream packets in original transport streams, and
the processing unit locates, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams.

5. The electronic device according to claim 4 further comprising:

a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device; and
a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream,
wherein the processing unit distributes the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

6. The electronic device according to claim 1, wherein the stream transmitting unit transmits the synthesized stream to the external device via a DVB-CI common interface, or a CI+ common interface,
the stream receiving unit receives the synthesized stream from the external device via a DVB-CI common interface, or a CI+ common interface, and
the external device is a conditional access module that executes descrambling.

7. A synthesized stream transmitting method comprising:

in transmitting a synthesized stream created by synthesizing transport stream packets of plural transport streams to an external device, bringing a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream.

8. A program under which a computer provides the functions of:

synthesized stream creating means that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
stream transmitting means that transmits the created synthesized stream to an external device;
processing information retaining means that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
count information adding means that brings a count information adding area provided in each of the transport stream packets into a state to which a particular count value is added for each of the transport stream packets of the synthesized stream transmitted to the external device;
stream receiving means that receives the synthesized stream from the external device; and
processing means that processes the respective transport stream packets of the received synthesized stream based on the processing information corresponding to the respective transport stream packets sequentially output from the processing information retaining means.

9. An electronic device comprising:

a synthesized stream creating unit that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
a stream transmitting unit that transmits the created synthesized stream to an external device;
a processing information retaining unit that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
a count information adding unit that adds count information sequentially counted while skipping a particular count value to both a count information adding area provided in each of the transport stream packets, and processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device;
a stream receiving unit that receives the synthesized stream from the external device; and
a processing unit that processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining unit and containing count information having the same value as the value of count information added to each of the transport

stream packets.

10. The electronic device according to claim 9, wherein the count information adding area is constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

11. The electronic device according to claim 10, wherein the partial area is a low-order 4-bit area or a low-order 3-bit area of the synchronous byte area.

12. The electronic device according to claim 9, wherein the processing information for processing the respective transport stream packets contains time information indicating time positions of the respective transport stream packets in original transport streams, and
the processing unit locates, in respective streams to which the respective transport stream packets of the received synthesized stream are distributed, the respective transport stream packets at time positions in accordance with the time information corresponding to the respective transport stream packets so as to reconstitute the plural transport streams.

13. The electronic device according to claim 12 further comprising:

a stream identification information adding unit that adds stream identification information for identifying original transport streams to the respective transport stream packets of the synthesized stream transmitted to the external device; and
a stream identification information obtaining unit that obtains the stream identification information from the respective transport stream packets of the received synthesized stream,
wherein the processing unit distributes the respective transport stream packets of the received synthesized stream to the respective streams in accordance with the stream identification information obtained from the respective transport stream packets.

14. The electronic device according to claim 9, wherein the stream transmitting unit transmits the synthesized stream to the external device via a DVB-CI common interface, or a CI+ common interface,
the stream receiving unit receives the synthesized stream from the external device via a DVB-CI common interface, or a CI+ common interface, and
the external device is a conditional access module that executes descrambling.

15. A synthesized stream transmitting method comprising:

in transmitting a synthesized stream created by synthesizing transport stream packets of plural transport streams to an external device, adding predetermined-bit count information sequentially incremented except for a particular count value to a count information adding area provided in each of the transport stream packets for each of the transport stream packets of the synthesized stream.

16. A program under which a computer provides the functions of:

synthesized stream creating means that synthesizes transport stream packets of plural transport streams to create a synthesized stream;
stream transmitting means that transmits the created synthesized stream to an external device;
processing information retaining means that retains processing information for a certain period, the processing information being output at transmission timing of the respective transport stream packets of the synthesized stream, and used for processing the respective transport stream packets;
count information adding means that adds count information sequentially counted while skipping a particular count value to both a count information adding area provided in each of the transport stream packets, and processing information output in correspondence with the transport stream packets for each of the transport stream packets of the synthesized stream transmitted to the external device;
stream receiving means that receives the synthesized stream from the external device; and
processing means that processes the respective transport stream packets of the received synthesized stream based on the processing information extracted from the processing information retaining means and containing count information having the same value as the value of count information added to each of the transport stream packets.

17. An electronic device comprising:

a stream receiving unit that receives a synthesized stream created by synthesizing transport stream packets of plural transport streams from an external device;
a processing unit that separates the respective transport stream packets of the received synthesized stream, decrypts the respective separated transport stream packets, and synthesizes the respective decrypted transport stream packets to create a synthesized stream;

a stream transmitting unit that transmits the created synthesized stream to the external device; and

a control unit that controls the processing unit based on count information added to a count information adding area provided in each of the transport stream packets of the received synthesized stream.

18. The electronic device according to claim 17, wherein the control unit controls such that the order of the respective transport stream packets of the created synthesized stream becomes the same order as the order of the respective transport stream packets of the received synthesized stream when the count information has a particular count value.

19. The electronic device according to claim 18, wherein the control unit raises the speed of decrypting operation when the count information has a particular count value.

20. The electronic device according to claim 17, wherein the count information adding area is constituted by a partial area of a synchronous byte area within a header of each of the transport stream packets.

FIG. 1

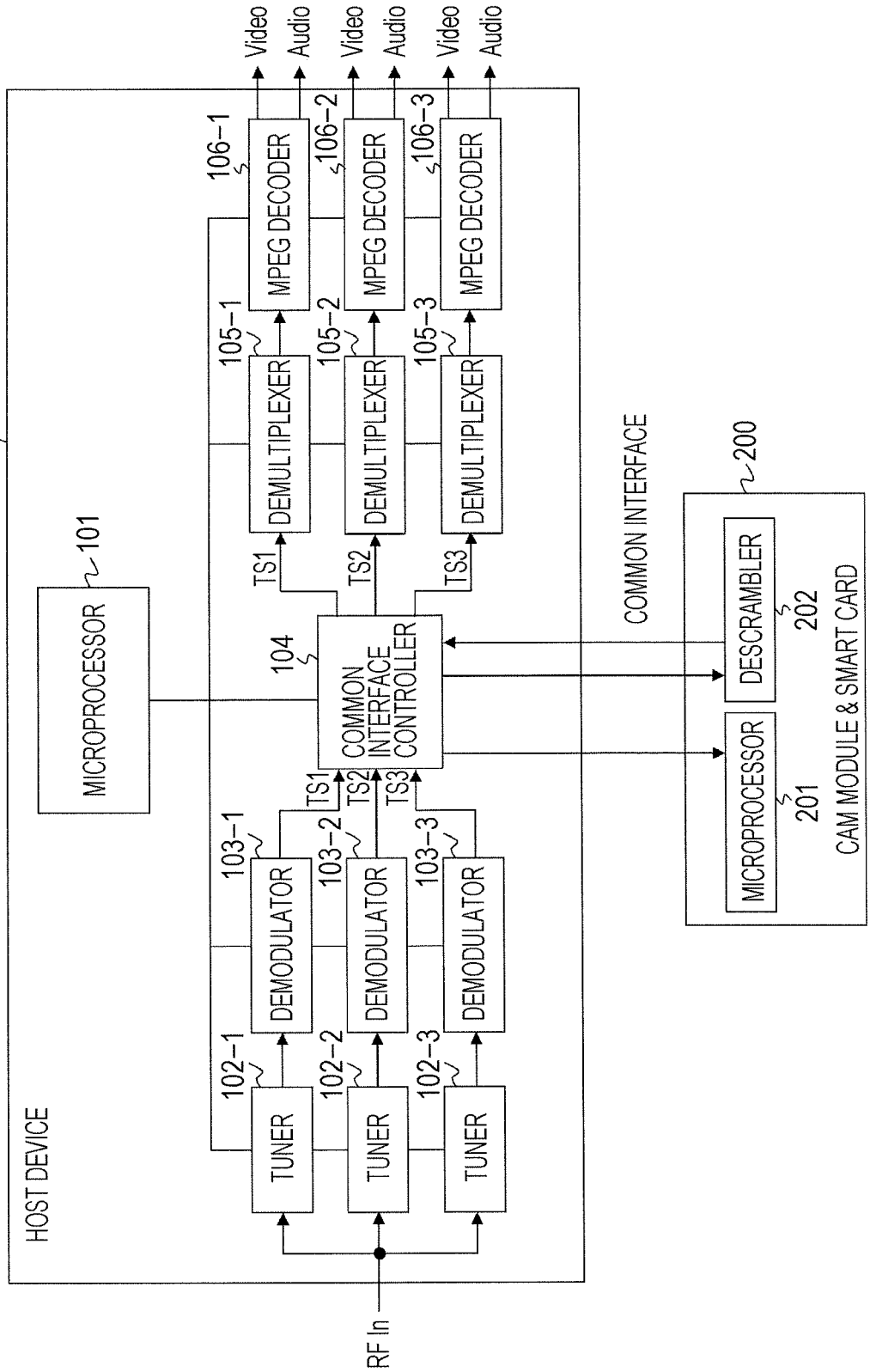

10
100
HOST DEVICE
MICROPROCESSOR
101
TUNER
102-1
102-2
102-3
DEMODULATOR
103-1
103-2
103-3
TS1
TS2
TS3
COMMON INTERFACE CONTROLLER
104
DEMULTIPLEXER
105-1
105-2
105-3
MPEG DECODER
106-1
106-2
106-3
Video
Audio
RF In
COMMON INTERFACE
200
MICROPROCESSOR
201
DESCRAMBLER
202
CAM MODULE & SMART CARD

FIG. 2

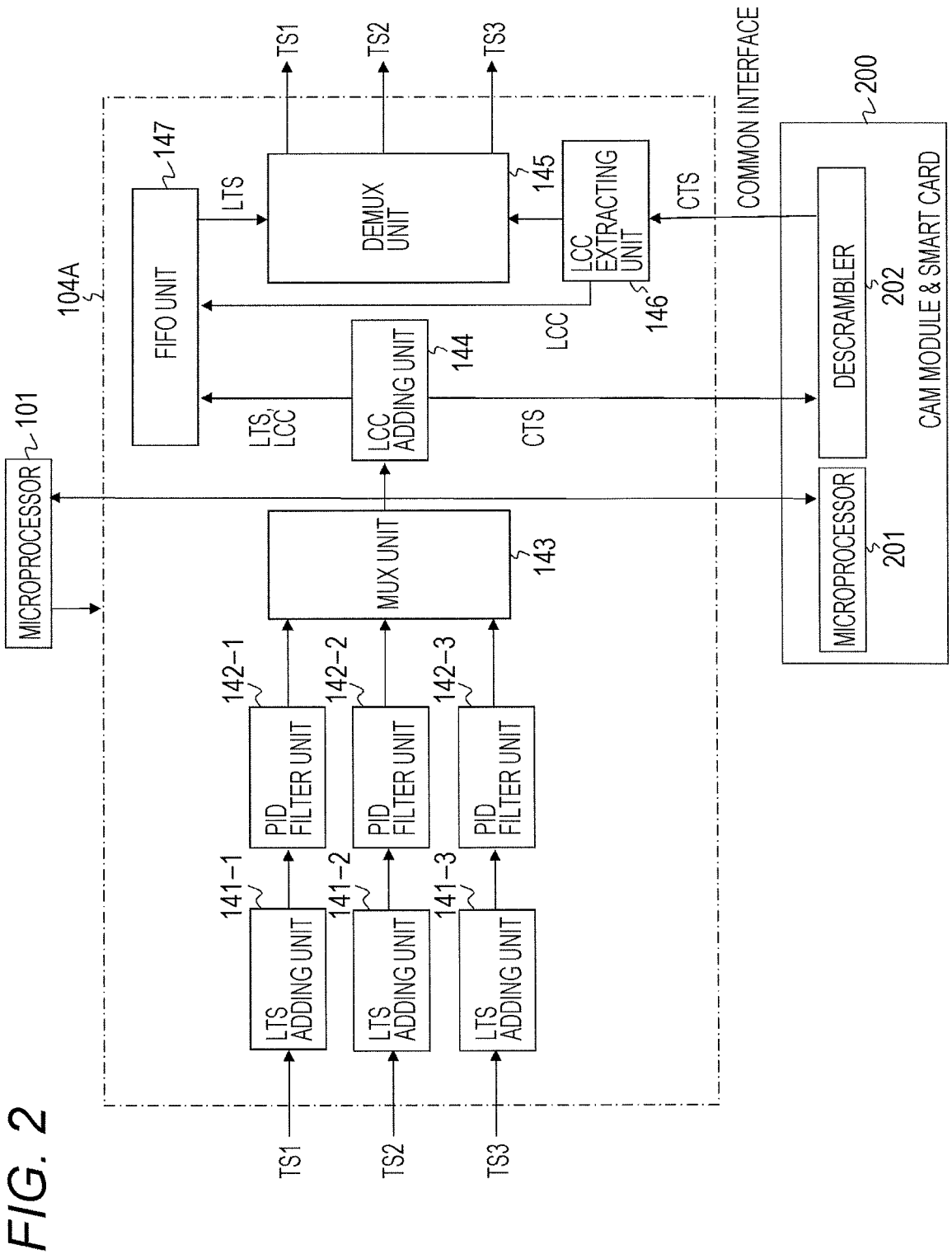

TS1
TS2
TS3
104A
147
FIFO UNIT
LTS
DEMUX UNIT
145
LCC EXTRACTING UNIT
CTS
COMMON INTERFACE
200
146
LCC
144
LCC ADDING UNIT
LTS, LCC
CTS
DESCRAMBLER
202
CAM MODULE & SMART CARD
MICROPROCESSOR
101
MUX UNIT
143
MICROPROCESSOR
201
142-1
142-2
142-3
PID FILTER UNIT
PID FILTER UNIT
PID FILTER UNIT
141-1
141-2
141-3
LTS ADDING UNIT
LTS ADDING UNIT
LTS ADDING UNIT
TS1
TS2
TS3

FIG. 3

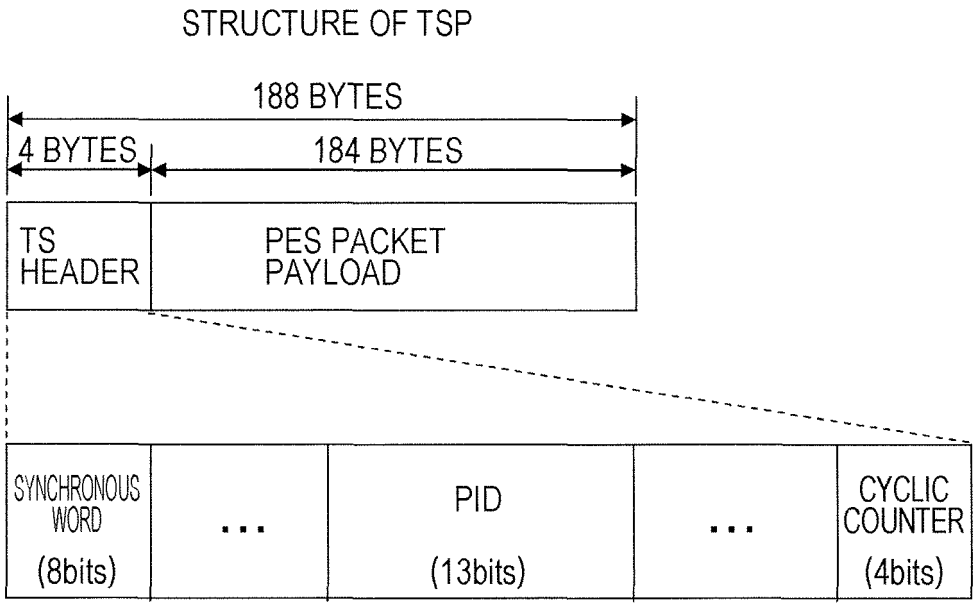

STRUCTURE OF TSP
188 BYTES
4 BYTES
184 BYTES
TS HEADER
PES PACKET PAYLOAD
SYNCHRONOUS WORD
(8bits)
...
PID
(13bits)
...
CYCLIC COUNTER
(4bits)

FIG. 4

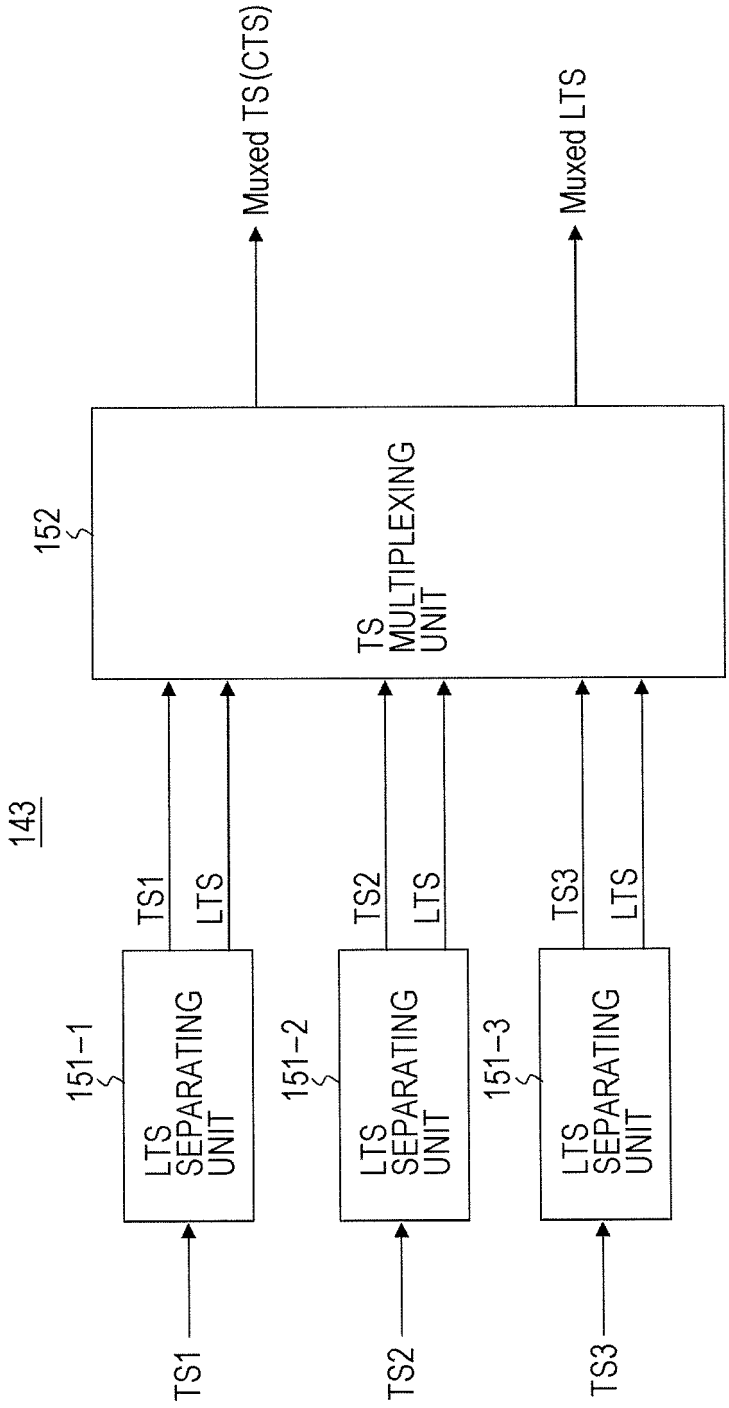

143
152
TS MULTIPLEXING UNIT
Muxed TS(CTS)
Muxed LTS
151-1
LTS SEPARATING UNIT
TS1
LTS
151-2
LTS SEPARATING UNIT
TS2
LTS
151-3
LTS SEPARATING UNIT
TS3
LTS
TS1
TS2
TS3

FIG. 5

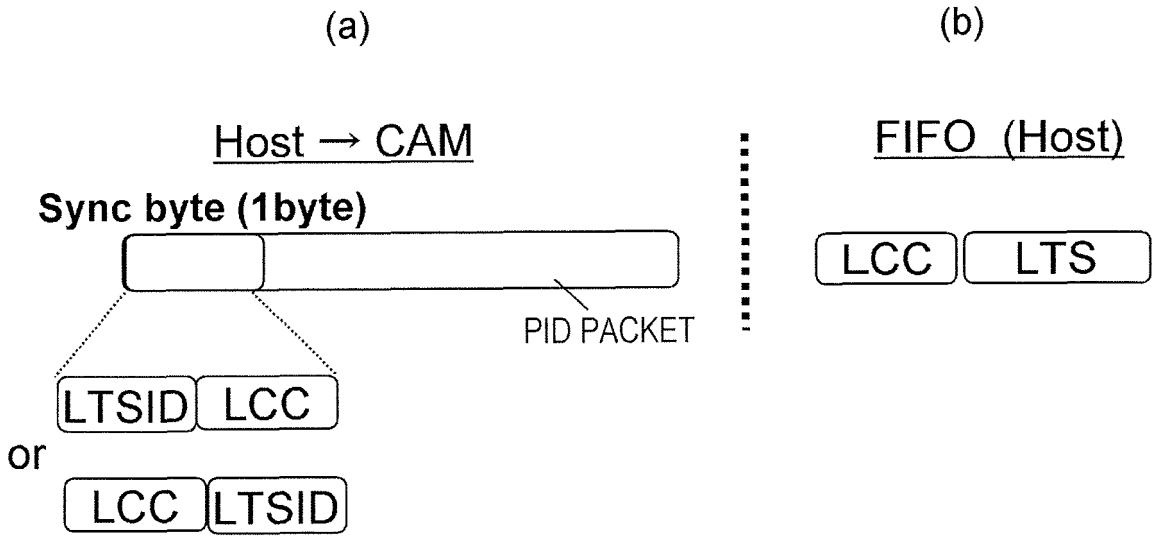

(a)
(b)
Host → CAM
FIFO (Host)
Sync byte (1byte)
PID PACKET
LCC
LTS
LTSID
LCC
or
LCC
LTSID

FIG. 6

	LTSID	LCC	Recover range of packet order change
1	6bit	2bit	64TS / recover less than **2** packets order change
2	5bit	3bit	32TS / recover less than **6** packets order change
3	4bit	4bit	16TS / recover less than **14** packets order change
4	3bit	5bit	8TS / recover less than **30** packets order change
5	2bit	6bit	4TS / recover less than **62** packets order change
6	1bit	7bit	2TS / recover less than **126** packets order change

FIG. 7

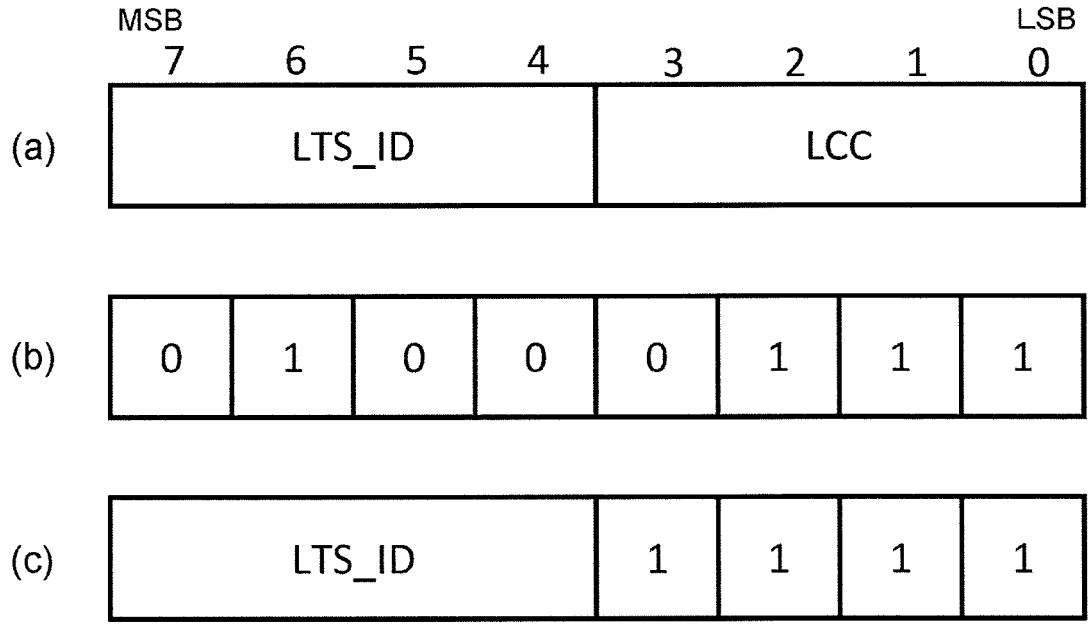

MSB
LSB
7 6 5 4 3 2 1 0
(a)
LTS_ID
LCC
(b)
0 1 0 0 0 1 1 1
(c)
LTS_ID
1 1 1 1

FIG. 8

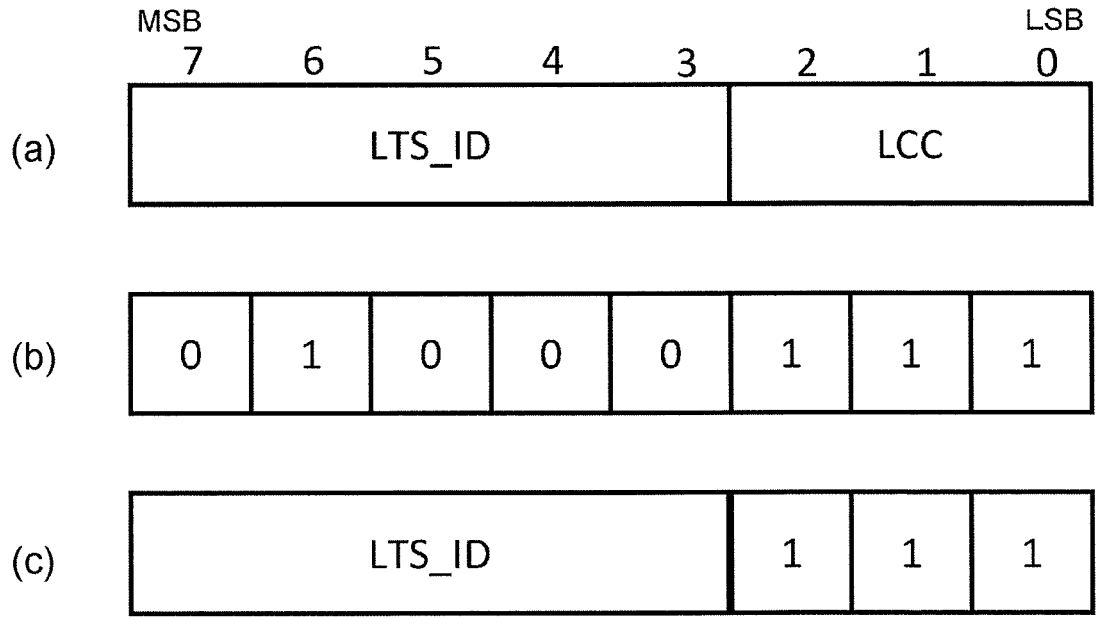

MSB
LSB
7 6 5 4 3 2 1 0
(a)
LTS_ID
LCC
(b)
0 1 0 0 0 1 1 1
(c)
LTS_ID
1 1 1

FIG. 9

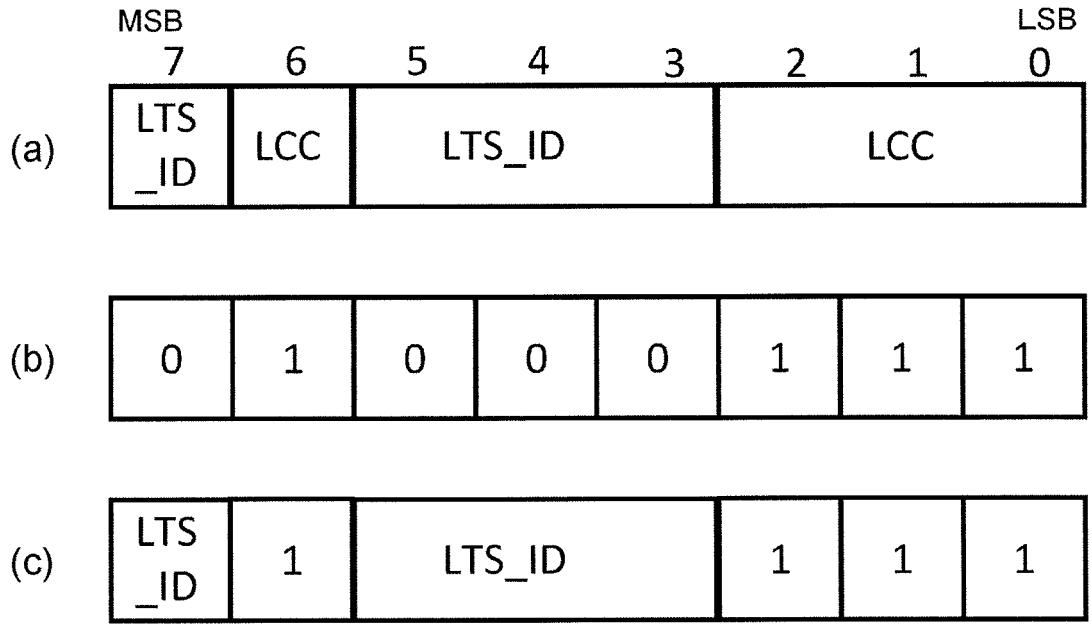

MSB
LSB
7 6 5 4 3 2 1 0
(a)
LTS _ID
LCC
LTS_ID
LCC
(b)
0 1 0 0 0 1 1 1
(c)
LTS _ID
1
LTS_ID
1 1 1

FIG. 10

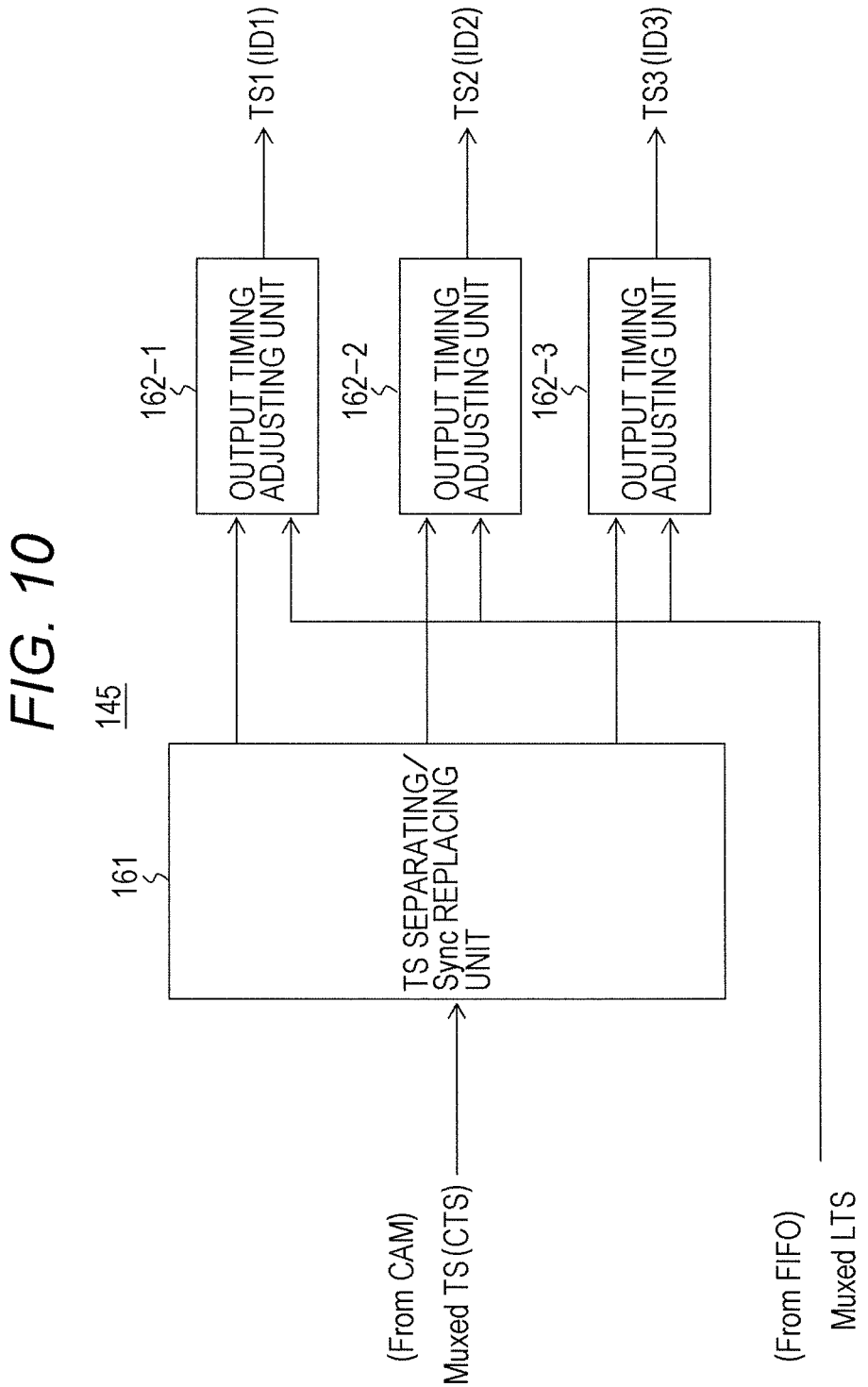

145
161
TS SEPARATING/
Sync REPLACING
UNIT
162-1
OUTPUT TIMING
ADJUSTING UNIT
162-2
OUTPUT TIMING
ADJUSTING UNIT
162-3
OUTPUT TIMING
ADJUSTING UNIT
TS1 (ID1)
TS2 (ID2)
TS3 (ID3)
(From CAM)
Muxed TS (CTS)
(From FIFO)
Muxed LTS

FIG. 11

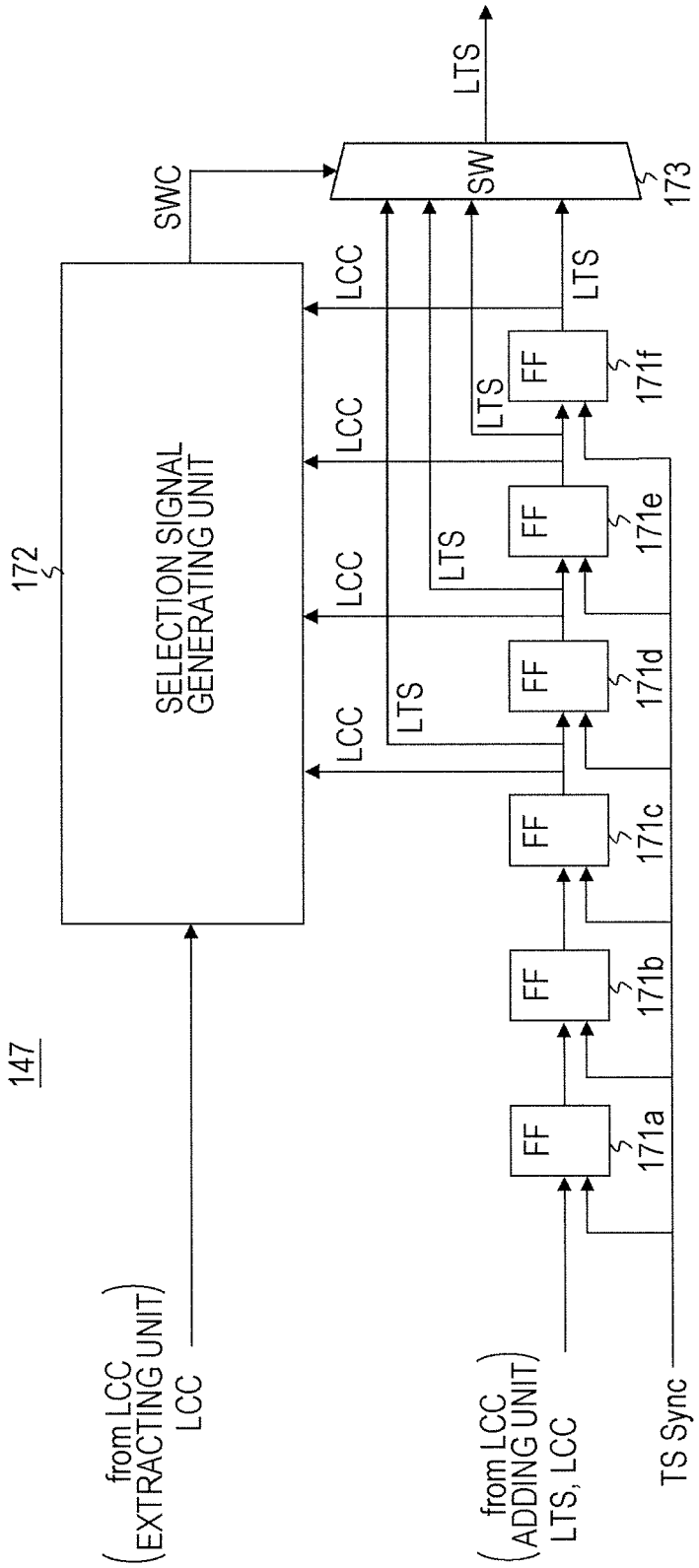

147
172
SELECTION SIGNAL GENERATING UNIT
SWC
SW
173
LTS
LCC
FF
171a
171b
171c
171d
171e
171f
from LCC (EXTRACTING UNIT) LCC
from LCC (ADDING UNIT) LTS, LCC
TS Sync

FIG. 12

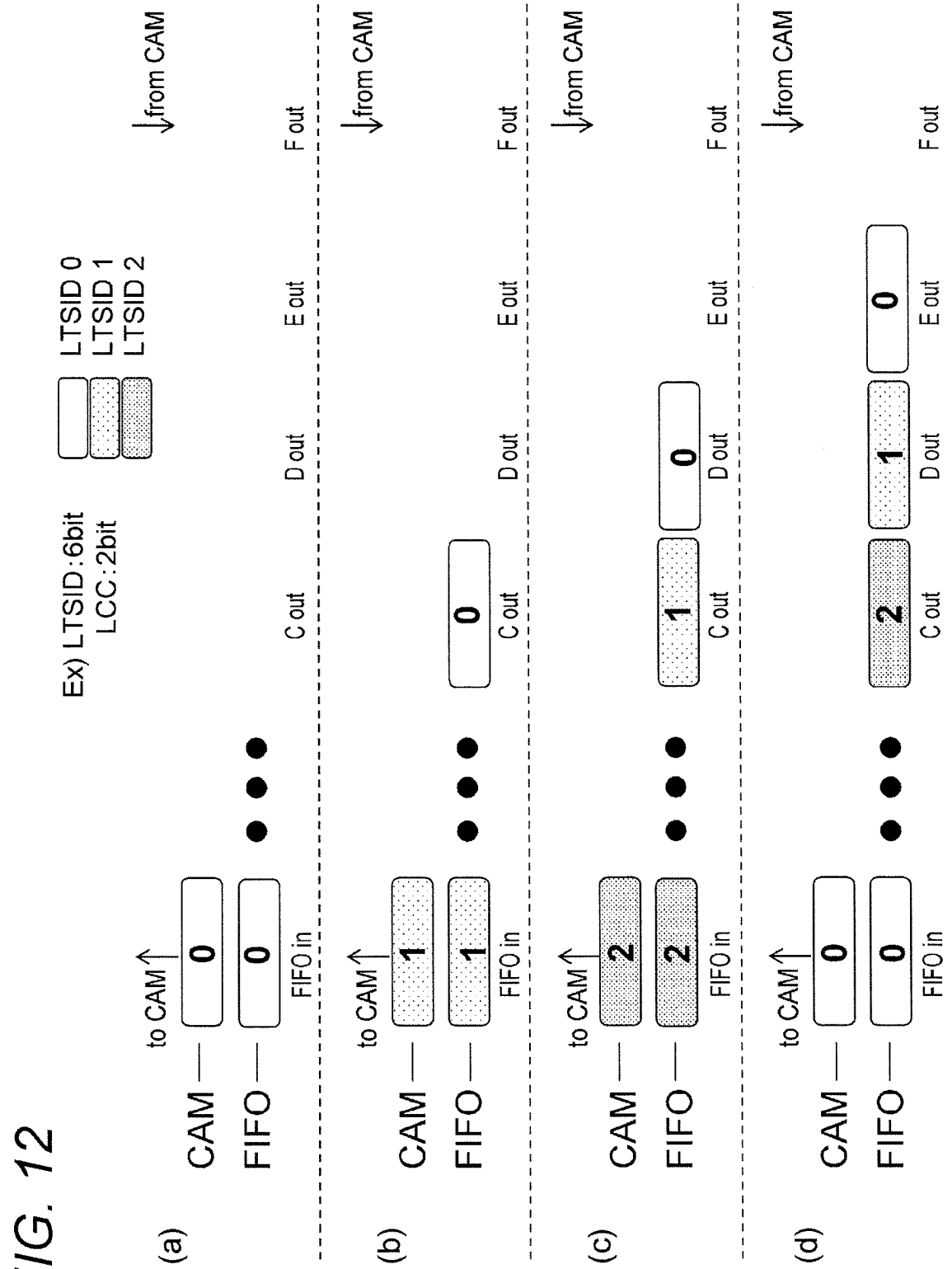

Ex) LTSID:6bit
LCC:2bit
LTSID 0
LTSID 1
LTSID 2
(a)
(b)
(c)
(d)
CAM
FIFO
to CAM
from CAM
FIFO in
C out
D out
E out
F out

FIG. 13

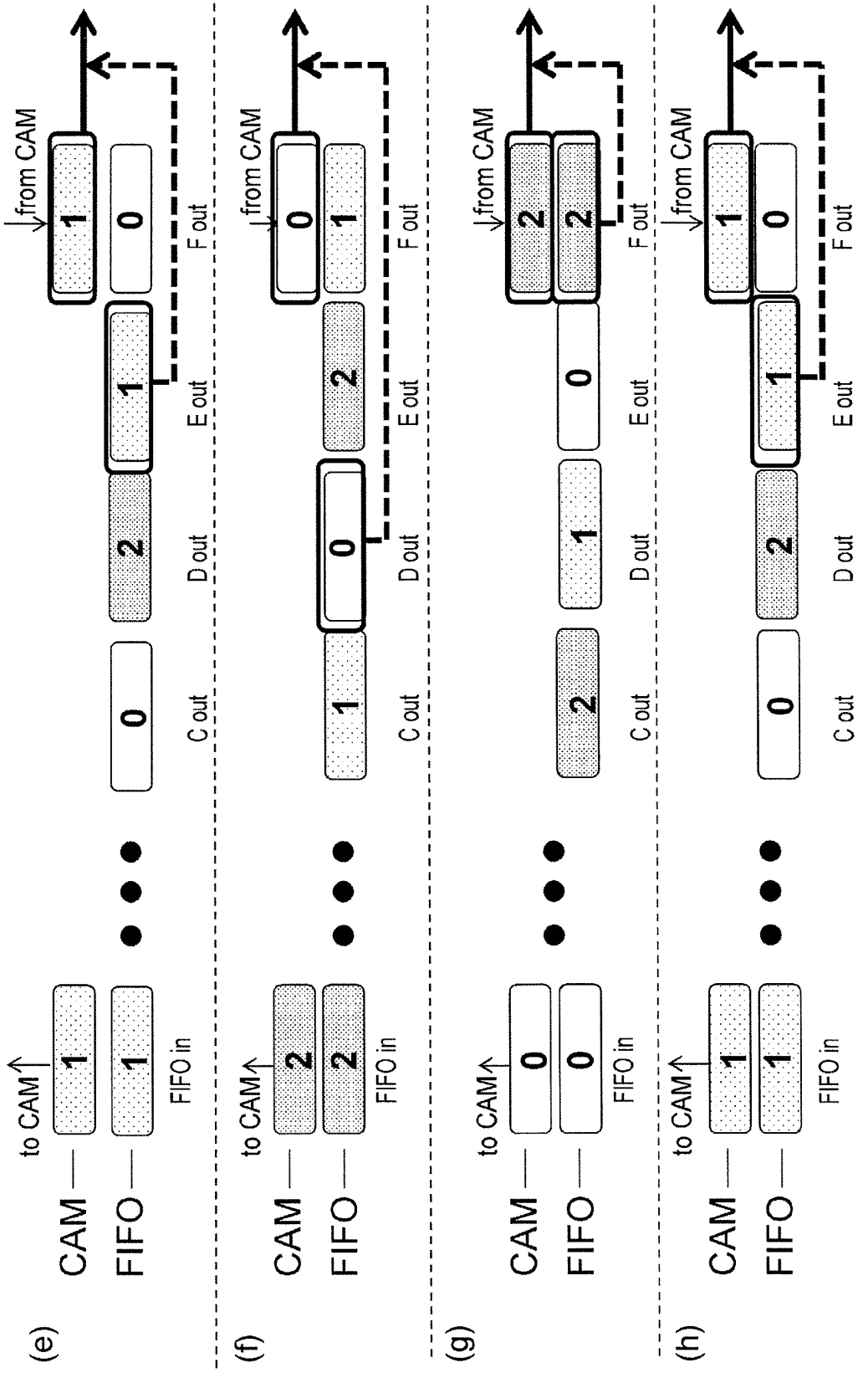


FIG. 14

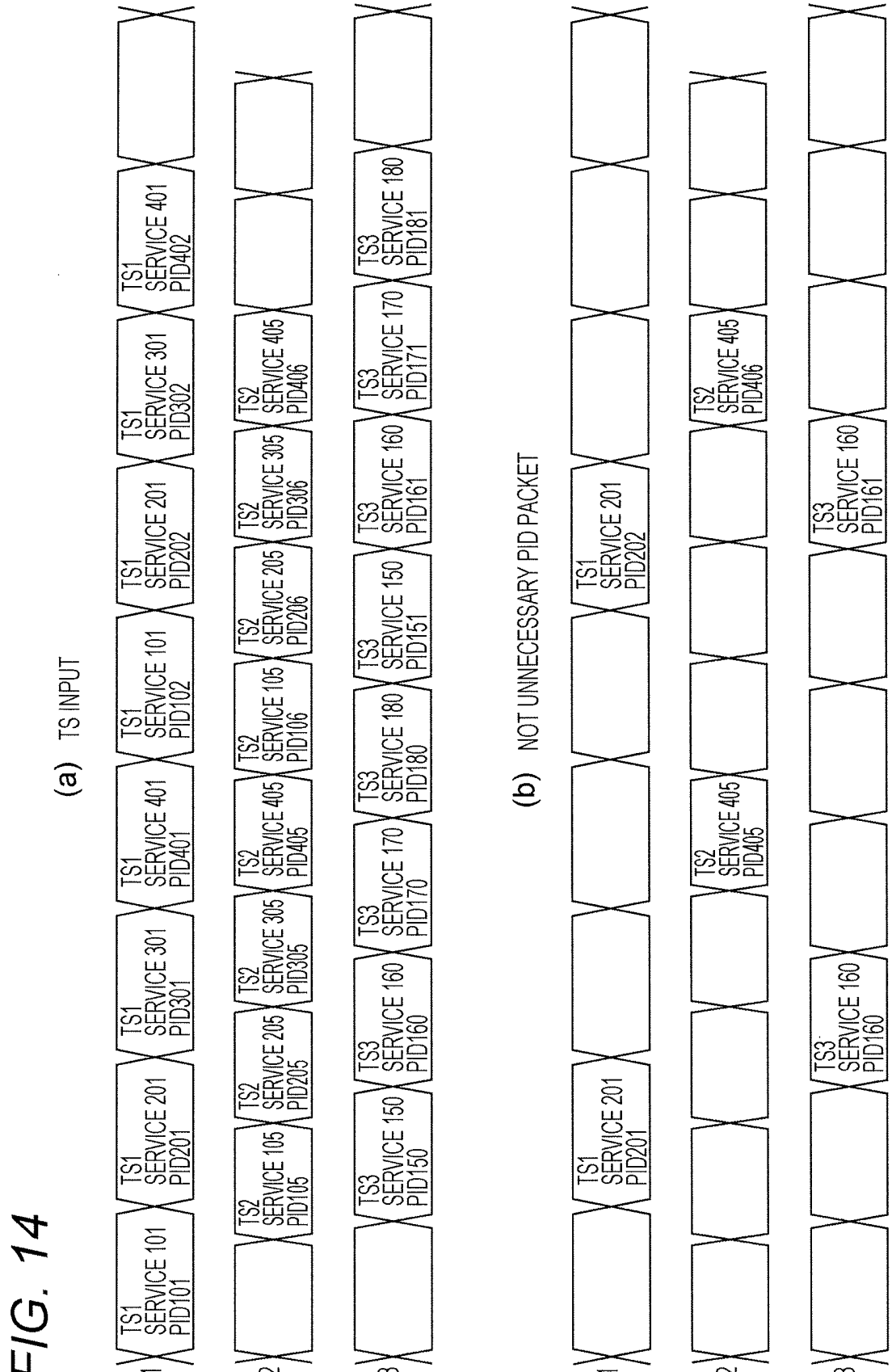

(a) TS INPUT
TS1
TS1 SERVICE 101 PID101
TS1 SERVICE 201 PID201
TS1 SERVICE 301 PID301
TS1 SERVICE 401 PID401
TS1 SERVICE 101 PID102
TS1 SERVICE 201 PID202
TS1 SERVICE 301 PID302
TS1 SERVICE 401 PID402
TS2
TS2 SERVICE 105 PID105
TS2 SERVICE 205 PID205
TS2 SERVICE 305 PID305
TS2 SERVICE 405 PID405
TS2 SERVICE 105 PID106
TS2 SERVICE 205 PID206
TS2 SERVICE 305 PID306
TS2 SERVICE 405 PID406
TS3
TS3 SERVICE 150 PID150
TS3 SERVICE 160 PID160
TS3 SERVICE 170 PID170
TS3 SERVICE 180 PID180
TS3 SERVICE 150 PID151
TS3 SERVICE 160 PID161
TS3 SERVICE 170 PID171
TS3 SERVICE 180 PID181
(b) NOT UNNECESSARY PID PACKET
TS1
TS1 SERVICE 201 PID201
TS1 SERVICE 201 PID202
TS2
TS2 SERVICE 405 PID405
TS2 SERVICE 405 PID406
TS3
TS3 SERVICE 160 PID160
TS3 SERVICE 160 PID161

FIG. 15

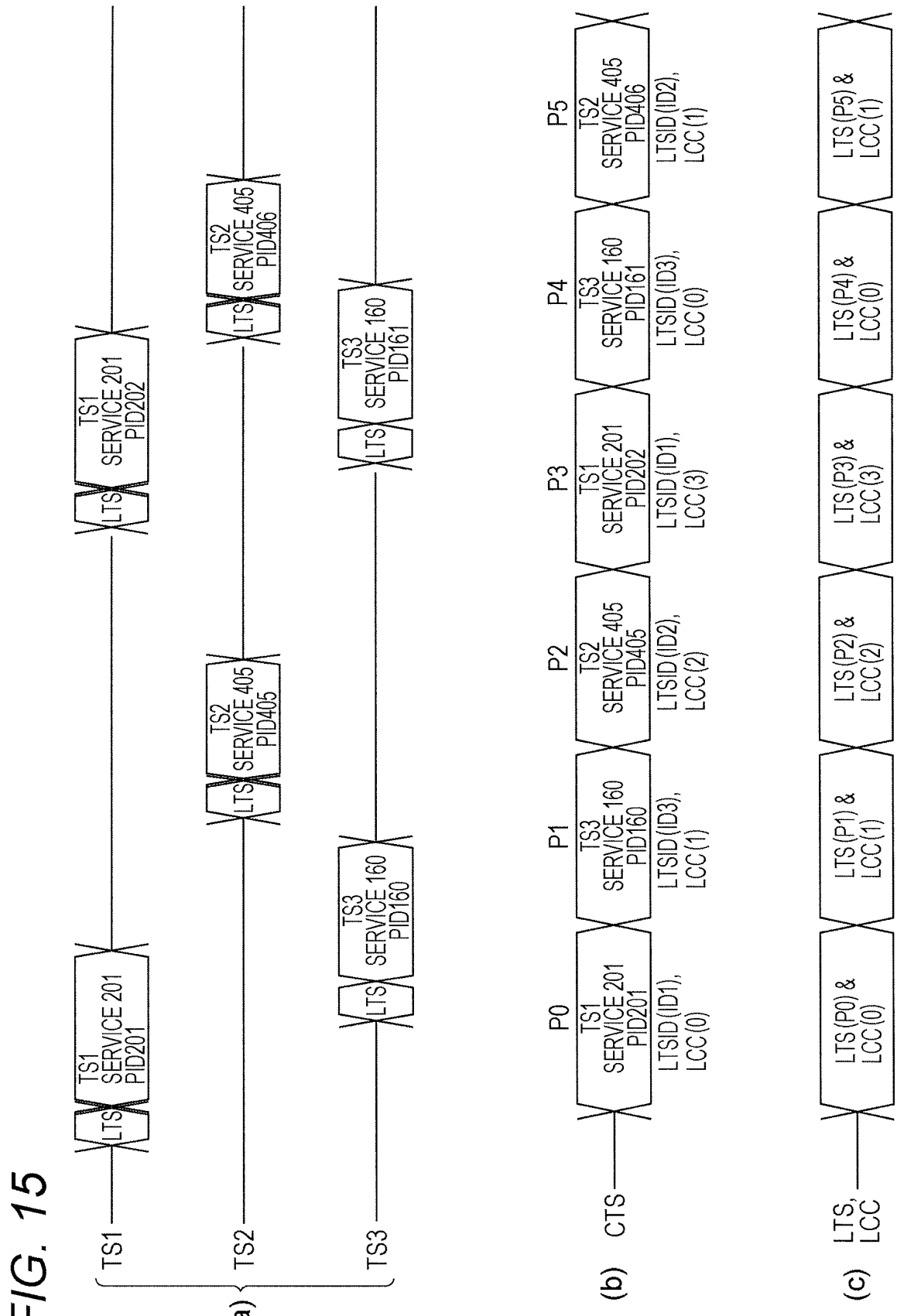

(a)
TS1
TS2
TS3
LTS
TS1 SERVICE 201 PID201
TS3 SERVICE 160 PID160
TS2 SERVICE 405 PID405
TS1 SERVICE 201 PID202
TS2 SERVICE 405 PID406
TS3 SERVICE 160 PID161
(b)
CTS
P0
P1
P2
P3
P4
P5
TS1 SERVICE 201 PID201
LTSID (ID1), LCC (0)
TS3 SERVICE 160 PID160
LTSID (ID3), LCC (1)
TS2 SERVICE 405 PID405
LTSID (ID2), LCC (2)
TS1 SERVICE 201 PID202
LTSID (ID1), LCC (3)
TS3 SERVICE 160 PID161
LTSID (ID3), LCC (0)
TS2 SERVICE 405 PID406
LTSID (ID2), LCC (1)
(c)
LTS, LCC
LTS (P0) & LCC (0)
LTS (P1) & LCC (1)
LTS (P2) & LCC (2)
LTS (P3) & LCC (3)
LTS (P4) & LCC (0)
LTS (P5) & LCC (1)

FIG. 16

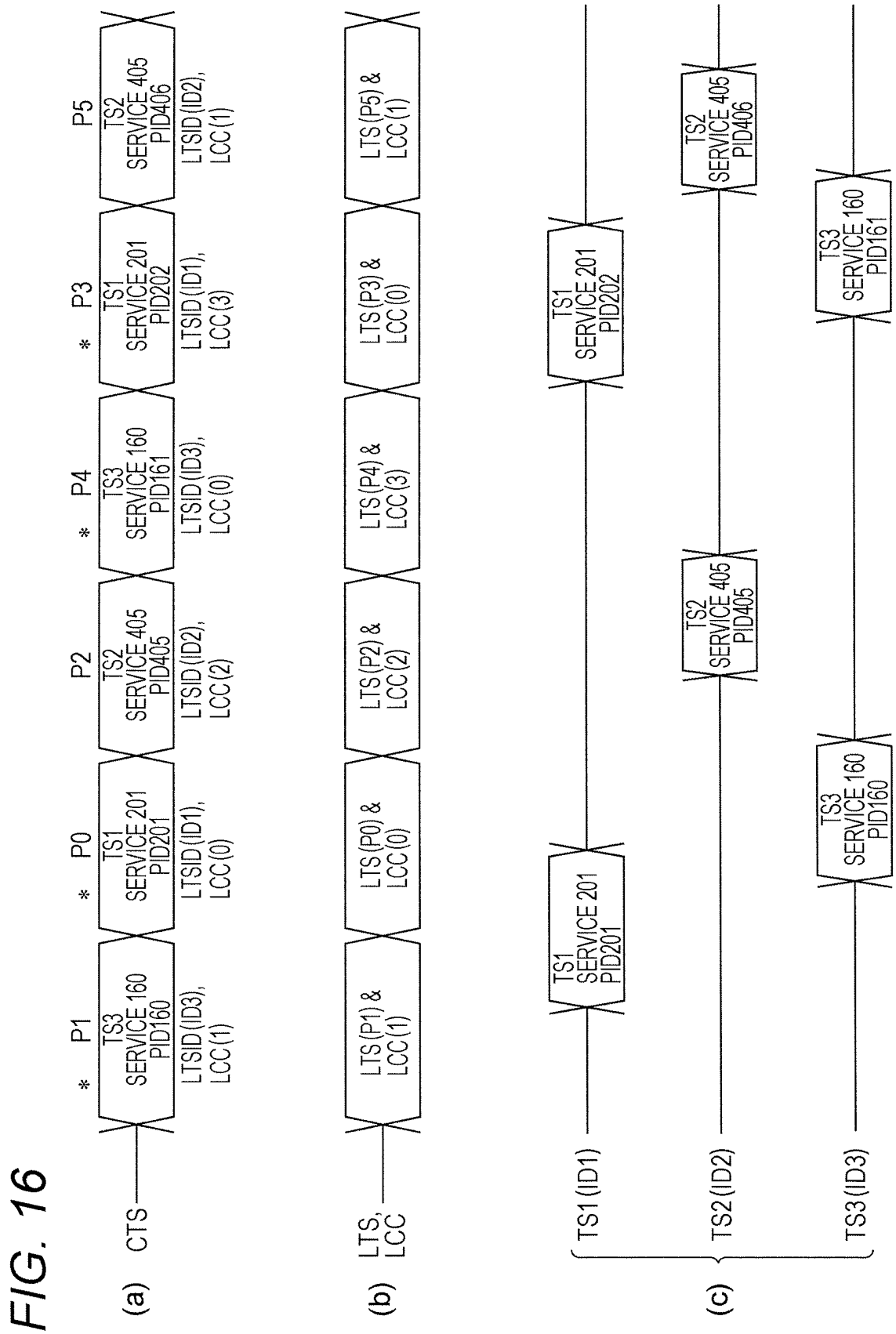

(a)
CTS
P1
TS3 SERVICE 160 PID160
LTSID (ID3), LCC (1)
P0
TS1 SERVICE 201 PID201
LTSID (ID1), LCC (0)
P2
TS2 SERVICE 405 PID405
LTSID (ID2), LCC (2)
P4
TS3 SERVICE 160 PID161
LTSID (ID3), LCC (0)
P3
TS1 SERVICE 201 PID202
LTSID (ID1), LCC (3)
P5
TS2 SERVICE 405 PID406
LTSID (ID2), LCC (1)
(b)
LTS, LCC
LTS (P1) & LCC (1)
LTS (P0) & LCC (0)
LTS (P2) & LCC (2)
LTS (P4) & LCC (3)
LTS (P3) & LCC (0)
LTS (P5) & LCC (1)
(c)
TS1 (ID1)
TS1 SERVICE 201 PID201
TS2 SERVICE 405 PID405
TS1 SERVICE 201 PID202
TS2 (ID2)
TS3 SERVICE 160 PID160
TS2 SERVICE 405 PID406
TS3 (ID3)
TS3 SERVICE 160 PID161

FIG. 17

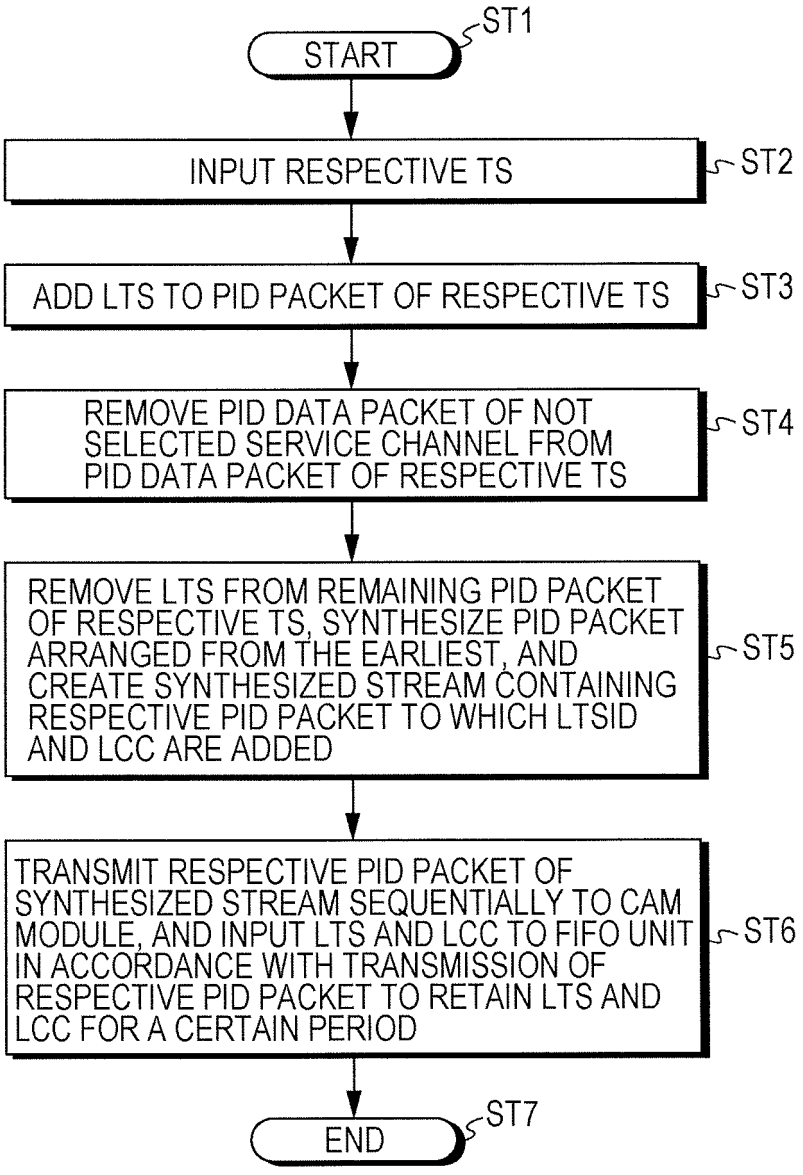

START
ST1
INPUT RESPECTIVE TS
ST2
ADD LTS TO PID PACKET OF RESPECTIVE TS
ST3
REMOVE PID DATA PACKET OF NOT SELECTED SERVICE CHANNEL FROM PID DATA PACKET OF RESPECTIVE TS
ST4
REMOVE LTS FROM REMAINING PID PACKET OF RESPECTIVE TS, SYNTHESIZE PID PACKET ARRANGED FROM THE EARLIEST, AND CREATE SYNTHESIZED STREAM CONTAINING RESPECTIVE PID PACKET TO WHICH LTSID AND LCC ARE ADDED
ST5
TRANSMIT RESPECTIVE PID PACKET OF SYNTHESIZED STREAM SEQUENTIALLY TO CAM MODULE, AND INPUT LTS AND LCC TO FIFO UNIT IN ACCORDANCE WITH TRANSMISSION OF RESPECTIVE PID PACKET TO RETAIN LTS AND LCC FOR A CERTAIN PERIOD
ST6
END
ST7

FIG. 18

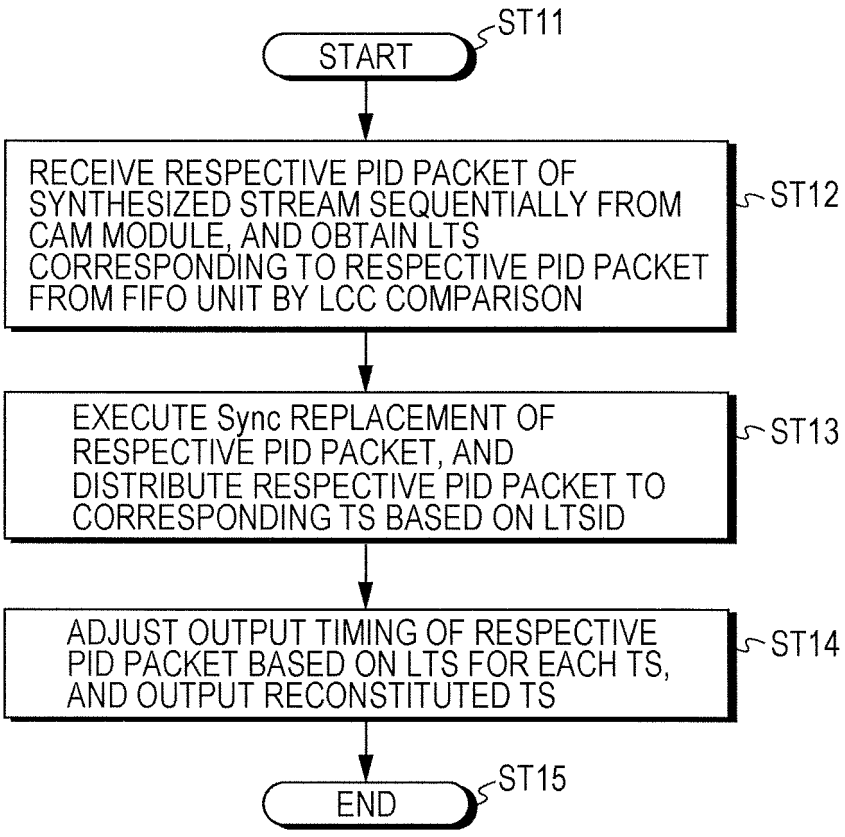

START
ST11
RECEIVE RESPECTIVE PID PACKET OF SYNTHESIZED STREAM SEQUENTIALLY FROM CAM MODULE, AND OBTAIN LTS CORRESPONDING TO RESPECTIVE PID PACKET FROM FIFO UNIT BY LCC COMPARISON
ST12
EXECUTE Sync REPLACEMENT OF RESPECTIVE PID PACKET, AND DISTRIBUTE RESPECTIVE PID PACKET TO CORRESPONDING TS BASED ON LTSID
ST13
ADJUST OUTPUT TIMING OF RESPECTIVE PID PACKET BASED ON LTS FOR EACH TS, AND OUTPUT RECONSTITUTED TS
ST14
END
ST15

FIG. 19

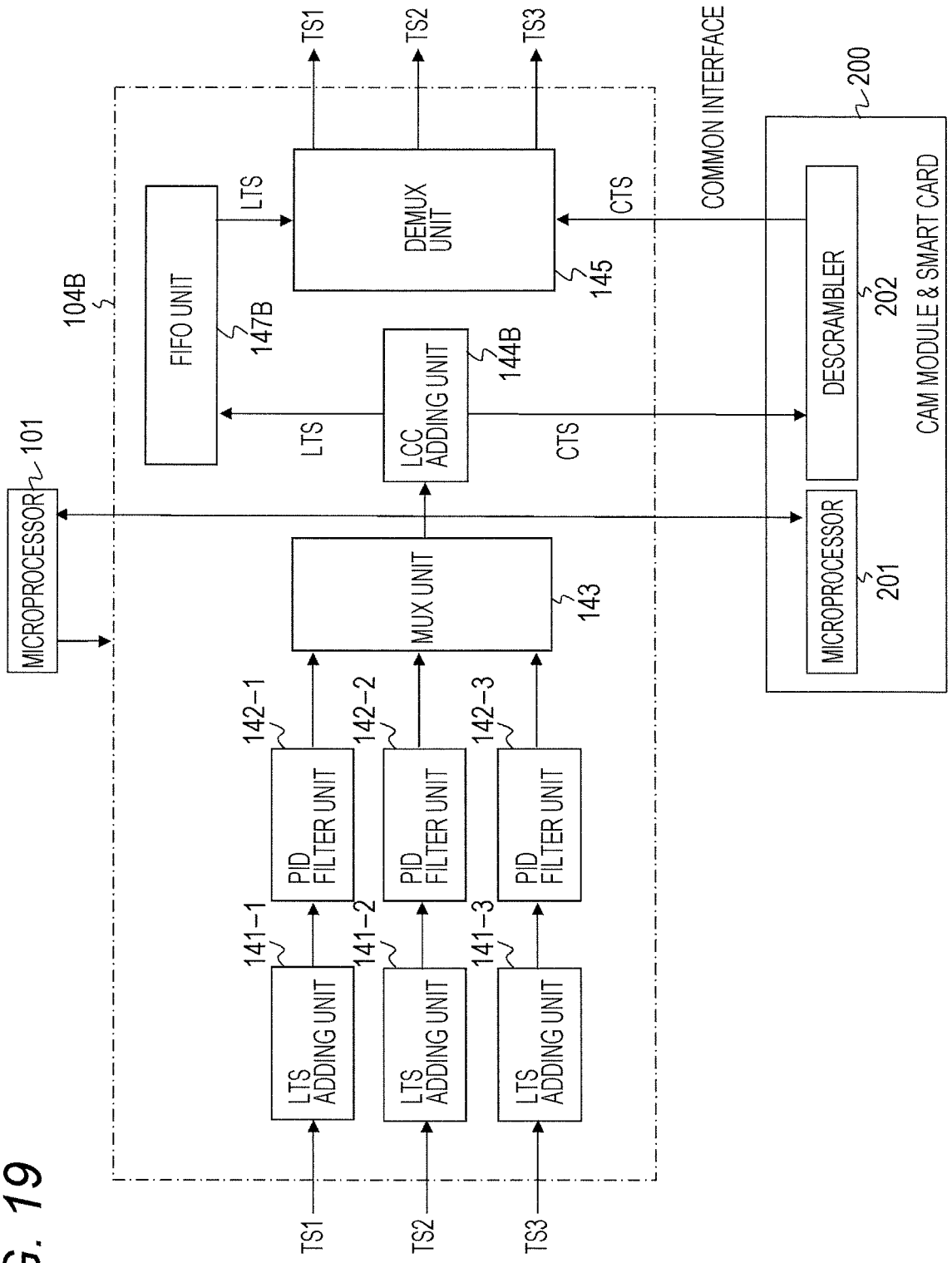

104B
MICROPROCESSOR
101
FIFO UNIT
147B
LTS
DEMUX UNIT
145
CTS
COMMON INTERFACE
200
TS1
TS2
TS3
LCC ADDING UNIT
144B
LTS
CTS
DESCRAMBLER
202
CAM MODULE & SMART CARD
MICROPROCESSOR
201
MUX UNIT
143
142-1
142-2
142-3
PID FILTER UNIT
PID FILTER UNIT
PID FILTER UNIT
141-1
141-2
141-3
LTS ADDING UNIT
LTS ADDING UNIT
LTS ADDING UNIT
TS1
TS2
TS3

FIG. 20

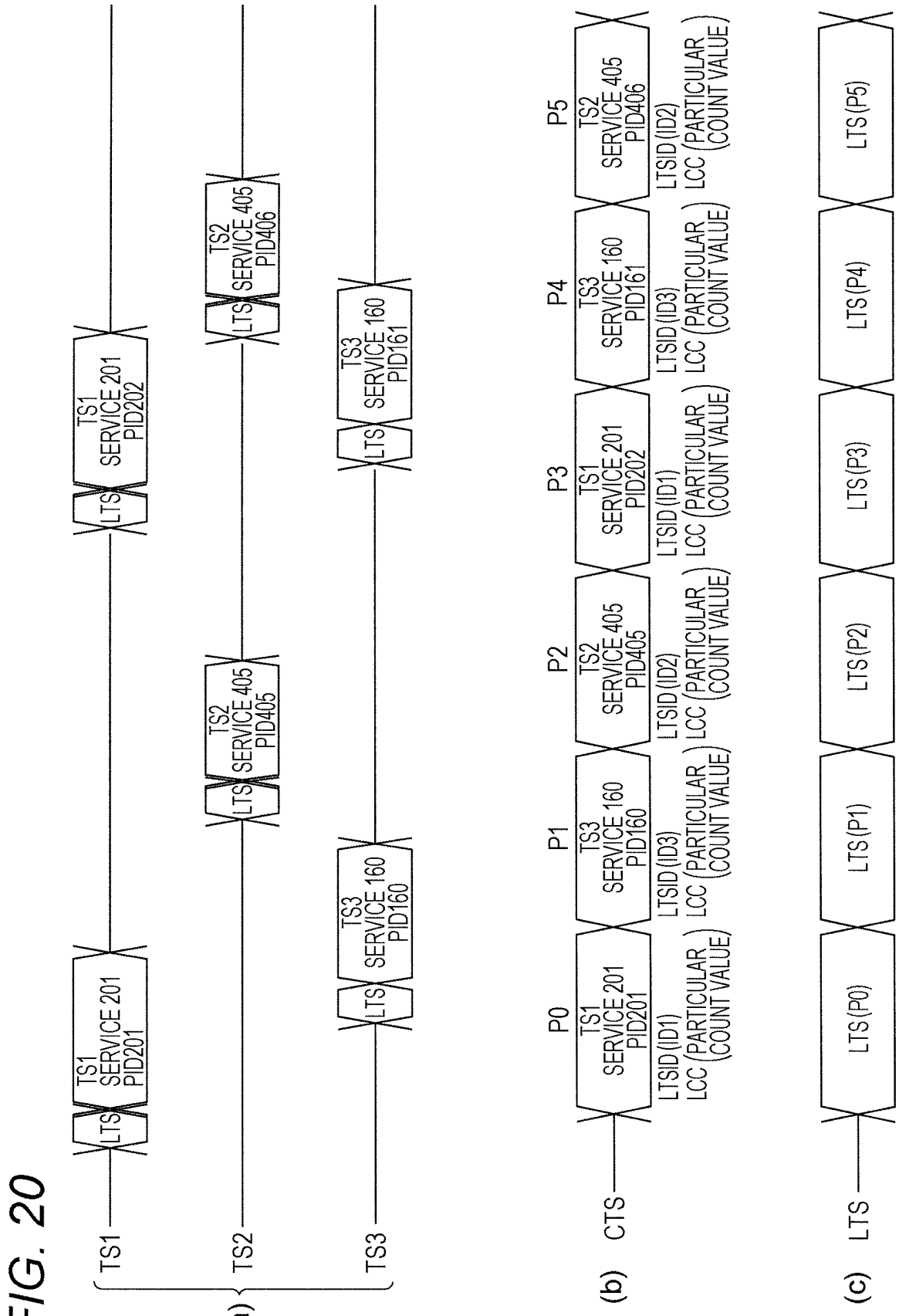

(a)
TS1
TS2
TS3
LTS
TS1 SERVICE 201 PID201
TS3 SERVICE 160 PID160
TS2 SERVICE 405 PID405
TS1 SERVICE 201 PID202
TS2 SERVICE 405 PID406
TS3 SERVICE 160 PID161
(b)
CTS
P0
P1
P2
P3
P4
P5
LTSID (ID1) LCC (PARTICULAR (COUNT VALUE)
LTSID (ID3) LCC (PARTICULAR (COUNT VALUE)
LTSID (ID2) LCC (PARTICULAR (COUNT VALUE)
LTSID (ID1) LCC (PARTICULAR (COUNT VALUE)
LTSID (ID3) LCC (PARTICULAR (COUNT VALUE)
LTSID (ID2) LCC (PARTICULAR (COUNT VALUE)
(c)
LTS
LTS (P0)
LTS (P1)
LTS (P2)
LTS (P3)
LTS (P4)
LTS (P5)

FIG. 21

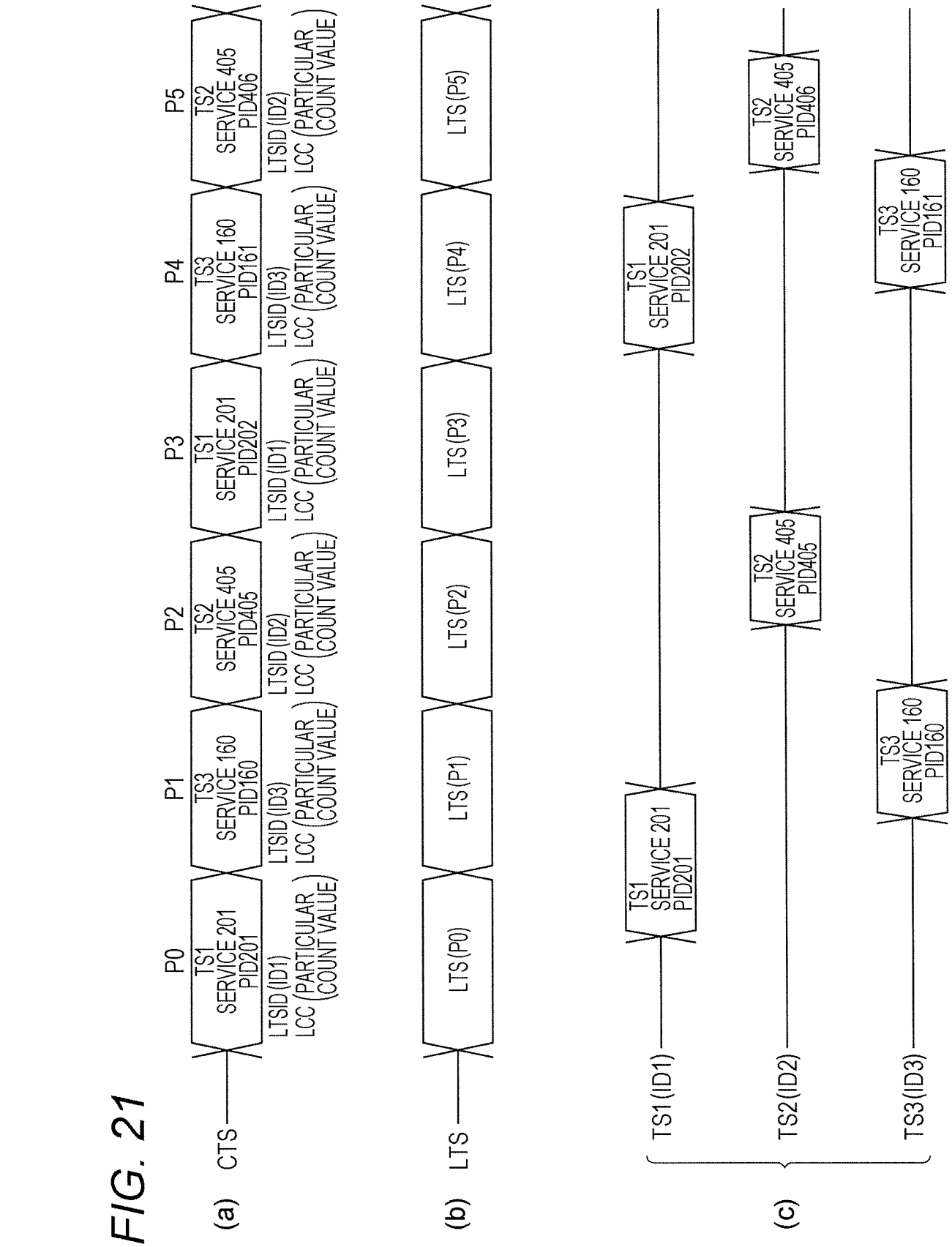

(a)
CTS
P0
TS1 SERVICE 201 PID201
LTSID (ID1) LCC (PARTICULAR (COUNT VALUE)
P1
TS3 SERVICE 160 PID160
LTSID (ID3) LCC (PARTICULAR (COUNT VALUE)
P2
TS2 SERVICE 405 PID405
LTSID (ID2) LCC (PARTICULAR (COUNT VALUE)
P3
TS1 SERVICE 201 PID202
LTSID (ID1) LCC (PARTICULAR (COUNT VALUE)
P4
TS3 SERVICE 160 PID161
LTSID (ID3) LCC (PARTICULAR (COUNT VALUE)
P5
TS2 SERVICE 405 PID406
LTSID (ID2) LCC (PARTICULAR (COUNT VALUE)
(b)
LTS
LTS (P0)
LTS (P1)
LTS (P2)
LTS (P3)
LTS (P4)
LTS (P5)
(c)
TS1 (ID1)
TS1 SERVICE 201 PID201
TS1 SERVICE 201 PID202
TS2 (ID2)
TS2 SERVICE 405 PID405
TS2 SERVICE 405 PID406
TS3 (ID3)
TS3 SERVICE 160 PID160
TS3 SERVICE 160 PID161

FIG. 22

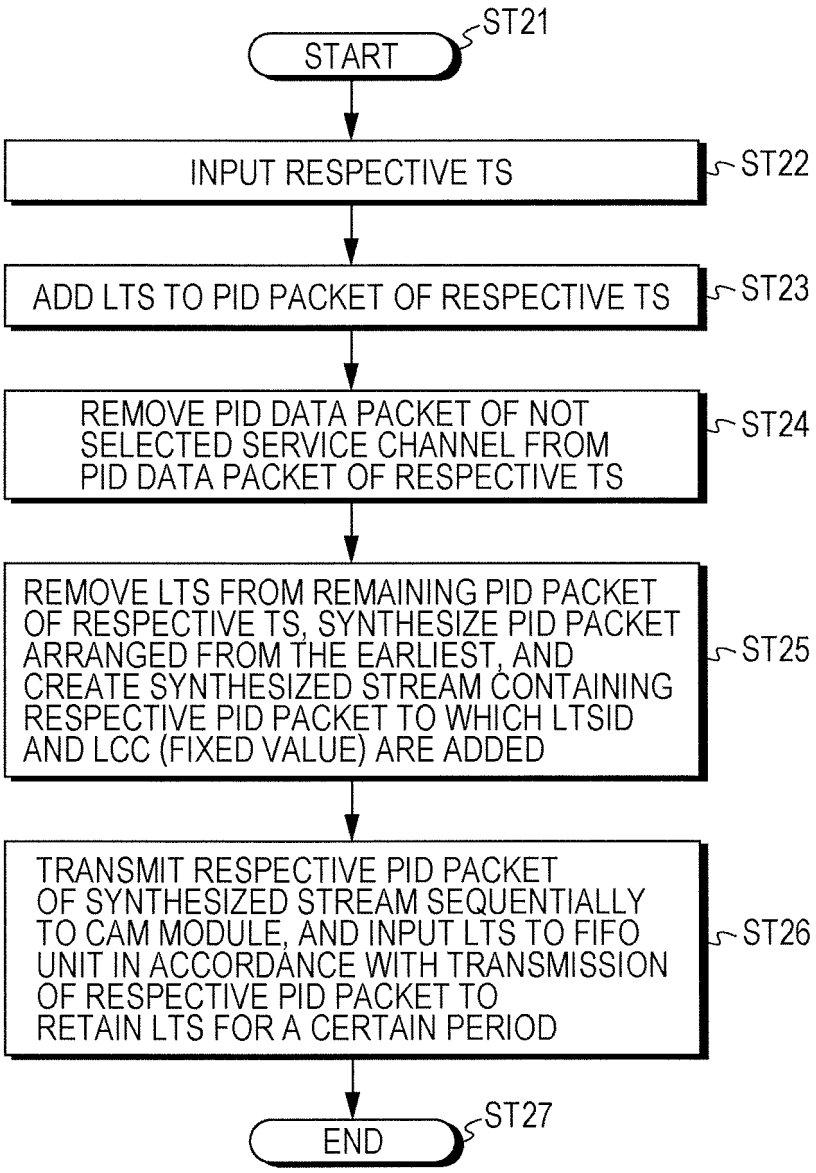

START
ST21
INPUT RESPECTIVE TS
ST22
ADD LTS TO PID PACKET OF RESPECTIVE TS
ST23
REMOVE PID DATA PACKET OF NOT SELECTED SERVICE CHANNEL FROM PID DATA PACKET OF RESPECTIVE TS
ST24
REMOVE LTS FROM REMAINING PID PACKET OF RESPECTIVE TS, SYNTHESIZE PID PACKET ARRANGED FROM THE EARLIEST, AND CREATE SYNTHESIZED STREAM CONTAINING RESPECTIVE PID PACKET TO WHICH LTSID AND LCC (FIXED VALUE) ARE ADDED
ST25
TRANSMIT RESPECTIVE PID PACKET OF SYNTHESIZED STREAM SEQUENTIALLY TO CAM MODULE, AND INPUT LTS TO FIFO UNIT IN ACCORDANCE WITH TRANSMISSION OF RESPECTIVE PID PACKET TO RETAIN LTS FOR A CERTAIN PERIOD
ST26
END
ST27

FIG. 23

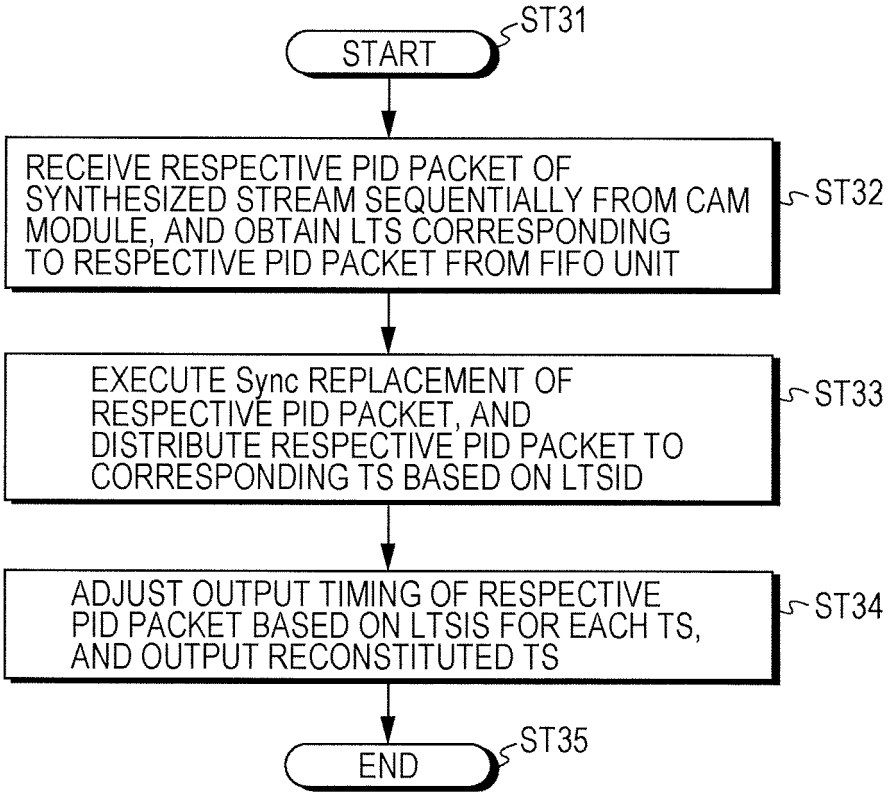

START
ST31
RECEIVE RESPECTIVE PID PACKET OF SYNTHESIZED STREAM SEQUENTIALLY FROM CAM MODULE, AND OBTAIN LTS CORRESPONDING TO RESPECTIVE PID PACKET FROM FIFO UNIT
ST32
EXECUTE Sync REPLACEMENT OF RESPECTIVE PID PACKET, AND DISTRIBUTE RESPECTIVE PID PACKET TO CORRESPONDING TS BASED ON LTSID
ST33
ADJUST OUTPUT TIMING OF RESPECTIVE PID PACKET BASED ON LTSIS FOR EACH TS, AND OUTPUT RECONSTITUTED TS
ST34
END
ST35

FIG. 24

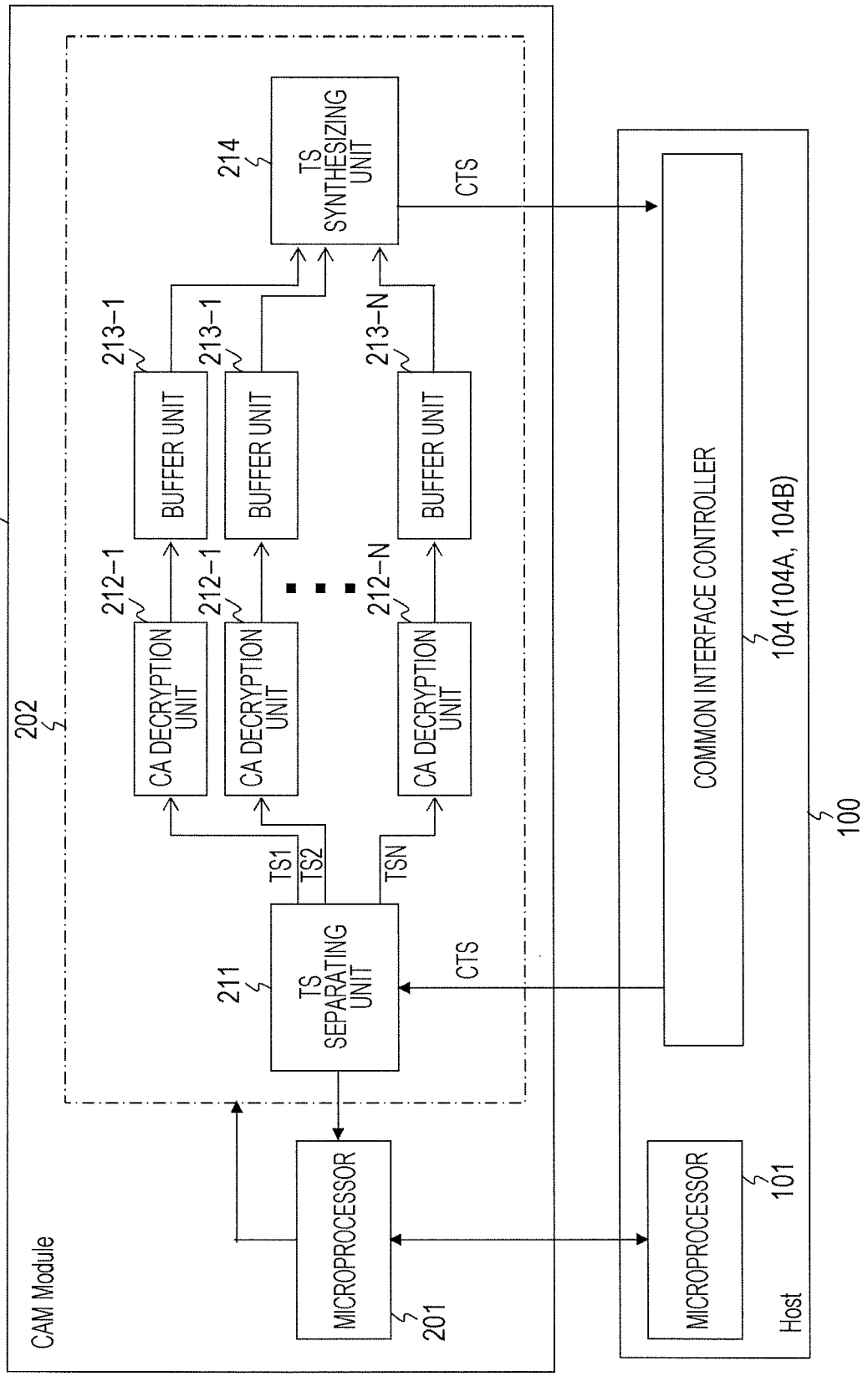

CAM Module
200
202
MICROPROCESSOR
201
TS SEPARATING UNIT
211
TS1
TS2
TSN
CTS
CA DECRYPTION UNIT
212-1
212-1
212-N
BUFFER UNIT
213-1
213-1
213-N
TS SYNTHESIZING UNIT
214
CTS
COMMON INTERFACE CONTROLLER
104 (104A, 104B)
MICROPROCESSOR
101
Host
100

FIG. 25

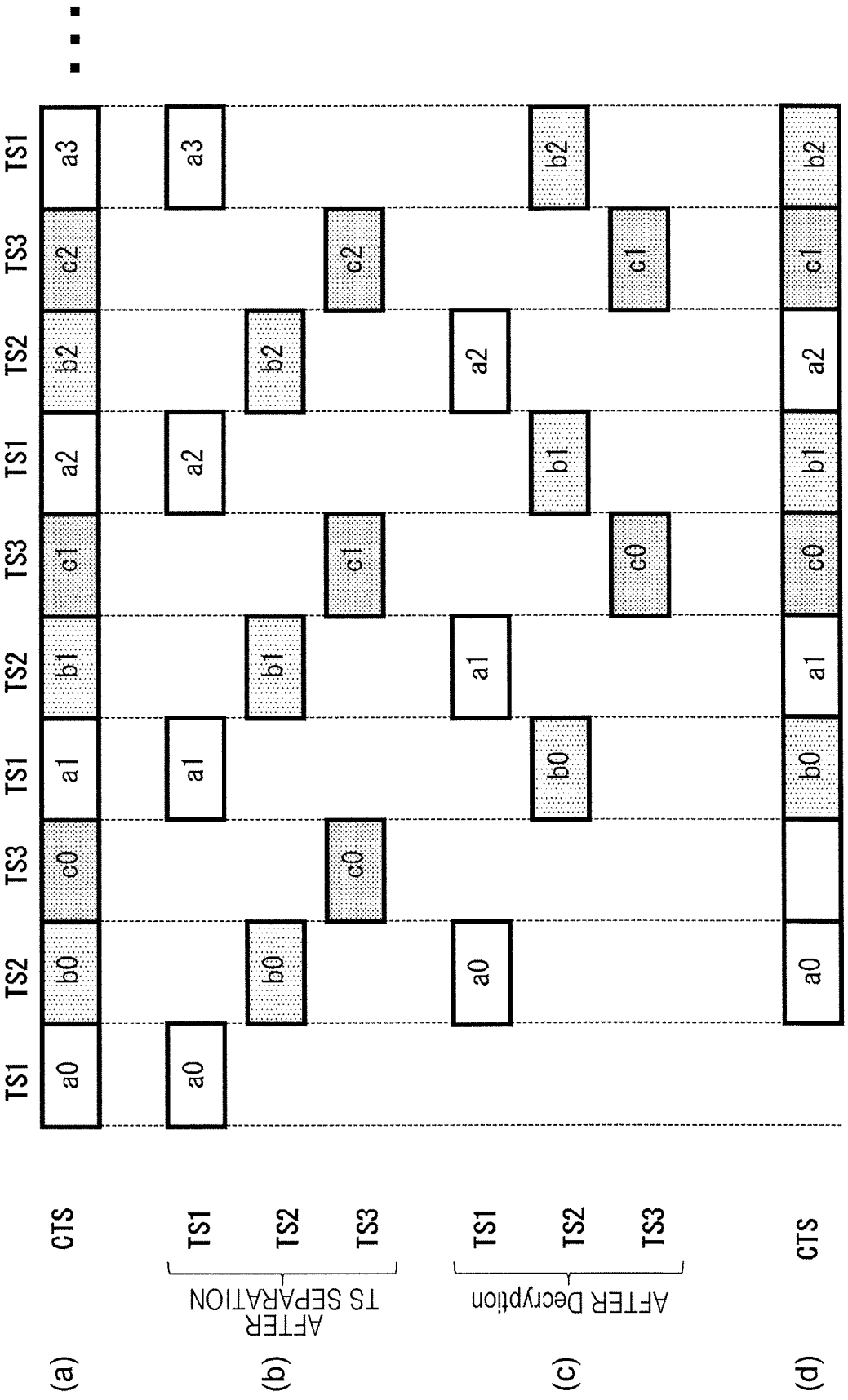

(a)
CTS
TS1
TS2
TS3
TS1
TS2
TS3
TS1
TS2
TS3
TS1
a0
b0
c0
a1
b1
c1
a2
b2
c2
a3
(b)
AFTER TS SEPARATION
TS1
TS2
TS3
a0
b0
c0
a1
b1
c1
a2
b2
c2
a3
(c)
AFTER Decryption
TS1
TS2
TS3
a0
a1
b0
a2
b1
c0
b2
c1
(d)
CTS
a0
b0
a1
c0
b1
a2
c1
b2

FIG. 26

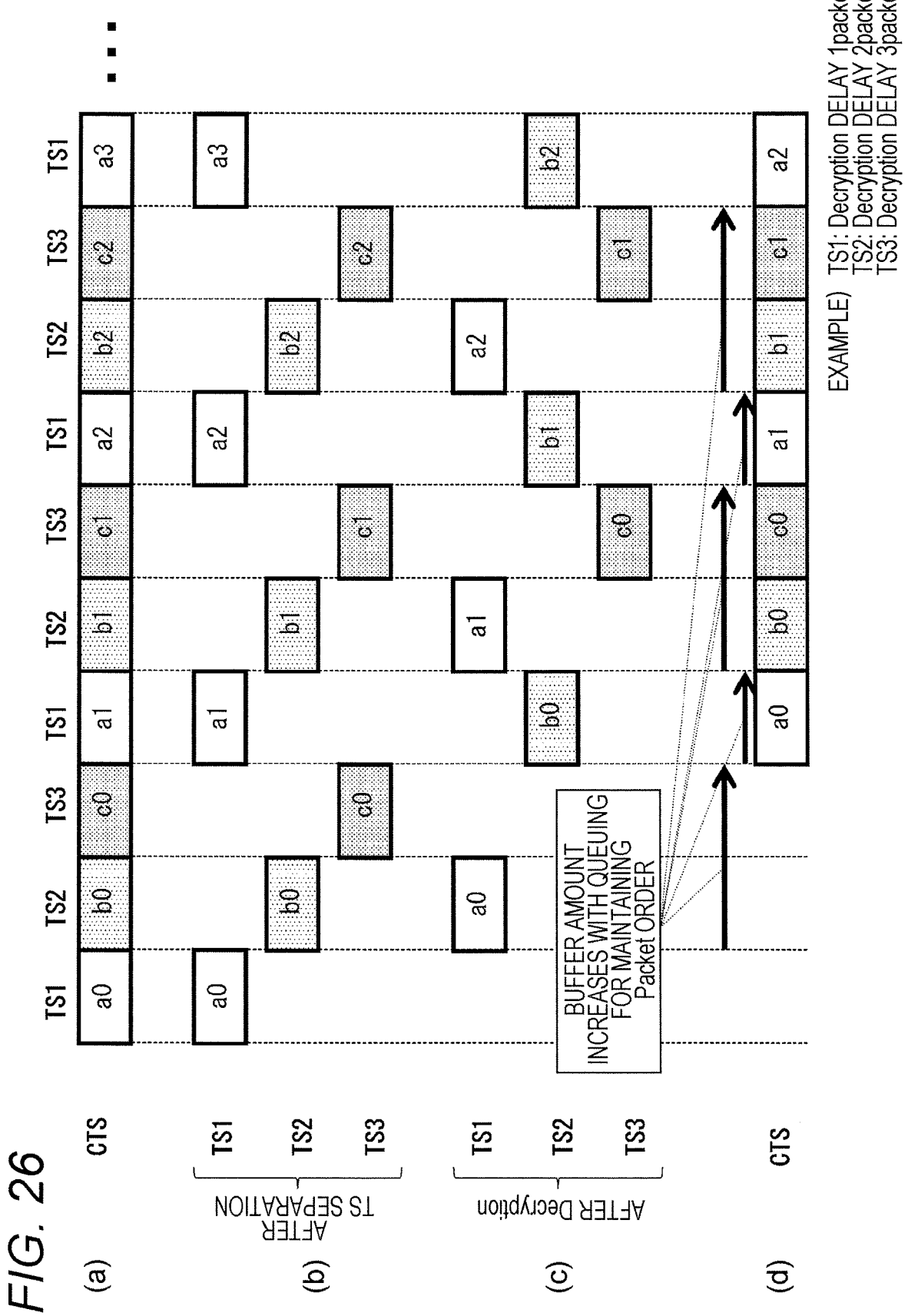

(a)
CTS
TS1
TS2
TS3
(b)
AFTER TS SEPARATION
(c)
AFTER Decryption
BUFFER AMOUNT INCREASES WITH QUEUING FOR MAINTAINING Packet ORDER
(d)
CTS
EXAMPLE)
TS1: Decryption DELAY 1packet
TS2: Decryption DELAY 2packet
TS3: Decryption DELAY 3packet

FIG. 27

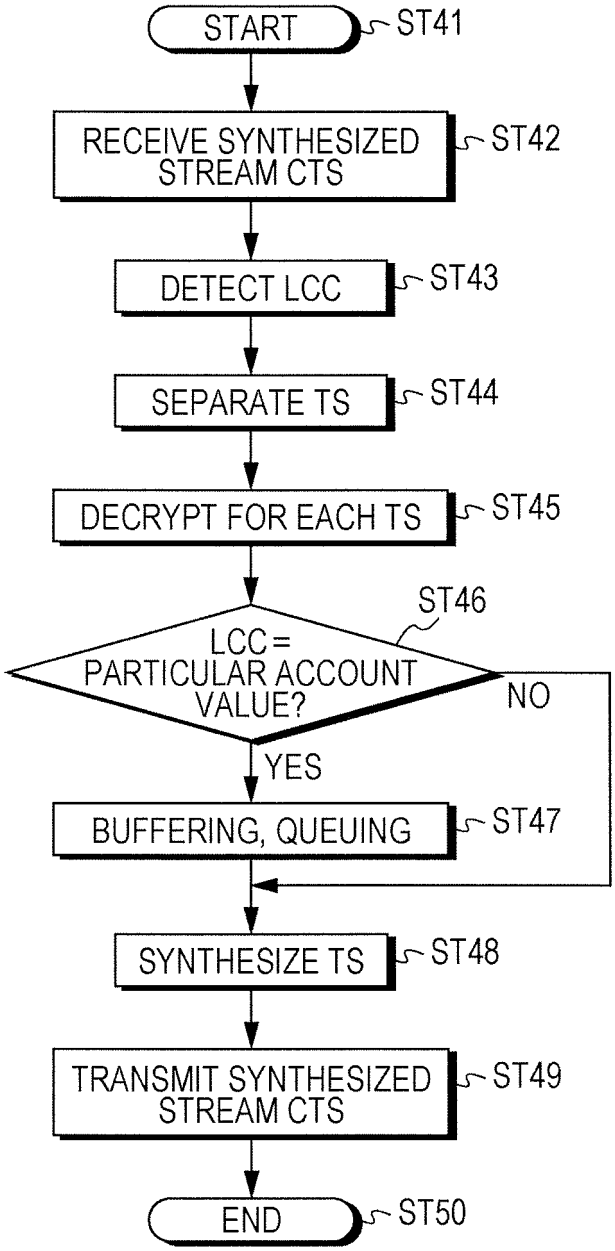

START
ST41
RECEIVE SYNTHESIZED STREAM CTS
ST42
DETECT LCC
ST43
SEPARATE TS
ST44
DECRYPT FOR EACH TS
ST45
ST46
LCC = PARTICULAR ACCOUNT VALUE?
NO
YES
BUFFERING, QUEUING
ST47
SYNTHESIZE TS
ST48
TRANSMIT SYNTHESIZED STREAM CTS
ST49
END
ST50

FIG. 28

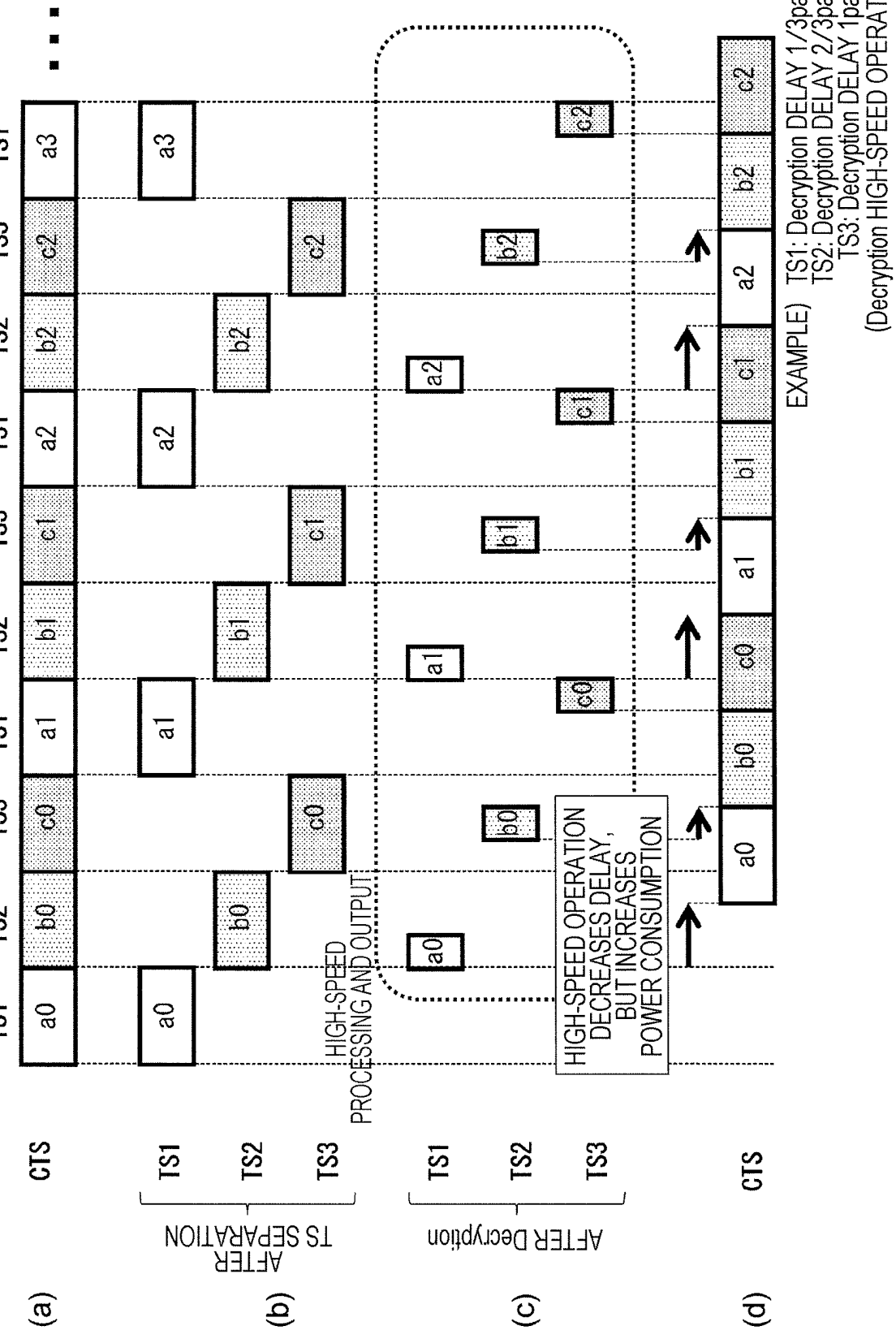

(a)
CTS
TS1
TS2
TS3
TS1
TS2
TS3
TS1
TS2
TS3
TS1
a0
b0
c0
a1
b1
c1
a2
b2
c2
a3
(b)
AFTER TS SEPARATION
TS1
TS2
TS3
HIGH-SPEED PROCESSING AND OUTPUT
(c)
AFTER Decryption
TS1
TS2
TS3
HIGH-SPEED OPERATION DECREASES DELAY, BUT INCREASES POWER CONSUMPTION
(d)
CTS
EXAMPLE)
TS1: Decryption DELAY 1/3packet
TS2: Decryption DELAY 2/3packet
TS3: Decryption DELAY 1packet
(Decryption HIGH-SPEED OPERATION)

FIG. 29

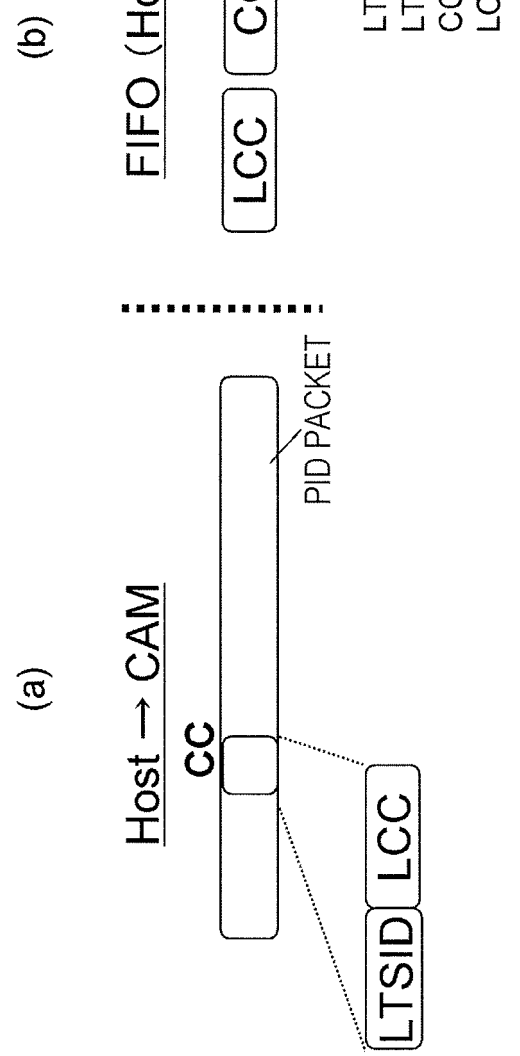

(a)
Host → CAM
CC
LTSID
LCC
PID PACKET
(b)
FIFO (Host)
LCC
CC
LTS
LTSID = Local TS Identifier
LTS = Local Time Stamp
CC = Original Continuity Counter
LCC = Local Continuity Counter

FIG. 30

	LTSID	LCC	Recover range of packet order change
1	2bit	2bit	4TS / recover less than 2 packets order change
2	1bit	3bit	2TS / recover less than 6 packets order change

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2013/077398

A. CLASSIFICATION OF SUBJECT MATTER
H04N21/4385(2011.01)i, *H04N21/418*(2011.01)i, *H04N21/434*(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N21/4385, H04N21/418, H04N21/434

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2013
Kokai Jitsuyo Shinan Koho 1971-2013 Toroku Jitsuyo Shinan Koho 1994-2013

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	EP 1463320 A2 (SONY UNITED KINGDOM LTD.), 29 September 2004 (29.09.2004), paragraphs [0050] to [0063]; fig. 3 & US 2004/0252833 A1 & GB 2399972 A & GB 306958 D0 & KR 10-2004-0084828 A & CN 1543216 A	7,15 17,18 1-6,8-14,16, 19,20
X Y A	US 7508454 B1 (Luc Vantalon), 24 March 2009 (24.03.2009), column 3, line 9 to column 4, line 19; fig. 1 (Family: none)	7,15 17,18 1-6,8-14,16, 19,20

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December, 2013 (20.12.13)	07 January, 2014 (07.01.14)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2013/077398

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2001-86481 A (Matsushita Electric Industrial Co., Ltd.), 30 March 2001 (30.03.2001), paragraphs [0044], [0124], [0149] to [0151]; fig. 2, 14, 15 (Family: none)	17,18 1-16,19,20
A	JP 2009-171575 A (Irdeto Access B.V.), 30 July 2009 (30.07.2009), paragraphs [0025] to [0033]; fig. 1, 2 & US 2009/0183004 A1 & EP 2079237 A1 & CA 2648209 A & KR 10-2009-0078308 A	1-20
A	JP 11-306132 A (Toshiba Corp.), 05 November 1999 (05.11.1999), paragraphs [0054] to [0066]; fig. 2 & US 6973022 B1 & WO 1999/044141 A1	1-20

Form PCT/ISA/210 (continuation of second sheet) (July 2009)

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 7508454 B **[0005]**