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(54) A lighting controller

(57) A lighting controller comprises an operating power input for receiving alternating current, a master processor, and one or more slave processors. Each slave processor is configured to use respective switching components to manipulate half-waves of alternating current for outputting a phase-cut alternating current. An internal control bus conveys control commands indicative of desired extent of said manipulating from the master processor to the slave processors. The master processor is configured to time transmissions of control commands on the internal control bus in a predetermined relationship with zero crossing points between half-waves of the alternating current.

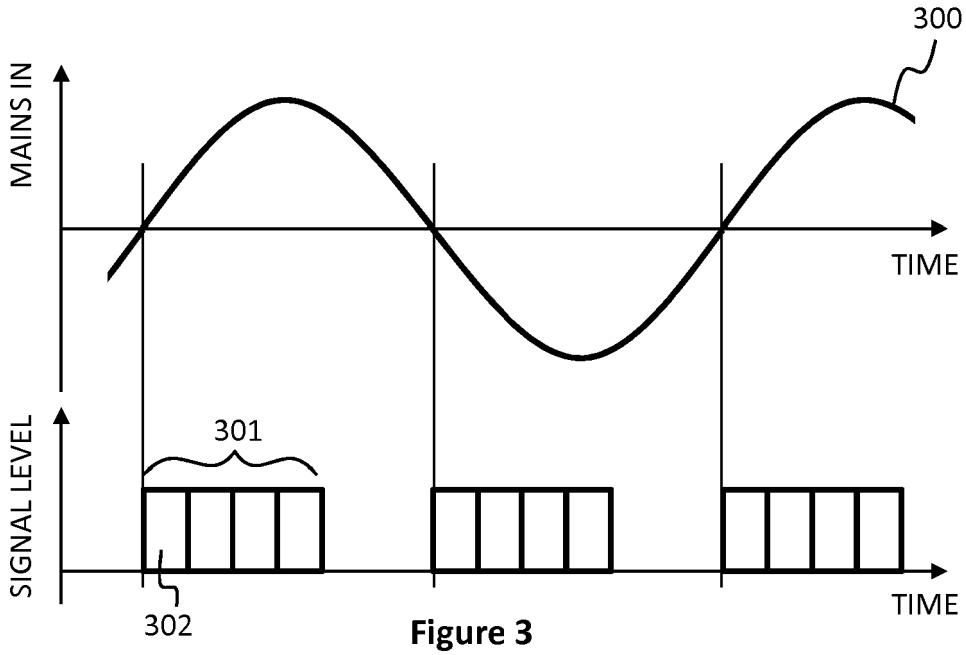

Figure 3

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Description

FIELD OF THE INVENTION

[0001] The invention relates to control of operation of one or more light sources. In particular, embodiments of the invention relate to a lighting controller in which a master processor is able to convey both operating commands and timing information to one or more slave processors that control the delivery of operating power to devices coupled to outputs of the lighting controller. Embodiments of the invention also relate to a method and to a computer program for conveying operating commands and timing information from the master processor to the slave processor(s).

BACKGROUND

[0002] Lighting controllers frequently include processor-controlled multichannel dimmers. A channel means an individual AC output: for example a four-channel dimmer can dim four luminaires or luminaire groups independently of each other. A multichannel dimmer typically comprises a main processor or master, which receives all dimming commands and other commands concerning all channels from for example a human-operated control device, and conveys them further to auxiliary processors or slaves, each of which controls an individual channel. One or more channels may be equipped with on/off switching relays or other means that enable using the lighting controller also for other purposes than just dimming.

[0003] Sometimes one wants to use a channel to dim old-fashioned incandescent lamps or so-called retrofit LED lamps, which are mechanically and electrically compatible with incandescent lamps. For this purpose the output of a channel in the dimmer must comprise suitable switching components that the dimmer can use to phase-cut the output AC, i.e. to cut off a predetermined portion from each AC half-wave. For the phase-cutting to take place appropriately, the slave processor controlling that channel must have at its disposal information about the timing of the AC half-waves. It would naturally be possible to equip each slave processor with its own AC zero crossing detection means, but in order to avoid redundant components in the lighting controller it is common that the master processor (or an indicator circuit associated therewith) finds out the timing of the AC half-waves and conveys this information to the slaves.

[0004] Fig. 1 illustrates a structure of the kind described above in a four-channel dimmer. AC mains come to the MAINS input, from which it is lead to the channel-specific switching components 101, 102, 103, and 104 of all four channels. The lamps to be dimmed are coupled to the outputs of the channels. The master processor 105 receives, through a data connection (CTRL IN), control commands, which it conveys further to the slave processors 111, 112, 113, and 114 according to need. It is possible, although not mandatory, that the control commands go to the slave processors through optoisolators 121, 122, 123, and 124. An example of a control command is a command for a certain channel to dim the produced illumination to a certain percentage of full brightness. After a slave processor has received such a command, it controls the switching components of that channel so that they cut the required portion out of every AC half-wave.

[0005] All processors are able to listen to all commands transmitted in the control bus, but the commands are specified to each slave processor through the use of a suitable communications protocol.

[0006] The exact timing of zero voltage points between AC half-waves is important for the slave processors in driving the switching components correctly. The master processor 105 has a zero voltage detection (ZVD) circuit 106 at its disposal. This circuit measures, when the zero voltage point between half-waves occurs. This timing information should find its way to the slave processors.

[0007] In prior art multichannel dimmers, such as the one in fig. 1, it has been customary to draw a dedicated timing line from the zero voltage detection circuit 106 to the slave processors 111, 112, 113, and 114. If galvanic isolation between channels is desired, dedicated optoisolators 131, 132, 133, and 134 are needed also for the timing line(s). This adds manufacturing costs and may increase the possibilities of malfunctioning.

[0008] Another drawback of prior art lighting controllers of the kind shown in fig. 1 is the jitter that occurs in zero voltage detection. The AC mains voltage that the ZVD circuit 106 monitors contains small-scale interference, which introduces error into finding the exact moment of time when the voltage crosses zero. The jitter in ZVD becomes particularly annoying if the outputs of the lighting control-ler drive LED lights, because these may analyze the length of each half-wave in the AC they receive from the controller and control the brightness of the LEDs accordingly. Jitter in ZVD timing ultimately causes variation in the lighting intensity of the LEDs, which a human observer may consider annoying.

SUMMARY

[0009] Consequently, it is an object of the present invention to provide an internal structure and operating technique of a multichannel lighting controller that is suitable for accurately controlling the switching of AC half-waves in channels of the lighting controller while simultaneously providing reliability and enabling a simple structure that is advantageous to manufacture.

[0010] The objects of the invention are reached by a lighting controller, by a method, and by a computer program as defined by the respective independent claims.

[0011] According to an example embodiment, a lighting controller for driving one or more luminaires is provided. The lighting controller comprises an operating power input for receiving alternating current, a master

processor, one or more slave processors, each said slave processor configured to use respective switching components to manipulate half-waves of said alternating current for outputting a phase-cut alternating current at a respective output of the lighting controller, and an internal control bus for conveying control commands indicative of desired extent of said manipulating from said master processor to said one or more slave processors. Said master processor is configured to time transmissions of said control commands on said internal control bus in a predetermined relationship with zero crossing points between said half-waves of said alternating current.

[0012] According to another example embodiment, a method for producing phase-cut alternating current in a lighting controller is provided. The method comprises:

observing zero crossing points in incoming alternating current,

transmitting control commands from a master processor to a slave processor on an internal control bus of said lighting controller in a predetermined relationship with zero crossing points between half-waves of said alternating current, and

manipulating half-waves of said alternating current under control of said slave processor to produce said phase-cut alternating current, using content of said control commands to determine the extent of said manipulating and using timing of said control commands on said internal bus to determine the timing of said manipulating.

[0013] According to another example embodiment, a computer program is provided for transmitting control commands from a master processor to a slave processor on an internal control bus of a lighting controller. The computer program includes one or more sequences of one or more instructions which, when executed by one or more master processors, cause said one or more master processors to transmit to said slave processor a control command, the content of which determines the extent to which said slave processor should manipulate half-waves of an alternating current to produce a phase-cut alternating current, and the timing of which determines the timing of said manipulating.

[0014] According to another example embodiment, a computer program is provided for manipulating half-waves of alternating current under control of one or more slave processors to produce phase-cut alternating current in a lighting controller. The computer program includes one or more sequences of one or more instructions which, when executed by said one or more slave processors, cause said one or more slave processors to use content of control commands received on an internal control bus of said lighting controller to determine the extent of said manipulating and to use timing of said control commands on said internal bus to determine the timing of said manipulating.

[0015] The computer programs may be embodied on a volatile or a non-volatile computer-readable record medium, for example as a computer program product comprising at least one computer readable non-transitory medium having program code stored thereon, the program code, which when executed by an apparatus, causes the apparatus at least to perform the operations described hereinbefore for the computer program in accordance with an example embodiment.

[0016] The exemplifying embodiments of the invention presented in this patent application are not to be interpreted to pose limitations to the applicability of the appended claims. The verb "to comprise" and its derivatives are used in this patent application as an open limitation that does not exclude the existence of also unrecited features. The features described hereinafter are mutually freely combinable unless explicitly stated otherwise.

[0017] The novel features which are considered as characteristic of the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following detailed description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Figure 1 schematically illustrates a lighting controller according to prior art.

Figure 2 schematically illustrates a lighting controller in accordance with an example embodiment.

Figure 3 illustrates an exemplifying way to time transmissions on a control bus.

Figure 4 illustrates another exemplifying way to time transmissions on a control bus.

Figure 5 illustrates yet another exemplifying way to time transmissions on a control bus.

Figure 6 illustrates an example of details in a master processor.

Figure 7 illustrates an example of details in a slave processor.

Figure 8 illustrates an example of a method.

Figure 9 illustrates an example of details of a method.

Figure 10 illustrates another example of details of a

method.

DESCRIPTION OF SOME EMBODIMENTS

[0019] Figure 2 schematically illustrates an exemplifying lighting controller 200 suitable for example for providing controlled operating power to four dimmable luminaires or luminaire groups. Also other kinds of loads can be coupled to the outputs of the four channels of the lighting controller 200. Displaying four outputs in the example embodiment is not a limiting feature; the same structural and functional solutions are easily generalized to any number of output channels.

[0020] For receiving alternating current the lighting controller 200 comprises an operating power input, which in fig. 2 appears with a reference designator MAINS IN. Switching components 101, 102, 103, 104 are provided at each channel for outputting manipulated half-waves of the alternating current, for example phase-cut alternating current. At each channel a slave processor 211, 212, 213, 214 is configured to control and use the respective switching components.

[0021] The lighting controller 200 comprises a master processor 205 and an internal control bus 206 for conveying, from the master processor 205 to the slave processors 211, 212, 213, 214, control commands indicative of desired type and extent of manipulating that the slave processors should do to the half-waves output from their respective channels. In other words, for example if trailing edge type phase-cut AC should be obtained from channel 1, with 60% of the length of each half-wave remaining, the master processor 205 uses the internal control channel 206 to send to the slave processor 211 of the first channel a control command, which the slave processor 211 interprets as an instruction to implement phase cutting of said kind.

[0022] Optoisolators 121, 122, 123, 124 may be provided to galvanically isolate the slave processors 211, 212, 213, 214 from the internal control bus 206, but these are not necessary, if galvanic isolation between channels is not needed in the lighting controller 200.

[0023] As a difference to the lighting controller according to prior art that was explained previously with reference to fig. 1, the lighting controller 200 does not comprise a separate timing line to the slave processors 211, 212, 213, 214. The master processor 205 is configured to time transmissions of control commands on the internal control bus 206 in a predetermined relationship with zero crossing points between half-waves of the alternating current. The master processor 205 may become aware of the timing of said zero crossing points for example through a zero voltage detection (ZVD) circuit 207 that is coupled between the AC lines and the master processor 205 within the lighting controller 200. As an alternative, there could be a ZVD circuit external to the lighting controller, with a coupling from such an external ZVD circuit to the master processor 205.

[0024] Fig. 3 illustrates an example embodiment of timing transmissions of control commands in the internal control bus 206 in a predetermined relationship with zero crossing points between half-waves in the alternating current 300. In particular, in the example illustrated in fig. 3, the master processor is configured to transmit the control commands on the internal control bus in frames, of which frame 301 is an example. Three vertical lines illustrate the location of zero crossing points on the time axis in fig. 3. A predetermined part, here the beginning, of each transmitted frame coincides in time with a zero crossing point between half-waves in the alternating current 300. The part of each frame that coincides in time with a zero crossing point could also be the end of the frame, or some reference point between the beginning and the end of the frame.

[0025] Another example of a feature that is schematically illustrated in fig. 3 is the use of slave-processor-specific time slots. In the example of fig. 2 the lighting controller has four slave processors, so in a corresponding way each frame in fig. 3 has four slave-processor-specific time slots, of which slot 302 of frame 301 is shown as an example. In this example the master processor is configured to transmit control commands to a particular slave processor in a slave-processor-specific time slot of the frames. Each slave processor has been programmed to handle a received frame appropriately, so that the slave processor knows to read control commands destined to itself from the correct time slot in the frame, while simultaneously using the predetermined part of the frame - e.g. the beginning - as an indication of the timing of a zero crossing point in the alternating current.

[0026] Fig. 4 illustrates another example embodiment of timing transmissions of control commands in the internal control bus 206 in a predetermined relationship with zero crossing points between half-waves in the alternating current 300. In particular, in the example illustrated in fig. 4, the master processor is configured to transmit the control commands on the internal control bus one at a time, so that a predetermined part of each transmitted individual control command coincides in time with a zero crossing point between half-waves in the alternating current. An individual control command 401 is shown as an example. It consists of a header part 402 and a payload part 403. In the header part 402 the master processor inserts a recipient identifier, which tells, to which slave processor the control command is meant. In the payload part 403 the master processor inserts the actual content of the control command.

[0027] A common feature to the examples shown in figs. 3 and 4 is that the master processor is configured to transmit each frame (in the embodiment of fig. 3) or each individual control command (in the embodiment of fig. 4) in a time that is shorter than a half-wave in the alternating current 300. In particular, the embodiment of fig. 3 involves the advantage that a new control command can be transmitted to each slave processor once during each half-wave period. Taken that the slave processors

will use their respective switching components to manipulate the alternating current on a half-wave-wise basis, it is not likely that more frequent delivery of control commands to slave processors than once per half-wave length would be necessary. It is, however, possible to make the transmission of control commands even more frequent, for example so that the master processor transmits a whole frame - with a dedicated time slot for each slave processor - two times, three times or even more frequently during each half-wave period.

[0028] Fig. 5 illustrates an example embodiment that goes towards the other extreme, i.e. transmitting a frame 501 that is longer than a half-wave period in the alternating current. A slave-processor-specific time slot 502 is shown as an example. The embodiment of fig. 5 involves the advantage of particularly large capacity for transmitting even very long and complicated control commands to the slave processors without requiring the control command transmission and reception arrangements to be capable of very fast signal processing. However, the embodiment of fig. 5 requires programming the slave processors so that they know, how many zero crossing points will occur between the beginnings (or other predetermined parts) of two consecutive frames, so that they can maintain an appropriate time base for switching.

[0029] Fig. 6 illustrates details of an example embodiment in which the master processor 205 digitally filters the ZVD signals. The lighting controller comprises a zero voltage detector (ZVD) 207 that is configured to produce an indication signal, like a transition between two digital states, indicating when a zero crossing point occurs between half-waves in the alternating current. The master processor 205 is configured to digitally filter a sequence of indication signals produced by the ZVD 207 to produce a digitally filtered zero crossing time base.

[0030] The reason for applying digital filtering is the possible occurrence of jitter in the output of the ZVD 207. The alternating current, the zero crossing points of which should be detected, should ideally be a smooth, clean sine wave, the zero crossing points of which occur at exactly constant time intervals. In reality, imperfections in the generation and delivery of mains AC cause the indications of zero crossing points to be generated at more or less irregular intervals. Switching in a lighting controller should follow possible slow, long-term variations in the timing of zero-crossing points, so that it does not develop any significant timing bias but remains synchronized with the general rhythm of the half-waves in the alternating current. However, rapid variations in the timing of zero-crossing points (and hence also in the sequence of indication signals output by the ZVD 207) are typically caused by random interference, the effect of which should cancel out in the long term.

[0031] The digital filtering applied by the master processor 205 has the nature of lowpass filtering, and it serves to remove the effect of rapid random variations in the time intervals between consecutive indication signals output by the ZVD 207. A digital filtering block 601 is schematically shown in fig. 6. It takes the sequence of indication signals received from the ZVD 207, performs low pass filtering, and outputs a digitally filtered zero crossing time base.

[0032] Other parts or functionalities of the master processor 205 that are shown in fig. 6 are the control command receiver 602 for receiving control commands through an auxiliary bus, a processing part 603 for interpreting the auxiliary control commands, a command forming part 604 for forming the control commands to be sent to the slave processors, and a control command transmitter 605 for transmitting control commands on the internal bus 206. Corresponding functionalities were known in prior art master processors, and do not need to be described here further. As a difference to prior art solutions, the control command transmitter 605 is configured to time transmissions of the control commands on said internal control bus in a predetermined relationship with the digitally filtered zero crossing time base that is available at the output of the digital filtering block 601.

[0033] The invention does not require digitally filtering the zero crossing point indications, if it can be otherwise ensured that these indications are sufficiently free of short-term interference. Even if filtering is performed, it is not necessary to do it in the master processor. Fig. 7 illustrates schematically some parts of an example of a slave processor 211. A control command receiver 701 is configured to receive control commands on the internal control bus 206 of the lighting controller. An optoisolator may be employed at the input of the control command receiver 701, but is not separately shown in fig. 7. The handling of received control commands takes place in two branches. In fig. 7 it is assumed that the master processor did not perform digital filtering of the indication signals produced by the ZVD circuit, for which reason a digital filtering block 703 exists in the slave processor 211. If the master processor already included digital filtering, block 703 can be omitted and the timing of the received control commands is directly taken to block 704, which uses it to maintain the time base for switching in the slave processor 211.

[0034] The content of the received control commands is interpreted in a part of the slave processor 211 that is schematically illustrated as the processing block 702. Switching signals are formed correspondingly in block 706, with their timing synchronized to the time base maintained in block 704, and given to one or more switch driver circuits 707 that perform the actual driving of the MOSFETs or other switches through which the alternating current flows to the output of the corresponding channel.

[0035] Block 703 in fig. 7 and block 601 are basically alternatives to each other, although it is not excluded to divide the digital filtering of the zero crossing indications into two. In that case the master processor would perform coarse filtering and the slave processor would finalize the effect of filtering, including the removal of possible additional jitter that could have been caused by imper-

fections in timing the transmission of control commands on the internal control bus.

[0036] Fig. 8 illustrates a method for producing phase-cut alternating current in a lighting controller according to an example embodiment. Step 801 represents receiving alternating current in the lighting controller. Step 802 represents observing zero crossing points in the incoming alternating current, and step 803 represents transmitting control commands from a master processor to a slave processor on an internal control bus of the lighting controller in a predetermined relationship with zero crossing points between half-waves of said alternating current. Here the predetermined relationship means particularly a relationship in time, so that the timing of control commands transmitted on the internal control bus serves as an indication of the timing of detected zero crossing points.

[0037] Step 804 in fig. 8 represents receiving the control commands in a slave processor of the lighting controller. Step 805 represents manipulating half-waves of the alternating current under control of the slave processor to produce phase-cut alternating current. The slave processor uses content of the control commands to determine the extent of said manipulating, and timing of the control commands on said internal bus to determine the timing of said manipulating. Step 806 represents outputting the resulting phase-cut alternating current from the lighting controller.

[0038] The transmission of control commands at step 803 may take place in frames, so that a predetermined part of each transmitted frame coincides in time with a zero crossing point between half-waves in the alternating current. In such an embodiment control commands to a particular slave processor may be transmitted in a slave-processor-specific time slot of the frames. As an alternative, the transmission of control commands at step 803 may take place one at a time, so that a predetermined part of each transmitted individual control command coincides in time with a zero crossing point between half-waves in the alternating current. Irrespective of which of these alternatives is used, each transmission on the internal control bus may be shorter than a half-wave in the alternating current.

[0039] Figs. 9 and 10 show how the method may comprise digitally filtering a sequence of indication signals indicating when zero crossing points occur between half-waves of said alternating current, thus producing a digitally filtered zero crossing time base, and using the digitally filtered zero crossing time base to determine the timing of said manipulating. In the embodiment illustrated in fig. 9 digital filtering 902 takes place in the master processor, between the steps of observing 901 zero crossing points in the incoming alternating current and transmitting 903 control commands from the master processor to the slave processor on the internal control bus. These are shown with different reference designators than in fig. 8 because the digital filtering at step 902 may imply changes to the other steps; for example, the detection of zero crossing points at step 901 may be originally accomplished at a lower level of accuracy (i.e. with cheaper components) if the filtering at step 902 can be relied upon to remove any resulting jitter.

[0040] In the embodiment illustrated in fig. 10 digital filtering 1002 takes place in the slave processor between the steps of receiving 1001 control commands from the master processor and manipulating 1003 half-waves of the alternating current under control of the slave processor to produce phase-cut alternating current.

[0041] Computer programs according to various embodiments can be classified into computer programs of the master processor and computer programs of the slave processor. Computer programs of the first kind include one or more sequences of one or more instructions which, when executed by one or more master processors, cause said one or more master processors to transmit to a slave processor a control command, the content of which determines the extent to which said slave processor should manipulate half-waves of an alternating current to produce a phase-cut alternating current, and the timing of which determines the timing of said manipulating. They may also comprise one or more sequences of one or more instructions which, when executed by said one or more master processors, cause said one or more master processors to digitally filter a received sequence of indications indicating when zero crossing points occur between half-waves in said alternating current, thus producing a digitally filtered zero crossing time base, and to time transmissions of control commands on said internal control bus in a predetermined relationship with said digitally filtered zero crossing time base.

[0042] Computer programs of the slave processor include one or more sequences of one or more instructions which, when executed by one or more slave processors, cause said one or more slave processors to use content of control commands received on an internal control bus of the lighting controller to determine the extent of manipulating half-waves of an alternating current to produce a phase-cut alternating current, and to use timing of said control commands on said internal bus to determine the timing of said manipulating.

[0043] Reference to a processor should not be understood to encompass only programmable processors, but also dedicated circuits such as field-programmable gate arrays (FPGA), application specific circuits (ASIC), signal processors, etc. Features described in the preceding description may be used in combinations other than the combinations explicitly described. Although functions have been described with reference to certain features, those functions may be performable by other features whether described or not. Although features have been described with reference to certain embodiments, those features may also be present in other embodiments whether described or not.

Claims

1. A lighting controller for controlling one or more light sources, the lighting controller comprising:

   an operating power input for receiving alternating current,
   a master processor,
   one or more slave processors, each said slave processor configured to use respective switching components to manipulate half-waves of said alternating current for outputting a phase-cut alternating current at a respective output of the lighting controller, and
   an internal control bus for conveying control commands indicative of desired extent of said manipulating from said master processor to said one or
   more slave processors;

   wherein said master processor is configured to time transmissions of said control commands on said internal control bus in a predetermined relationship with zero crossing points between said half-waves of said alternating current.

2. A lighting controller according to claim 1, wherein said master processor is configured to transmit said control commands on said internal control bus in frames, so that a predetermined part of each transmitted frame coincides in time with a zero crossing point between half-waves in said alternating current.

3. A lighting controller according to claim 2, wherein said master processor is configured to transmit control commands to a particular slave processor in a slave-processor-specific time slot of the frames.

4. A lighting controller according to claim 1, wherein said master processor is configured to transmit said control commands on said internal control bus one at a time, so that a predetermined part of each transmitted individual control command coincides in time with a zero crossing point between half-waves in said alternating current.

5. A lighting controller according to any of claims 1 to 4, wherein:

   said master processor is configured to transmit each frame or each individual control command in a time that is shorter than a half-wave in said alternating current.

6. A lighting controller according to any of claims 1 to 5, wherein:

   the lighting controller comprises a zero voltage detector configured to produce an indication signal indicating when a zero crossing point occurs between half-waves in said alternating current,
   said master processor is configured to digitally filter a sequence of indication signals produced by said zero-voltage detector to produce a digitally filtered zero crossing time base, and
   said master processor is configured to time transmissions of said control commands on said internal control bus in a predetermined relationship with said digitally filtered zero crossing time base.

7. A method for producing phase-cut alternating current in a lighting controller, comprising:

   observing zero crossing points in incoming alternating current,
   transmitting control commands from a master processor to a slave processor on an internal control bus of said lighting controller in a predetermined relationship with zero crossing points between half-waves of said alternating current, and
   manipulating half-waves of said alternating current under control of said slave processor to produce said phase-cut alternating current, using content of said control commands to determine the extent of said manipulating and using timing of said control commands on said internal bus to determine the timing of said manipulating.

8. A method according to claim 7, wherein said control commands are transmitted on said internal control bus in frames, so that a predetermined part of each transmitted frame coincides in time with a zero crossing point between half-waves in said alternating current.

9. A method according to claim 8, wherein control commands to a particular slave processor are transmitted in a slave-processor-specific time slot of the frames.

10. A method according to claim 7, wherein said control commands are transmitted on said internal control bus one at a time, so that a predetermined part of each transmitted individual control command coincides in time with a zero crossing point between half-waves in said alternating current.

11. A method according to any of claims 7 to 10, wherein each transmission on said internal control bus is shorter than a half-wave in said alternating current.

12. A method according to any of claims 7 to 11, comprising:

digitally filtering a sequence of indication signals indicating when zero crossing points occur between half-waves of said alternating current, thus producing a digitally filtered zero crossing time base, and

using the digitally filtered zero crossing time base to determine the timing of said manipulating.

13. A computer program for transmitting control commands from a master processor to a slave processor on an internal control bus of a lighting controller, the computer program including one or more sequences of one or more instructions which, when executed by one or more master processors, cause said one or more master processors to transmit to said slave processor a control command, the content of which determines the extent to which said slave processor should manipulate half-waves of an alternating current to produce a phase-cut alternating current, and the timing of which determines the timing of said manipulating.

14. A computer program according to claim 13, comprising one or more sequences of one or more instructions which, when executed by said one or more master processors, cause said one or more master processors to:

digitally filter a received sequence of indications indicating when zero crossing points occur between half-waves in said alternating current, thus producing a digitally filtered zero crossing time base, and

time transmissions of said control command on said internal control bus in a predetermined relationship with said digitally filtered zero crossing time base.

15. A computer program for manipulating half-waves of alternating current under control of one or more slave processors to produce phase-cut alternating current in a lighting controller, the computer program including one or more sequences of one or more instructions which, when executed by said one or more slave processors, cause said one or more slave processors to use content of control commands received on an internal control bus of said lighting controller to determine the extent of said manipulating and to use timing of said control commands on said internal bus to determine the timing of said manipulating.

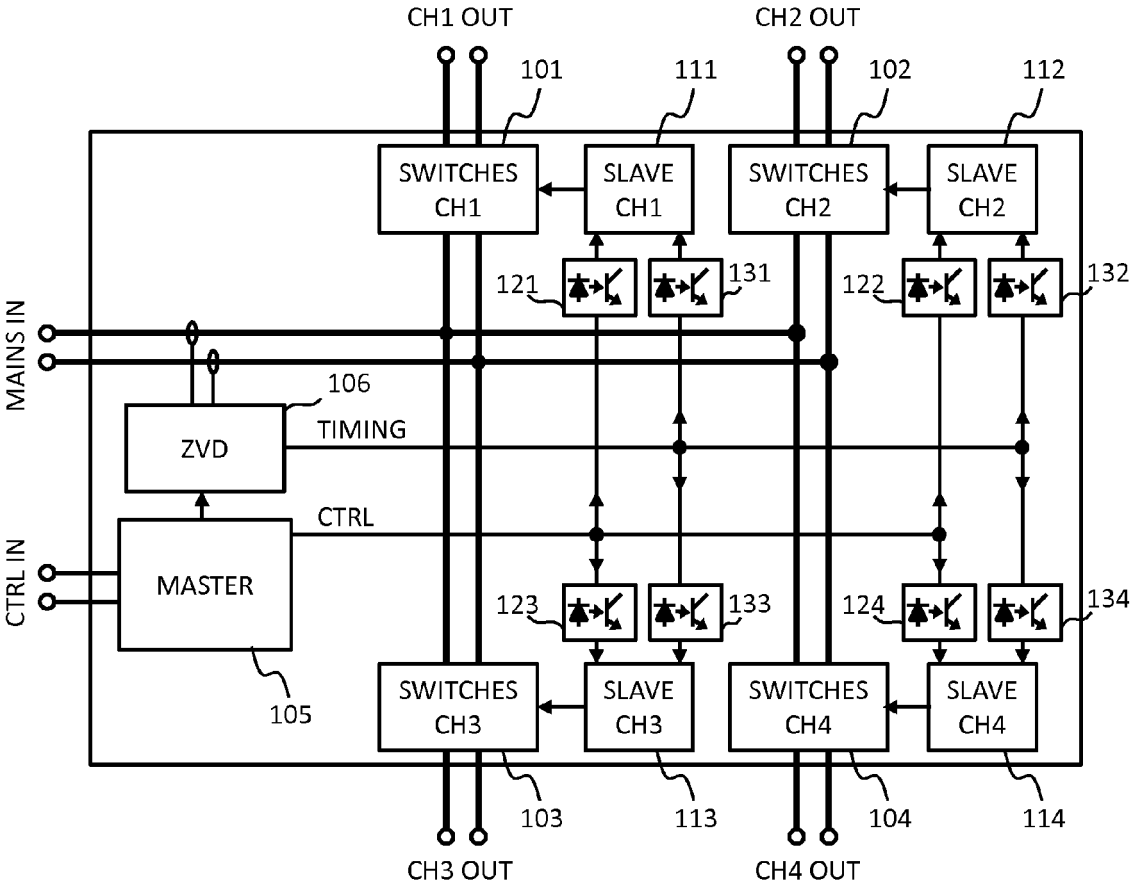
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Figure 1

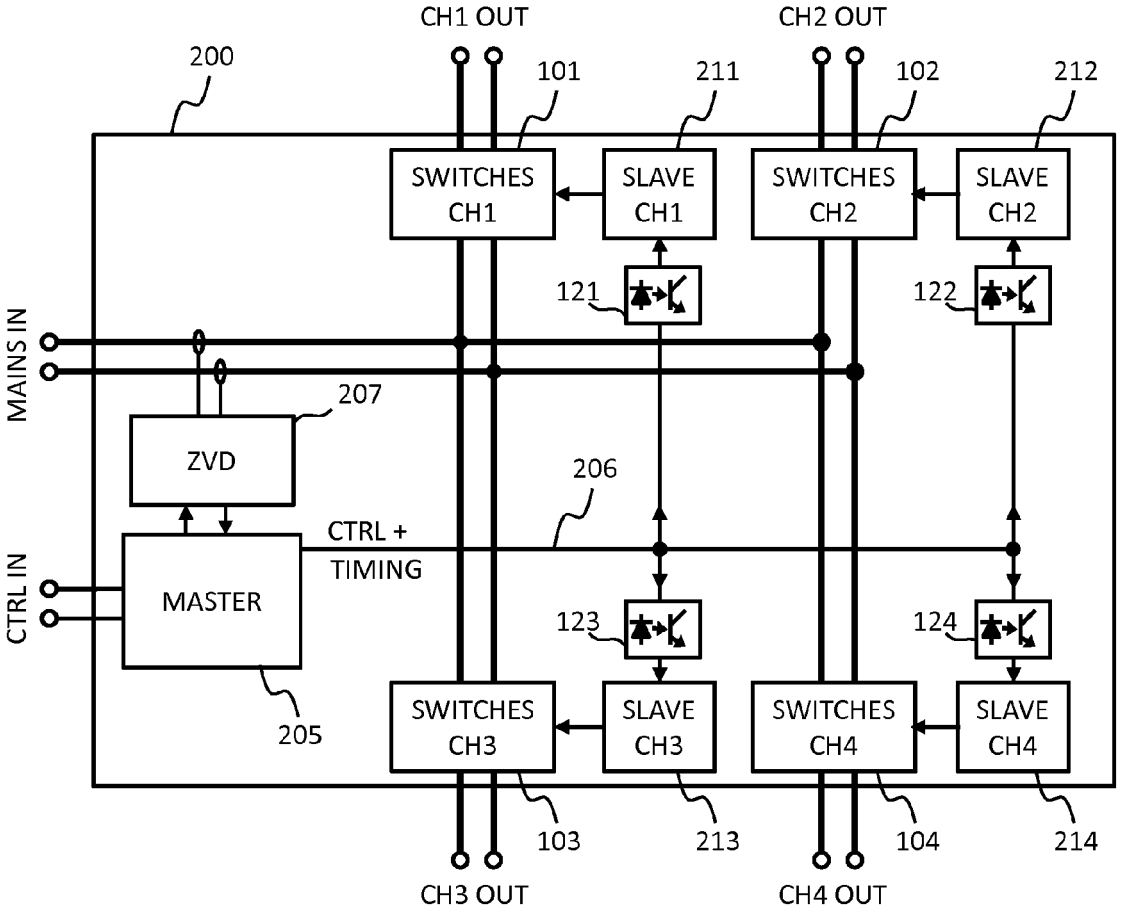

Figure 2

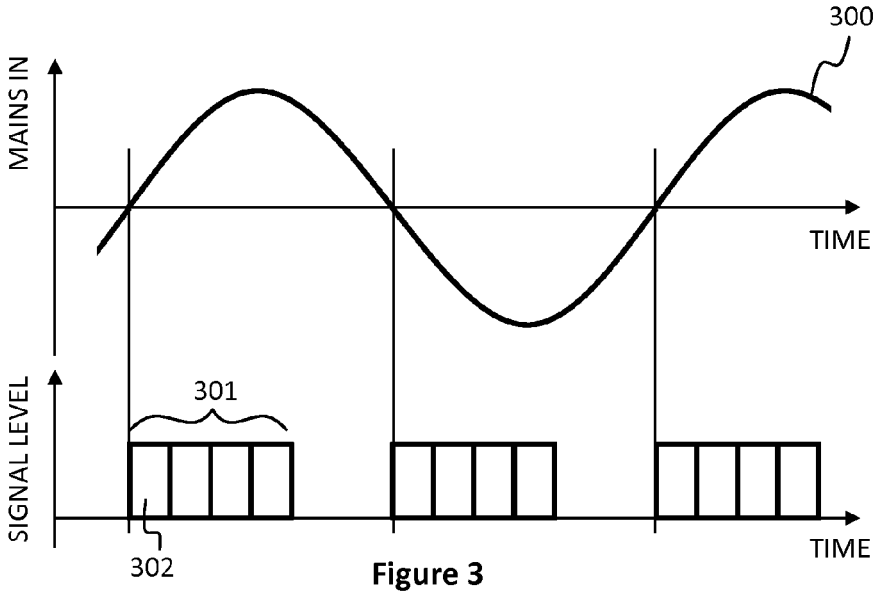

Figure 3

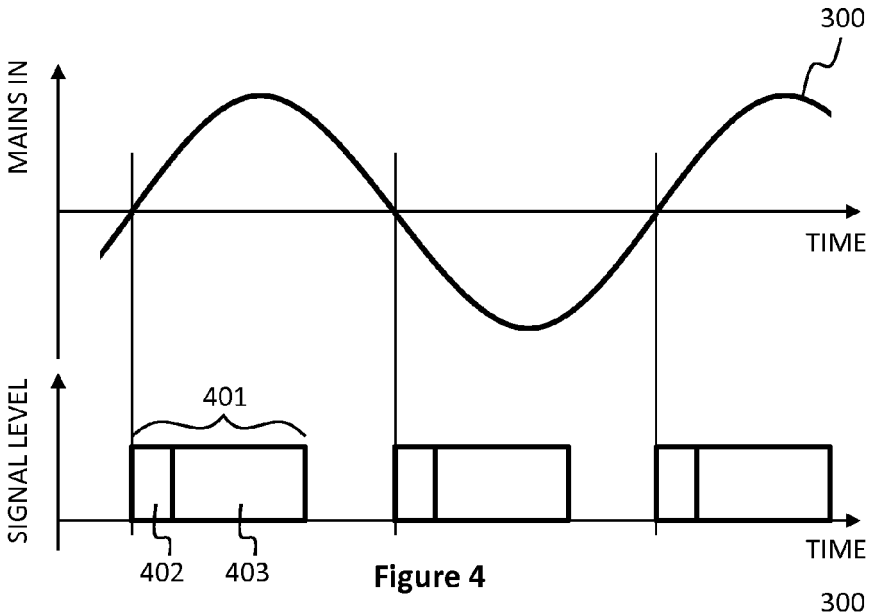

Figure 4

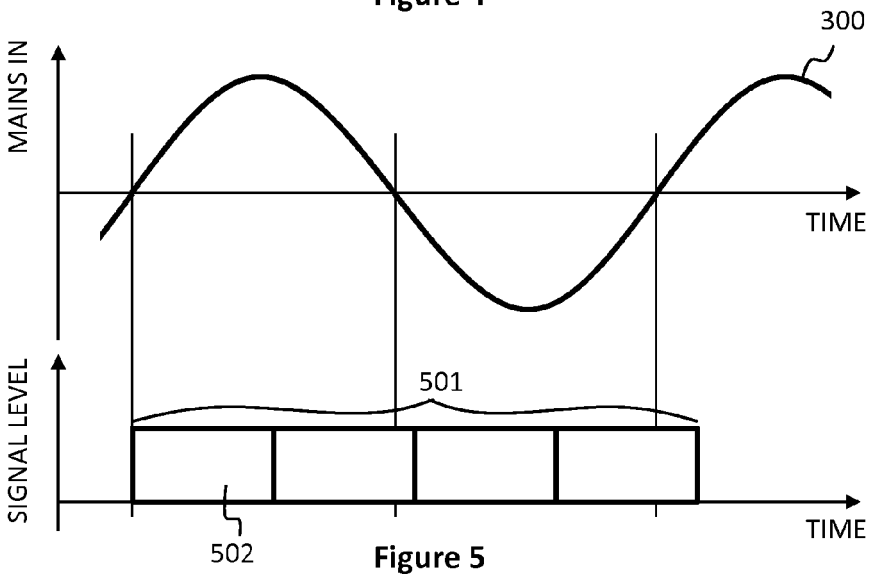

Figure 5

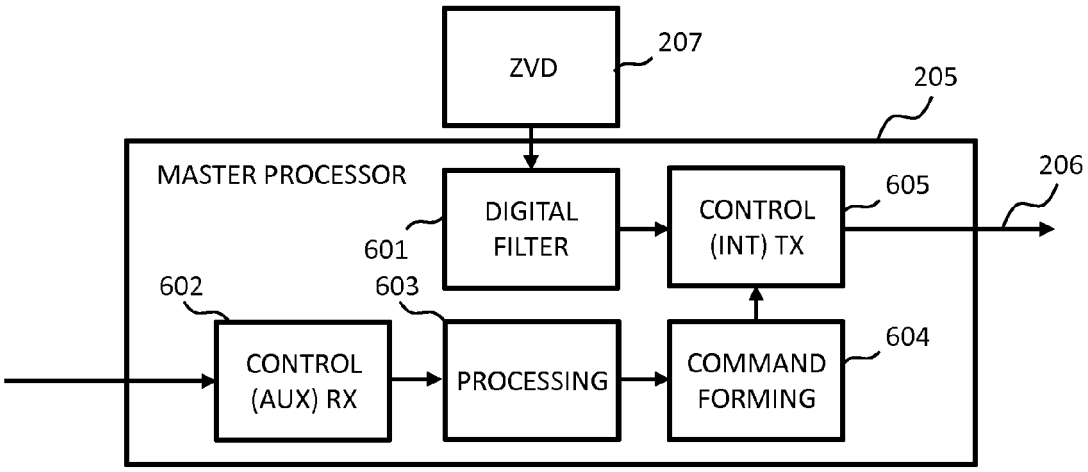

Figure 6

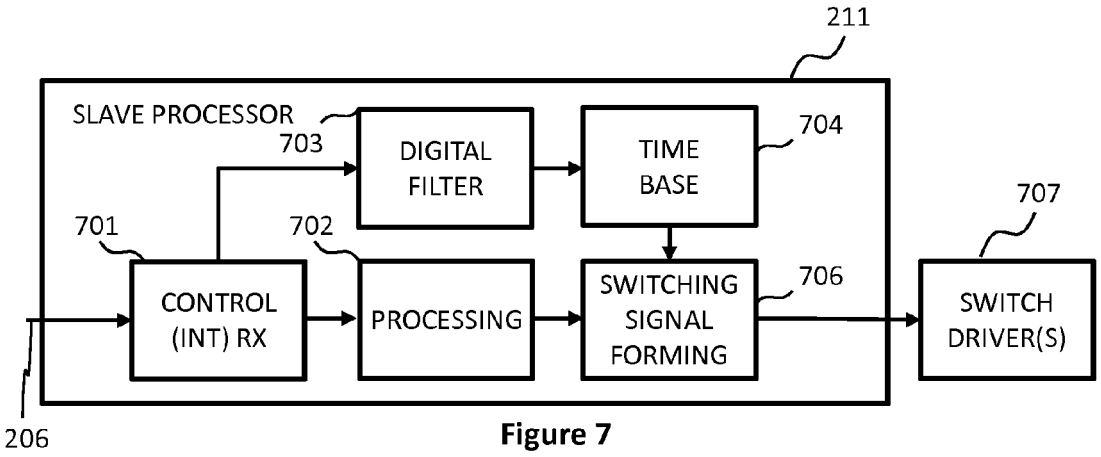

Figure 7

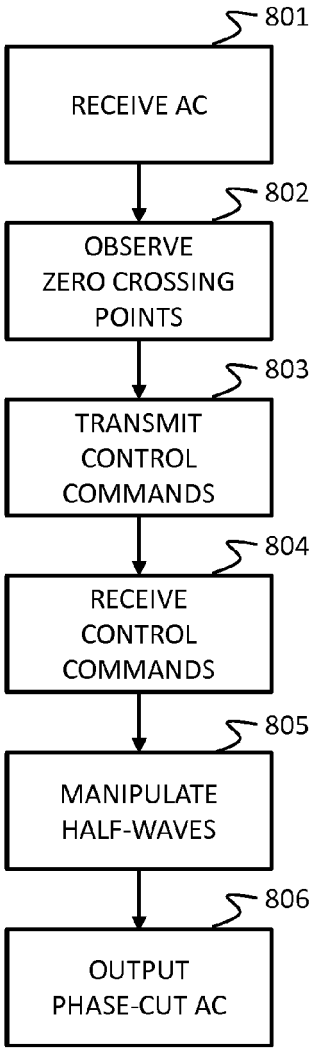

Figure 8

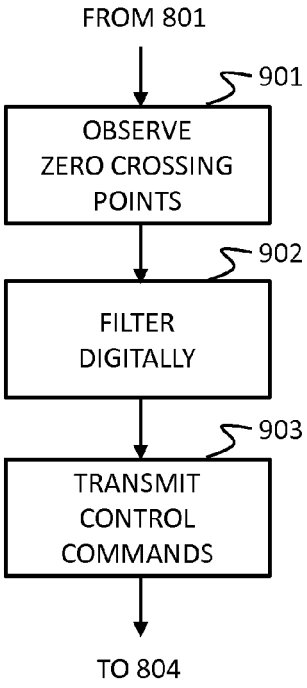

Figure 9

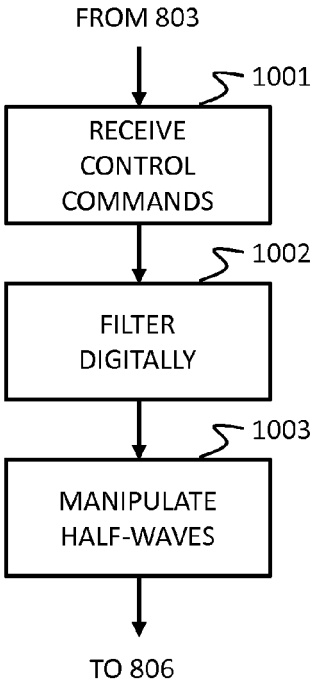

Figure 10

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EUROPEAN SEARCH REPORT

Application Number
EP 14 16 2186

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	JP 2014 003600 A (YOSHIKAWA RF SEMICON CO LTD) 9 January 2014 (2014-01-09) * the whole document *	1-15	INV. H05B37/02
X	WO 2013/061206 A2 (KONINKL PHILIPS ELECTRONICS NV [NL]) 2 May 2013 (2013-05-02)	1-5, 7-11,13, 15	
A	* abstract; figures 1-6 * * page 1, paragraph 1 * * page 2, paragraph 2 - page 7, paragraph 2 * * page 10, paragraph 1 - page 20, paragraph 1 *	6,12,14	
X	EP 0 390 035 A2 (TOSHIBA LIGHTING & TECHNOLOGY [JP]) 3 October 1990 (1990-10-03)	1-5, 7-11,13, 15	
A	* column 1, lines 1-6; figures 1-6, 9-11 * * column 3, line 35 - column 5, line 32 * * column 6, line 17 - column 9, line 10 *	6,12,14	
X	US 5 825 135 A (CHANG CHIN-HSIUNG [TW]) 20 October 1998 (1998-10-20)	1-5, 7-11,13, 15	TECHNICAL FIELDS SEARCHED (IPC) H04B H05B H02M
A	* column 1, lines 6-10; figures 3, 4 * * column 3, lines 14-52 *	6,12,14	
A	EP 2 621 248 A1 (SI GI IMPIANTI ELETTRICI DI SILENZI GIANLUCA E SIMONE S N C [IT]) 31 July 2013 (2013-07-31) * figures 5-7 *	1-15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	3 September 2014	Brosa, Anna-Maria

CATEGORY OF CITED DOCUMENTS

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03-09-2014

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2014003600 A	09-01-2014	JP 2014003600 A	09-01-2014
		WO 2013175810 A1	28-11-2013
WO 2013061206 A2	02-05-2013	EP 2749140 A2	02-07-2014
		US 2013141015 A1	06-06-2013
		WO 2013061206 A2	02-05-2013
EP 0390035 A2	03-10-1990	EP 0390035 A2	03-10-1990
		JP H02256193 A	16-10-1990
		US 5019747 A	28-05-1991
US 5825135 A	20-10-1998	NONE	
EP 2621248 A1	31-07-2013	NONE	

EPO FORM P0459

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