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(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

VERFAHREN ZUR HERSTELLUNG EINES HALBLEITERBAUELEMENTS

PROCÉDÉ DE FABRICATION D'UN DISPOSITIF À SEMI-CONDUCTEURS

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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device manufacturing method.

BACKGROUND ART

[0002] As a semiconductor device used for power semiconductor devices, diodes and IGBTs (Insulated Gate Bipolar Transistor) having a withstand voltage of 400V, 600 V, 1200V, 1700V, 3300V or more are known. These diodes and IGBTs are used for power conversion devices, such as convertors and invertors, and are demanded to have low loss, low noise and high breakdown tolerance, as well as low cost. As an example of the semiconductor device used for power semiconductor devices, a pin (p-intrinsic-n) diode will be described.

[0003] Fig. 36 is a cross-sectional view depicting a key portion of a conventional diode. As illustrated in Fig. 36, in the conventional diode, a p-type layer (not illustrated) is selectively disposed on a front surface side of an n^--type semiconductor substrate to be an n^--type drift layer 101, and in the p-type layer, a p-type anode layer 102 is selectively disposed, and a termination withstand voltage structure is disposed on a periphery surrounding the p-type anode layer 102.

[0004] On the rear surface side of the n^--type semiconductor substrate, an n^+-type cathode layer 104 is disposed in a position on the opposite side of the p-type anode layer 102. The reference numeral 103 denotes an anode electrode, and 105 denotes a cathode electrode.

[0005] In the case of the conventional diode, a reverse recovery loss is reduced by introducing heavy metal or defects into the n-type drift layer 101, so that the carrier lifetime of the n^--type drift layer 101 is decreased, and annihilation of the carriers is quickened during reverse recovery. At this time, if a carrier lifetime distribution, in which the carrier lifetime on the cathode side of the n^--type drift layer 101 is longer than the carrier lifetime on the anode side, is created, reverse recovery current/voltage waveforms, where oscillation of current/voltage waveforms during reverse recovery or surge (current generated by a transition abnormal voltage) due to oscillation of voltage waveforms are hardly generated and recovery is soft, can be obtained.

[0006] According to a proposed semiconductor device, in which the carrier lifetime is controlled like this, (e.g. Patent Document 1 (paragraph 0037)), defects, which were formed in the drift region when hydrogen ions are irradiated from the rear surface of the silicon substrate, have a peak in a position deeper than the intermediate depth of the drift region from the substrate front surface, and recombination of the carriers in a position deeper than the intermediate depth of the drift region from the substrate front surface is accelerated, whereby the carrier lifetime control function is implemented.

[0007] According to another proposed device (e.g. Patent Document 2), lifetime of carriers near the pn junction between the p-type anode layer and the n^--type drift layer and the lifetime of carriers near the n^-n^+ junction between the n^--type drift layer and the n^+-type cathode layer in the n^--drift layer are controlled by a double sided irradiation or protons, or by a double irradiation of protons and electron beams, so that the lifetime of carriers near the pn junction is controlled to be shorter than the lifetime of carriers near the n^-n^+ junction

[0008] Further, Patent Document 3 discloses a semiconductor device having an MOS gate structure comprising an N^- drift layer, a field stop layer, a P collector layer, a collector electrode, a P base layer, an N^+ emitter region, a gate insulating film, and a gate electrode, and an emitter electrode. A Frenkel defect of higher than heat balancing density is introduced in the N^- drift layer and the sum of the lifetime of electrons and the lifetime of holes in the N^- drift layer 1 is 0.1 to 60 μs. Further, the sum of the depth-directional thickness of the N^- drift layer and the depth-directional thickness of the field stop layer is smaller than the diffusion length of electrons and holes when the Frenkel defect density of the N^- drift layer is the heat balancing density.

[0009] Further, Patent Document 4 discloses a method for producing a semiconductor device including an implantation step of performing proton implantation from a rear surface of a semiconductor substrate of a first conductivity type and a formation step of performing an annealing process for the semiconductor substrate in an annealing furnace to form a first semiconductor region of the first conductivity type which has a higher impurity concentration than the semiconductor substrate after-the implantation step. In the formation step, the furnace is in a hydrogen atmosphere and the volume concentration of hydrogen is in the range of 6% to 30%.

Patent Document 1: Japanese Patent Application Laid-open No. 2011-049300
Patent Document 2: Japanese Patent Application Laid-open No. H08-102545
Patent Document 3: JP 2008 211148 A
Patent Document 4: EP 2 793 251 A1

DISCLOSURE OF THE INVENTION

[0010] There is a method for obtaining the above mentioned predetermined carrier lifetime distribution by selectively irradiating such light ions as helium (He) and protons onto the anode side of the n^--type drift layer and decreasing the lifetime of the carriers in a portion where the light ions are irradiated, but in this case, the light ion irradiation device itself is expensive, which increases the manufacturing cost, and leak current may increase. It is also possible to locally decrease the carrier lifetime by dispersion of heavy metal, such as platinum (Pt), but problems are that the temperature characteristic of the reverse recovery current-voltage (I-V) curve becomes negative, and a dedicated manufacturing line is required to prevent heavy metal contamination.

[0011] One method for controlling a lifetime of carriers at low cost, without generating problems resulting from light ion irradiation and heavy metal diffusion, is decreasing the lifetime of carriers by generating defects in the semiconductor substrate by electron beam irradiation. However, in the case of electron beam irradiation which has high acceleration energy, an electron beam transmits through the semiconductor substrate, and the carrier lifetime becomes uniform. If the acceleration energy is decreased by locally decreasing the carrier lifetime, defects may not be generated because the mass of electrons is small. Thus in the case of electron beam irradiation, it is difficult to selectively form defects in the semiconductor substrate and locally control the carrier lifetime.

[0012] To solve the problems of the prior art described above, it is an object of the present invention to provide a semiconductor manufacturing method that can locally control carrier lifetime at low cost without increasing leak current or contaminating the manufacturing line.

[0013] To solve the above mentioned problems and to achieve the object of the present invention, a semiconductor device manufacturing method according to the present method is a semiconductor device manufacturing method in which the lifetime of carriers is locally controlled, and has the characteristics as further specified in claim 1.

[0014] The semiconductor device manufacturing method according to the present invention is characterized in that the lifetime of the carriers in a region which is depleted during ON time is increased in the first implantation step.

[0015] To solve the above mentioned problems and achieve the object of the present invention, defects are formed in a semiconductor substrate by dangling bonds generated by breaking of inter-atomic bonds of atoms constituting the semiconductor substrate. A high hydrogen concentration region, of which hydrogen concentration is higher than a front surface side of the semiconductor substrate, is formed in a surface layer of a rear surface of the semiconductor substrate by introducing hydrogen atoms. In the high hydrogen concentration region, defects are less than those on the front surface side of the semiconductor substrate, and the lifetime of the carriers is longer than that on the front surface side of the semiconductor substrate.

[0016] The semiconductor device is characterized in that the above mentioned invention further includes a second conductivity type layer which is formed on the front surface of the semiconductor substrate, and a first conductivity type layer which is formed on the rear surface of the first conductivity type semiconductor substrate.

[0017] The semiconductor device is characterized in that the hydrogen concentration in the high hydrogen concentration region is higher than the hydrogen concentration of bulk single crystals.

[0018] According to the above mentioned invention, the defects are formed throughout the semiconductor substrate by electron beam irradiation, and then the defects on the substrate rear surface side are locally recovered by the hydrogen ion implantation from the substate rear surface, whereby the carrier lifetime on the substrate rear surface side can be made longer than the carrier lifeline on the substrate front surface side. Therefore even if the carrier lifetime control is performed using electron beam irradiation, the carrier lifetime can be locally controlled.

[0019] According to the semiconductor device manufacturing method of the present invention, carrier lifetime can be locally controlled at low cost without increasing leak current or contaminating the manufacturing line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Fig. 1 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 1;

Fig. 2 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 3 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 4 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 5 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 6 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 7 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 1;

Fig. 8A is a characteristic diagram depicting an impurity concentration distribution of the semiconductor device according to Embodiment 1;

Fig. 8B is a characteristic diagram depicting an impurity concentration distribution of the semiconductor device according to Embodiment 1;

Fig. 9 is a characteristic diagram depicting the hydrogen dose dependency of the ON voltage of the semiconductor device according to Embodiment 1;

Fig. 10 is a characteristic diagram depicting the hydrogen dose dependency of the reverse recovery waveform of the semiconductor device according to Embodiment 1;

Fig. 11 is a flow chart depicting an overflow of a semiconductor device manufacturing method according to Embodiment 2;

Fig. 12A is a characteristics diagram depicting the impurity concentration distribution of the semiconductor device according to Embodiment 2;

Fig. 12B is a characteristics diagram depicting the impurity concentration distribution of the semiconductor device according to Embodiment 2;

Fig. 13 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 3;

Fig. 14 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 4;

Fig. 15 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 5;

Fig. 16 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 6;

Fig. 17 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 7;

Fig. 18 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 19 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 20 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 21 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 22 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 23 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 24 is a cross-sectional view depicting a state during manufacturing the semiconductor device according to Embodiment 7;

Fig. 25 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 8;

Fig. 26 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 9;

Fig. 27 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 10;

Fig. 28 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 11;

Fig. 29A is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 12;

Fig. 29B is a plan view depicting an example of a structure of the semiconductor device according to Embodiment 12;

Fig. 29C is a cross-sectional view depicting a cross-sectional structure at the sectional line A-A' in Fig. 29B;

Fig. 30 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 13;

Fig. 31 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 14;

Fig. 32 is a cross-sectional view depicting an example of a semiconductor device manufactured by the semiconductor device manufacturing method according to Embodiment 14;

Fig. 33 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 15;

Fig. 34 is a flow chart depicting an overview of a semiconductor device manufacturing method according to Embodiment 16;

Fig. 35 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 16; and

Fig. 36 is a cross-sectional view depicting a key portion of a conventional diode.

[0021] The inventive method is disclosed as a process option within Embodiment 1. Embodiments 2-16 relate to examples which do not form part of the claimed invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0022] Preferred embodiments of a semiconductor device and a semiconductor device manufacturing method according to the present invention and according to examples not forming part of the claimed invention will be described in detail with reference to the accompanying drawings. In this description and in the accompanying drawings, a layer or a region with an n or p superscript means that the majority carrier of the layer or the region is electrons or holes respectively. + or - attached to n or p indicates that the impurity concentration is higher or lower respectively than a layer or a region where + or - is not attached. In the following description of the embodiments and the accompanying drawings, a same composing element is denoted with a same reference symbol, for which redundant description is omitted.

(Embodiment 1)

[0023] A semiconductor device manufacturing method according to Embodiment 1 will be described using an example of fabricating (manufacturing) a pin diode. Fig. 1 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 1. Fig. 2 to Fig. 7 are cross-sectional views depicting a state during manufacturing the semiconductor according to Embodiment 1. Fig. 8A and Fig. 8B are characteristic diagrams depicting an impurity concentration distribution of the semiconductor device according to Embodiment 1. First, a front surface element structure constituted by a p-type anode layer 2, an anode electrode 3, a terminal withstand voltage structure (not illustrated), and a passivation film (not illustrated) is formed on the front surface side of an n-type semiconductor substrate to be an n^--type drift layer 1 (step S1). In concrete terms, a p-type layer to be a p-type anode layer 2 and a p-type layer to be a guard ring constituting the terminal withstand voltage structure are selectively formed on the surface layer of the front surface of the n-type semiconductor substrate.

[0024] Then PSG (Phospho Silicate Glass), for example, is formed as an inter-layer insulation film (not illustrated), so as to cover the front surface of the n-type semiconductor substrate. Then the inter-layer insulation film is selectively removed, and a contact hole to expose the p-type anode layer 2 and the guard ring is formed. Then as a field plate for the anode electrode 3 and the terminal withstand voltage structure, an Al-Si (Aluminum-Silicon) film, for example, is deposited to be implanted in the contact hole, whereby a passivation film is formed on the Al-Si film. The terminal withstand voltage structure is a region that surrounds an active region where the p-type anode layer 2 is formed, and maintains the withstand voltage by relaxing the electric field on the substrate front surface side. The active region is a region where current flows in the ON state.

[0025] Then as illustrated in Fig. 2, electron beams are irradiated (hereafter called "electron beam irradiation 11") throughout the n^--type semiconductor substrate from the front surface side of the n^--type semiconductor substrate (step S2). For the electron beam irradiation 11, the acceleration energy may be 1MeV or more, 10 MeV or less, and the dose may be 20 kGy or more, 600 kGy or less (preferably 90 kGy or more, 200 kGy or less), for example. Then as illustrated in Fig. 3, furnace annealing (heat treatment) is performed at a temperature of 330°C or more, 380°C or less (e.g. 360°C) for one hour or more, five hours or less (step S3).

[0026] By the electron beam irradiation 11 and furnace annealing in steps S2 and S3, defects (lattice defects) 12 are formed through the n^--type semiconductor substrate, for example, and the carrier lifetime is adjusted so that an appropriate ON voltage and reverse recovery loss are implemented. The defects 12 formed by the electron beam irradiation 11 are holes formed by the dangling bonds generated by breaking of the inter-atomic bonds of silicon (Si) of the n^--type semiconductor substrate by the electron beam irradiation 11. In Fig. 3, × indicates a defect 12 (the same for Fig. 4 to Fig. 7) .

[0027] Then as illustrated in Fig. 4, the n^--semiconductor substrate is ground from the rear surface side until reaching the position 1a at which actual thickness of the semiconductor device as a product is implemented (step S4). Then, in an example not forming part of the claimed invention, and as illustrated in Fig. 5, n-type impurities, such as phosphorus (P) and arsenic (As), are ion-implanted, (hereafter called "n^--type impurity ion implantation 13": second implantation step) from the ground rear surface side of the n-type semiconductor substrate, whereby an n^+-type cathode layer 4 is formed on the surface layer of the rear surface of the n^--type semiconductor substrate (step S5).

[0028] The dose of the n-type impurity ion implantation 13 is $1.0 \times 10^{15}/cm^2$ or more, $1.0 \times 10^{16}/cm^2$ or less, for example. The acceleration energy of the n-type impurity ionimplantation 13 is an energy that does not generate defects (lattice defects) in the n^+-cathode layer 4, or is an energy with which the defects generated by the n-type impurity ion implantation 13 are recovered by the later mentioned hydrogen ion implantation and laser annealing. In concrete terms, the acceleration energy of the n-type impurity ion implantation 13 may be 20 keV to 100 keV, for example, and is preferably about 70 keV to 80 keV.

[0029] Then, in an example not forming part of the claimed invention, and as illustrated in Fig. 6, hydrogen (H) is ion-implanted (hereafter called "hydrogen ion implantation 14": first implantation step) from the ground rear surface side of the n^--type semiconductor substrate, whereby the hydrogen implanted region having a hydrogen concentration not lower than the hydrogen concentration of the n^--type semiconductor substrate before the start of the manufacturing steps is formed (step S6). The hydrogen concentration of the n^--type semiconductor substrate before the start of the manufacturing steps refers to the hydrogen concentration of bulk single crystal silicon grown by a standard crystal growth method, such as the Czochralski Method and the Float Zone Method. The hatched region in Fig. 6 indicates the hydrogen implanted region. The implantation depth of the hydrogen ion implantation 14 is preferably not greater than the penetration depth of a laser from the substrate rear surface in the later mentioned laser annealing.

[0030] In concrete terms, the acceleration energy of the hydrogen ion implantation 14 is about 5 keV or more, 500 keV or less, preferably about 5 keV or more, 250 keV or less, for example. It is preferable that the range Rp of the hydrogen ion implantation 14 (that is, depth of the hydrogen implanted region from the substrate rear surface) is relatively shallow, such as 0.1 μm or more, 3 μm or less (acceleration energy in this case is about 5 keV or more, 250 keV or less, for example). This is because the hydrogen termination of the dangling bonds is accelerated, and the defects 12 generated by the electron beam irradiation 11 are more easily recovered. In the hydrogen implanted region, the defects 12 generated by the electron beam irradiation 11 is locally recovered, and the defects generated by the n-type impurity ion implantation 13 is locally recovered. Thereby the lifetime of carriers on the rear surface side (cathode side) of the n^--type semiconductor substrate becomes longer than the lifetime of carriers on the front surface side (anode side) of the n-type semiconductor substrate. The acceleration energy with which the Rp of the hydrogen ion implantation 14 becomes 0.1 μm is about 5 keV, and the acceleration energy with which this Rp becomes 3 μm is about 500 keV. The hydrogen dose of the hydrogen ion implantation 14 is preferably about $1.0 \times 10^{13}/cm^2$ or more, for example. This is because the ON voltage Vf can be decreased and the soft recovery characteristic of the diode can be improved as the hydrogen dose increases.

[0031] The n-type impurity ion implantation 13 and the hydrogen ion implantation 14 may be executed, in another example not forming part of the claimed invention, in reverse order (mass separation implantation) or are, in accordance with the claimed invention, executed simultaneously (non-mass separation implantation). If the n-type impurity ion implantation 13 and the hydrogen ion implantation 14 are executed simultaneously by non-mass separation implantation, ion implantation, of which ion source is a mixed gas containing n-type impurities and hydrogen (hydrogen atoms (H) and hydrogen molecules (H_2)), such as hydrogen phosphide (PH x (x = 1 ~ 5): e.g. phosphine (PH_3)) and hydrogen arsenide (AsHx: e.g. arsine (AsH_3)), is performed with an acceleration energy of about 10 keV to 1 MeV. In this case, the ion implantation is performed such that the dose of the n-type impurity becomes the dose of the n-type impurity ion implantation 13 with the above mentioned acceleration energy of the n-type impurity ion implantation 13. The dose of the hydrogen in this ion implantation is determined by a number of hydrogen atoms included in the composition formula of the mixed gas to be the ion source, hence the dose of hydrogen enters the above mentioned preferable range.

[0032] Then the n^+-type cathode layer 4 is activated by laser annealing, for example (step S7). For the laser annealing in step S7, a YAG laser or a semiconductor laser may be used, or a CW (Continuous Wave) laser may be combined with the YAG laser or the semiconductor laser. In step S7, furnace annealing, such as RTA (Rapid Thermal Annealing), may be performed instead of laser annealing. To perform the furnace annealing in step S7, it is preferable to perform the furnace annealing at a temperature of 300°C or more, 500°C or less, for 30 minutes or more, 10 hours or less, for example, and in concrete terms, the furnace annealing at 350°C for about 1 hour, for example, is preferable. Then a cathode electrode 5, that contacts the n^+-type cathode layer 4, is formed as the rear surface electrode (step S8), whereby the pin diode illustrated in Fig. 7 is completed.

[0033] Fig. 8A and Fig. 8B show the impurity concentration distribution on the rear surface side (cathode side) of the n^--type semiconductor substrate of the completed pin diode. Fig. 8A shows the impurity concentration distribution when the n-type impurity ion implantation 13 and the hydrogen ion implantation 14 are simultaneously performed by non-mass separation implantation, in accordance with the claimed invention. Fig. 8B shows the impurity concentration distribution when the n-type impurity ion implantation 13 and the hydrogen ion implantation 14 are separately performed by mass separation implantation, in an example not forming part of the claimed invention. in Fig. 8A and Fig. 8B, the depth = 0 μm is the position of the ground rear surface of the n^--type semiconductor substrate (that is, the interface between the n^+-type cathode layer 4 and the cathode electrode 5), and the portion deeper than the n^+-type cathode layer 4 is the n-type drift layer 1 (the same for Fig. 12A and Fig. 12B).

[0034] As shown in Fig. 8A, in the case of the non-mass separation implantation, the hydrogen implanted region 6 formed by the hydrogen ion implantation 14 has a first concentration peak 6-1 of the hydrogen molecules (H_2), and a second concentration peak 6-2 of the hydrogen atoms (H) which is formed in a deeper portion from the substrate rear surface than the first concentration peak 6-1. The first and second concentration peaks 6-1 and 6-2 of the hydrogen implanted region 6 are formed in deeper positions from the substrate rear surface than the concentration peak 4-1 of the n^+-type cathode layer 4. The first concentration peak 6-1 is formed corresponding to the hydrogen molecules, and the second concentration peak 6-2 is formed corresponding to the hydrogen atoms. In Fig. 8A, the reference character d denotes the depth of the hydrogen implanted region 6 from the substrate rear surface (that is, the implantation depth of the hydrogen ion implantation 14). The first and second concentration peaks 6-1 and 6-2 of the hydrogen implanted region 6 are formed to overlap with each other. In other words, the width in the depth direction (thickness) of the hydrogen implanted region 6, generated by non-mass separation implantation, is the width from the edge of the first concentration peak of the hydrogen molecules (H_2) on the substrate rear surface side to the edge of the second concentration peak of the hydrogen atoms on the substrate front surface side. Therefore the defects generated by the electron beam irradiation can be recovered in a wide range where the hydrogen implanted region 6 is formed.

[0035] In the case of the mass-separation implantation, on the other hand, the hydrogen implanted region 6, formed by the hydrogen ion implantation 14, has one concentration peak 6-3 of the hydrogen atoms, as shown in Fig. 8B (a). Therefore compared with the case of the non-mass separation implantation, the width of the hydrogen implanted region 6 in the depth direction becomes narrow, but in the case of th mass separation implantation, a dedicated ion implantation device is not required, and an existent ion implantation device can be used. Therefore cost can be reduced. Further, a plurality of concentration peaks 6-3 to 6-5 of the hydrogen atoms can be generated in different depths from the substrate rear surface, as shown in Fig. 8B (b), by performing a plurality of times of hydrogen ion implantation 14 based on the mass separation implementation using a different acceleration energy. For example, it is assumed that one concentration peak 6-3 of the hydrogen atoms was generated by performing one hydrogen ion implantation 14 based on the mass separation implementation at acceleration energy 20 keV. In this case, if two times of hydrogen ion implantation 14 are performed at acceleration energy 10 keV and 30 keV, one concentration peak 6-3 of the hydrogen atoms can be generated in a region at a 1 μm or less depth from the substrate rear surface, and the concentration peaks 6-4 and 6-5 of the hydrogen atoms can be generated on the substrate rear surface side and on the substrate front surface side of the concentration peak 6-3 respectively. Hence the hydrogen implanted region 6 can be formed in a range equivalent to the non-mass separation implantation by generating a concentration peak 6-3 and concentration peaks 6-4 and 6-5, so as to overlap with one another by appropriately adjusting each acceleration energy of a plurality of times of hydrogen ion implantation 14.

[0036] The ON voltage and the current/voltage waveform during reverse recovery of the semiconductor device according to Embodiment 1 will be described next. Fig. 9 is a characteristic diagram depicting the hydrogen dose dependency of the ON voltage of the semiconductor device according to Embodiment 1. Fig. 10 is a characteristic diagram depicting the hydrogen dose dependency of the reverse recovery waveform of the semiconductor device according to Embodiment 1. Fig. 9 shows the hydrogen dose dependency of the reverse recovery waveform when the n-type impurity ion implantation 13 and the hydrogen ion implantation 14 are executed separately by mass separation implantation, in an example not forming part of the claimed invention. As shown in Fig. 9, the ON voltage Vf decreases as the hydrogen dose (H^+ dose), implemented by the hydrogen ion implantation 14, increases. Fig. 9 shows the measured values when the hydrogen dose of the hydrogen ion implantation 14 is $1.0 \times 10^{12}/cm^2$ to $1.0 \times 10^{16}/cm^2$, but the ON voltage Vf still reduces as the hydrogen dose increases even when the hydrogen dose of the hydrogen ion implantation 14 is more than $1.0 \times 10^{16}/cm^2$. As shown in Fig. 10, the reverse recovery peak current Irp (peak value A of the anode current during reverse recovery), which is determined by the carrier concentration on the surface front surface side, is approximately the same value regardless the hydrogen dose of the hydrogen ion implantation 14. The tail current B of the reverse recovery current waveform (reverse recovery changes), on the other hand, increases as the hydrogen dose of the hydrogen ion implantation 14 increases, presenting a soft recovery. Therefore as the results in Fig. 9 and Fig. 10 show, the carrier lifetime on the cathode side of the n^--type drift layer 1 is recovered by the hydrogen ion implantation 14. As described above, the range of the hydrogen dose of the hydrogen ion implantation 14 is $1.0 \times 10^{12}/cm^2$ to $1.0 \times 10^{16}/cm^2$. Preferably the range is $1.0 \times 10^{13}/cm^2$ to $1.0 \times 10^{16}/cm^2$ where the ON voltage decreases. It is more preferable that the range is $1.0 \times 10^{14}/cm^2$ to $1.0 \times 10^{16}/cm^2$ where the ON voltage is sufficiently low, or $1.0 \times 10^{15}/cm^2$ to $1.0 \times 10^{16}/cm^2$ where the ON voltage further stabilizes.

[0037] The present inventors confirmed (not illustrated) that if the hydrogen implanted region 6 is formed by non-mass separation implantation using phosphine, such that the hydrogen dose of the hydrogen ion implantation 14 is within the above mentioned range, for example, then the ON voltage Vf can be 1.40 V or less, and the ON voltage Vf can be reduced to 1.38V by the mass separation implantation. The ON voltage Vf can be decreased by the non-mass separation implantation because the first and second concentration peaks 6-1 and 6-2 having concentration peaks at different depths from the substrate rear surface are generated, as mentioned above, and the width of the hydrogen implanted region 6 in the depth direction can be made wider than the case of generating only the concentration peak 6-3 of the hydrogen atoms, as in the case of mass separation implantation.

[0038] As described above, according to Embodiment 1, defects are formed throughout the n^--type semiconductor substrate by the electron beam irradiation, and then the defects on the substrate rear surface side are locally recovered by the hydrogen ion implantation from the substrate rear surface, whereby the carrier lifetime on the substrate rear surface side can be made longer than the carrier lifetime on the substrate front surface side. Hence, even if the carrier lifetime control is performed using the electron beam irradiation, the carrier lifetime can be locally controlled. Therefore the local carrier lifetime control can be performed at low cost without increasing the leak current or contaminating the manufacturing line. This means that the carrier lifetime on the cathode side (substrate rear surface side) of the n^--type drift layer can be made longer than the carrier lifetime on the anode side (substrate front surface side) of the n^--type drift layer, and the soft recovery characteristic of the diode can be improved. As a result, a diode, where oscillation of the current/voltage waveform during reverse recovery and surge due to oscillation of the voltage waveform are decreased, can be provide.

(Embodiment 2)

[0039] A semiconductor device manufacturing method according to Embodiment 2, which is not forming part of the claimed invention, will be described using an example of fabricating a pin diode, which includes an n-type field stop (FS) layer constituted by a hydrogen inducing donor, inside the n^--type drift layer. Fig. 11 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 2. Fig. 12A and Fig. 12B are characteristic diagrams depicting an impurity concentration distribution of the semiconductor device according to Embodiment 2. A difference of the semiconductor device manufacturing method according to Embodiment 2 from the semiconductor device manufacturing method according to Embodiment 1 is that the implantation depth of the hydrogen ion implantation from the substrate rear surface is made deeper than the penetration depth of the laser from the substrate rear surface in the laser annealing for activating the n^+-type cathode layer 4.

[0040] First, a front surface element structure is formed on the front surface side of the n^--type semiconductor substrate to be the n^--type drift layer in the same manner as Embodiment 1 (step S11). Then the n^--type semiconductor substrate is ground from the rear surface side until reaching a position at which thickness of the semiconductor device as a product is implemented (step S12). The method for grinding the rear surface of the n^--type semiconductor substrate is the same as Embodiment 1. Then hydrogen ions are implanted from the rear surface side of the n^--type semiconductor substrate, and hydrogen is implanted into a region for forming the n-type field stop (FS) layer 21 inside the n^-type drift layer (step S13). In step S13, the n-type FS layers 21a to 21c, of which depths from the substrate rear surface are different, are formed, hence the hydrogen ion implantation may be performed a plurality of times while changing the acceleration energy in various ways.

[0041] The hydrogen ion implantation in step S13 is proton implantation, for example, and is performed at a higher acceleration energy than the hydrogen ion implantation of Embodiment 1. In other words, in step S13, the implantation depth of the hydrogen ion implantation (that is, the range Rp of the hydrogen ion implantation) is deeper than the penetration depth of the laser which is irradiated from the substrate rear surface in the later mentioned laser annealing step for activating the n^+-cathode layer. The dose of the hydrogen ion implantation is $1 \times 10^{13}/cm^2$ or more, $1 \times 10^{15}/cm^2$ or less, for example, and is preferably $1 \times 10^{14}/cm^2$ or more. The acceleration energy of the hydrogen ion implantation is 500 keV or more, for example, preferably 1 MeV or more, 3 MeV or less. The hydrogen ion implantation may be executed a plurality of times at a 500 keV or less low acceleration energy, for example.

[0042] For the hydrogen ion implantation, the high acceleration energy (1 MeV to 3 MeV) and the low acceleration energy (less than 1 MeV, preferably 500 keV or less) may be combined for a plurality of times. In this case, for the hydrogen ion implantation, the acceleration energy of the ion implantation, to form the n-type FS layer 21c which is shallowest from the substrate rear surface, is set to 500 keV or less, for example. In concrete terms, the acceleration energy of each hydrogen ion implantation that is performed by combining the high acceleration energy and the low acceleration energy a plurality of times may be 400 keV, 800 keV, 1100 keV and (1500 keV), for example, or may be 400 keV, 1500 keV and 2100 keV. The dose of each hydrogen ion implantation at this time is not especially limited, and may be a dose that implements the impurity concentration required for each n-type FS layer 21, such as $3 \times 10^{14}/cm^2$, $1 \times 10^{13}/cm^2$, $1 \times 10^{13}/cm^2$ and ($1 \times 10^{13}/cm^2$), for example.

[0043] Fig. 12A shows the impurity concentration distribution of the n-type FS layers 21a to 21c formed by performing the hydrogen ion implantation a plurality of times. The acceleration energy of each hydrogen ion implantation, to form the n-type FS layers 21a to 21c, is 2100 keV, 1500 keV and 400 keV respectively. In this case, the ranges of the n-type FS layers 21a to 21c are 52 μm, 30 μm and 4.4 μm respectively. Fig. 12B shows the impurity concentration distribution of the n-type FS layer 21 formed by hydrogen ion implantation performed once. The acceleration energy of the hydrogen ion implantation for forming the n-type FS layer 21 is 550 keV. In this case, the range of the n-type FS layer 21 is 6.9 μm.

[0044] Then the furnace annealing for ionizing hydrogen atoms introduced to the n^--type semiconductor substrate and generating a hydrogen induced donor (hereafter called "first furnace annealing") is performed (step S14). The temperature of the first furnace annealing is higher than the temperature of the second furnace annealing after the electron beam irradiation, which is performed later, and is preferably 300°C or more, 500°C or less, for example, such as 380°C or more, 400°C or less in concrete terms. This temperature may be 330°C or more, 350°C or less. The first furnace annealing processing time may be 30 minutes or more, 10 hours or less, for example. In concrete terms, the first furnace annealing is performed at about a 350°C temperature for about one hour. By the first furnace annealing, the generation of a hydrogen induced donor is accelerated, and a donor layer, which has a concentration peak higher than the carrier concentration of the n^--type semiconductor substrate, is formed inside the n^--type drift layer. This donor layer is the n-type FS layer 21. Further, by the hydrogen ion implantation at a high acceleration energy and the first furnace annealing, a hydrogen implanted region 22 having a hydrogen concentration equal to or higher than the hydrogen concentration of the bulk substrate is formed in a region shallower than the n-type FS layer 21 from the substrate rear surface (on the cathode side of the n^--type semiconductor substrate), in the same manner as in Embodiment 1. This hydrogen implanted region 22 may be a donor layer.

[0045] Then the electron beam irradiation and the furnace annealing (hereafter called "second furnace annealing") are performed (steps S15 and S16), in the same manner as in Embodiment 1, so as to generate the defects 12 throughout the n^--type semiconductor substrate. In this case, the hydrogen implanted region 22 has been formed on the cathode side of the n^--type semiconductor substrate, hence a number of defects 12 of the n^--type semiconductor substrate is less in the cathode side than in the anode side. Then in the same manner as in Embodiment 1, the n^+-type cathode layer 4 is formed by performing the n-type impurity ion implantation (step S17) and the laser annealing (step S18), and then the rear surface electrode is formed (step S19), whereby the pin diode, including the n-type FS layer 21 constituted by the hydrogen induced donor, is completed.

[0046] If the hydrogen ion implantation in step S13 is performed a plurality of times, combining the high acceleration energy and the low acceleration energy, or if the hydrogen ion implantation in step S13 is performed a plurality of times using low acceleration energy, the hydrogen concentration at a shallow depth, such as 3 μm from the substrate rear surface, can be the bulk substrate concentration or more with certainty by the hydrogen ion implantation at low acceleration energy.

[0047] As described above, according to Embodiment 2, the hydrogen implanted region is formed in a portion to provide a long carrier lifetime on the substrate rear side, even if the hydrogen ion implantation is performed targeting a region deeper then the portion to provide a long carrier lifetime on the substrate rear side, hence an effect similar to Embodiment 1 can be implemented.

(Embodiment 3)

[0048] A semiconductor device manufacturing method according to Embodiment 3, which is not forming part of the claimed invention, will be described next. Fig. 13 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 3. A difference of the semiconductor device manufacturing method according to Embodiment 3 from the semiconductor device manufacturing method according to Embodiment 1 is that the electron beam irradiation and the furnace annealing are performed after the laser annealing. The semiconductor device manufacturing method according to Embodiment 3 is useful when defects are formed in a shallow region, such as 3 μm or less from the substrate rear side, by the hydrogen ion implantation (e.g. a case of fabricating a pin diode which does not include an FS layer).

[0049] In concrete terms, in the same manner as in Embodiment 1, the front surface element structure is formed (step S21). Then the rear surface grinding (step S22), the hydrogen ion implantation (step S23), the n-type impurity ion implantation (step S24), the laser annealing (step S25), the electron beam irradiation (step S26), the furnace annealing (step S27), and the rear surface electrode formation (step S28) are sequentially performed, where a pin diode is completed. In step S23, the hydrogen ion implantation may be performed a plurality of times, in the same manner as in Embodiment 1. The conditions of the rear surface grinding, the hydrogen ion implantation, the n-type impurity ion implantation, the laser annealing, the electron beam irradiation, the furnace annealing, and the rear surface electrode formation are the same as Embodiment 1.

[0050] As mentioned above, the electron beam irradiation and the furnace annealing are performed after the laser annealing. Therefore the carrier lifetime distribution adjusted by the electron beam irradiation and furnace annealing based on the impurity concentration distribution of the hydrogen implanted region is not influenced by the dispersion of the laser annealing. Hence a change in the desired carrier lifetime distribution obtained by the hydrogen ion implantation and electron beam irradiation can be prevented.

[0051] As described above, according to Embodiment 3, an effect similar to Embodiment 1 can be implemented.

(Embodiment 4)

[0052] A semiconductor device manufacturing method according to Embodiment 4, which is not forming part of the claimed invention, will be described next. Fig. 14 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 4. A difference of the semiconductor device manufacturing method according to Embodiment 4 from the semiconductor device manufacturing method according to Embodiment 3 is that the hydrogen ion implantation is performed after the laser annealing and before the electron beam irradiation.

[0053] In concrete terms, in the same manner as in Embodiment 3, the front surface element structure is formed and the rear surface is ground sequentially (steps S31, S32). Then the n-type impurity ion implantation (step S33), the laser annealing (step S34), the hydrogen ion implantation (step S35), the electron beam irradiation (step S36), the furnace annealing (step S37) and the rear surface electrode formation (step S38) are sequentially performed, whereby the pin diode is completed. Conditions of the n-type impurity ion implantation, the laser annealing, the hydrogen ion implantation, the electron beam irradiation, the furnace annealing and the rear surface electrode formation are the same as Embodiment 3.

[0054] In the laser annealing, the irradiation surface on the semiconductor substrate, where the laser is irradiated, may in some cases melt. If the hydrogen ion implantation is performed before the laser annealing in such a case, the implanted hydrogen may be emitted outside the substrate surface because of the melting of the substrate irradiation surface by the laser irradiation, and the hydrogen termination effect may be decreased. If the hydrogen ion implantation is performed after the laser annealing, as in Embodiment 4, emission of hydrogen outside the substrate surface, can be prevented, and a decrease in the hydrogen termination effect can be controlled.

[0055] As described above, according to Embodiment 4, an effect similar to Embodiment 3 can be implemented.

(Embodiment 5)

[0056] A semiconductor device manufacturing method according to Embodiment 5, which is not forming part of the claimed invention, will be described next. Fig. 15 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 5. A difference of the semiconductor device manufacturing method according to Embodiment 5 from the semiconductor device manufacturing method according to Embodiment 3 is that first furnace annealing for activating impurities is performed after the laser annealing and before the electron beam irradiation. The semiconductor device manufacturing method according to Embodiment 5 is useful when protons, for example, implanted in the deeper region from the substrate rear surface, are activated (e.g. in the case of fabricating a pin diode including a plurality of stages of FS layers).

[0057] In concrete terms, in the same manner as in Embodiment 3, the front surface element structure formation (step S41), the rear surface grinding (step S42), the hydrogen ion implantation (step S43), the n-type impurity ion implantation (step S44) and the laser annealing (step S45) are sequentially performed. In step S43, in the same manner as in Embodiment 2, hydrogen is implanted into the region to form the n-type FS layer disposed in a deep region which is 3 μm or more, particularly 10 μm or more, from the substrate rear surface, for example, by a plurality of times of hydrogen ion implantation, and a hydrogen implanted region is formed in a region shallower than the n-type FS layer from the substrate rear surface. Then the furnace annealing for activating the impurities (first furnace annealing) is performed (step S46). The conditions of the first furnace annealing may be the same as the first furnace annealing of Embodiment 2, for example. By this first furnace annealing, protons implanted into a position deeper from the substrate rear surface are activated, and a plurality of stages of n-type FS layers are formed, for example. Then in the same manner as in Embodiment 3, the electron beam irradiation (step S47), furnace annealing for forming defects (second furnace annealing) (step S48), and rear surface electrode formation (step S49) are sequentially performed, whereby the pin diode is completed.

[0058] As described above, according to Embodiment 5, an effect similar to Embodiments 1 to 4 can be implemented.

(Embodiment 6)

[0059] A semiconductor device manufacturing method according to Embodiment 6, which is not forming part of the claimed invention, will be described next. Fig. 16 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 6. A difference of the semiconductor device manufacturing method according to Embodiment 6 from the semiconductor device manufacturing method according to Embodiment 5 is that the hydrogen ion implantation is performed after the laser annealing and before the first furnace annealing.

[0060] In concrete terms, in the same manner as in Embodiment 5, the front surface element structure is formed and the rear surface is ground sequentially (steps S51, S52). Then the n-type impurity ion implantation (step S53), the laser annealing (step S54), the hydrogen ion implantation (step S55), the first furnace annealing (step S56), the electron beam irradiation (step S57), the second furnace annealing (step S58) and the rear surface electrode formation (step S59) are sequentially performed, whereby the pin diode is completed. Conditions of the n-type impurity ion implantation, the laser annealing, hydrogen ion implantation, the first furnace annealing, the electron beam irradiation, the second furnace annealing and the rear surface electrode formation are the same as Embodiment 5.

[0061] As described above, according to Embodiment 6, an effect similar to Embodiments 4 and 5 can be implemented.

(Embodiment 7)

[0062] A semiconductor device manufacturing method according to Embodiment 7, which is not forming part of the claimed invention, will be described next. Fig. 17 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 7. Fig. 18 to Fig. 24 are cross-sectional views depicting each state during manufacturing the semiconductor device according to Embodiment 7. The semiconductor device manufacturing method according to Embodiment 7 is a method of fabricating an IGBT having an n-type FS layer in a deep region from the substrate rear surface (e.g. see Fig. 24) by applying Embodiment 2. In the case of fabricating an IGBT as well, the hydrogen implanted region can be formed in a region shallower than the n-type FS layer 40 from the substrate rear surface, by the hydrogen ion implantation 54 that implants hydrogen into the region to form the n-type FS layer 40, and carrier lifetime can be adjusted, in the same manner as in Embodiment 2. The semiconductor device manufacturing method according to Embodiment 7 is useful when the n-type FS layer 40 is formed in a deep region from the substrate rear surface where impurities cannot be introduced by ion implantation of elements, such as phosphorus and arsenic, of which ranges are shorter than hydrogen.

[0063] In concrete terms, as illustrated in Fig. 18, a standard MOS gate (Metal-Oxide film-Semiconductor insulation gate) structure and a front surface element structure constituted by, an emitter electrode 38, a termination withstand voltage structure (not illustrated), a passivation film (not illustrated) or the like are formed (step S61) on the front surface side of the n^--type semiconductor substrate, which becomes an n^--type drift layer 31. The MOS gate structure is constituted by a p-type base layer 32, a trench 33, a gate insulation film 34, a gate electrode 35 and an n^+-type emitter region 36. The reference numeral 37 denotes an inter-layer insulation film. Then as illustrated in Fig. 19, the n^--type semiconductor substrate is ground from the rear surface side until reaching a position 31a at which actual thickness of the semiconductor device as a product is implemented (step S62).

[0064] Then as illustrated in Fig. 20, p-type impurities, such as boron (B), are ion-implanted (hereafter called "p-type impurity ion implantation 51": second implantation step) from the ground rear surface side of the n^--type semiconductor substrate, and the p-type impurities 52 are introduced into the region to form the p^+-type collector layer 39 (step S63). In Fig. 20, × indicates the p-type impurities 52 introduced into the region to form the p^+-type collector layer 39. Then as illustrated in Fig. 21, the p-type impurities 52 implanted on the rear surface side of the n^--type semiconductor substrate are activated by the laser annealing 53 (step S64). Thereby the p^+-type collector layer 39 is formed on the surface layer of the rear surface of the n^--type semiconductor substrate.

[0065] Then as illustrated in Fig. 22, the hydrogen ion implantation 54 is performed from the ground rear surface side of the n^--type semiconductor substrate, and hydrogen is implanted into the region to form the n-type FS layer 40 inside the n^--type drift layer 31 (step S65). For the hydrogen ion implantation in step S65, proton implantation is performed, for example, in the same manner as in Embodiment 2. In step S65, a plurality of n-type FS layers 40, of which depths from the substrate rear surface are different, are formed, hence the hydrogen ion implantation may be performed a plurality of times, while changing the acceleration energy in various ways. By this hydrogen ion implantation 54, the hydrogen implanted region is formed in a shallower region from the substrate rear surface than the n-type FS layer 40. In Fig. 22, × indicates a defect 55.

[0066] Then as illustrated in Fig. 23, the furnace annealing for ionizing hydrogen atoms and generating a hydrogen induced donor is performed, whereby the hydrogen induced donor generation of the hydrogen atoms inside the hydrogen implanted region is accelerated, and a donor layer to be the n-type FS layer 40 is formed (step S66). The conditions of the furnace annealing in step S66 may be the same as the first furnace annealing of Embodiment 2, for example. Then as illustrated in Fig. 24, the collector electrode 41, which contacts the p^+-type collector layer 39, is formed as the rear surface electrode on the rear surface of the n^--type semiconductor substrate (step S67), whereby the IGBT, including the n-type FS layer 40 constituted by the hydrogen induced donor, is completed.

[0067] If the p^+-type collector layer 39 is formed by the boron ion implantation, lattice defects, such as vacancy and divacancy, remain on the p^+-type collector layer 39 and the semiconductor substrate in the vicinity thereof. If the hydrogen ions are implanted after the p^+-type collector layer 39 is formed, the hydrogen terminates the dangling bonds due to the remaining lattice defects. Thereby the lifetime in the p^+-type collector layer 39 increases, and hole implantation efficiency can be increased. As a result, the ON voltage of the IGBT can be decreased.

[0068] As mentioned above, the hydrogen ion implantation 54 and furnace annealing for forming the n-type FS layer 40 are performed after the laser annealing to activate the p^+-type collector layer 39. Therefore the n-type FS layer 40 is not influenced by the dispersion of laser annealing 53. Hence a change in the desire impurity concentration distribution and diffusion depth of the n-type FS layer 40, obtained by the hydrogen ion implantation 54 and furnace annealing, can be prevented.

[0069] As described above, according to Embodiment 7, an effect similar to Embodiment 1 to 6 can be implemented.

(Embodiment 8)

[0070] A semiconductor device manufacturing method according to Embodiment 8, which is not forming part of the claimed invention, will be described next. Fig. 25 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 8. A difference of the semiconductor device manufacturing method according to Embodiment 8 from the semiconductor device manufacturing method according to Embodiment 7 is that the hydrogen ion implantation is performed after the rear surface grinding and before the p-type impurity ion implantation. Even if the sequence of hydrogen ion implantation, p-type impurity ion implantation and laser annealing is changed, the n-type FS layer can be formed in a deep region from the substrate rear surface, and carrier lifetime can be adjusted based on the hydrogen dose of the hydrogen implanted region formed in a shallower region than the n-type FS layer from the substrate rear surface, in the same manner as in Embodiment 7.

[0071] In concrete terms, in the same manner as in Embodiment 7, the front surface element structure is formed and the rear surface is ground sequentially (steps S71, S72). Then the hydrogen ion implantation (step S73), the p-type impurity ion implantation (step S74), the laser annealing (step S75), the furnace annealing (step S76), and the rear surface electrode formation (step S77) are sequentially performed, whereby the IGBT including the n-type FS layer is completed. The conditions of the hydrogen ion implantation, the p-type impurity ion implantation, the laser annealing, the furnace annealing and the rear surface electrode formation are the same as Embodiment 7.

[0072] As described above, according to Embodiment 8, an effect similar to Embodiment 1 to 6 can be implemented.

(Embodiment 9)

[0073] A semiconductor device manufacturing method according to Embodiment 9, which is not forming part of the claimed invention, will be described next. Fig. 26 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 9. A difference of the semiconductor device manufacturing method according to Embodiment 9 from the semiconductor device manufacturing method according to Embodiment 8 is that the n-type FS layer is formed in a shallow region from the substrate rear surface by the n-type impurity ion implantation and laser annealing. The semiconductor device manufacturing method according to Embodiment 9 is useful when the n-type FS layer is formed in a shallow region from the substrate rear surface where impurities can be introduced by the ion implantation of elements, such as phosphorus and arsenic, of which ranges are shorter than hydrogen.

[0074] In concrete terms, in the same manner as in Embodiment 8, the front surface element structure is formed and the rear surface is ground sequentially (steps S81, S82). Then the hydrogen ion implantation is performed from the ground rear surface side of the n^--type semiconductor substrate, and the hydrogen implanted region is formed at a predetermined depth from the substrate rear surface (step S83). For the hydrogen ion implantation in step S83, only the hydrogen implanted region is formed, in the same manner as in Embodiment 1. The conditions of the hydrogen ion implantation are the same as Embodiment 1. For example, n-type impurities, such as phosphorus, are ion-implanted from the rear surface side of the n^--type semiconductor substrate (n-type impurity ion implantation), and the n-type impurities are introduced to the region to form the n-type FS layer (step S84).

[0075] Then the p-type impurities are introduced to the region to form the p^+-type collector layer by the p-type impurity ion implantation (step S85). Then the n-type impurities and the p-type impurities implanted in the rear surface side of the n^--type semiconductor substrate are activated (step S86). Thereby the p^+-type collector layer is formed on the surface layer of the rear surface of the n^--type semiconductor substrate, and the n-type FS layer is formed in a region deeper than the p^+-type collector layer from the substrate rear surface. Then the rear surface electrode is formed (step S87), whereby the IGBT, including the n-type FS layer, is completed. The conditions of the p-type impurity ion implantation and the rear surface electrode formation may be the same as Embodiment 8. Step S84 which introduces the n-type impurities and step S85 which introduces the p-type impurities may be reversed.

[0076] As described above, according to Embodiment 9, the effect similar to Embodiments 1 to 6 can be implemented.

(Embodiment 10)

[0077] A semiconductor device manufacturing method according to Embodiment 10, which is not forming part of the claimed invention, will be described next. Fig. 27 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 10. A difference of the semiconductor device manufacturing method according to Embodiment 10 from the semiconductor device manufacturing method according to Embodiment 9 is that the hydrogen ion implantation is performed between the n-type impurity ion implantation and the p-type impurity ion implantation.

[0078] In concrete terms, in the same manner as in Embodiment 9, the front surface element structure is formed and the rear surface is ground sequentially (steps S91, S92). Then the n-type impurity ion implementation (step S93), the hydrogen ion implantation (step S94), the p-type impurity ion implantation (step S95), the laser annealing (step S96) and the rear surface electrode formation (step S97) are sequentially performed, whereby the IGBT, including the n-type FS layer, is completed. The conditions of the n-type impurity ion implantation, the hydrogen ion implantation, the p-type impurity ion implantation, the laser annealing and the rear surface electrode formation are the same as Embodiment 9. Step S93 which introduces the n-type impurities and step S95 which introduces the p-type impurities may be reversed.

[0079] As described above, according to Embodiment 10, an effect similar to Embodiment 9 can be implemented.

(Embodiment 11)

[0080] A semiconductor device manufacturing method according to Embodiment, which is not forming part of the claimed invention, will be described next. Fig. 28 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 11. A difference of the semiconductor device manufacturing method according to Embodiment 11 from the semiconductor device manufacturing method according to Embodiment 9 is that the hydrogen ion implantation is performed between the p-type impurity ion implantation and the laser annealing.

[0081] In concrete terms, in the same manner as in Embodiment 9, the front surface element structure is formed and the rear surface is ground sequentially (steps S101, S102). Then the n-type impurity ion implantation (step S103), the p-type impurity ion implantation (step S104), the hydrogen ion implantation (step S105), the laser annealing (step S106) and the rear surface electrode formation (step S107) are sequentially performed, whereby the IGBT, including the n-type FS layer, is completed. The conditions of the n-type impurity ion implantation, the p-type impurity ion implantation, the hydrogen ion implantation, the laser annealing and the rear surface electrode formation are the same as Embodiment 9. The sequence of the n-type impurity ion implantation and the p-type impurity ion implantation may be reversed.

[0082] As described above, according to Embodiment 11, an effect similar to Embodiments 9 and 10 can be implemented.

(Embodiment 12)

[0083] A semiconductor device manufacturing method according to Embodiment 12, which is not forming part of the claimed invention, will be described next. Fig. 29A is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 12. Fig. 29B is a plan view depicting an example of a structure of the semiconductor device according to Embodiment 12. Fig. 29C is a cross-sectional view depicting a cross-sectional structure at the sectional line A-A' in Fig. 29B. The semiconductor device manufacturing method according to Embodiment 12 is a method of fabricating a reverse conducting IGBT (RC-IGBT) where an IGBT, which includes the n-type FS layer 40 and a free wheeling diode (FWD), are disposed on a same n^--type semiconductor substrate by applying Embodiment 2.

[0084] In the case of fabricating the RC-IGBT as well, the hydrogen implanted region can be formed in a region shallower than the n-type FS layer 40 from the substrate rear surface by the hydrogen ion implantation that implants hydrogen in the region to form the n-type FS layer 40, in the same manner as in Embodiment 2. Thereby leak current can be decreased. The semiconductor device manufacturing method according to Embodiment 12 is useful when the n-type FS layer 40 is formed in a deep region from the substrate rear surface, where impurities cannot be introduced by ion implantation.

[0085] In concrete terms, a standard MOS gate structure of IGBT, and a front surface element structure, which is constituted by a p-type anode layer 2 of FWD, a front surface electrode that has the functions of an emitter electrode 38 and an anode electrode (hereafter called "emitter electrode 38"), a termination withstand voltage structure, and a passivation film, are formed on the front surface side of the n^--type semiconductor substrate to be the n^--type drift layer 31 (step S110). The MOS gate structure is constituted by a p-type base layer 32, a trench 33, a gate insulation film 34, a gate electrode 35 and an n^+-type emitter region 36. The reference numeral 37 denotes an inter-layer insulation film. Then the rear surface is ground (step S111). Then p-type impurities are introduced to the region to form the p^+-type collector layer 39 by the p-type impurity ion implantation from the ground rear surface side of the n^--type semiconductor substrate (step S112). The n-type impurities are introduced to the region to form the n^+-type cathode layer 4 by the n-type impurity ion implantation from the ground rear surface side of the n^--type semiconductor substrate (step S113).

[0086] Then the n-type impurities and the p-type impurities implanted on the rear surface side of the n^--type semiconductor substrate are activated by laser annealing (step S114). Thereby the p^+-type collector layer 39 is selectively formed on the surface layer on the rear surface of the n^--type semiconductor substrate, and the n^+-cathode layer 4 is formed so as to be parallel with the p^+-type collector layer 39 in the direction parallel with the principal surface of the substrate, and in contact with the p^+-type collector layer 39. Then hydrogen ions are implanted from the ground rear surface side of the n^--type semiconductor substrate, so as to implant hydrogen into a region to form the n-type FS layer 40 inside the n^--type drift layer 31 (step S115). For the hydrogen ion implantation in step S115, protons are implanted, for example, in the same manner as in Embodiment 2. By this hydrogen ion implantation, a hydrogen implanted region is formed in a region shallower than the n-type FS layer 40 from the substrate rear surface.

[0087] Then the first furnace annealing is performed for ionizing hydrogen atoms introduced to the n^--type semiconductor substrate and generating the hydrogen induced donor, whereby the generation of a hydrogen induced donor is accelerated and a donor layer to be the n-type FS layer 40 is formed (step S116). Then in order to introduce a lifetime killer (defects or impurities) into a region shallower than the n-type FS layer 40 from the substrate rear surface, electron beams are irradiated or helium (He) ions are implanted (hereafter called "helium ion implantation") (step S117), then the second furnace annealing is performed (step S118). Thereby the carrier lifetime is adjusted so that an appropriate ON voltage and reverse recovery loss, based on the hydrogen dose of the hydrogen implanted region, are implanted. Then the rear surface electrode 41, which functions as the collector electrode and the cathode electrode and which is in contact with the p^+-type collector layer 39 and the n^+-type cathode layer 4 is formed (step S119), whereby the RC-IGBT is completed.

[0088] The conditions of the rear surface grinding, the n-type impurity ion implantation, the hydrogen ion implantation and the first furnace annealing may be the same as Embodiment 2, for example. The conditions of the p-type impurity ion implantation and the laser annealing may be the same as Embodiment 7, for example. If the electron beam irradiation is performed in step S117, the conditions of the electron beam irradiation and the second furnace annealing in steps S117 and S118 may be the same as Embodiment 2. Soft recovery of the FWD can be implemented. If helium ion implantation is performed in step S117, the conditions of the helium ion implantation and the second furnace annealing in steps S117 and S118 may be the same as the later mentioned Embodiment 16. Since the hydrogen ion implantation is performed after the laser annealing, the n-type FS layer 40 is not influenced by dispersion of the laser annealing.

[0089] As described above, according to Embodiment 12, an effect similar to Embodiments 1 to 6 can be implemented.

(Embodiment 13)

[0090] A semiconductor device manufacturing method according to Embodiment 13, which is not forming part of the claimed invention, will be described next. Fig. 30 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 13. A difference of the semiconductor device manufacturing method according to Embodiment 13 from the semiconductor device manufacturing method according to Embodiment 12 is that the n-type FS layer is formed by n-type impurity ion implantation and laser annealing. The semiconductor device manufacturing method according to Embodiment 13 is useful when the n-type FS layer is formed in a shallow region from the substrate rear surface where impurities can be introduced by ion implantation.

[0091] In concrete terms, the front surface element structure is formed and the rear surface is ground sequentially (steps S120, S121), in the same manner as in Embodiment 12. Then the hydrogen ion implantation is performed from the ground rear surface side of the n^--type semiconductor substrate, and the hydrogen implanted region is formed to have a predetermined depth from the substrate rear surface (step S122). In the hydrogen ion implantation in step S122, only the hydrogen implanted region is formed, in the same manner as in Embodiment 1. The conditions of the hydrogen ion implantation is the same as Embodiment 1, for example. Then n-type impurities, such as phosphorus, are ion-implanted from the rear surface side of the n^--type semiconductor substrate (hereafter called "first n-type impurity ion implantation"), and the n-type impurities are introduced to the region to form the n-type FS layer (step S123) .

[0092] Then the p-type impurities are introduced to the region to form the p^+-type collector layer by the p-type impurity ion implantation (step S124). Then the n-type impurities are ion-implanted from the rear surface side of the n^--type semiconductor substrate (hereafter called "second n-type impurity ion implantation"), and the n-type impurities are introduced to the region to form the n^+-type cathode layer (step S125). Then the n-type impurities and the p-type impurities implanted on the rear surface side of the n^--type semiconductor substrate are activated (step S126). Then the p^+-type collector layer and the n^+-type cathode layer are formed on the surface layer on the rear surface of the n^--type semiconductor substrate, and the n-type FS layer is formed in a region deeper than the p^+-type collector layer from the substrate rear surface.

[0093] Then the lifetime killer irradiation (step S127), the furnace annealing (step S128) and the rear surface electrode formation (step S129) are sequentially performed, whereby the RC-IGBT is completed. The conditions of the first n-type impurity ion implantation may be the same as the n-type impurity ion implantation in Embodiment 9. The conditions of the p-type impurity ion implantation, the second n-type impurity ion implantation, the laser annealing, the lifetime killer irradiation and the rear surface electrode formation may be the same as Embodiment 12. The conditions of the furnace annealing may be the same as the second furnace annealing of Embodiment 12. The hydrogen ion implantation may be performed after the rear surface grinding and before the laser annealing, and may be performed at any timing after the rear surface grinding and before the laser annealing. Particularly, hydrogen has the effect of terminating dangling bonds generated by lattice defects, such as vacancy and divacancy, that remain on the rear surface by phosphorus or boron ion implantation. As a result, the efficiency of hole implantation of IGBT and electron implantation efficiency of a diode can be increased respectively.

[0094] As described above, according to Embodiment 13, an effect similar to Embodiment 1 to 6 can be implemented.

(Embodiment 14)

[0095] A semiconductor device manufacturing method according to Embodiment 14, which is not forming part of the claimed invention, will be described next. Fig. 31 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 14. Fig. 32 is a cross-sectional view depicting an example of a semiconductor device manufactured by the semiconductor device manufacturing method according to Embodiment 14. The semiconductor device manufacturing method according to Embodiment 14 is a method of fabricating a reverse blocking IGBT (RB-IGBT) illustrated in Fig. 32 by applying Embodiment 1. The reverse leak current can be decreased by forming a hydrogen implanted layer 70, in which generation of a hydrogen induced donor is accelerated, inside the p^+-type collector layer 68 of the RB-IGBT.

[0096] In concrete terms, a standard MOS gate structure, an emitter electrode 67 and a front surface element structure, which is constituted by a p-type separation diffusion layer 73, a termination withstand voltage structure, and a passivation film (not illustrated), are formed on the front surface side of the n^--type semiconductor substrate to be the n^--type drift layer 61 (step S131). The MOS gate structure is constituted by a p-type base layer 62, an n^+-type emitter region 63, a gate insulation film 64 and a gate electrode 65. The termination withstand voltage structure is constituted by a p-type guard ring region 71 and a field plate 72. The depth of the p-type separation diffusion layer 73 is deeper than the depth of the p-type base layer 62 or the p-type guard ring region 71. The reference numeral 66 denotes an inter-layer insulation film.

[0097] Then the n^--type semiconductor substrate is ground from the rear surface side until reaching the position at which actual thickness of the semiconductor device as a product is implemented (step S132). In step S132, the p-type separation diffusion layer 73 is exposed to the ground rear surface of the n^--type semiconductor substrate. Thereby the p-type separation diffusion layer 73 is disposed so as to penetrate from the substrate front surface to the rear surface, and be in contact with the p^+-type collector layer 68 in a later step. Then p-type impurities are introduced to the region to form the p^+-type collector layer 68 by the p-type impurity ion implantation (step S133). Then the p-type impurities implanted on the rear surface side of the n^--type semiconductor substrate is activated by the laser annealing 53 (step S134). Thereby the p^+-type collector layer 68 that is in contact with the p-type separation diffusion layer 73 is formed on the surface layer of the rear surface of the n^--type semiconductor substrate.

[0098] Then a hydrogen implanted region is formed inside the p^+-type collector layer 68 by hydrogen ion implantation (step S135). Then the furnace annealing is performed for ionizing hydrogen atoms and generating the hydrogen induced donor, whereby generation of the hydrogen induced donor of the hydrogen atoms inside the hydrogen implanted region is accelerated, and a hydrogen implanted layer 70 is formed inside the p^+-type collector layer 68 (step S136). Then the collector electrode 69 in contact with the p^+-type collector layer 68 is formed (step S137), whereby the RB-IGBT is completed. The conditions of the rear surface grinding, the hydrogen ion implantation and the furnace annealing may be the same as Embodiment 1. The conditions of the p-type impurity ion implantation, the laser annealing and the rear surface electrode formation may be the same as Embodiment 7.

[0099] In the case of RB-IGBT, the implanted hydrogen has an effect to terminate dangling bonds generated by lattice defects, such as vacancy and divacancy, in the p^+-type collector layer 68 on the rear surface. As a result, leak current, when reverse bias voltage is applied to the pn junction between the p^+-type collector layer 68 and the n^--type drift layer 61 on the rear surface (reverse leak current), can be decreased.

[0100] As described above, according to Embodiment 14, an effect similar to Embodiment 1 to 6 can be implemented.

(Embodiment 15)

[0101] A semiconductor device manufacturing method according to Embodiment 15, which is not forming part of the claimed invention, will be described next. Fig. 33 is a flow chart depicting an overview of the semiconductor device manufacturing method according to Embodiment 15. A difference of the semiconductor device manufacturing method according to Embodiment 15 from the semiconductor device manufacturing method according to Embodiment 14 is that the hydrogen ion implantation is performed after the rear surface grinding and before the p-type impurity ion implantation. In other words, the sequence of hydrogen ion implantation, the p-type impurity ion implantation and the laser annealing may be changed.

[0102] In concrete terms, a front surface element structure is formed and a rear surface is ground sequentially (steps S141, S142), in the same manner as in Embodiment 14. Then hydrogen ion implantation (step S143), the p-type impurity ion implantation (step S144), the laser annealing (step S145), the furnace annealing (step S146) and the rear surface electrode formation (step S147) are sequentially performed, whereby the RB-IGBT is completed. In step S143, the hydrogen ion implantation is performed such that the hydrogen implanted region is formed in the region to form the p^+-type collector layer 68. The conditions of the hydrogen ion implantation, the p-type impurity ion implantation, the laser annealing, the furnace annealing and the rear surface electrode formation are the same as Embodiment 14. The hydrogen ion implantation and the p-type impurity ion implantation may be performed simultaneously by ion implantation, of which ion source is a mixed gas containing p-type impurities, such as diborane (B_2H_6), and hydrogen, for example.

[0103] As described above, according to Embodiment 15, an effect similar to Embodiment 14 can be implemented.

(Embodiment 16)

[0104] A semiconductor device manufacturing method according to Embodiment 16, which is not forming part of the claimed invention, will be described next. Fig. 34 and Fig. 35 are diagrams depicting an overview of the semiconductor device manufacturing method according to Embodiment 16. A difference of the semiconductor device manufacturing method according to Embodiment 16 from the semiconductor device manufacturing method according to Embodiment 1 is that the carrier lifetime is adjusted by helium (He) ion implantation (hereafter called "helium ion implantation 81") and hydrogen ion implantation 82. In concrete terms, in the case of the semiconductor device manufacturing method according to Embodiment 16, the helium ion implantation 81 may be performed instead of the electron beam irradiation in the semiconductor device manufacturing method according to Embodiment 1, or the helium ion implantation 81 may be performed before or after the electron beam irradiation.

[0105] Fig. 34A shows an example of an impurity concentration distribution of a pin diode fabricated by the semiconductor device manufacturing method according to Embodiment 16. Fig. 34B, Fig. 34C and Fig. 35 show carrier lifetime distributions during manufacturing the semiconductor device according to Embodiment 16. In Fig. 34, depth = 0 μm is the position of the front surface of the n^--type semiconductor substrate (that is, the interface between the p-type anode layer 2 and the anode electrode) (this is the same for Fig. 35). In the pin diode shown in Fig. 34A, the region from the pn junction between the p-type anode layer 2 and the n^--type drift layer 1 to the anode side portion of the n-type FS layer 21 (the region between the two vertical dotted lines) is a region that is depleted when the rated current is applied (hereafter called "depletion region 80").

[0106] To fabricate this pin diode, a front surface element structure is formed first, in the same manner as in Embodiment 1 (step S1). Then as shown in Fig. 34B, helium ions, accelerated by a cyclotron (accelerator), for example, is implanted from the anode side to the n^--type semiconductor substrate (helium ion implantation 81), instead of the electron beam irradiation (step S2) or before or after the electron beam irradiation. Thereby defects are generated in the region from the substrate rear surface to a predetermine depth (hereafter called "defect region 83a"), and the carrier lifetime on the front surface side (anode side) of the n^--type semiconductor substrate becomes shorter than the carrier lifetime on the rear surface side (cathode side) of the n^--type semiconductor substrate. The carrier lifetime distribution of the defect region 83a becomes a wide distribution (broad distribution) having one peak in a diminishing direction of the carrier lifetime. Therefore the defect region 83a reaches a depth that overlaps (superposes) with the depletion region 80.

[0107] Then, in the same manner as in Embodiment 1, the steps from the furnace annealing to the n-type impurity ion implantation (steps S3 to S5) are sequentially performed. Then as shown in Fig. 34C, the hydrogen implanted region 22 is formed by performing the hydrogen ion implantation 82 (step S6) in the same manner as Embodiment 1, and defects in the portion 84 of the defect region 83a (dotted line) overlapping with the depletion region 80 are recovered. In the state of the defect region 83a overlapping with the depletion region 80, leak current (recovering peak current Irp) increases as mentioned above, but if the hydrogen implanted region 22 is formed by the hydrogen ion implantation 82, carrier lifetime recovers in a range that is wider than the width of the hydrogen implanted region 22 by about 40 μm to the substrate front surface side and to the substrate rear surface side respectively. Thereby the carrier lifetime in the portion 84 of the defect region 83a overlapping with the depletion region 80 approximately returns to the state before the helium ion implantation 81, and the width of the defect region 83b (solid line) after the hydrogen ion implantation 82 becomes a width that does not overlap with the depletion region 80. As a result, the leak current can be decreased.

[0108] Furthermore, as shown in Fig. 35, if the defect region 83c (dotted line), of which carrier lifetime is short, is formed by the helium ion implantation 81 and a part [of the defect region 83c] is recovered by the hydrogen ion implantation 82, it becomes possible to return to the carrier lifetime which is equivalent to the carrier lifetime of the region 83a (solid line) where the same amount of lifetime killer was introduced by the helium ion implantation 81 alone. Moreover, the characteristics of the pin diode are improved, and leak current can be further reduced than the case of forming the lifetime killer by the helium ion implantation 81 alone. Normally when a particle type lifetime killer is formed, thermal treatment is performed in a hydrogen atmosphere after the particles are irradiated, whereby defects having an energy level around the center of the energy band that largely contributes to increasing the leak current is selectively removed. The effect obtained by this thermal treatment in the hydrogen atmosphere is probably obtained by the hydrogen ion implantation 82 as well. After the hydrogen ion implantation 82, the laser annealing (step S7) and later steps are sequentially performed, in the same manner as in Embodiment 1, whereby the pin diode is completed.

[0109] In the case of fabricating the pin diode that includes the n-type FS layer 21 as shown in Fig. 34A, Embodiment 16 can be applied to Embodiment 2. Embodiment 16 may be applied to Embodiments 3 to 15.

[0110] As described above, according to Embodiment 16, an effect similar to Embodiments 1 to 15 can be implemented.

[0111] The present invention is not limited to the embodiments described above, but may be modified in numerous ways within a scope of the invention which is defined by the appended claims.

INDUSTRIAL APPLICABILITY

[0112] As described above, the semiconductor device manufacturing method according to the present invention are useful for power semiconductor devices which are used for power conversion devices, such as convertors and invertors, and power supply devices of various industrial machines.

EXPLANATION OF REFERENCE NUMERALS

[0113]

1	n^--type drift layer
2	p-type anode layer
3	anode electrode
4	n^+-type cathode layer
5	cathode electrode
6, 22	hydrogen implanted region
11	electron beam irradiation
12	defect
13	n-type impurity ion implantation
14	hydrogen ion implantation
21	n-type field stop layer

Claims

1. A method for manufacturing a semiconductor device in which a lifetime of carriers is locally controlled, wherein the semiconductor device is a pin diode, the method comprising:

    forming an n^--type semiconductor substrate to be an n^--type drift layer (1), the semiconductor substrate having a front surface and a rear surface and having a cathode side and an anode side, the cathode side being closer to the rear surface of the semiconductor substrate than the anode side;
    forming a p-type anode layer (2) on the front surface of the semiconductor substrate;
    performing electron beam irradiation (11) from the front surface side of the semiconductor substrate so as to form defects, which are formed

throughout the semiconductor substrate by dangling bonds generated by breaking of interatomic bonds of Si atoms constituting the semiconductor substrate by the electron beam irradiation;
forming an n^+-type cathode layer on the rear surface of the semiconductor substrate;
characterized in that the method further comprises:
simultaneously performing n-type impurity ion implantation (13) and hydrogen ion implantation (14) from the rear surface of the semiconductor substrate and thereby forming the n^+-type cathode layer and a hydrogen implanted region (6), wherein:

in the hydrogen implanted region (6) a first concentration peak (6-1) of hydrogen molecules and a second concentration peak (6-2) of hydrogen atoms are formed with the second concentration peak (6-2) being formed in a deeper portion from the rear surface of the semiconductor substrate than the first concentration peak (6-1);
the first concentration peak (6-1) and the second concentration peak (6-2) are formed in deeper positions from the rear surface of the semiconductor substrate than a concentration peak (4-1) of the n-type impurity of the cathode layer (4);
the first concentration peak (6-1) and the second concentration peak (6-2) are formed to overlap with each other; and
defects (12) on the cathode side are locally recovered in the hydrogen implanted region (6) by hydrogen terminating the dangling bonds.

2. The method according to claim 1, wherein a carrier lifetime on the cathode side is higher than the carrier lifetime on the anode side.

Patentansprüche

1. Verfahren zur Herstellung einer Halbleitervorrichtung, in der eine Ladungsträgerlebensdauer lokal gesteuert wird, wobei die Halbleitervorrichtung eine pin-Diode ist und das Verfahren umfasst:

Bilden eines n^--Halbleitersubstrats, sodass es eine n^--Driftschicht (1) ist, wobei das Halbleitersubstrat eine Vorderfläche und eine Rückfläche sowie eine Kathodenseite und eine Anodenseite aufweist und die Kathodenseite sich näher an der Rückfläche des Halbleitersubstrats befindet als die Anodenseite;
Bilden einer p-Anodenschicht (2) auf der Vorderfläche des Halbleitersubstrats;
Ausführen einer Elektronenstrahlbestrahlung (11) von der Vorderflächenseite des Halbleitersubstrats, um Defekte zu bilden, die durch nichtpaarige Bindungen in dem gesamten Halbleitersubstrat gebildet werden, die durch das Brechen von interatomaren Bindungen von das Halbleitersubstrat bildenden Si-Atomen durch die Elektronenstrahlbestrahlung erzeugt werden;
Bilden einer n^+-Kathodenschicht auf der Rückfläche des Halbleitersubstrats;
dadurch gekennzeichnet, dass das Verfahren ferner umfasst:
gleichzeitiges Ausführen von n-Dotierungsionenimplantation (13) und Wasserstoffionenimplantation (14) von der Rückfläche des Halbleitersubstrats und dadurch Bilden der n^+-Kathodenschicht und einer wasserstoffimplantierten Region (6), wobei:

in der wasserstoffimplantierten Region (6) ein erster Konzentrationspeak (6-1) von Wasserstoffmolekülen und ein zweiter Konzentrationspeak (6-2) von Wasserstoffatomen gebildet werden und der zweite Konzentrationspeak (6-2) in einem tieferen Abschnitt von der Rückfläche des Halbleitersubstrats gebildet wird als der erste Konzentrationspeak (6-1);
der erste Konzentrationspeak (6-1) und der zweite Konzentrationspeak (6-2) in tieferen Positionen von der Rückfläche des Halbleitersubstrats gebildet werden als ein Konzentrationspeak (4-1) des n-Dotierstoffs der Kathodenschicht (4);
der erste Konzentrationspeak (6-1) und der zweite Konzentrationspeak (6-2) derart gebildet werden, dass sie einander überlappen; und
Defekte (12) auf der Kathodenseite durch Beenden der nichtpaarigen Bindungen mittels Wasserstoff in der wasserstoffimplantierten Region (6) lokal wiederhergestellt werden.

2. Verfahren nach Anspruch 1, wobei eine Ladungsträgerlebensdauer auf der Kathodenseite höher ist als die Ladungsträgerlebensdauer auf der Anodenseite.

Revendications

1. Procédé de fabrication d'un dispositif à semi-conducteur dans lequel la durée de vie des porteurs est contrôlée localement, dans lequel le dispositif à semi-conducteur est une diode pin, le procédé comprenant de:

former un substrat semi-conducteur de type n pour être une couche de dérive de type n (1), le substrat semi-conducteur ayant une surface avant et une surface arrière et ayant un côté de cathode et un côté d'anode,
le côté de cathode étant plus proche de la surface arrière du substrat à semi-conducteur que le côté d'anode;
former une couche d'anode de type p (2) sur la surface avant du substrat semi-conducteur;
effectuer une irradiation par faisceau d'électrons (11) à partir du côté de surface avant du substrat semi-conducteur de manière à former des défauts, qui sont formés dans tout le substrat semi-conducteur par des liaisons pendantes générées par la rupture de liaisons interatomiques d'atomes de Si constituant le substrat semi-conducteur par l'irradiation par faisceau d'électrons;
former une couche de cathode de type n+ sur la face arrière du substrat semi-conducteur,
caractérisé en ce que le procédé comprend en outre de: effectuer simultanément une implantation d'ions d'impuretés de type n (13) et une implantation d'ions hydrogène (14) à partir de la surface arrière du substrat semi-conducteur et former ainsi
la couche de cathode de type n+ et
une région implantée d'hydrogène (6), dans laquelle:

> dans la région implantée d'hydrogène (6), un premier pic de concentration (6-1) de molécules d'hydrogène et un deuxième pic de concentration (6-2) d'atomes d'hydrogène sont formés avec le deuxième pic de concentration (6-2) étant formé dans une partie plus profonde de la surface arrière du substrat semi-conducteur que le premier pic de concentration (6-1);
> le premier pic de concentration (6-1) et le deuxième pic de concentration (6-2) sont formés dans des positions plus profondes à partir de la surface arrière du substrat semi-conducteur qu'un pic de concentration (4-1) de l'impureté de type de la couche de cathode (4) ;
> le premier pic de concentration (6-1) et le deuxième pic de concentration (6-2) sont formés afin de se superposer; et
> les défauts (12) sur le côté de cathode sont récupérés localement dans la région implantée d'hydrogène (6) par l'hydrogène terminant les liaisons pendantes.

2. Procédé selon la revendication 1, dans lequel la durée de vie du porteur côté cathode est supérieure à la durée de vie du porteur du côté d'anode.

FIG.1

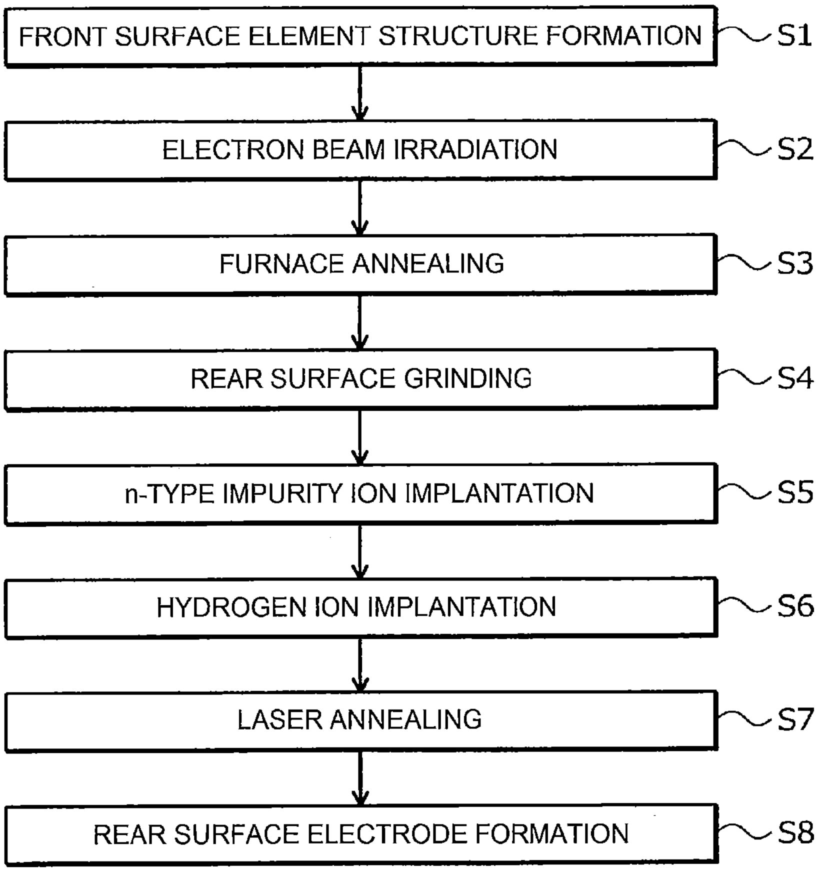

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S1
ELECTRON BEAM IRRADIATION
S2
FURNACE ANNEALING
S3
REAR SURFACE GRINDING
S4
n-TYPE IMPURITY ION IMPLANTATION
S5
HYDROGEN ION IMPLANTATION
S6
LASER ANNEALING
S7
REAR SURFACE ELECTRODE FORMATION
S8

FIG.2

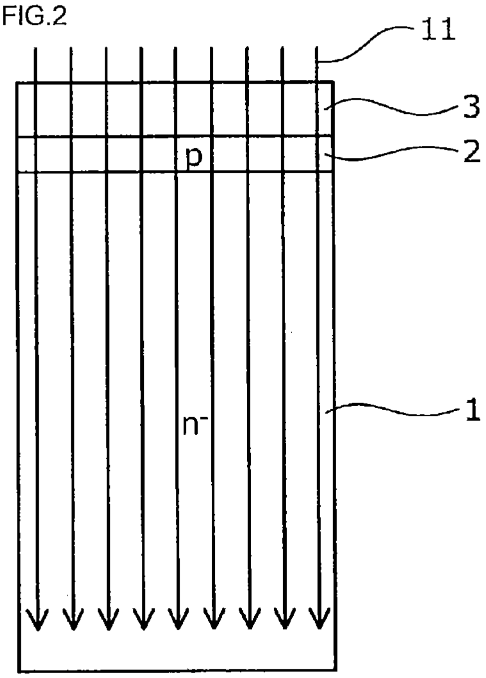

11
3
p
2
n-
1

FIG.3

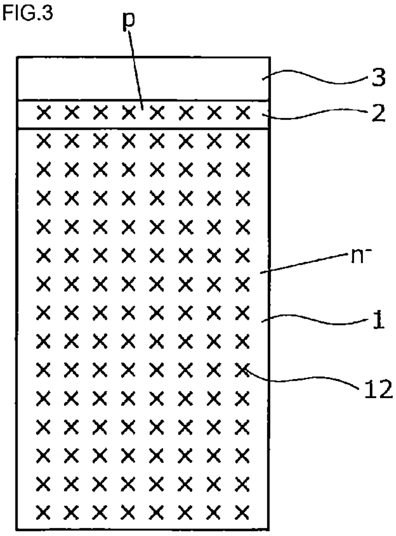


FIG.4

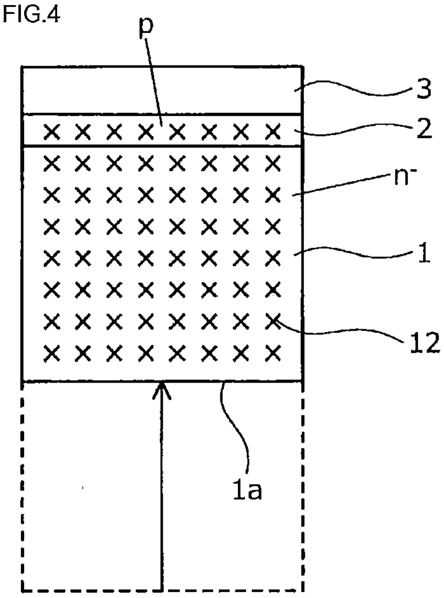


FIG.5

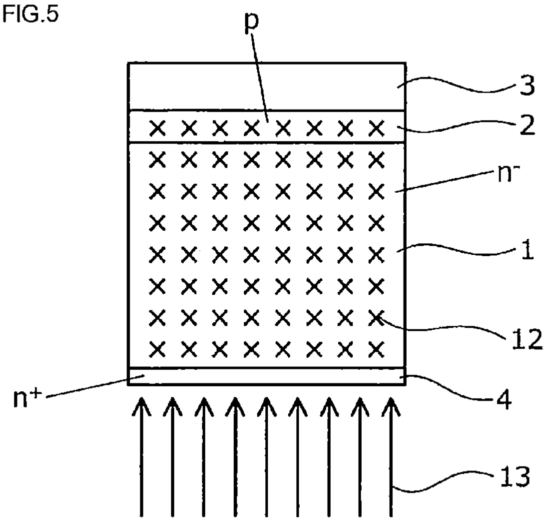


FIG.6

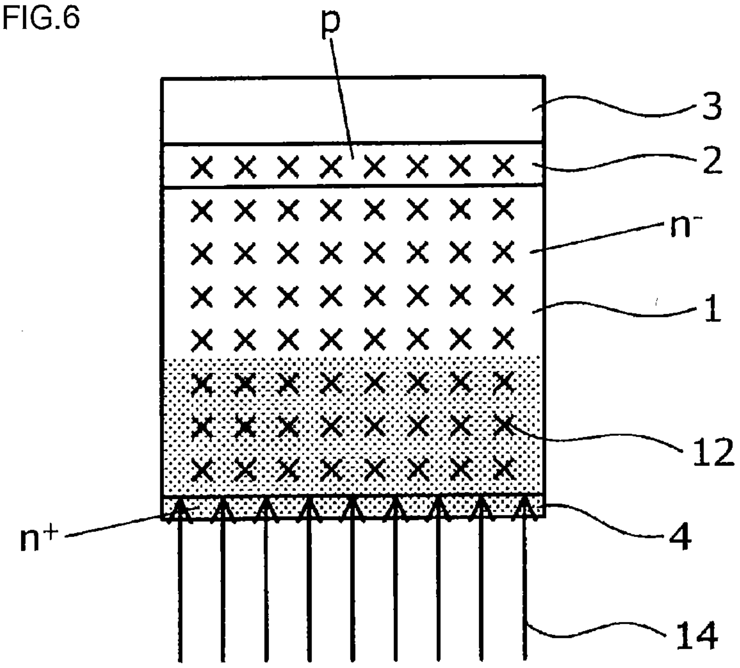


FIG.7

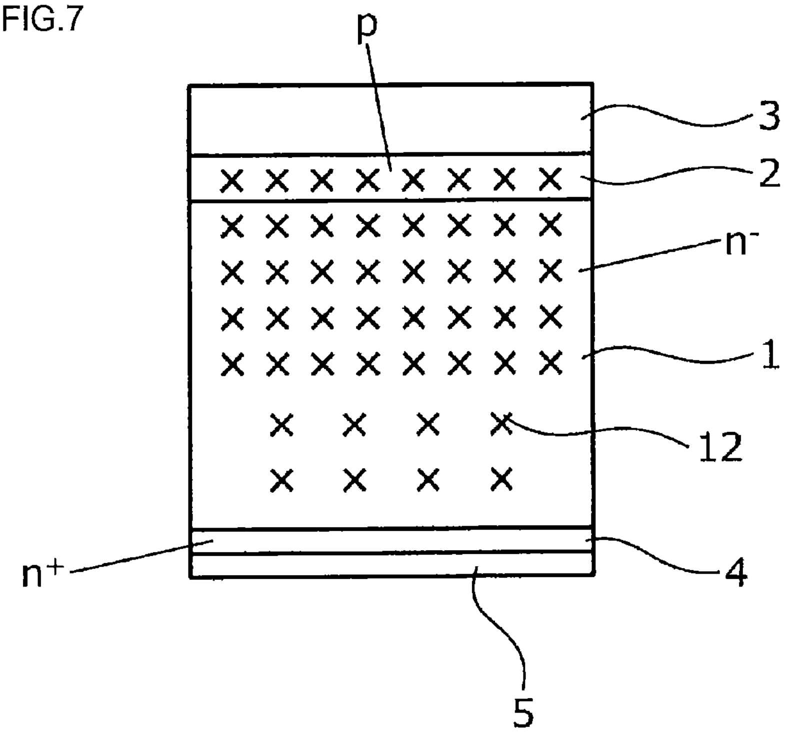


FIG.8A

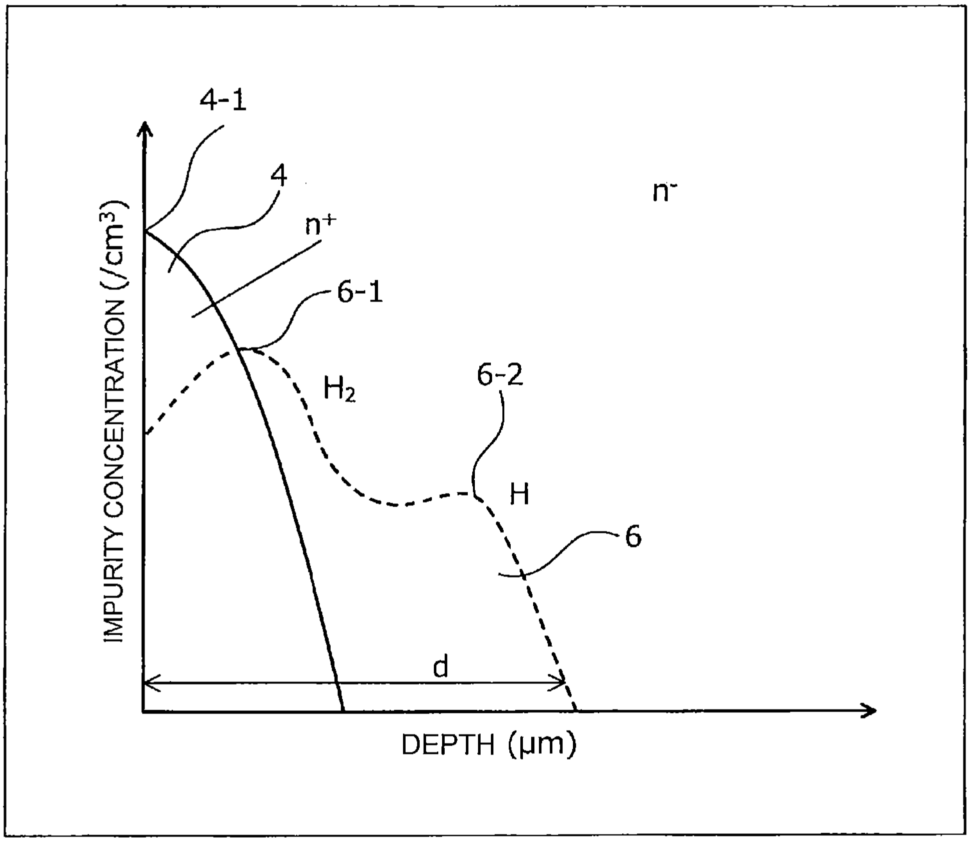


FIG.8B

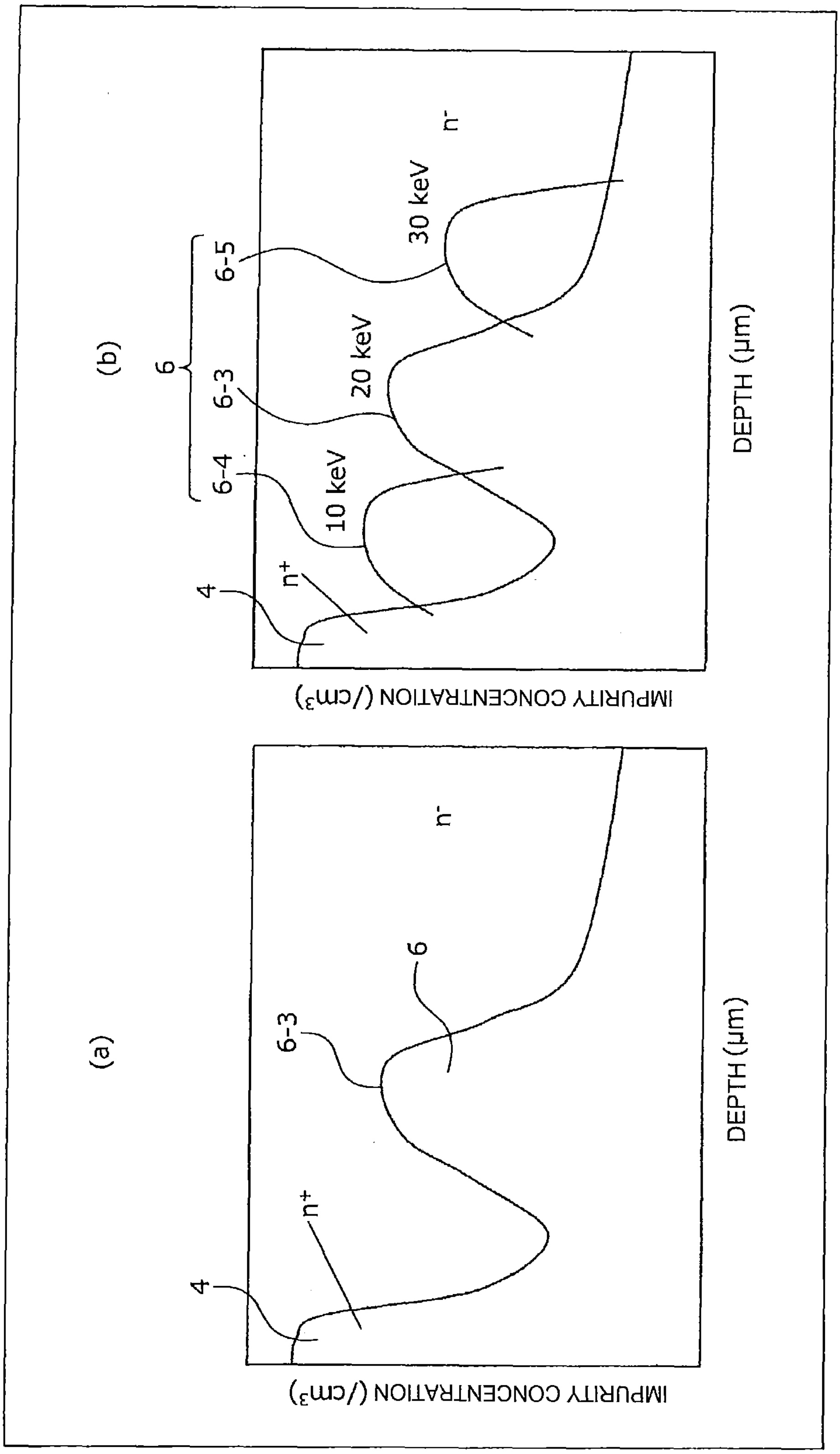

(a)
4
n+
6-3
6
n-
IMPURITY CONCENTRATION (/cm3)
DEPTH (μm)
(b)
6
6-4
6-3
6-5
10 keV
20 keV
30 keV
4
n+
n-
IMPURITY CONCENTRATION (/cm3)
DEPTH (μm)

FIG.9

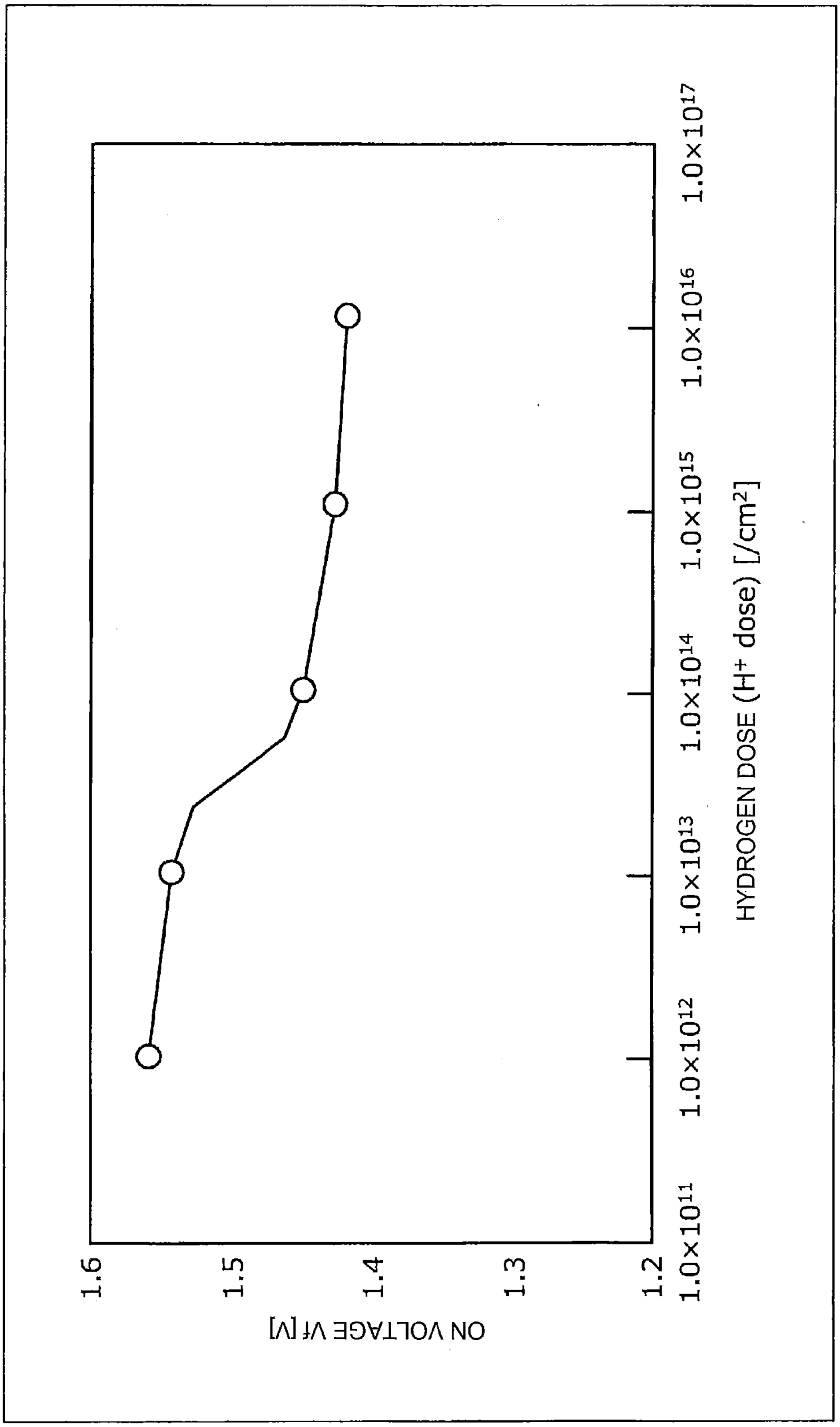

ON VOLTAGE Vf [V]
1.6
1.5
1.4
1.3
1.2
1.0×10¹¹
1.0×10¹²
1.0×10¹³
1.0×10¹⁴
1.0×10¹⁵
1.0×10¹⁶
1.0×10¹⁷
HYDROGEN DOSE (H+ dose) [/cm²]

FIG.10

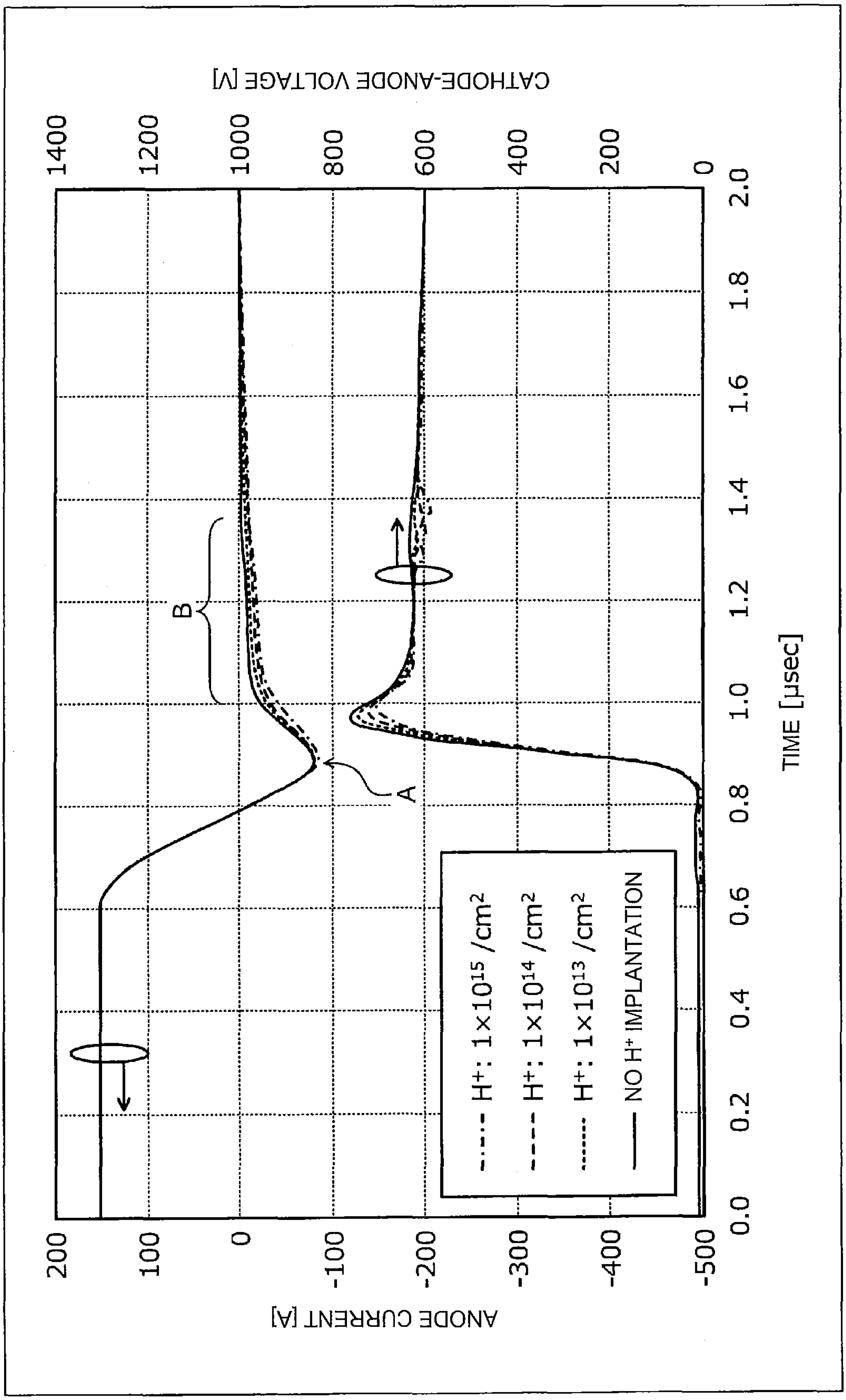

CATHODE-ANODE VOLTAGE [V]
1400
1200
1000
800
600
400
200
0
ANODE CURRENT [A]
200
100
0
-100
-200
-300
-400
-500
TIME [μsec]
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
A
B
H+: 1×10^15 /cm^2
H+: 1×10^14 /cm^2
H+: 1×10^13 /cm^2
NO H+ IMPLANTATION

FIG.11

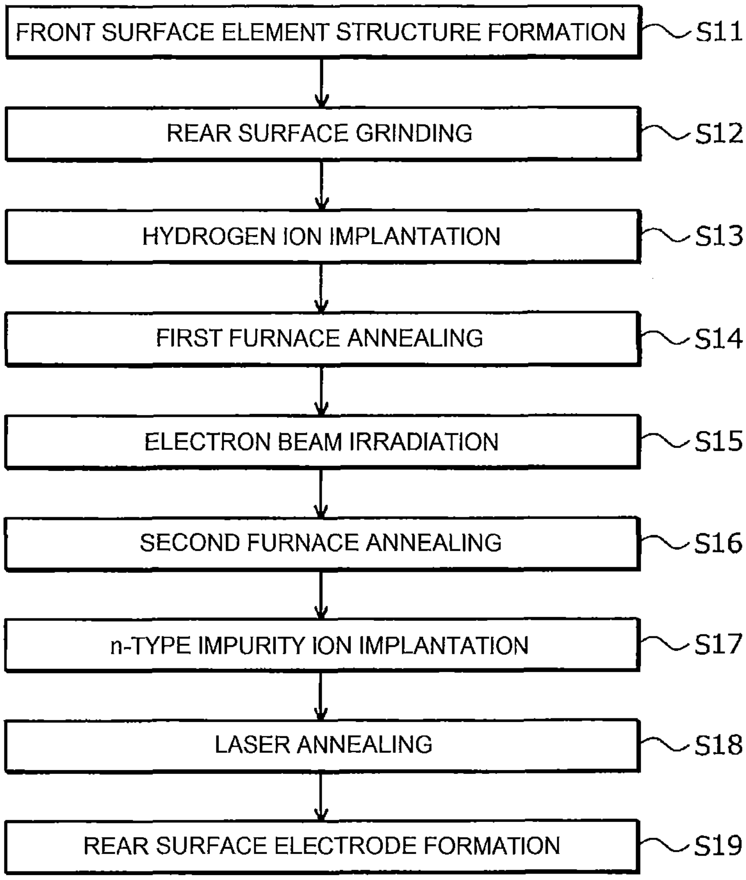


FIG.12A

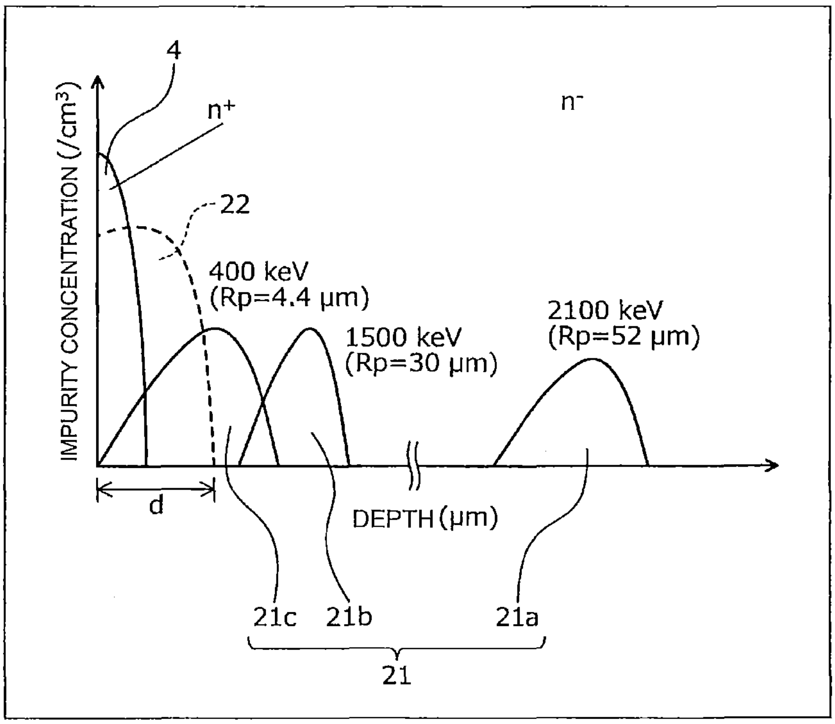


FIG.12B

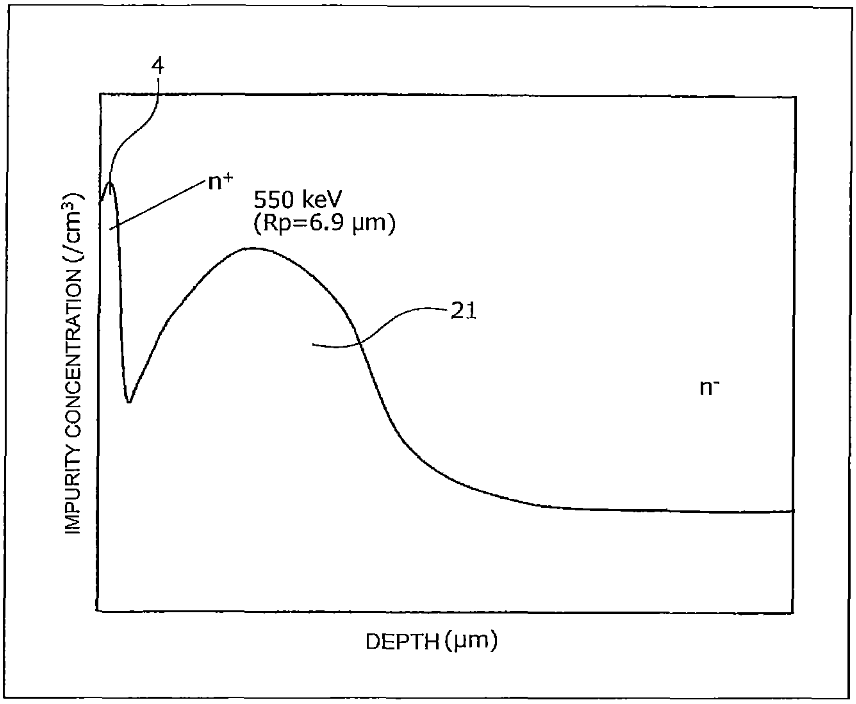


FIG.13

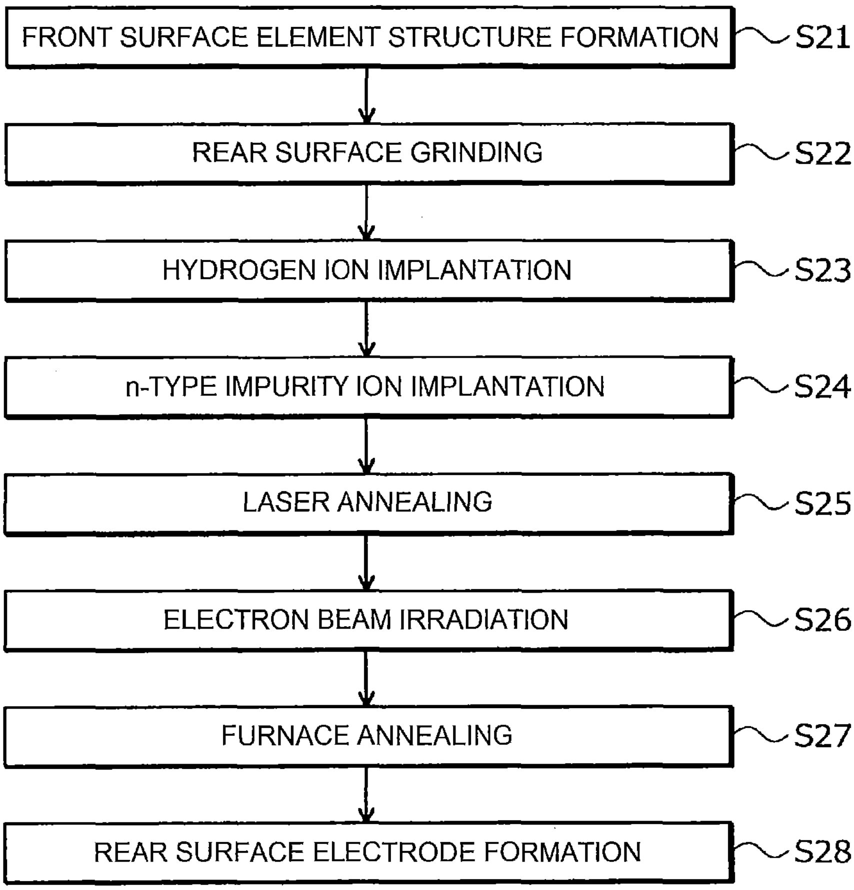


FIG.14

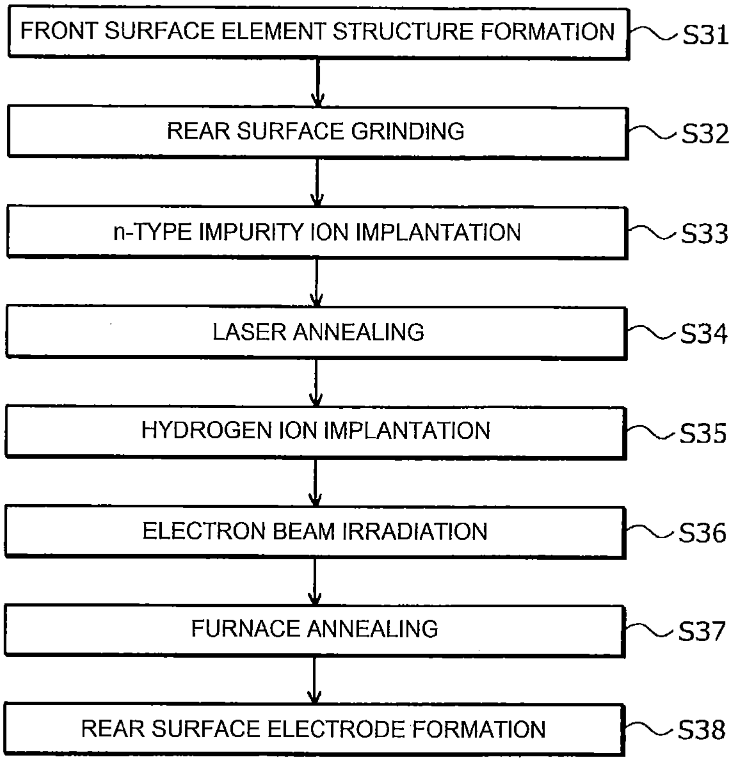

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S31
REAR SURFACE GRINDING
S32
n-TYPE IMPURITY ION IMPLANTATION
S33
LASER ANNEALING
S34
HYDROGEN ION IMPLANTATION
S35
ELECTRON BEAM IRRADIATION
S36
FURNACE ANNEALING
S37
REAR SURFACE ELECTRODE FORMATION
S38

FIG.15

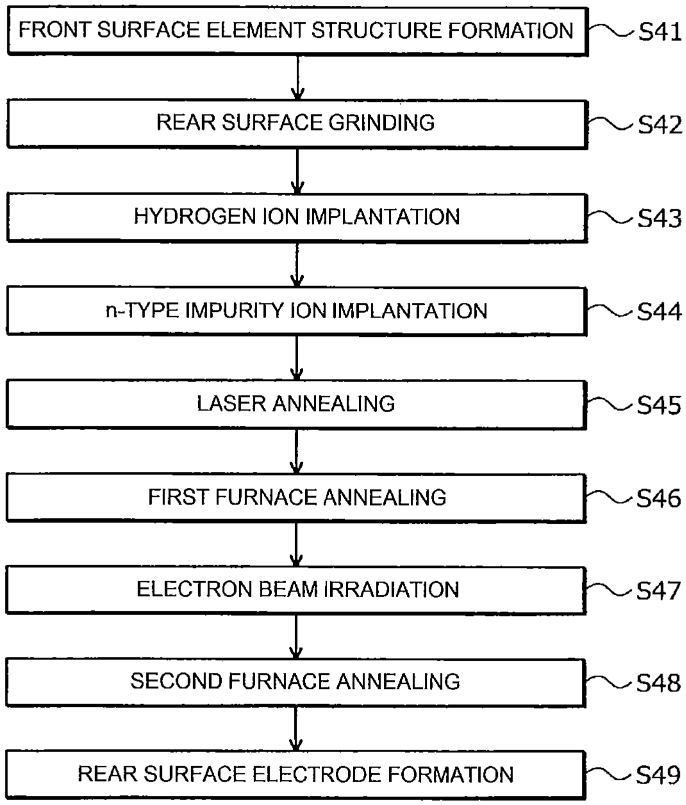

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S41
REAR SURFACE GRINDING
S42
HYDROGEN ION IMPLANTATION
S43
n-TYPE IMPURITY ION IMPLANTATION
S44
LASER ANNEALING
S45
FIRST FURNACE ANNEALING
S46
ELECTRON BEAM IRRADIATION
S47
SECOND FURNACE ANNEALING
S48
REAR SURFACE ELECTRODE FORMATION
S49

FIG.16

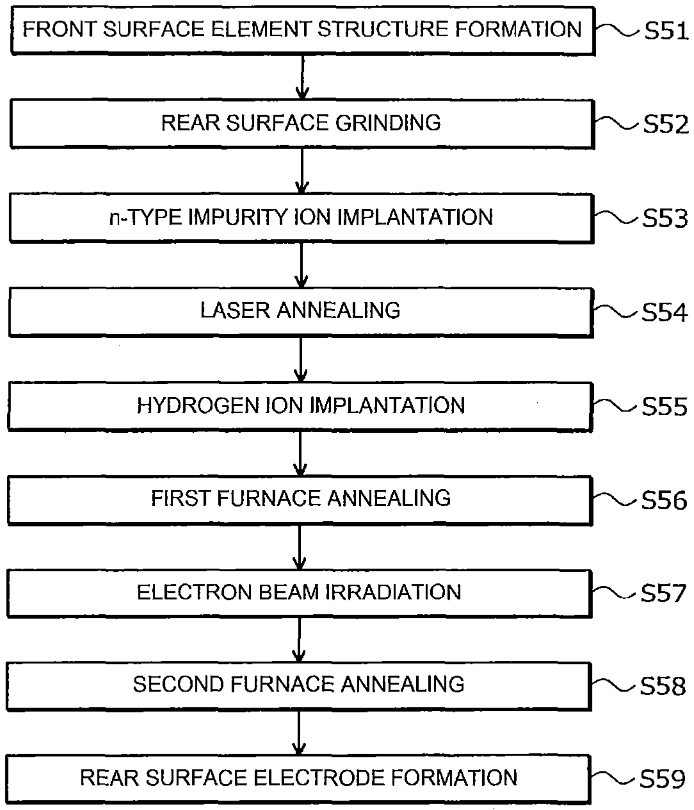

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S51
REAR SURFACE GRINDING
S52
n-TYPE IMPURITY ION IMPLANTATION
S53
LASER ANNEALING
S54
HYDROGEN ION IMPLANTATION
S55
FIRST FURNACE ANNEALING
S56
ELECTRON BEAM IRRADIATION
S57
SECOND FURNACE ANNEALING
S58
REAR SURFACE ELECTRODE FORMATION
S59

FIG.17

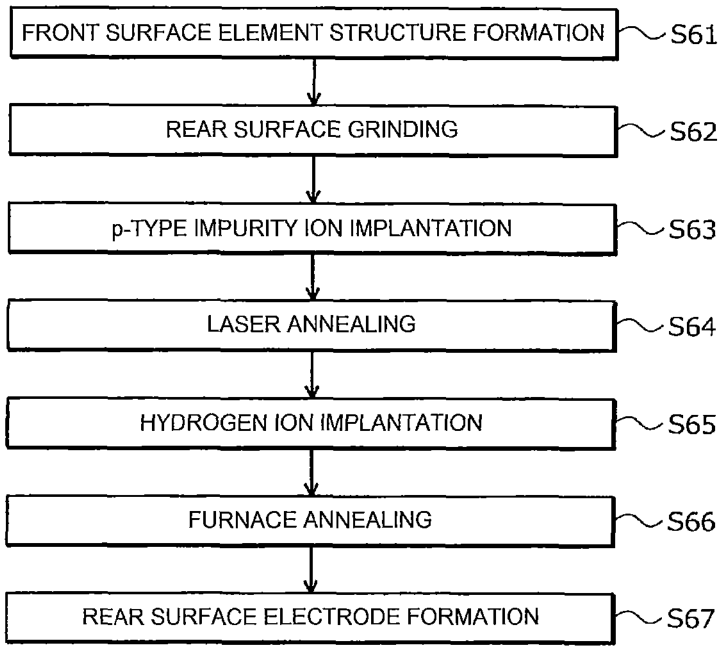

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S61
REAR SURFACE GRINDING
S62
p-TYPE IMPURITY ION IMPLANTATION
S63
LASER ANNEALING
S64
HYDROGEN ION IMPLANTATION
S65
FURNACE ANNEALING
S66
REAR SURFACE ELECTRODE FORMATION
S67

FIG.18

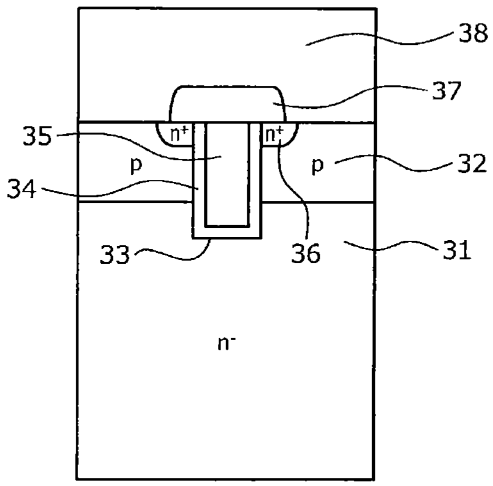


FIG.19

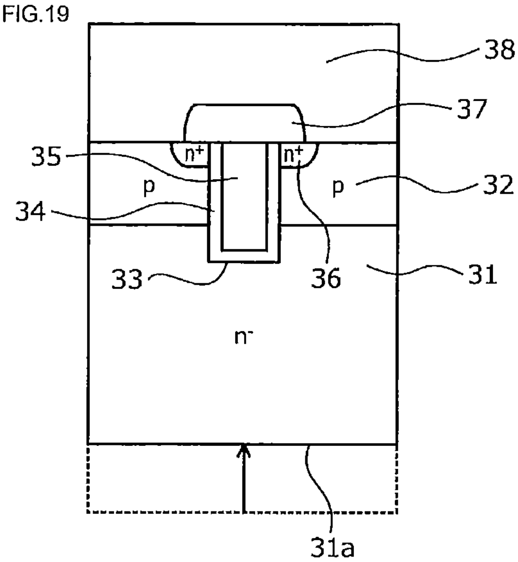


FIG.20

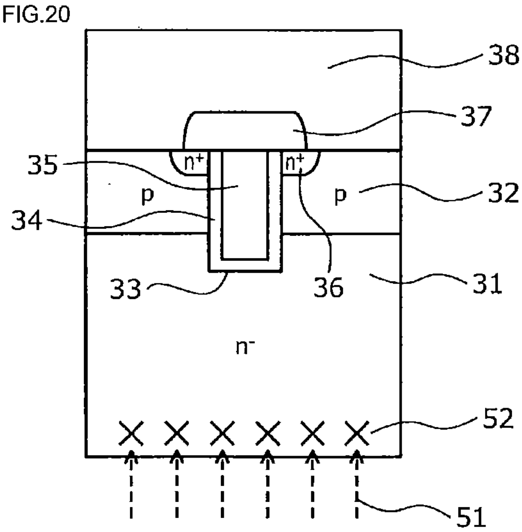


FIG.21

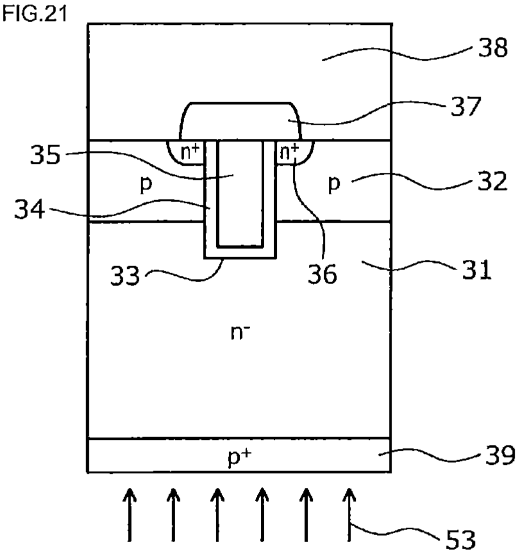


FIG.22

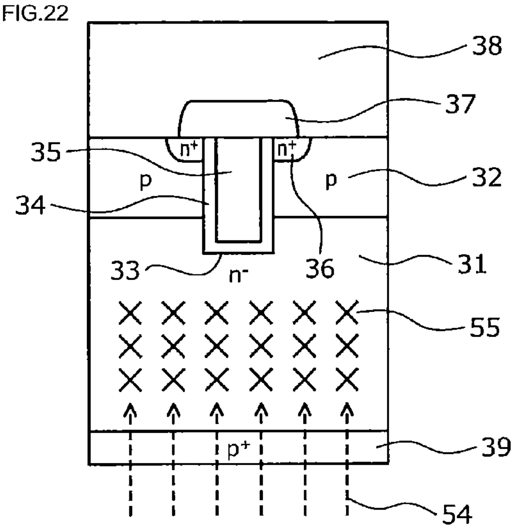


FIG.23

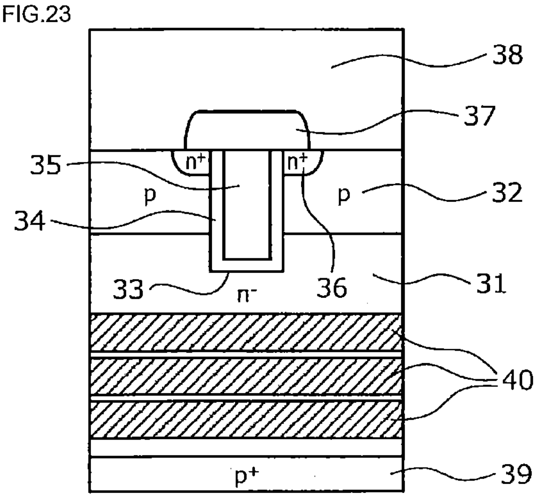


FIG.24

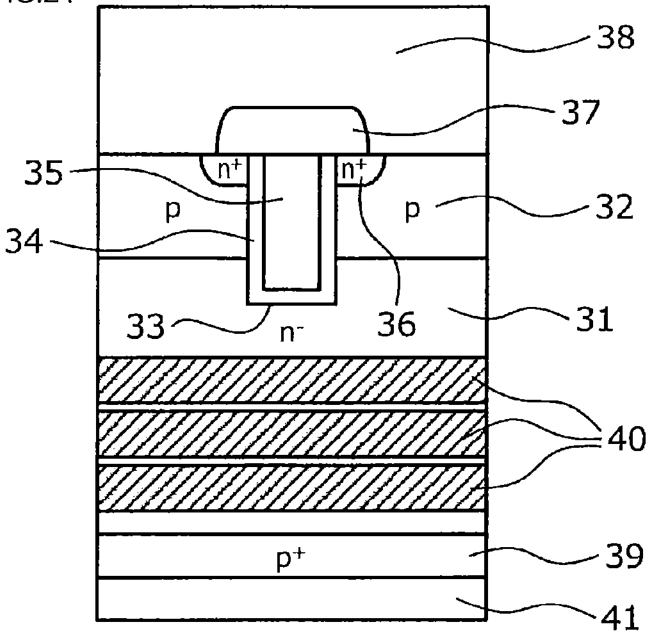

38
37
35
n+
n+
p
p
32
34
33
n-
36
31
40
p+
39
41

FIG.25

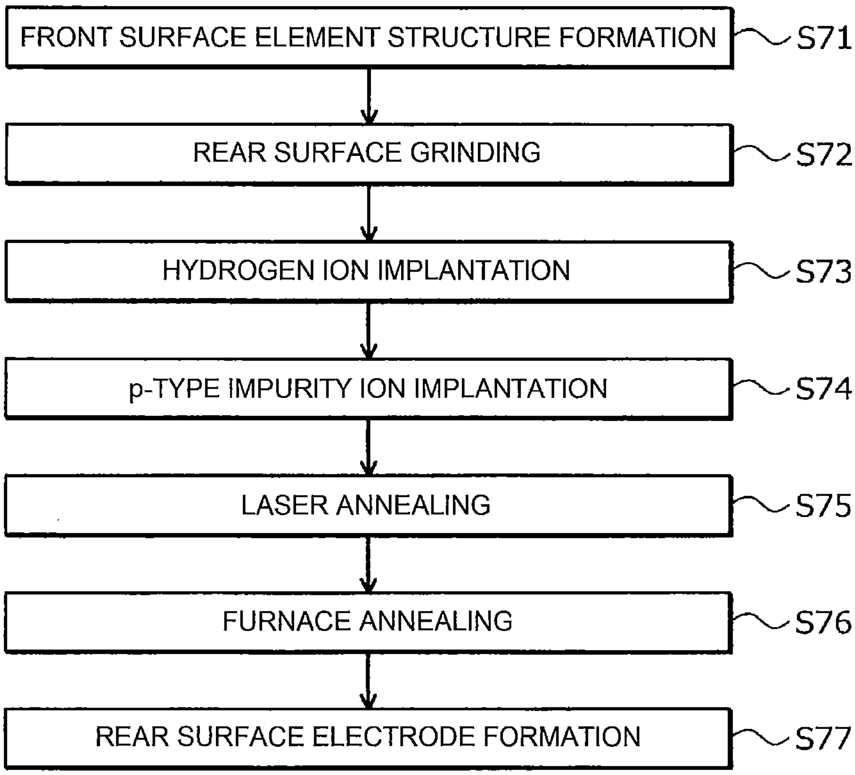

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S71
REAR SURFACE GRINDING
S72
HYDROGEN ION IMPLANTATION
S73
p-TYPE IMPURITY ION IMPLANTATION
S74
LASER ANNEALING
S75
FURNACE ANNEALING
S76
REAR SURFACE ELECTRODE FORMATION
S77

FIG.26

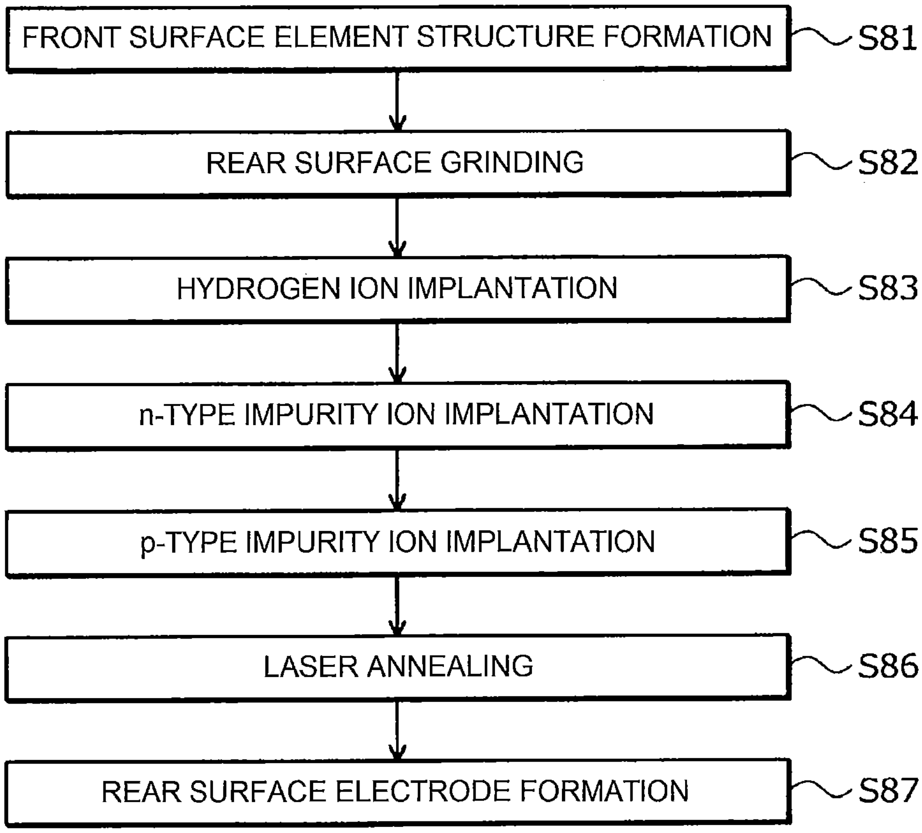

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S81
REAR SURFACE GRINDING
S82
HYDROGEN ION IMPLANTATION
S83
n-TYPE IMPURITY ION IMPLANTATION
S84
p-TYPE IMPURITY ION IMPLANTATION
S85
LASER ANNEALING
S86
REAR SURFACE ELECTRODE FORMATION
S87

FIG.27

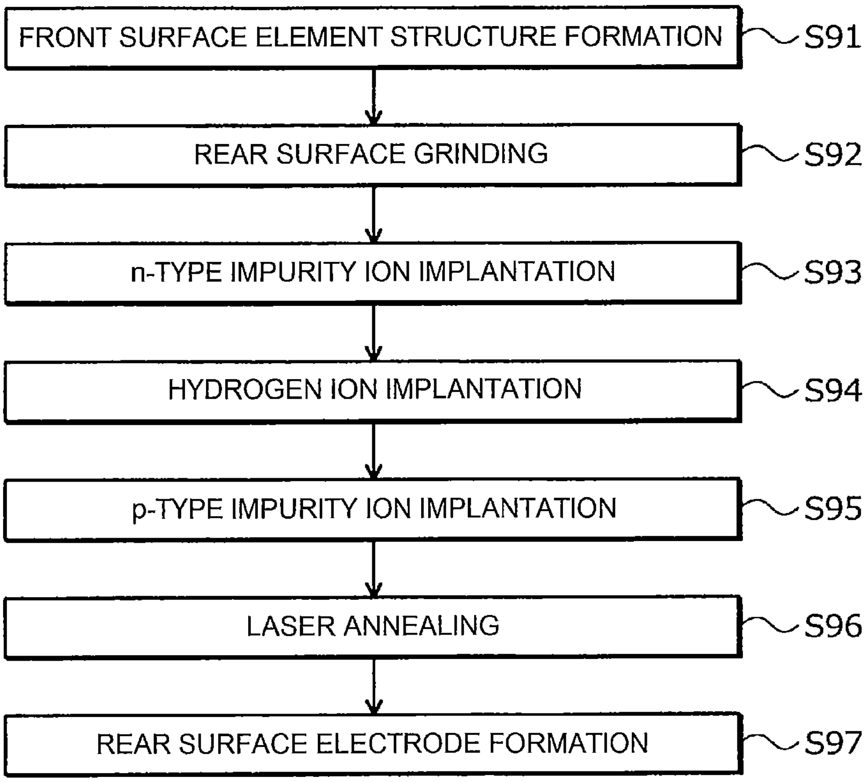

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S91
REAR SURFACE GRINDING
S92
n-TYPE IMPURITY ION IMPLANTATION
S93
HYDROGEN ION IMPLANTATION
S94
p-TYPE IMPURITY ION IMPLANTATION
S95
LASER ANNEALING
S96
REAR SURFACE ELECTRODE FORMATION
S97

FIG.28

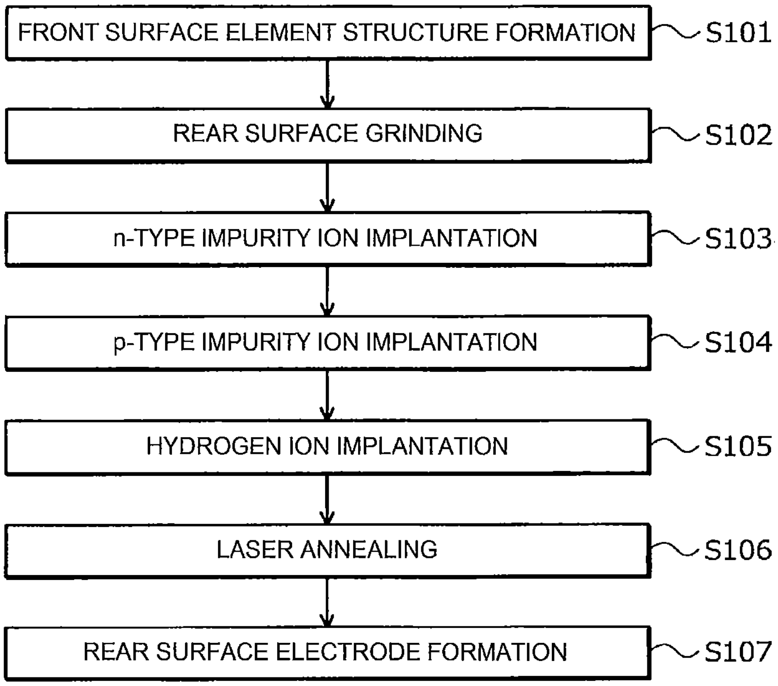


FIG.29A

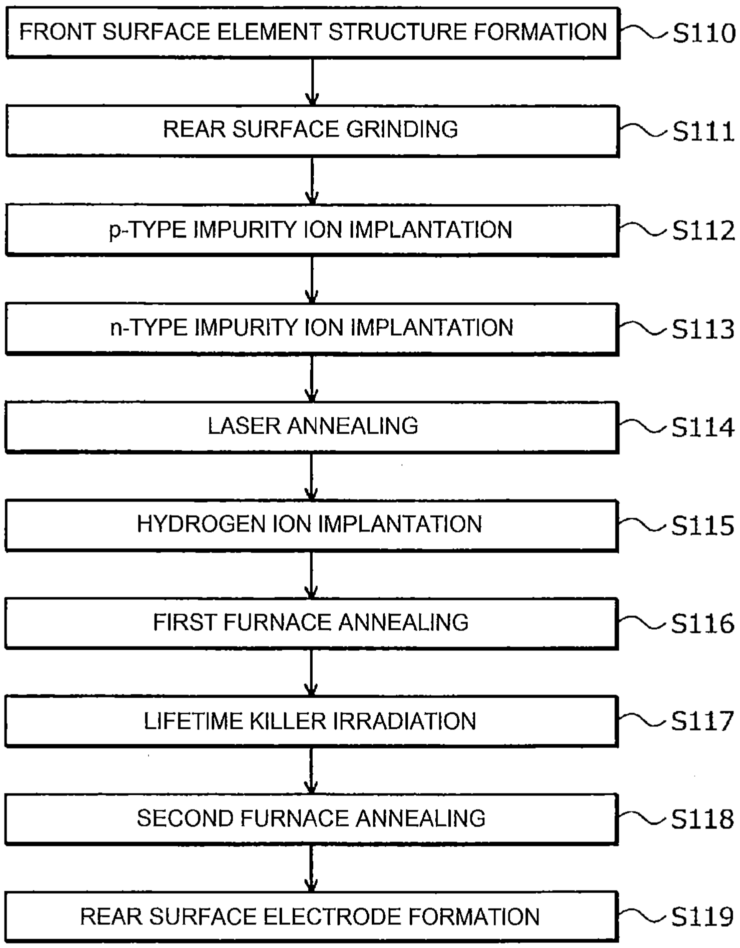


FIG.29B

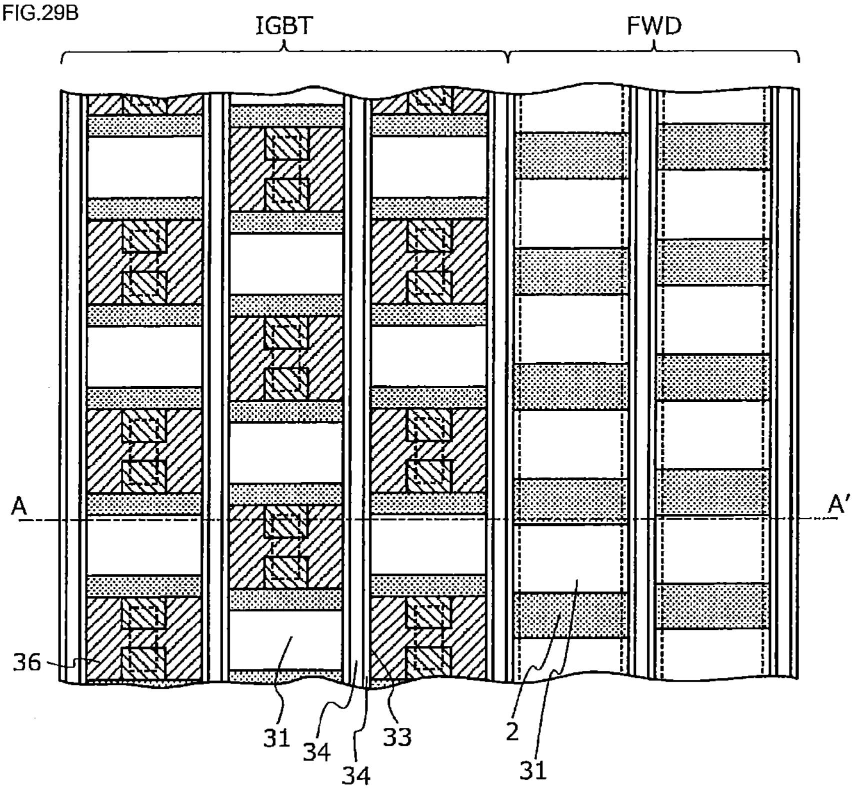


FIG.29C

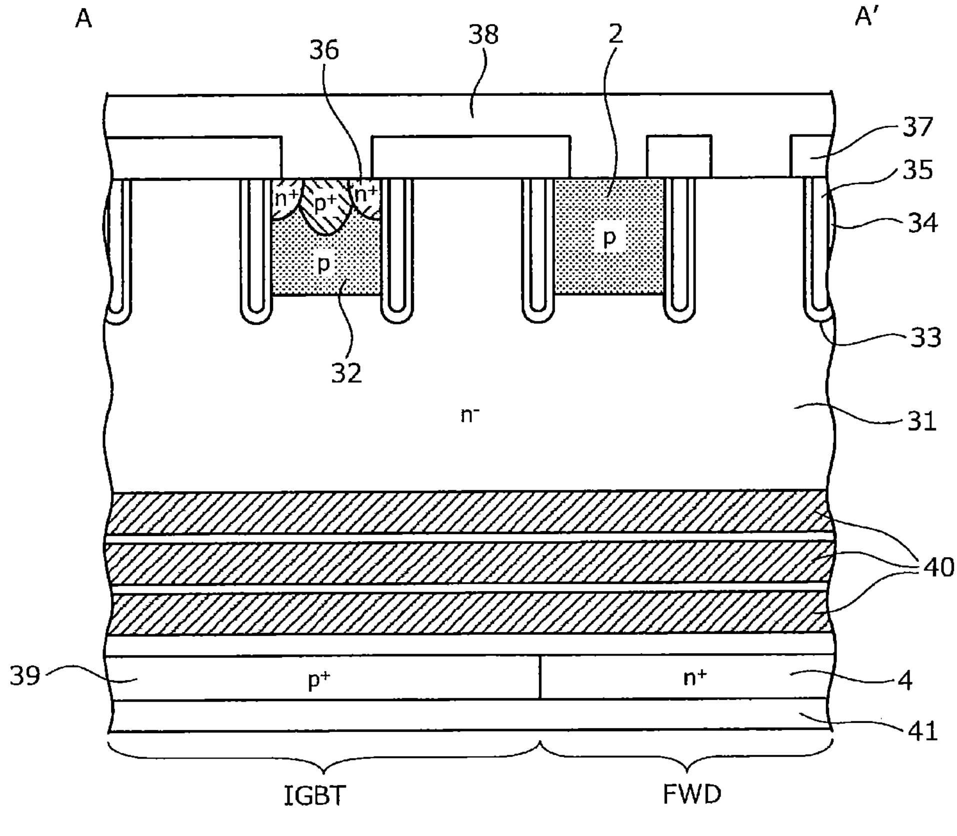


FIG.30

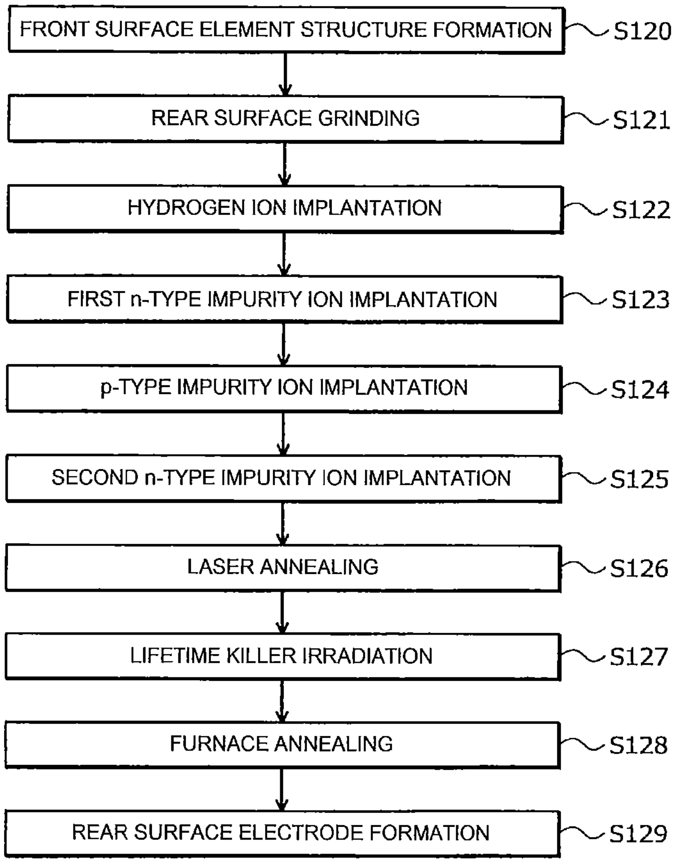

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S120
REAR SURFACE GRINDING
S121
HYDROGEN ION IMPLANTATION
S122
FIRST n-TYPE IMPURITY ION IMPLANTATION
S123
p-TYPE IMPURITY ION IMPLANTATION
S124
SECOND n-TYPE IMPURITY ION IMPLANTATION
S125
LASER ANNEALING
S126
LIFETIME KILLER IRRADIATION
S127
FURNACE ANNEALING
S128
REAR SURFACE ELECTRODE FORMATION
S129

FIG.31

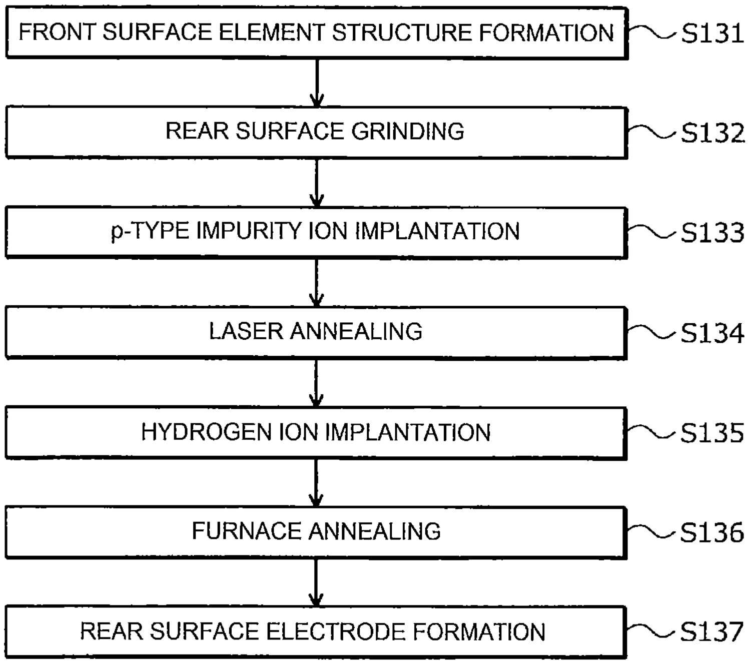

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S131
REAR SURFACE GRINDING
S132
p-TYPE IMPURITY ION IMPLANTATION
S133
LASER ANNEALING
S134
HYDROGEN ION IMPLANTATION
S135
FURNACE ANNEALING
S136
REAR SURFACE ELECTRODE FORMATION
S137

FIG.32

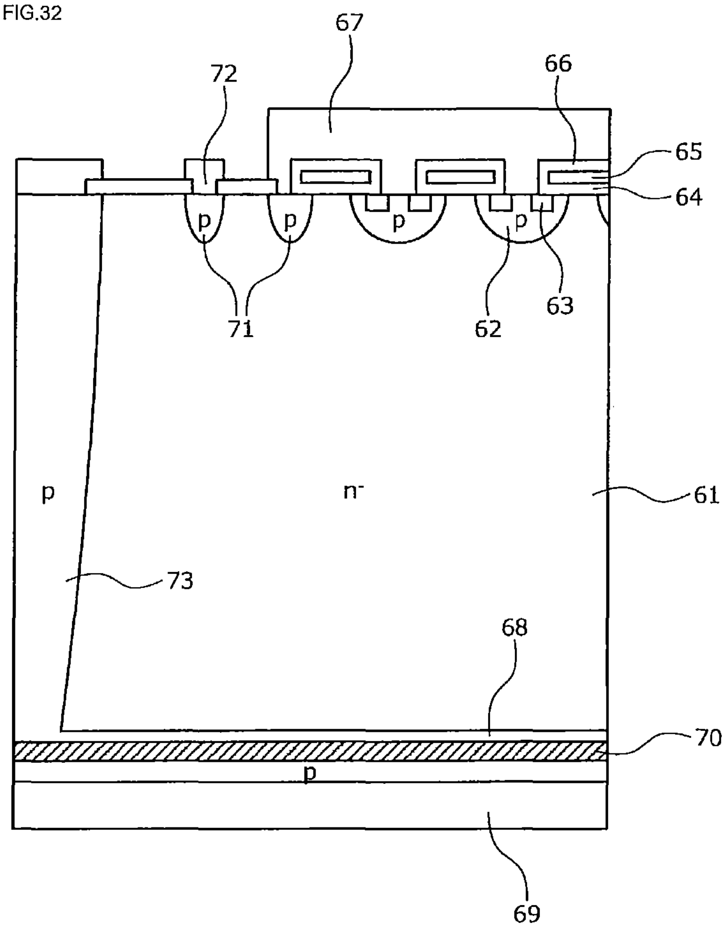

67
72
66
65
64
p
p
p
p
71
62
63
p
n-
61
73
68
70
p
69

FIG.33

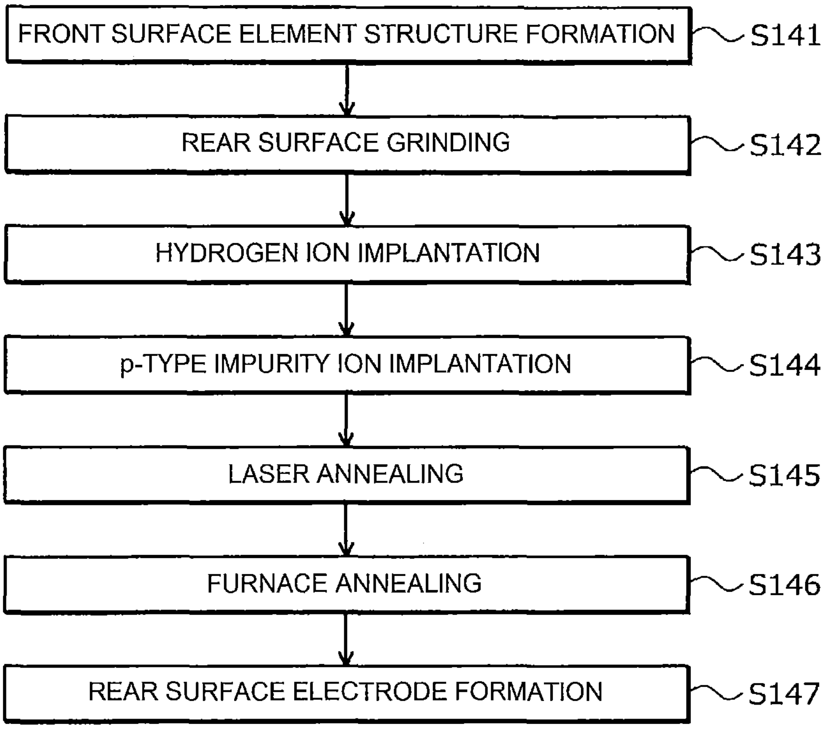

FRONT SURFACE ELEMENT STRUCTURE FORMATION
S141
REAR SURFACE GRINDING
S142
HYDROGEN ION IMPLANTATION
S143
p-TYPE IMPURITY ION IMPLANTATION
S144
LASER ANNEALING
S145
FURNACE ANNEALING
S146
REAR SURFACE ELECTRODE FORMATION
S147

FIG.34

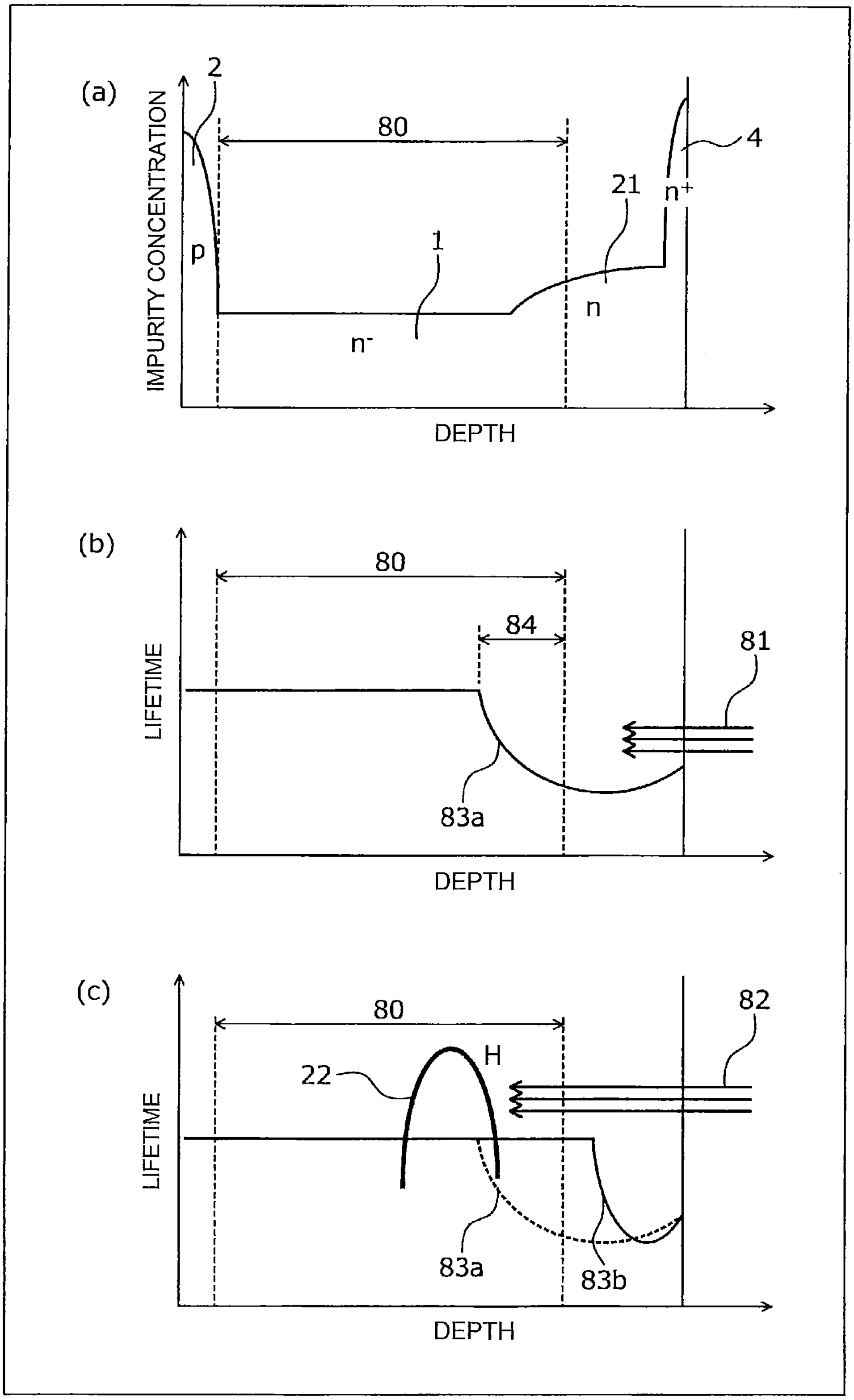

(a)
2
80
4
21
n^+
1
p
n
n^-
IMPURITY CONCENTRATION
DEPTH
(b)
80
84
81
LIFETIME
83a
DEPTH
(c)
80
82
H
22
LIFETIME
83a
83b
DEPTH

FIG.35

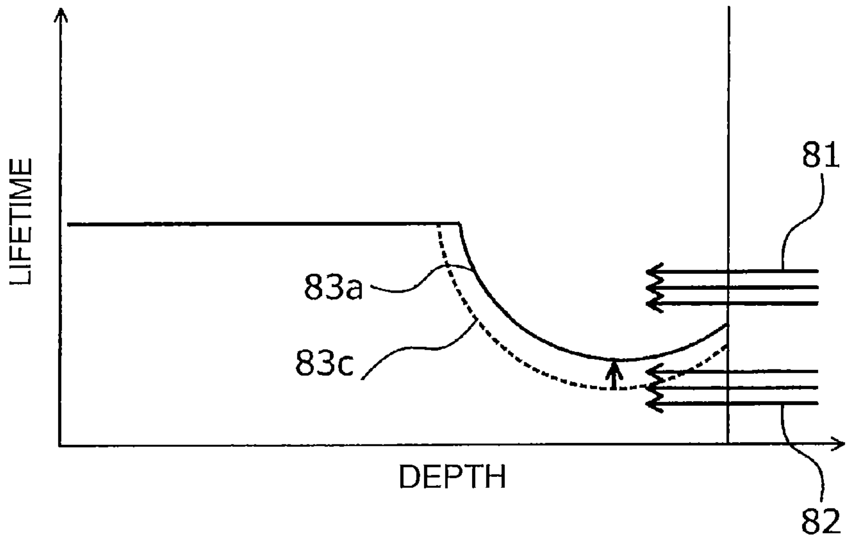
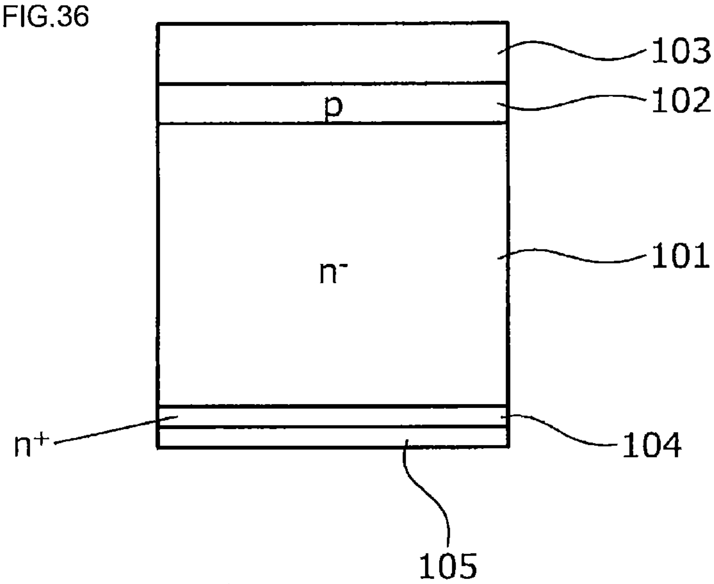


FIG.36



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- JP H08102545 A **[0009]**
- JP 2008211148 A **[0009]**
- EP 2793251 A1 **[0009]**