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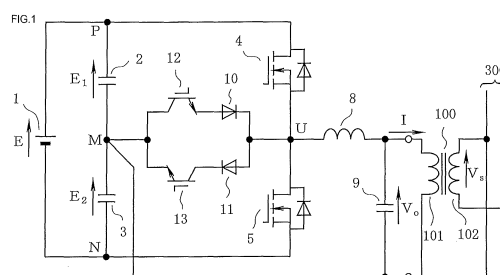
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(54) **THREE-LEVEL INVERTER**

(57) A series circuit of capacitors 2 and 3 and a series circuit of semiconductor switches 4 and 5 such as SiC-MOSFETs are connected in parallel to a direct current power source 1, and one end of a bidirectional switch formed of semiconductor switches 12 and 13, such as IGBTs, and diodes 10 and 11, such as SiC-SBDs, is connected to a series connection point (an M point) of the capacitors 2 and 3, while the other end of the bidirectional switch is connected to a series connection point of the semiconductor switches 4 and 5, thereby configuring a three-level inverter which can output three voltage levels by operating the semiconductor switches 4, 5, 12, and 13. The three-level inverter is operated so as to satisfy at least one of the condition that the peak value of an alternating current output voltage V_o is a value of 80% or more of the voltage of the capacitors 2 and 3 and the condition that an output power factor is 0.8 or more. By so doing, heretofore known inexpensive elements can be utilized for one portion of the semiconductor switches, thus achieving an increase in efficiency and a reduction in size while reducing cost.



- 1 : DIRECT CURRENT POWER SOURCE
2, 3, 9 : CAPACITOR
4, 5 : SEMICONDUCTOR SWITCH
8 : REACTOR
10, 11 : DIODE
12, 13 : SEMICONDUCTOR SWITCH
100 : TRANSFORMER
101 : PRIMARY WINDING
102 : SECONDARY WINDING
300 : POWER SYSTEM

Description

Technical Field

[0001] The present invention relates to a configuration of a three-level inverter which enables an improvement in power conversion efficiency and a reduction in the size and cost of a device.

Background Art

[0002] Fig. 6 shows one phase of circuit of a three-level inverter disclosed in PTL 1.

[0003] In Fig. 6, 1 is a direct current power source such as a solar cell, and a voltage E thereof is divided into voltages E_1 and E_2 (normally, $E_1 = E_2$) by capacitors 2 and 3 connected in series.

[0004] Semiconductor switches (hereafter also referred to simply as switches) 4 to 7, each formed of a MOSFET, can control a conduction/interruption of a forward current, and attain a conduction state always for a reverse current. The switches 6 and 7, connected in series in directions opposite to each other, configure a bidirectional switch which can control a conduction/interruption of both forward and reverse currents. Herein, the switches 4 and 5 are referred to as upper and lower arms, and a series circuit of the switches 6 and 7 as an intermediate arm, for the sake of convenience. An LC filter is configured of a reactor 8 and a capacitor 9, and the output terminals of the two ends of the capacitor 9 are interconnected to a power system 300 via a transformer 100.

[0005] A U point (an alternating current terminal) in Fig. 6 attains the same potential as a P point by turning on the switch 4, an N point by turning on the switch 5, and an M point by turning on the switches 6 and 7 that configure a bidirectional switch. That is, the circuit can output three voltage levels by the switches 4 to 7 attaining an on-state, and has the characteristics that it is sufficient that the breakdown voltage of the switches 6 and 7 is 1/2 of that of the switches 4 and 5.

[0006] Fig. 7 shows output voltage waveforms of the circuit, wherein an output voltage V_o is controlled to form a sine wave by causing the pulse train of a U-M voltage having the three voltage levels to pass through the LC filter.

[0007] When using the circuit of Fig. 6 as an interconnection inverter for solar power generation, the voltage E of the direct current power source (solar cell) 1 fluctuates greatly in accordance with environmental conditions.

[0008] Meanwhile, the alternating current output voltage V_o is matched with a system voltage V_s by the transformer 100. The system voltage V_s fluctuates within a slight range, but is approximately constant, and as the transformer ratio of the transformer 100 is also constant unless a tap changing is carried out, it is necessary to keep the alternating current output voltage V_o at a substantially constant value proportional to the system volt-

age V_s .

[0009] The circuit of Fig. 6 is one kind of voltage inverter, and as the alternating current output voltage V_o is controllable within a range in which the peak value thereof is equal to or less than a direct current input voltage, the positive peak of V_o is equal to or less than E_1 , and the negative peak is equal to or less than E_2 , as shown in Fig. 7.

[0010] Consequently, V_o is taken to be a voltage which can be output even when E_1 and E_2 are minimum values within an operating range, and V_o is kept constant by determining the transformer ratio of the transformer 100 based on the size of V_o , and by widening the pulse width of PWM control when E_1 and E_2 are low ((a) of Fig. 7) and narrowing the pulse width when E_1 and E_2 are high ((b) of Fig. 7).

[0011] Fig. 8 shows a phase relationship between the alternating current output voltage V_o and a current I .

[0012] In the interconnection inverter for solar power generation, in order to supply power generated therein to the power system 300, a power factor 1 operation wherein the phase of the system voltage V_s , that is, the phase of the output voltage V_o is approximately coincident with the phase of the output current I , as shown in (a) of Fig. 8, is carried out, but there is also a case in which by deliberately injecting reactive power, a polarity non-coincidence period T_c is created to reduce the power factor, as shown in (b) of Fig. 8, thus carrying out a voltage adjustment at an interconnection point.

[0013] Current paths (1) to (4) shown in (a) of Fig. 6 previously described are in the cases of the power factor 1 in which the output voltage and the output current are coincident in polarity, wherein (1) and (3) are the paths in a voltage application period T_a in Fig. 7, and (2) and (4) are the paths in a freewheeling period T_b .

[0014] When a direct current voltage is low, as in (a) of Fig. 7, a time ratio at which the switch 4 or 5 conducts is high, and a conduction loss ratio in the upper and lower arms is high, in particular, in the vicinity of the peak of V_o . When the direct current voltage is high, as shown in (b) of Fig. 7, a time ratio at which the switch 6 or 7 conducts is high, and a conduction loss ratio in the intermediate arm is high. When the direct current voltage is set so as to be always high using a voltage fluctuation compensation circuit to be described hereafter, as shown in (c) of Fig. 7, a conduction loss ratio in the upper and lower arms is high in the same way as in (a) of Fig. 7.

[0015] A shift from the path (1) to (2) in (a) of Fig. 6 is carried out by turning off the switch 4. Also, a shift from the path (2) to (1) is carried out by turning on the gate of the switch 7, turning off the gate of the switch 6 in advance, and after blocking a short circuit current in a path from the switch 4 through the switch 6 (the main body portion of the MOSFET) to the switch 7, turning on the gate of the switch 4. With the turning on of the switch 4, a reverse parallel diode of the switch 6 interrupts a current by reverse recovery. Shifts from the path (3) to (4) and from (4) to (3) are the same as above because the pairs

of shifts are symmetrical operations. Consequently, in (a) of Fig. 6, the switch 4 or 5 generates a turn-on loss or a turn-off loss, and the switch 6 or 7 generates a reverse recovery loss.

[0016] Meanwhile, paths (5) to (8) shown in (b) of Fig. 6 are in a case in which the output voltage and the output current are not coincident in polarity, wherein (5) and (7) are the paths in the voltage application period T_a in Fig. 7, and (6) and (8) are the paths in the freewheeling period T_b . Without going into detail, in (b) of Fig. 6, the switch 6 or 7 generates a turn-on loss and a turn-off loss, and the switch 4 or 5 generates a reverse recovery loss.

[0017] As in the above, in this heretofore known technology, the ratio of conduction losses, and the contents of switching losses, generated by respective semiconductor switches vary depending on operating conditions.

Citation List

Patent Literature

[0018] PTL 1: JP-A-2010-288415 (Fig. 3, etc.)

Summary of Invention

Technical Problem

[0019] As a semiconductor switch which is applied in the circuit of Fig. 6, in recent years, a semiconductor switching element, such as a MOSFET made of SiC (silicon carbide) (hereafter referred to as a SiC-MOSFET), which can operate fast is being put into practical use. This kind of new type element also has the advantages that a fast switching is possible, a conduction loss is low for forward and reverse currents, it is possible to reduce the size of the LC filter by setting a switching frequency to be high, and the like, compared with a heretofore known IGBT (insulated gate bipolar transistor) made of silicon.

[0020] However, a new type element such as a SiC-MOSFET has the problem that it is expensive compared with a heretofore known product and that the use of this kind of new type element for all the switches 4 to 7 leads to an increase in the cost of a device.

[0021] Therefore, a problem to be solved by the invention is to provide a three-level inverter which enables an increase in efficiency and a reduction in size while reducing cost by utilizing heretofore known inexpensive elements for one portion of semiconductor switches.

Solution to Problem

[0022] In order to solve the heretofore described problem, the invention according to claim 1 is a three-level inverter including:

a first semiconductor switch and second semiconductor switch which can control a conduction/interruption of a forward current by applying an on-signal or an off-signal to a control terminal, and which attain a conduction state always for a reverse current, wherein

a series circuit of a first capacitor and second capacitor and a series circuit of the first semiconductor switch and second semiconductor switch are connected in parallel to a direct current power source, wherein

one end of a bidirectional switch which can control a conduction/interruption of both forward and reverse currents is connected to a series connection point of the first capacitor and second capacitor, and the other end of the bidirectional switch is connected to a series connection point of the first semiconductor switch and second semiconductor switch, wherein the bidirectional switch has:

a third semiconductor switch and fourth semiconductor switch which can control a conduction/interruption of a forward current by applying an on-signal or an off signal to a control terminal, and which attain one of a conduction state always for a reverse current, an interruption state always for the reverse current, or a non-conduction state having no breakdown voltage; a first diode connected in series to the third semiconductor switch; and a second diode connected in series to the fourth semiconductor switch, the bidirectional switch being configured by connecting a series circuit of the third semiconductor switch and first diode, and a series circuit of the fourth semiconductor switch and second diode, in parallel in opposite directions, and wherein

the three-level inverter can output three voltage levels by operating the first to fourth semiconductor switches, the three-level inverter being operated

so as to satisfy at least one of the condition that the peak value of an alternating current output voltage is a value of 80% or more of the voltage of the first capacitor or second capacitor and the condition that an output power factor is 0.8 or more.

[0023] In the invention according to claim 2, the three-level inverter described in claim 1 is such that the first semiconductor switch and the second semiconductor switch are each configured of a semiconductor switching element made of SiC (silicon carbide), or are each configured of a reverse parallel circuit of a semiconductor switching element made of SiC and a Schottky barrier diode made of SiC (a SiC-SBD).

[0024] In the invention according to claim 3, the three-level inverter described in claim 1 or 2 is such that IGBTs or MOSFETs made of silicon are used as the third semiconductor switch and fourth semiconductor switch, and

diodes whose reverse recovery time is equal to or shorter than a switching time of the first semiconductor switch or second semiconductor switch are used as the first diode and second diode.

[0025] In the invention according to claim 4, the three-level inverter described in claim 3 is characterized in that the first diode and the second diode are SiC-SBDs.

[0026] The invention according to claim 5 includes, between the direct current power source and the series circuit of the first capacitor and second capacitor, a voltage fluctuation compensation circuit which, when there is a voltage fluctuation in the direct current power source, stabilizes a voltage across the series circuit by compensating for the voltage fluctuation of the direct current power source.

[0027] As described in claim 6, the invention may be such that the first semiconductor switch and the second semiconductor switch are housed in a first module, the third semiconductor switch and the fourth semiconductor switch are housed in a second module, and the first diode and the second diode are housed in a third module, and that the first to third modules are connected by a conductor bar of a low inductance.

[0028] Also, as described in claim 7, the invention may be such that the first semiconductor switch and the second semiconductor switch are housed in a first module, and the third semiconductor switch, the first diode, the fourth semiconductor switch, and the second diode are housed in a fourth module, and that the first module and the fourth module are connected by a conductor bar of a low inductance.

[0029] Furthermore, as described in claim 8, the invention may be such that the first semiconductor switch and the second semiconductor switch are housed in a first module, the third semiconductor switch and the first diode are housed in a fifth module, and the fourth semiconductor switch and the second diode are housed in a sixth module, and that the first, fifth and sixth modules are connected by a conductor bar of a low inductance.

Advantageous Effects of Invention

[0030] According to the invention, even when heretofore known inexpensive elements are used for half of the semiconductor switches configuring the three-level inverter, it is possible to obtain efficiency substantially equal to that when new type elements are used for all the semiconductor switches, and there is no possibility of causing a reduction in power conversion efficiency or an increase in the size of the device, either, as a result of this.

Brief Description of Drawings

[0031]

[Fig. 1] Fig. 1 is a circuit diagram showing a first embodiment of the invention.

[Fig. 2] Fig. 2 is a circuit diagram showing a second embodiment of the invention.

[Fig. 3] Fig. 3 gives circuit diagrams showing configuration examples of an intermediate arm of each embodiment.

[Fig. 4] Fig. 4 gives configuration diagrams wherein semiconductor switches and diodes in each embodiment are modularized.

[Fig. 5] Fig. 5 gives illustrations of layout and wiring structures using the modules of Fig. 4.

[Fig. 6] Fig. 6 is a circuit diagram of one phase of a three-level inverter disposed in PTL 1.

[Fig. 7] Fig. 7 gives waveform diagrams of a U-M voltage and alternating current output voltage of the circuit of Fig. 6.

[Fig. 8] Fig. 8 gives waveform diagrams showing a phase relationship between an alternating current output voltage and current of the circuit of Fig. 6.

Description of Embodiments

[0032] Hereafter, a description will be given, along the drawings, of embodiments of the invention.

[0033] Fig. 1 is a circuit diagram showing a first embodiment of the invention. In Fig. 1, a series circuit of a first capacitor 2 and second capacitor 3 (the respective voltages of the two capacitors are taken as $E_1=E_2$) and a series circuit of a first semiconductor switch 4 and second semiconductor switch 5 such as SiC-MOSFETs, which can operate fast, are connected in parallel to a direct current power source 1 (the voltage is taken as E) such as a solar cell. The series circuit of the semiconductor switches 4 and 5 is referred to as upper and lower arms in the same way as in Fig. 6.

[0034] Also, hereafter, signs 4 and 5 will be described as being MOSFETs.

[0035] A series circuit of a reactor 8 and capacitor 9, configuring an LC filter, is connected between a series connection point (a U point) of the MOSFETs 4 and 5 and a series connection point (an M point) of the capacitors 2 and 3, and a primary winding 101 of a transformer 100 is connected across the capacitor 9. Also, a secondary winding 102 of the transformer 100 is connected to a power system 300.

[0036] A series circuit of a third semiconductor switch 12 and first diode 10 and a series circuit of a fourth semiconductor switch 13 and second diode 11 are connected in parallel to each other between the M point and the U point, and an intermediate arm is configured of the semiconductor switches 12 and 13 and diodes 10 and 11. Herein, the semiconductor switches 12 and 13 are elements which can control a conduction/interruption of a forward current and do not depend on any characteristics upon a reverse current, and IGBTs made of, for example, silicon are used as the elements. Hereafter, signs 12 and 13 will be described as being IGBTs.

[0037] The diodes 10 and 11 are fast diodes, having a low reverse recovery loss, whose reverse recovery time

is equal to or shorter than a switching time of the semiconductor switch 4 or semiconductor switch 5, and for example, SiC-SBDs can be used as the diodes. Of course, the diodes 10 and 11 do not have to be SiC-SBDs as long as they are fast diodes having a low reverse recovery loss.

[0038] Herein, the circuit of Fig. 1 is of a configuration such as to output a single-phase alternating current voltage, but may be configured in such a way as to output a three-phase alternating current voltage by connecting three phases of upper and lower arms formed of the respective semiconductor switches 4 and 5 in parallel and connecting the intermediate arms, each formed of the semiconductor switches 12 and 13, between the series connection point of the semiconductor switches 4 and 5 of the respective upper and lower arms and the M point.

[0039] As applicable conditions of the circuit, it is supposed that the voltage fluctuation range of the direct current power source 1 can be reduced by some means, and consequently, that the rated value of an alternating current output voltage V_o does not have to be set to be small taking into account a drop in direct current voltage. In this case, it is supposed that the circuit is operated with the peak value of the alternating current output voltage V_o set so as to be 80[%] or more of the direct current E_1 or E_2 , wherein the fluctuation range of the direct current voltage is taken as 10[%] or less, and an amount reduced due to the upper limit of the pulse width at the U point and to a drop in voltage in the circuit is taken as 10[%] or less.

[0040] The U-M voltage and alternating current output voltage V_o at this time are as shown in (c) of Fig. 7 previously described, and a freewheeling period T_b , in which the intermediate arm conducts, becomes significantly shorter than in (b) of Fig. 7. Herein, two elements' worth of forward voltage drop occurs when the intermediate arm is configured of a series circuit of IGBTs and diodes, as shown in Fig. 1. The same situation also applies in the circuit of Fig. 6, and as the intermediate arm exhibits low resistance characteristics in both forward and reverse directions when using SiC-MOSFETs in the intermediate arm, it is possible to reduce the forward voltage drop by increasing the number of parallel connections.

[0041] Meanwhile, an IGBT and a diode are such that as forward voltage drop characteristics have a current-independent constant voltage component, there is a limit on the reduction in the forward voltage drop even though the number of parallel connections is increased. Consequently, as far as in conduction losses in the intermediate arm at the same current, the conduction loss is higher in Fig. 1 than in Fig. 6.

[0042] However, in the circuit configuration of Fig. 1, it is possible to reduce the effect of an increase in the conduction loss on the whole loss by lowering the time ratio of the freewheeling period T_b in which the intermediate arm conducts, as heretofore described.

[0043] This advantage becomes more significant when an output power factor is set so as to be 1 or a value

close to 1, for example, 0.8 or more. When the output power factor is 1 or a value close to 1 in this way, a period in Fig. 7, in which a voltage application period T_a increases, and a period, in which the instantaneous value of an output current increases, are approximately coincident. Conversely, as it is in the vicinity of zero crossing, in which the instantaneous value of the current is small, that the period in which the intermediate arm conducts increases, an increase in the whole loss decreases even though the forward voltage drop increases at that time.

[0044] Next, a description will be given of a switching loss on the condition that the output power factor is high.

[0045] In a period in which the output voltage and the output current are coincident in polarity, the upper and lower arms generate a turn-on loss and a turn-off loss, and the intermediate arm generates a reverse recovery loss, as a result of the same operation as in (a) of Fig. 6 previously described. In this embodiment, as fast elements such as SiC-MOSFETs are used for the upper and lower arms, that is, the semiconductor switches 4 and 5, and fast elements such as SiC-SBDs are used for the diodes 10 and 11 of the intermediate arm, all the respective losses of the upper and lower arms and intermediate arm decrease.

[0046] In a period in which the output voltage and the output current are not coincident in polarity, the IGBTs 12 and 13 of the intermediate arm generate a turn-on loss and a turn-off loss as a result of the same operation as in (b) of Fig. 6 previously described. The losses are higher than those generated by the SiC-MOSFETs, but a polarity non-coincidence period T_c is short, and furthermore, in the period T_c , as the instantaneous value of an output current I is comparatively small, it is natural that there is a small effect on the whole loss.

[0047] As above, it is possible, on the conditions that the peak of the alternating current output voltage V_o is close to the direct current voltage and that the output power factor is high, to replace half (in the example of Fig. 1, two of the four) of the semiconductor switches in the circuit with heretofore known inexpensive elements, such as IGBTs, substantially without increasing the losses.

[0048] It is also possible, from the same principle, to further reduce cost by replacing the reverse parallel diode of the MOSFET 4 or 5 with an element which is inferior in reverse recovery characteristics but inexpensive.

[0049] Next, a description will be given, based on Fig. 2, of a second embodiment of the invention.

[0050] In the second embodiment, in order to realize the condition that a direct current input voltage fluctuation of an inverter is small, regardless of the characteristics of an actual direct current power source 1 such as a solar cell, a voltage fluctuation compensation circuit 20 is connected between the direct current power source 1 and the series circuit of the capacitors 2 and 3.

[0051] In the voltage fluctuation compensation circuit 20 of Fig. 2, 21 is a semiconductor switch formed of, for example, a MOSFET, 22 is a diode connected in series

to the semiconductor switch 21, and 23 is a reactor connected between the positive electrode of the direct current power source 1 and the anode of the diode 22. The voltage fluctuation compensation circuit 20 configures a known DC/DC converter circuit called a boost chopper, wherein a P-N direct current voltage can be kept at a constant value by a switching operation of the semiconductor switch 21 even when there is a voltage fluctuation in the direct current power source 1.

[0052] The voltage fluctuation compensation circuit in this embodiment may be of any configuration as long as the circuit is a circuit which can always output a constant direct current voltage even though a direct current source voltage fluctuates.

[0053] The intermediate arm may be of configurations such as shown in Fig. 3 other than the configuration wherein a series connection point of the IGBTs 12 and 13 is connected to the M point, and a series connection point of the diodes 10 and 11 is connected to the U point, as shown in Figs. 1 and 2.

(a) of Fig. 3 is a configuration wherein a connection point of the collector of the IGBT 12 and the cathode of the diode 11 is connected to the M point, and a connection point of the collector of the IGBT 13 and the cathode of the diode 10 is connected to the U point, and (b) of Fig. 3 is a configuration wherein a connection point of the emitter of the IGBT 13 and the anode of the diode 10 is connected to the M point, and a connection point of the emitter of the IGBT 12 and the anode of the diode 11 is connected to the U point.

[0054] Also, as shown in (c) of Fig. 3, the collectors of the IGBTs 12 and 13 in (b) of Fig. 3 may be connected together. (c) of Fig. 3 is a configuration wherein the diodes 10 and 11 are combined into a reverse parallel diode for reverse voltage protection as protection means of the IGBTs 12 and 13 having no reverse breakdown voltage.

[0055] In the first embodiment and second embodiment, three semiconductor elements of different kinds exist in series in a direct current circle current path, such as from the MOSFET 4 through the diode 10 to the IGBT 12 in Fig. 1. Meanwhile, in a circuit using an element which switches fast, as a current change rate (di/dt) of the element is high, a surge voltage is generated due to an inductance existing on the circuit, and an application of an overvoltage to the element frequently becomes a problem. In order to prevent the problem, it is necessary to minimize the inductance of the heretofore described kind of direct current circle current path.

[0056] Meanwhile, a semiconductor switching element dealing with a large current is often housed in a block-shaped module having a wiring terminal and an insulating case.

[0057] Fig. 4 gives configuration diagrams wherein the semiconductor switches and diodes used in the circuit of Fig. 1 or 2 are modularized.

(a) of Fig. 4 is a first module 201 in which are housed the MOSFETs 4 and 5 of the upper and lower arms, (b) of Fig. 4 is a second module 202 in which is housed a diode portion (the diodes 10 and 11) of the intermediate arm, and (c) of Fig. 4 is a third module 203 in which is housed an IGBT portion (the IGBTs 12 and 13) of the intermediate arm. The modules 202 and 203 shown in (b) and (c) of Fig. 4 are used by connecting a P point, N point, and AC (U) point of one module to respective P, N, and AC(U) points of the other. Also, (d) of Fig. 4 is a fourth module 210 in which the diodes 10 and 11 and IGBTs 12 and 13 of the intermediate arm are collectively housed, and corresponds to the previously described circuit of (c) of Fig. 3.

[0058] Furthermore, (e) and (f) of Fig. 4 are examples in which the IGBT 13 and diode 11 configuring the intermediate arm are housed in a fifth module 220, and in the same way, the IGBT 12 and diode 10 are housed in a sixth module 221.

[0059] Next, (a) of Fig. 5 shows layout and wiring structures using the modules 201, 202, and 203 in (a), (b), and (c) of Fig. 4. The first module 201 for the upper and lower arms, the second module 202 of the diode portion, and the third module 203 of the IGBT portion are all formed in the same shape.

[0060] In (a) of Fig. 5, 204 is a wiring bar connected to the P point, 205 is a wiring bar connected to the N point, and 206 is a wiring bar connected to the U point. 207 is a wiring bar corresponding to a connection point of the diode 11 and IGBT 13 of the intermediate arm, 208 is a wiring bar corresponding to a connection point of the diode 10 and IGBT 12 of the intermediate arm, and 209 is a wiring bar corresponding to the potential of the M point.

[0061] In the layout and wiring structures, a current flowing by way of the U point from the P and N points is covered with the M point potential on the way back. It is well known that when the wiring bars are disposed in parallel, magnetic fluxes generated by a current which flows forward and backward in opposite directions are cancelled out, thus reducing the inductance, and the structure in (a) of Fig. 5 is for realizing this. This kind of structure has the advantage that a module of a commonly used configuration can be directly used in two-level circuits such as shown in (a) to (c) of Fig. 4.

[0062] Also, (b) of Fig. 5 shows a layout and wiring structure using the modules 201 and 210 in (a) and (d) of Fig. 4, wherein 211 is a wiring bar connected to the P point, 212 is a wiring bar connected to the N point, 213 is a wiring bar connected to the M point, and 214 is a wiring bar connected to the U point. The wiring bar 213 and the other wiring bars 211, 212, and 214 are disposed so as to overlap with each other in parallel on the modules 201 and 210. According to the structure, there is the advantage of it being possible to shorten the distance of a circle circuit compared with in (a) of Fig. 5.

(c) of Fig. 5 shows a layout and wiring structure using the modules 201, 220 and 221, wherein 222 is a wiring bar connected to the P point, 223 is a wiring bar connected to the N point, 224 is a wiring bar connected to the M point, and 225 is a wiring bar connected to the U point. The wiring bar 224 and the other wiring bars 222, 223, and 225 are disposed so as to overlap with each other in parallel on the modules 201, 220, and 221.

[0063] It goes without saying that the configuration of the modules and the shape of the wiring bars are not limited to the heretofore described.

Reference Signs List

[0064]

- 1: Direct current power source
- 2, 3, 9: Capacitor
- 4, 5: Semiconductor switch
- 8: Reactor
- 10, 11: Diode
- 12, 13: Semiconductor switch
- 20: Voltage fluctuation compensation circuit (boost chopper)
- 21: Semiconductor switch
- 22: Diode
- 23: Reactor
- 100: Transformer
- 101: Primary winding
- 102: Secondary winding
- 201, 202, 203, 210, 220, 221: Module
- 204, 205, 206, 207, 208, 209, 211, 212, 213, 214, 222, 223,
- 224, 225: Wiring bar
- 300: Power system

Claims

1. A three-level inverter, comprising:

a first semiconductor switch and second semiconductor switch which can control a conduction/interruption of a forward current by applying an on-signal or an off-signal to a control terminal, and which attain a conduction state always for a reverse current, wherein
a series circuit of a first capacitor and second capacitor and a series circuit of the first semiconductor switch and second semiconductor switch are connected in parallel to a direct current power source, wherein
one end of a bidirectional switch which can control a conduction/interruption of both forward and reverse currents is connected to a series connection point of the first capacitor and sec-

ond capacitor, and the other end of the bidirectional switch is connected to a series connection point of the first semiconductor switch and second semiconductor switch, wherein
the bidirectional switch has:

a third semiconductor switch and fourth semiconductor switch which can control a conduction/interruption of a forward current by applying an on-signal or an off signal to a control terminal, and which attain one of a conduction state always for a reverse current, an interruption state always for the reverse current, or a non-conduction state having no breakdown voltage; a first diode connected in series to the third semiconductor switch; and a second diode connected in series to the fourth semiconductor switch, the bidirectional switch being configured by connecting a series circuit of the third semiconductor switch and first diode, and a series circuit of the fourth semiconductor switch and second diode, in parallel in opposite directions, and wherein
the three-level inverter can output three voltage levels by operating the first to fourth semiconductor switches, the three-level inverter being operated
so as to satisfy at least one of the condition that the peak value of an alternating current output voltage is a value of 80% or more of the voltage of the first capacitor or second capacitor and the condition that an output power factor is 0.8 or more.

2. The three-level inverter according to claim 1, wherein the first semiconductor switch and the second semiconductor switch are each configured of a semiconductor switching element made of silicon carbide, or are each configured of a reverse parallel circuit of a semiconductor switching element made of silicon carbide and a Schottky barrier diode made of silicon carbide.
3. The three-level inverter according to claim 1 or 2, wherein IGBTs or MOSFETs made of silicon are used as the third semiconductor switch and fourth semiconductor switch, and diodes whose reverse recovery time is equal to or shorter than a switching time of the first semiconductor switch or second semiconductor switch are used as the first diode and second diode.
4. The three-level inverter according to claim 3, wherein the first diode and the second diode are Schottky barrier diodes made of silicon carbide.
5. The three-level inverter according to any one of

claims 1 to 4, including:

between the direct current power source and the series circuit of the first capacitor and second capacitor, a voltage fluctuation compensation circuit which stabilizes a voltage across the series circuit by compensating for a voltage fluctuation of the direct current power source. 5

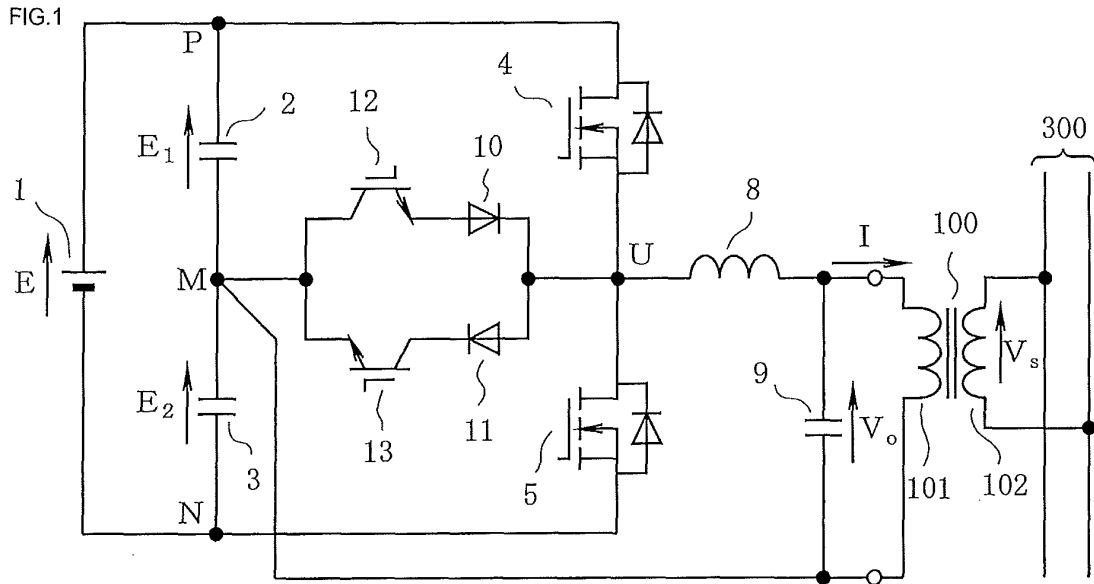
6. The three-level inverter according to any one of claims 1 to 4, wherein 10
the first semiconductor switch and the second semiconductor switch are housed in a first module, the third semiconductor switch and the fourth semiconductor switch are housed in a second module, and 15
the first diode and the second diode are housed in a third module, and that the first to third modules are connected by a conductor bar of a low inductance.
7. The three-level inverter according to any one of claims 1 to 4, wherein 20
the first semiconductor switch and the second semiconductor switch are housed in a first module, and the third semiconductor switch, the first diode, the fourth semiconductor switch, and the second diode 25
are housed in a fourth module, and that the first module and the fourth module are connected by a conductor bar of a low inductance.
8. The three-level inverter according to any one of claims 1 to 4, wherein 30
the first semiconductor switch and the second semiconductor switch are housed in a first module, the third semiconductor switch and the first diode are housed in a fifth module, and the fourth semiconductor switch and the second diode are housed in a sixth module, and that the first, fifth and sixth modules are 35
connected by a conductor bar of a low inductance.

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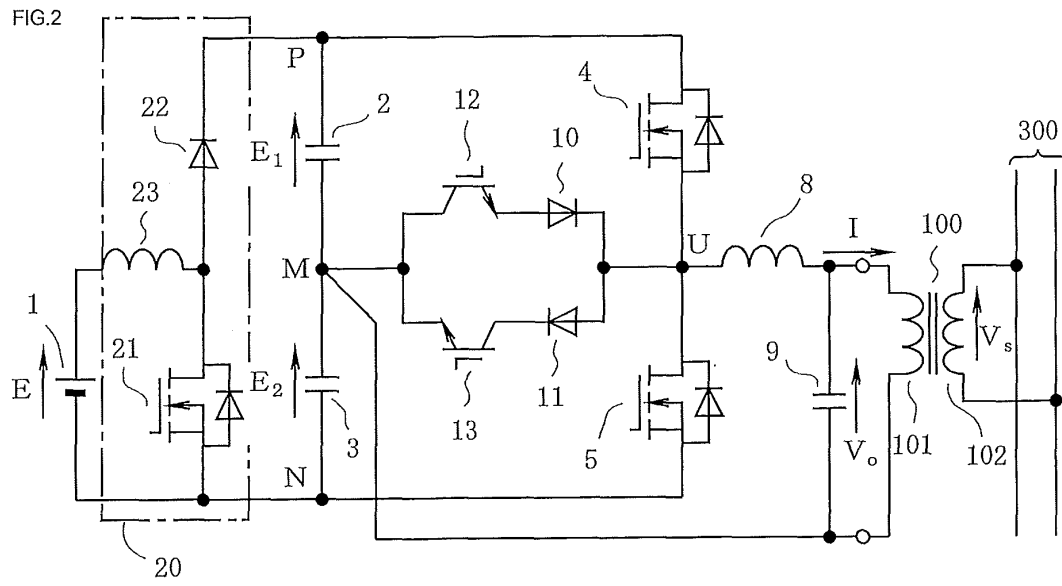
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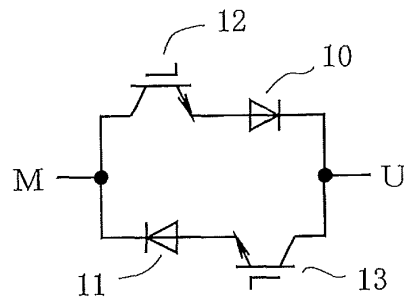


- 1 : DIRECT CURRENT POWER SOURCE
- 2, 3, 9 : CAPACITOR
- 4, 5 : SEMICONDUCTOR SWITCH
- 8 : REACTOR
- 10, 11 : DIODE
- 12, 13 : SEMICONDUCTOR SWITCH
- 100 : TRANSFORMER
- 101 : PRIMARY WINDING
- 102 : SECONDARY WINDING
- 300 : POWER SYSTEM

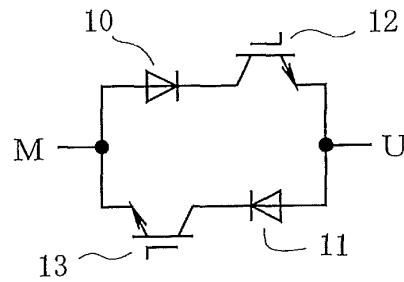


2 0 ; VOLTAGE FLUCTUATION COMPENSATION CIRCUIT
(BOOST CHOPPER)

FIG.3
(a)



(b)



(c)

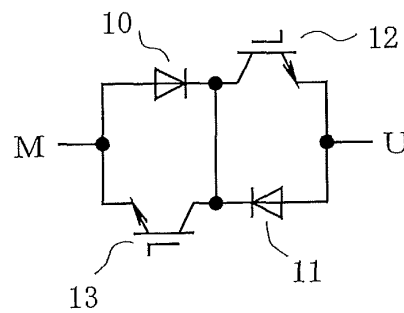
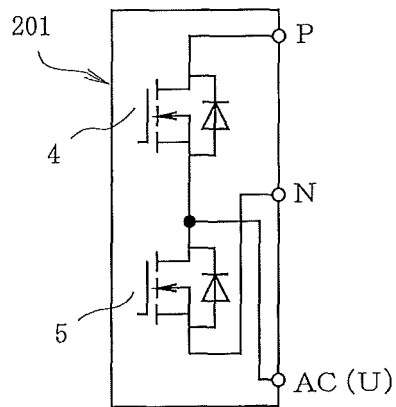
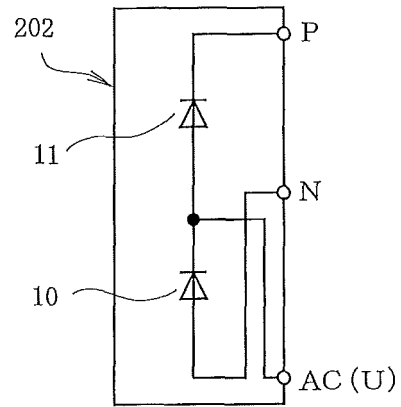


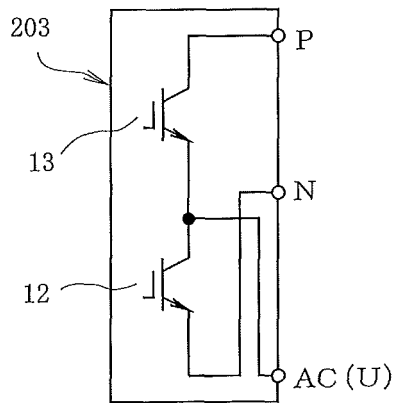
FIG.4 (a)



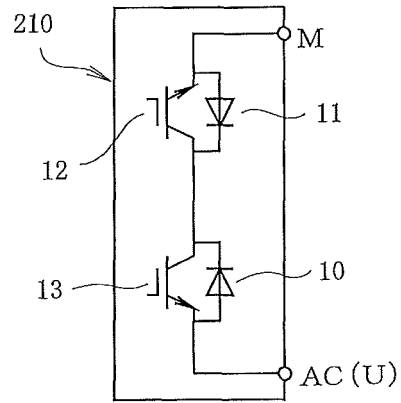
(b)



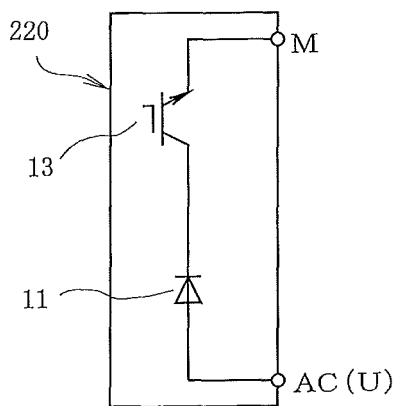
(c)



(d)



(e)



(f)

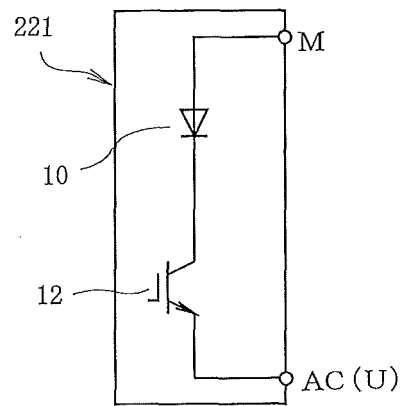


FIG.5

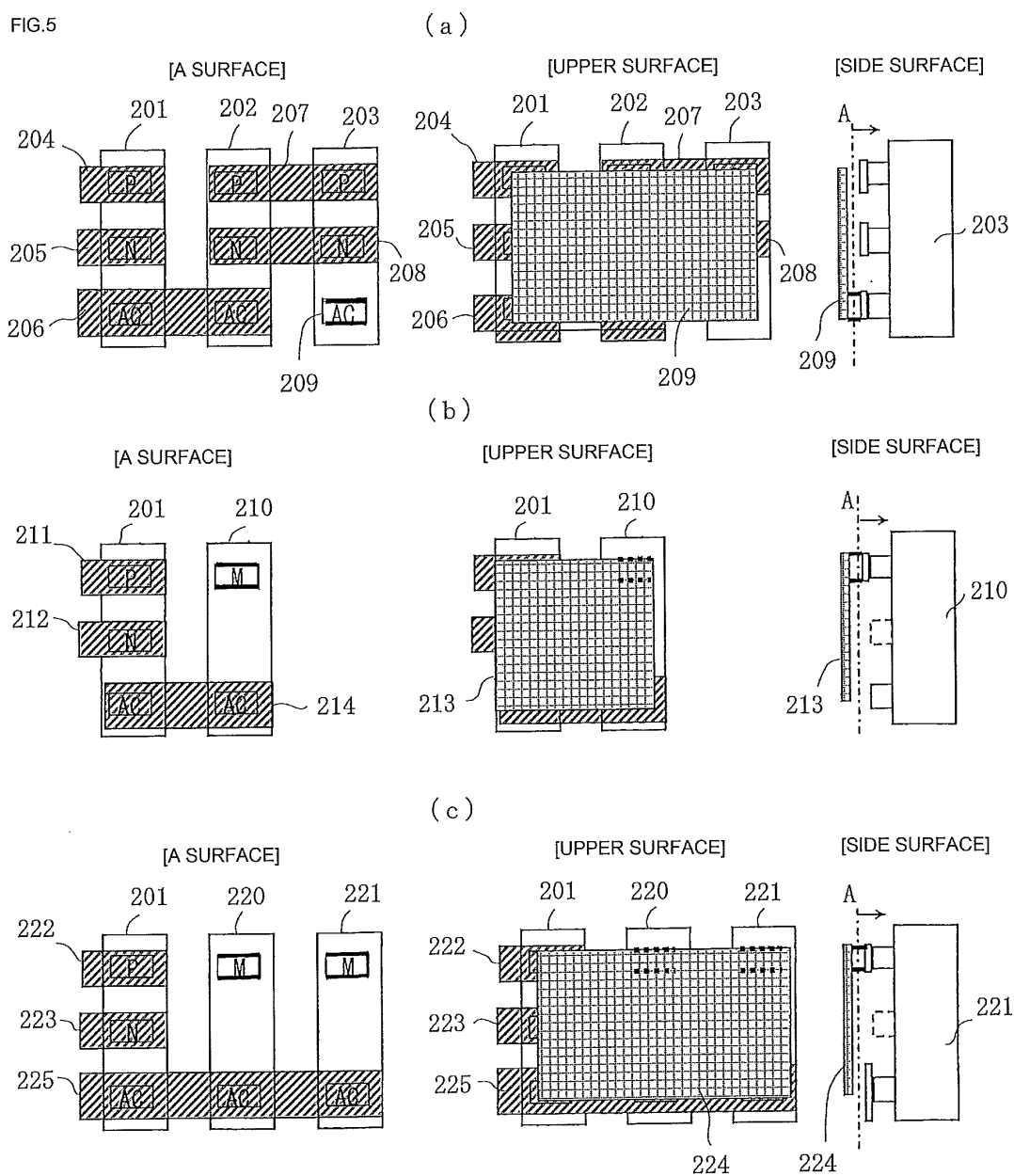
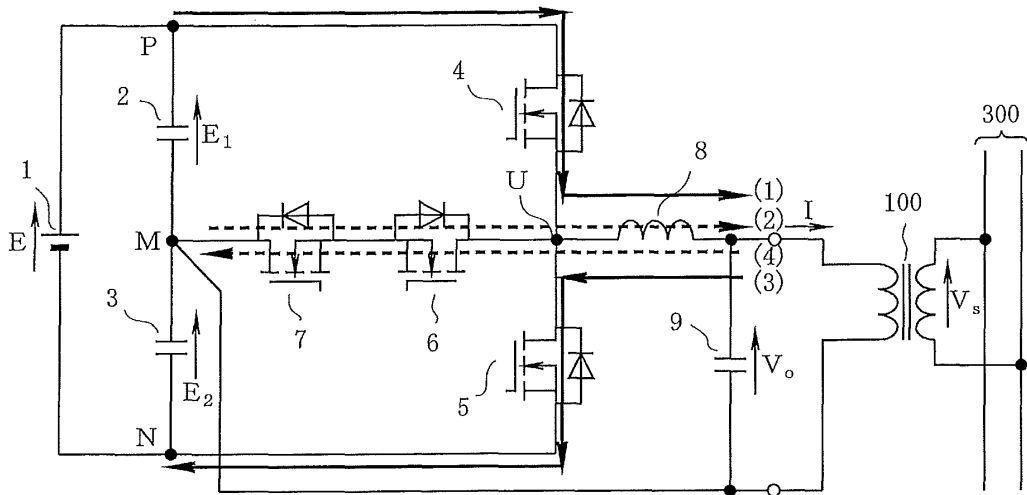


FIG.6

(a) OUTPUT VOLTAGE AND OUTPUT CURRENT ARE COINCIDENT IN POLARITY



(b) OUTPUT VOLTAGE AND OUTPUT CURRENT ARE NOT COINCIDENT IN POLARITY

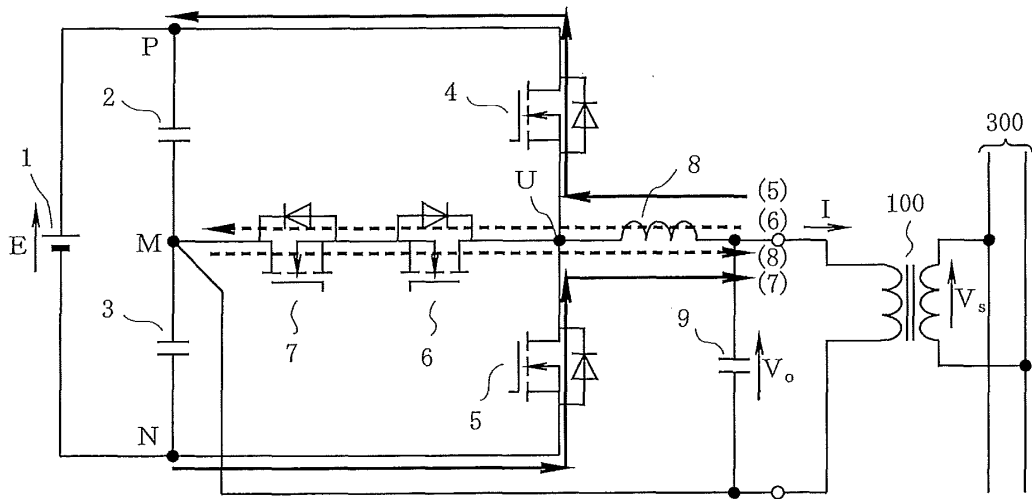
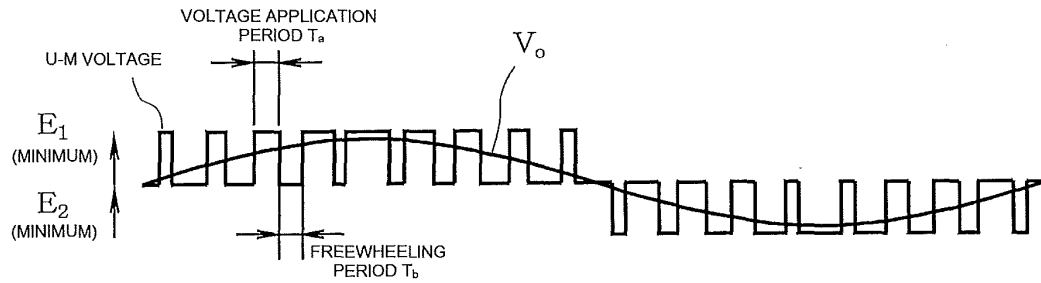
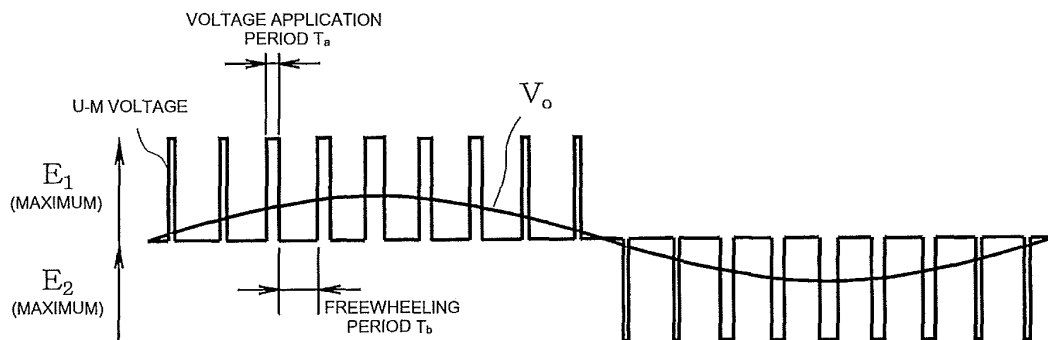


FIG.7 (a) WHEN DIRECT CURRENT VOLTAGE IS LOW



(b) WHEN DIRECT CURRENT VOLTAGE IS HIGH



(c) WHEN DIRECT CURRENT VOLTAGE IS SET SO AS TO BE ALWAYS HIGH

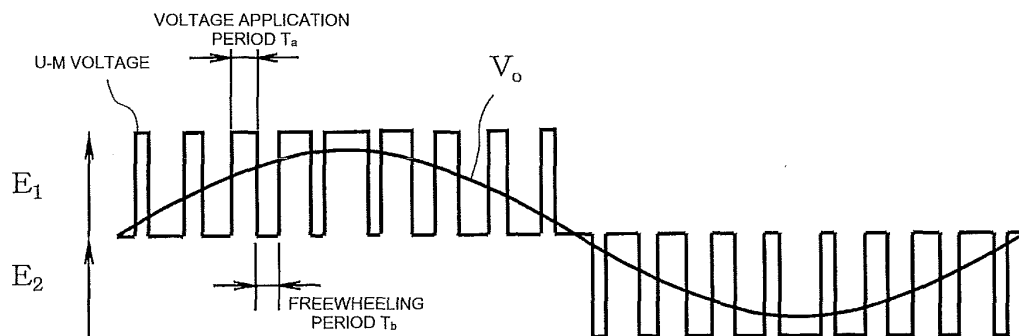
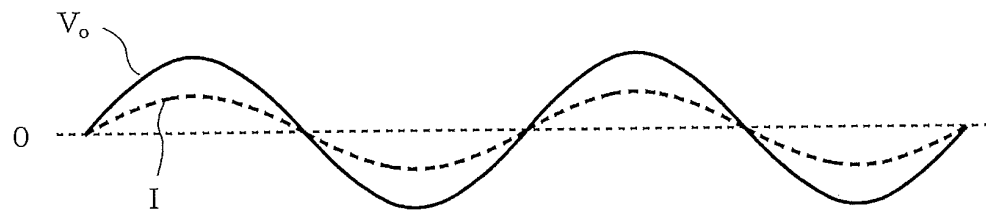
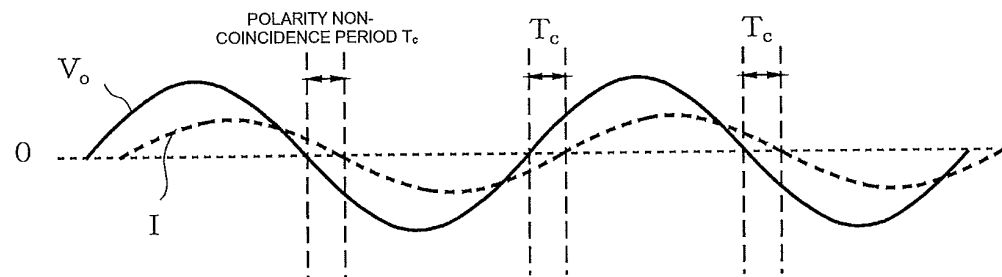


FIG.8 (a) [POWER FACTOR = 1]



(b) [POWER FACTOR = 0.8]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2013/076859

A. CLASSIFICATION OF SUBJECT MATTER

H02M7/483(2007.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M7/483

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2013

Kokai Jitsuyo Shinan Koho 1971-2013 Toroku Jitsuyo Shinan Koho 1994-2013

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5339018 B1 (Fuji Electric Co., Ltd.), 16 August 2013 (16.08.2013), entire text; all drawings (Family: none)	1-8
A	JP 2013-102674 A (Meidensha Corp.), 23 May 2013 (23.05.2013), entire text; all drawings (Family: none)	1-8
A	JP 2010-252450 A (Fuji Electric Systems Co., Ltd.), 04 November 2010 (04.11.2010), entire text; all drawings (Family: none)	1-8

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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Date of the actual completion of the international search
18 December, 2013 (18.12.13)Date of mailing of the international search report
07 January, 2014 (07.01.14)Name and mailing address of the ISA/
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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2010288415 A [0018]