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(71) Applicant: **Fuji Electric Co., Ltd.**
Kawasaki-shi 210-9530 (JP)

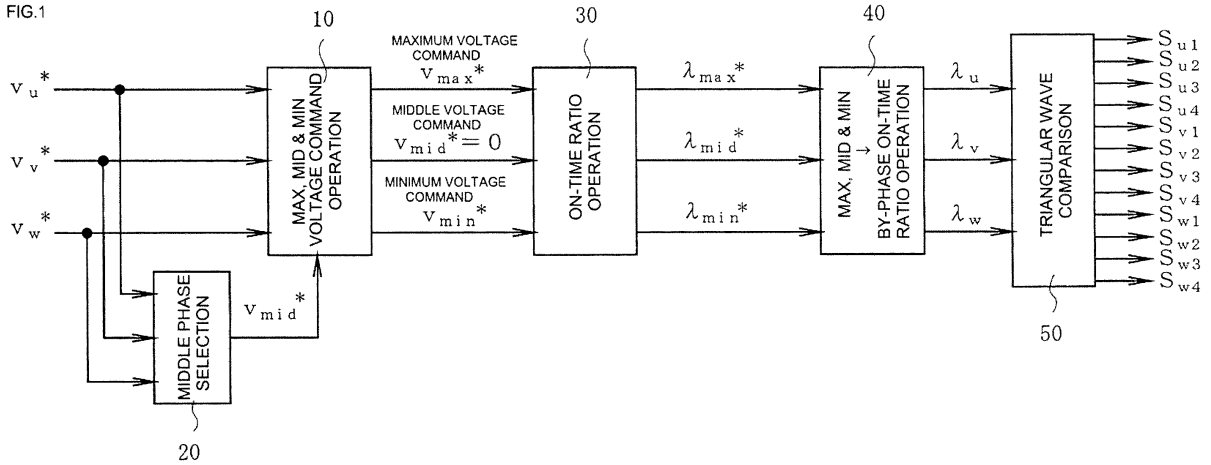
(72) Inventor: **SATO, Ikuya**
Kawasaki-shi, Kanagawa 210-9530 (JP)

(74) Representative: **MERH-IP Matias Erny Reichl Hoffmann**
Patentanwälte PartG mbB
Paul-Heyse-Strasse 29
80336 München (DE)

(54) CONTROL METHOD AND CONTROL SYSTEM OF THREE LEVEL INVERTER

(57) In a control method of a three-phase three-level inverter that makes switching elements in the inverter turned-on and -off according to an output voltage command to output three-phase AC voltage, the inverter having three of three-level inverters connected in parallel to one another each being capable of outputting a DC high voltage, DC middle voltage and DC low voltage, the method carries out operations for providing on-time ratios in one switching period of the switching elements, makes one inverter for one phase turn-on and -off switching elements respectively connected to a high voltage point and a middle voltage point with their respective on-time ratios to alternately output the DC high voltage and the DC middle voltage, makes one inverter for another phase fix the switching element connected to the middle voltage point in a turned-on state to output the DC middle voltage, and makes one inverter for the rest phase turn-on and -off the switching elements respectively connected to the middle voltage point and a low voltage point with their respective on-time ratios to alternately output the DC middle voltage and the DC low voltage.

FIG.1



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Description

BACKGROUND OF INVENTION

1. Field of the Invention

[0001] The present invention relates to a control method and a control system in a three-level inverter which outputs an AC voltage in three levels converted from a DC voltage by carrying out the switching of the DC voltage with the use of semiconductor switching elements, the control method and the control system enabling the inverter to reduce the number of times of the switching and to expand the range of the output voltage.

2. Background Art

[0002] FIGURE 13 is a circuit diagram showing the circuit configuration of an example of a common three-level inverter with respect to the circuit of one phase. Here, for simplifying the explanation, the circuit configuration with respect to only one phase (U-phase) of the output circuits of three phases is shown.

[0003] In FIG. 13, the three-level inverter is provided with DC power supplies 101 and 102 (letting each of the voltage values thereof be E_d), semiconductor switching elements S_1 to S_4 such as IGBTs and diodes D_1 and D_2. Signs N and U designate a neutral point and an output terminal, respectively. In the following explanations, in a DC circuit, the positive electrode of the DC power supply 101, the negative electrode of the DC power supply 102 and the neutral point N are to be also referred to as a high voltage point, a low voltage point and a middle voltage point, respectively. Moreover, the voltage E_d, the voltage $-E_d$ and a voltage 0 are to be referred to as a DC high voltage, a DC low voltage and a DC middle voltage, respectively.

[0004] In the three-level inverter, by the turning-on and -off operations of the semiconductor switching elements S_1 to S4 connected in series and the action of the diodes D_1 and D_2, it is possible to output the voltages at three levels in the DC circuit, namely the voltages E_d, 0, and $-E_d$ (here, the voltages drop at each element is ignored).

[0005] For example, with the semiconductor switching elements S_1 and S_2 being turned-on and the semiconductor switching elements S_3 and S_4 being turned-off, an output voltage becomes E_d, with the semiconductor switching elements S_2 and S_3 being turned-on and the semiconductor switching elements S_1 and S_4 being turned-off, an output voltage becomes 0, and with the semiconductor switching elements S_3 and S_4 being turned-on and the semiconductor switching elements S_1 and S_2 being turned-off, an output voltage becomes $-E_d$.

[0006] FIGURE 14 is a circuit diagram showing the circuit configuration of another example of a common three-level inverter with respect to the circuit of one phase.

[0007] In FIG. 14, the configuration of the circuit of a three-level inverter is shown with respect to one phase in which inverter the diodes D_1 and D_2 in the three-level inverter shown in FIG. 13 are omitted and a bidirectional switch S_{23} formed of the semiconductor switching elements S_2 and S_3 is used.

[0008] The levels of the output voltages of the three-level inverter are the same as the levels of the output voltages of the three-level inverter shown in FIG. 13. For example, with the semiconductor switching element S_1 being turned-on and with the semiconductor switching elements S_2 to S_4 being turned-off, the output voltage becomes E_d, with the semiconductor switching elements S_2 and S_3 being turned-on and with the semiconductor switching elements S_1 and S_4 being turned-off, the output voltage becomes 0, and with the semiconductor switching element S_4 being turned-on and with the semiconductor switching elements S_1 to S_3 being turned-off, the output voltage becomes $-E_d$.

[0009] In this way, the three-level inverter, by outputting voltages at three levels, can relax an abrupt change in a voltage applied to a load compared with a two-level inverter. In particular, when a motor is connected as a load, such a three-level inverter is effective in inhibiting a surge voltage to allow the three-level inverter to be widely used.

[0010] Here, for a control method of a three-level inverter, there is the method described in each of JP-A-2007-282484 (paragraphs [0008] to [0028] and FIG. 1 to FIG. 3, etc.) and JP-A-2010-206931 (paragraphs [0027] to [0036] and FIG. 1 to FIG. 3, etc.).

[0011] In JP-A-2007-282484 (paragraphs [0008] to [0028] andFIG. 1 to FIG. 3, etc.), a method is described in which an output voltage is provided on the basis of the frequency command or the amplitude command of an output voltage command with a dipolar modulation method carried out in a low output voltage region, a unipolar modulation method carried out in a middle output voltage region and an over modulation method carried out in a high output voltage region other than the former two regions, and control is carried out by switching the modulation methods according to the output voltage region.

[0012] In JP-A-2010-206931 (paragraphs [0027] to [0036] and FIG. 1 to FIG. 3, etc.), a control method is disclosed in which a plurality of output voltage vectors suited for an output voltage command are selected with the use of instantaneous space vectors and the selected vectors are made to be outputted in the order for preventing common mode voltages, with suggestion of making the voltage vectors cause transition so as not to increase the number of switching

operations more than that being necessary.

[Patent Documents]

[0013]

[Patent Document 1] JP-A-2007-282484 (paragraphs [0008] to [0028] and FIG. 1 to FIG. 3, etc.)
[Patent Document 2] JP-A-2010-206931 (paragraphs [0027] to [0036] and FIG. 1 to FIG. 3, etc.)

[0014] In the related three-level inverter described in JP-A-2007-282484, modulation methods are switched to various ones such as the unipolar modulation method and the dipolar modulation method according to the levels of output voltages in their respective output voltage regions. In the unipolar modulation method, however, when the output voltage command is positive, switching operations alternately occur with respect to one switching element between the high voltage point at the voltage E_d and the output terminal and one switching element between the middle voltage point at the voltage zero and the output terminal in the DC circuit for every one switching period. When the output voltage command is negative, switching operations alternately occur with respect to one switching element between the low voltage point at the voltage $-E_d$ and the output terminal and one switching element between the middle voltage point at the voltage zero and the output terminal in the DC circuit for every one switching period. That is, for each phase, the switching operations occur four times (the operation of one switching element changed from a turned-off state to a turned-on state and the operation of the switching element further returning from the turned-on state to the turned-off state are to be two times operations). Therefore, in three phases, the switching operations are to occur twelve times in total per one switching period.

[0015] While, in the dipolar modulation method, there is a problem in that the number of switching operations is to further increase in the low output voltage region to lower the efficiency of a system due to switching losses.

[0016] In addition, according to the related three-level inverter described in JP-A-2010-206931, the number of switching operations can be reduced by some orders of causing transitions of a plurality of output voltage vectors being selected. However, with the use of a counter (timer) such as a less expensive microcomputer, it is difficult to correctly manage the time ratio of each of voltage vectors, which requires a high expensive arithmetic unit with high performance to a possible increase in cost.

[0017] Accordingly, it is an object of the invention to provide a control method and a control system of a three-level inverter which are intended for downsizing and high efficiency with reduced losses by reducing the number of switching operations against the problem of the three-level inverter described in JP-A-2007-282484 and which enable cost reduction with the use of a counter such as a less expensive microcomputer against the problem of the three-level inverter described in JP-A-2010-206931.

SUMMARY OF THE INVENTION

[0018] For solving the foregoing problems, a first aspect of the invention is that in a control method of a three-level inverter wherein, with respect to a configuration in which three of three-level inverters are connected in parallel to each other,
the three level inverter carrying out turning-on and -off of a plurality of semiconductor switching elements of
at least one semiconductor switching element connected between a high voltage point of a DC circuit and one output terminal,
at least one semiconductor switching element connected between a middle voltage point of the DC circuit and the output terminal, and
at least one semiconductor switching element connected between a low voltage point of the DC circuit and the output terminal, and
enabling any one of three level voltages of a DC high voltage, DC middle voltage and DC low voltage as the base of an AC voltage for one-phase to be outputted from the output terminal,
the method makes a plurality of the semiconductor switching elements in each of the three three-level inverters turned-on and -off on the basis of output voltage commands of three-phase AC voltages to thereby make the three-phase AC voltage outputted, the method includes the steps of:
carrying out operations for obtaining on-time ratios of a plurality of the semiconductor switching elements in each of the three three-level inverters on the basis of the output voltage commands of the three-phase AC voltages;
dividing the one period of the output voltage command of the three-phase AC voltage into a plurality of sections; and in each of the sections,
making the three-level inverter for one-phase alternately turn-on and -off the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching

element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC high voltage and the DC middle voltage;
along with this, making the three-level inverter for another one-phase fix the at least one switching element connected between the middle voltage point and the output terminal in a turned-on state to output the DC middle voltage; and
along with this, further making the three-level inverter for the rest one-phase alternately turn-on and -off the at least one semiconductor switching element connected between the middle voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal with their respective operated on-time ratios in the one switching period to alternately output the DC middle voltage and the DC low voltage.

[0019] A second aspect is that in the control method as the first aspect, the method includes the steps of:

in each of the sections,
with respect to a phase with the value of the output voltage command being a maximum value, carrying out compensation of subtracting a middle value of the output voltage command in another phase from the maximum value to provide thus compensated value as the value of a maximum voltage command in the phase in the section;
with respect to the phase with the value of the output voltage command being the middle value, carrying out compensation of providing 0 as the value of a middle voltage command in the phase in the section;
with respect to the rest phase with the value of the output voltage command being a minimum value, carrying out compensation of subtracting the middle value of the output voltage command from the minimum value to provide thus compensated value as the value of a minimum voltage command in the phase in the section;
with respect to the phase with the value of the output voltage command being the minimum value, carrying out an operation of dividing the value of the maximum voltage command by the value of the DC high voltage to provide the on-time ratio of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the three-level inverter on the basis of the result of the division;
with respect to the phase with the value of the output voltage command being the middle value, carrying out an operation of providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the turned-on state in the three-level inverter in the phase on the basis of the value 0; and
with respect to the phase with the value of the output voltage command being the minimum value, carrying out an operation of dividing the value of the minimum voltage command by the value of the DC low voltage to provide the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the three-level inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal in the three-level inverter on the basis of the result of the division.

[0020] A third aspect is a control system for carrying out the control method of the first or second aspect which system includes:

a middle phase selecting means selecting, in each of the sections, an output voltage command of a phase with the value thereof being a middle value from the output voltage commands of the three-phase AC voltage;
a maximum, middle and minimum voltage command operating means classifying, in each of the sections, the output voltage commands of the three-phase AC voltage by value into a voltage command of a phase with the value thereof being a maximum value, the selected voltage command of the phase with the value thereof being the middle value and a voltage command of a phase with the value thereof being a minimum value, and carrying out the compensation of subtracting the selected middle value from each of the classified output voltage commands to output the compensated results as a maximum voltage command, a middle voltage command with zero value and a minimum voltage command;
an on-time ratio operating means carrying out, in each of the sections, an operation of dividing the value of the inputted maximum voltage command by the value of the DC high voltage to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between the high voltage point of the DC circuit and the one output terminal, carrying out an operation of converting the value 0 of the inputted middle voltage command into value 1 to output the value 1 as an operated value of the on-time ratio of fixing the at least one semiconductor switching element connected between the middle voltage point of the DC circuit and the one output terminal in the turned-on state, and carrying out an operation of dividing the value of the inputted minimum voltage command by the value of the DC low voltage to output the result of the operation as an

operated value of the on-time ratio of the at least one semiconductor switching element connected between the low voltage point of the DC circuit and the one output terminal;
a by-phase on-time ratio operating means classifying by phase, in each of the sections, the operated values of the on-time ratios, which are classified by values, and outputting the operated values classified by phase as voltages with the values thereof corresponding to the on-time ratios; and
a carrier comparing means making, in each of the sections, the voltages, inputted by phase with the values thereof corresponding to the on-time ratios, compared with a carrier, which converts the compared voltage into an on-off command with an on-time ratio corresponding to the compared voltage, to produce on-off commands with the on-time ratios by phase and provide the on-off commands as those for a plurality of the semiconductor switching elements in each of the three three-level inverters.

[0021] A fourth aspect is that in a control method of a three-level inverter wherein, with respect to a configuration in which three of three-level inverters are connected in parallel to each other,
the three level inverter carrying out turning-on and -off of a plurality of semiconductor switching elements of
at least one semiconductor switching element connected between a high voltage point of a DC circuit and one output terminal,
at least one semiconductor switching element connected between a middle voltage point of the DC circuit and the output terminal, and
at least one semiconductor switching element connected between a low voltage point of the DC circuit and the output terminal, and
enabling any one of three level voltages of a DC high voltage, DC middle voltage and DC low voltage as the base of an AC voltage for one-phase to be outputted from the output terminal,
the method makes a plurality of the semiconductor switching elements in each of the three three-level inverters turned-on and -off on the basis of output voltage commands of three-phase AC voltages to thereby make the three-phase AC voltage outputted, the method includes the steps of:
carrying out operations for obtaining on-time ratios of a plurality of the semiconductor switching elements in each of the three three-level inverters on the basis of the output voltage commands of the three-phase AC voltages;
dividing the one period of the output voltage command of the three-phase AC voltage into a plurality of sections; and
in each of the sections,
making the three-level inverter for one-phase fix one of the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal in a turned-on state to output one of the DC high voltage and the DC low voltage;
along with this, making the three-level inverter for another one-phase alternately turn-on and -off one of the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal with the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output one of the DC high voltage and the DC low voltage with the DC middle voltage; and
along with this, when making the three-level inverter for another one-phase output the DC high voltage, further making the three-level inverter for the rest one-phase alternately turn-on and-off the at least one semiconductor switching element connected between the low voltage point and the output terminal and the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC low voltage with the DC middle voltage; and
when making the three-level inverter for another one-phase output the DC low voltage, further making the three-level inverter for the rest one-phase alternately turn-on and -off the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC high voltage with the DC middle voltage.

[0022] A fifth aspect is that in the control method as the fourth aspect, the method includes the steps of:

in each of the sections,
when the output voltage command has the positive polarity and the absolute value of the maximum value,
with respect to a phase with the output voltage command having the positive polarity and the absolute value of the maximum value,
making the value of the DC high voltage as the maximum value of the compensated voltage command, providing the value of the DC high voltage as the maximum voltage command in the phase in the section, carrying out an

operation of dividing the maximum voltage command by the value of the DC high voltage and, on the basis of the result of the division, providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the low voltage point and the output terminal in the turned-on state in the three-level inverter in the phase;

with respect to a phase with the value of the output voltage command being a middle value,

carrying out compensation of adding the difference between the value of the DC high voltage and the maximum value of the output voltage command to the middle value of the voltage command, providing the value of the compensated voltage command as the value of the middle voltage command in the phase in the section, carrying out an operation of dividing the value of the middle voltage command by the value of the DC high voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the inverter in the phase;

with respect to a phase with the value of the output voltage command being a minimum value,

carrying out compensation of adding the difference between the value of the DC high voltage and the maximum value of the output voltage command to the minimum value of the voltage command, providing the value of the compensated voltage command as the value of the minimum voltage command in the phase in the section, carrying out an operation of dividing the value of the minimum voltage command by the value of the DC high voltage and, on the basis of the result of the division and the polarity of the minimum voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the high voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal in the inverter in the phase;

when the output voltage command has the negative polarity and the absolute value of the maximum value,

with respect to a phase with the output voltage command having the negative polarity and the absolute value of the maximum value,

making the absolute value of the DC low voltage as the maximum value of the compensated voltage command, providing the absolute value of the DC low voltage as the maximum voltage command in the phase in the section, carrying out an operation of dividing the absolute value of the maximum voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division, providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the low voltage point and the output terminal in the turned-on state in the three-level inverter in the phase;

with respect to a phase with the value of the output voltage command being a middle value,

carrying out compensation of subtracting the difference between the absolute value of the DC low voltage and the maximum value of the output voltage command from the middle value of the voltage command, providing the value of the compensated voltage command as the value of the middle voltage command in the phase in the section, carrying out an operation of dividing the value of the middle voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the inverter in the phase; and

with respect to a phase with the value of the output voltage command being a minimum value,

carrying out compensation of subtracting the difference between the absolute value of the DC low voltage and the maximum value of the output voltage command to the minimum value of the voltage command, providing the value of the compensated voltage command as the value of the minimum voltage command in the phase in the section, carrying out an operation of dividing the value of the minimum voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal.

[0023] A sixth aspect is a control system for carrying out the control method of the fourth or fifth aspect which system includes:

an absolute maximum value command discriminating means detecting, in each of the sections, an output voltage command of a phase with an absolute value of the maximum value from the output voltage commands of the three-phase AC voltage and carrying out an operation for providing a compensation value for the output voltage commands on the basis of the maximum value and the polarity thereof;
a maximum, middle and minimum voltage command operating means classifying, in each of the sections, the output voltage commands of the three-phase AC voltage by value into a voltage command of a phase with the value thereof being a maximum value, a voltage command of the phase with the value thereof being the middle value and a voltage command of a phase with the value thereof being a minimum value, carrying out the compensation of adding the compensation value when the polarity of the maximum value is positive and subtracting the compensation value when the polarity of the maximum value is negative, and outputting the compensated results as a maximum voltage command with the value thereof being one of the value of the DC high voltage and the absolute value of the DC low voltage, a middle voltage command and a minimum voltage command;
an on-time ratio operating means carrying out, in each of the sections, an operation of dividing the value of the inputted maximum voltage command by the value of one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to convert the value of the inputted maximum voltage command to 1 to output the result of the operation as an operated value of the on-time ratio of fixing the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point and the one output terminal in the turned-on state, carrying out an operation of dividing the value of the inputted middle voltage command by one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point of the DC circuit and the one output terminal, and carrying out an operation of dividing the value of the inputted minimum voltage command by one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point of the DC circuit and the one output terminal;
a by-phase on-time ratio operating means classifying by phase, in each of the sections, the operated values of the on-time ratios, which are classified by values, and outputting the operated values classified by phase as voltages with the values thereof corresponding to the on-time ratios; and

[0024] a carrier comparing means making, in each of the sections, the voltages, inputted by phase with the values thereof corresponding to the on-time ratios, compared with a carrier, which converts the compared voltage into an on-off command with an on-time ratio corresponding to the compared voltage, to produce on-off commands with the on-time ratios by phase and provide the on-off commands as those for a plurality of the semiconductor switching elements in each of the three three-level inverters.

[0025] A seventh aspect of the invention is a control method in which the method of the first or the second aspect is carried out when the amplitude of a three-phase output voltage command is equal to or less than a specified value and carried out as the method of the fourth or fifth aspect when the amplitude of the three-phase output voltage command is equal to or more than the specified value.

[0026] In addition an eighth aspect is that in the control system of the third aspect or the sixth aspect, the carrier is a triangular wave.

[0027] According to the first to sixth aspects of the invention, the number of switching operations can be reduced when compared with related art to make it possible to reduce losses and increase the efficiency of the system. In addition, on-off commands with specified on-time ratios can be produced with the use of a less expensive device such as a microcomputer to make it possible to provide a control system with reduced cost.

[0028] In particular, according to the fourth to sixth aspects and the eighth aspect, saturation in voltage commands and distortions in waveforms can be avoided to enable the range of an output voltage to be expanded.

[0029] Furthermore, according to the seventh aspect of the invention, by distinguishing between the control method in a low output voltage region and that in a high voltage region, output voltages can be controlled over a wide range.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030]

FIG. 1 is a functional block diagram showing a configuration of a control system according to a first embodiment of

the invention;

FIG. 2 is a waveform diagram showing the waveforms of three-phase output voltage commands v_u^*, v_v^* and v_w^* in the control system according to the first embodiment;

FIG. 3 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 2 are compensated, respectively, together with the waveform of a zero-phase voltage command 3w in the first embodiment;

FIG. 4 is a waveform diagram showing the operation of the triangular wave comparison means according to the first embodiment in a part of the section 1 with (a) showing the waveforms of the on-time ratios in their respective U-, V- and W-phases together with the waveform of the triangular wave, and (b), (c) and (d) showing the waveforms of the on-off commands in the U-, V- and W-phases, respectively;

FIG. 5 is a functional block diagram showing a configuration of a control system according to a second embodiment of the invention;

FIG. 6 is a waveform diagram showing the waveforms of three-phase output voltage commands v_u^*, v_v^* and v_w^* in the control system according to the second embodiment;

FIG. 7 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FI. 6 are compensated, respectively, together with the waveform of a zero-phase voltage command 3w in the second embodiment;

FIG. 8A is a waveform diagram showing the waveform of the voltage command v_{u0} taken out from FIG. 7;

FIG. 8B is a waveform diagram showing the waveform of the voltage command v_{v0} taken out from FIG. 7;

FIG. 8C is a waveform diagram showing the waveform of the voltage command v_{w0} taken out from FIG. 7;

FIG. 8D is a waveform diagram showing the waveform of the zero-phase voltage command 3w taken out from FIG. 7;

FIG. 9 is a waveform diagram showing the operation of the triangular wave comparison means according to the second embodiment in a part of the section 1 with (a) showing the waveforms of the on-time ratios in their respective U-, V- and W-phases together with the waveform of the triangular wave, (b), (c) and (d) showing the waveforms of the on-off commands in the U-, V- and W-phases, respectively;

FIG. 10 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 2 are compensated with their respective amplitudes increased from illustrated 0.5 to 0.8 in the first embodiment;

FIG. 11 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 6 are compensated with their respective amplitudes increased from illustrated 0.5 to 0.8 in the second embodiment;

FIG. 12 is an explanatory diagram showing the discrimination for switching between the control according to the first embodiment and the control according to the second embodiment;

FIG. 13 is a circuit diagram showing the circuit configuration of an example of a common three-level inverter with respect to the circuit of one phase; and

FIG. 14 is a circuit diagram showing the circuit configuration of another example of a common three-level inverter with respect to the circuit of one phase.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0031] In the following, embodiments of the invention will be explained with reference to the attached drawings.

[0032] FIGURE 1 is a functional block diagram showing a configuration of a control system according to a first embodiment (corresponding to the first to the third aspects) of the invention. The control system is formed with, for example, hardware and software of a microcomputer system. Here, the embodiment will be explained as a control system controlling the previously explained three-level inverter shown in FIG. 14. The embodiment, however, can be also applied to the control of the three-level inverter shown in FIG. 13.

[0033] FIGURE 2 is a waveform diagram showing the waveforms of three-phase output voltage commands v_u^*, v_v^* and v_w^* in the control system according to the first embodiment.

[0034] In FIG. 1, reference numeral 10 denotes a maximum, middle and minimum voltage command operating means. To the operating means 10, three-phase AC output voltage commands v_u^*, v_v^* and v_w^* as those shown in FIG. 2 are inputted which are obtained by operations performed on the basis of frequency commands, for example.

[0035] As is shown in FIG. 2, the one period of each of the voltage commands is divided into six, from the section 1 to the section 6, for example. In each section, a middle phase selecting means 20 shown in FIG. 1 selects a voltage command, the value of which is a middle value, as a middle voltage command v_{mid} from the inputted voltage commands v_u^*, v_v^* and v_w^*. Along with this, the maximum, middle and minimum voltage command operating means 10 classifies the voltage commands v_u^*, v_v^* and v_w^* in each section by value into maximum voltage commands v_{max}, middle voltage commands v_{mid}, and minimum voltage commands v_{min} as those shown in a discrimination table given as Table 1.

Table 1

SECTION	MAX. VOLTAGE COMMAND v_{max}	MIDDLE VOLTAGE COMMAND v_{mid}	MIN. VOLTAGE COMMAND v_{min}
1	v_u^*	v_v^*	v_w^*
2	v_v^*	v_u^*	v_w^*
3	v_v^*	v_w^*	v_u^*
4	v_w^*	v_v^*	v_u^*
5	v_w^*	v_u^*	v_v^*
6	v_u^*	v_w^*	v_v^*

[0036] With the sections determined as those shown in FIG. 2, as is apparent from Table 1 and FIG. 2, as the middle voltage command v_{mid}, the voltage commands v_v^*, v_u^* and v_w^* are to be arranged in their respective sections in the order of $v_v^* \rightarrow v_u^* \rightarrow v_w^*$ so that the order is repeated in cycles.

[0037] Here, the maximum, middle and minimum voltage command operating means 10 shown in FIG. 1 carries out compensation in which each of the maximum voltage command v_{max}, middle voltage command v_{mid} and minimum voltage command v_{min} in each of the sections shown in Table 1 has the middle voltage command v_{mid} in the section subtracted therefrom as is expressed in the expressions (1) with the respective resulting outputs of a maximum voltage command v_{max}^*, middle voltage command v_{mid}^* and minimum voltage command v_{min}^*. The compensation is carried out so that the compensated middle voltage command v_{mid}^* always becomes as $v_{mid}^* = 0$:

$$\left.\begin{aligned} v_{max}^* &= v_{max} - v_{mid} \\ v_{mid}^* &= v_{mid} - v_{mid} = 0 \\ v_{min}^* &= v_{min} - v_{mid} \end{aligned}\right\}. \qquad (1)$$

[0038] FIGURE 3 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 2 are compensated according to the expressions (1).

[0039] For example, in the section 1, the maximum voltage command v_{max}, middle voltage command v_{mid} and minimum voltage command v_{min} before being compensated by the expressions (1) are the output voltage command v_u^* in the U-phase, the output voltage command v_v^* in the V-phase and the output voltage command v_w^* in the W-phase, respectively, which are shown in Fig. 2. Thus, in correspondence with this, after the compensation, the maximum voltage command v_{max}^* is designated as v_{u0} in the U-phase, the middle voltage command v_{mid}^* (=0) is designated as v_{v0} in the V-phase, and the minimum voltage command v_{min}^* is designated as v_{w0} in the W-phase.

[0040] As is expressed by the foregoing expression (1), the maximum voltage command v_{max}^* is given as $v_{max}^* = v_{max} - v_{mid}$. Then, the voltage command v_{u0} as the maximum voltage command v_{max}^* becomes $v_u^* - v_v^*$, the difference between the output voltage command v_u^* with the maximum voltage and the output voltage command v_v^* with the middle voltage in the section 1 shown in FIG. 2. Moreover, by the expression (1), the middle voltage command v_{mid}^* is given as $v_{mid}^* = 0$. Then, the voltage command v_{v0} as the middle voltage command v_{mid}^* becomes zero in the section 1. In addition, by the expression (1), the minimum voltage command v_{min}^* is given as $v_{mm}^* = v_{min} - v_{mid}$. Then, the voltage command v_{w0} as the minimum voltage command v_{min}^* becomes $v_w^* - v_v^*$, the difference between the output voltage command v_w^* with the minimum voltage and the output voltage command v_v^* with the middle voltage in the section 1.

[0041] In the section 2, as is shown in FIG. 2, the maximum voltage command v_{max}, middle voltage command v_{mid} and minimum voltage command v_{min} before being compensated by the expressions (1) are the output voltage commands v_v^*, v_u^* and v_w^*, respectively. Then, the voltage command v_{v0} is outputted as the maximum voltage command v_{max}^*, the voltage command v_{u0} is outputted as the voltage command v_{mid}^* (= 0) and the voltage command v_{w0} is outputted as the minimum voltage command v_{min}^*. Similarly in the following, also with respect to each of the sections 3 to 6, as each of the voltage commands v_{max}^*, v_{mid}^* and v_{min}^* after being compensated, any one of v_{u0}, v_{v0} and v_{w0} is to be outputted.

[0042] In FIG. 3, in addition to the compensated voltage commands λ_{u0}, v_{v0} and v_{w0} in their respective phases, a

compensated zero-phase voltage command 3w is also shown. The zero-phase voltage command 3w is a command derived by carrying out the compensation of subtracting the middle voltage command v_{mid} from the zero-phase voltage with the value zero in the same way as is expressed in the expressions (1) with respect to each section in FIG. 2. However, since the zero-phase voltage is the reference voltage for a voltage in each phase, then, in a line-to-line voltage as a difference between a voltage in a certain phase and a voltage in another phase, the zero-phase voltages with respect to their respective voltages cancel out each other. Therefore, in each of the voltage commands v_{u0}, v_{v0} and v_{w0} which is provided as the difference between the voltage command in a certain phase and the voltage command in another phase as is expressed in the expressions (1), the zero-phase voltage commands 3w cancel out each other. Thus, the control of an output voltage according to each of the voltage commands λ_{u0}, v_{v0} and v_{w0} will be unaffected by the zero-phase voltage command 3w.

[0043] Return to FIG. 1. To an on-time ratio operating means 30, the maximum voltage command v_{max}^*, middle voltage command v_{mid}^* (=0) and minimum voltage command v_{min}^* in each section are inputted which are those after being compensated. The on-time ratio operating means 30 carries out operations by the following expressions (2) with the values of the maximum voltage command v_{max}^* and minimum voltage command v_{min}^* of the voltage commands and the values of the DC voltages Ed (DC high voltage) and -Ed (DC low voltage) in the DC circuit of the inverter to obtain on-time ratios λ_{max}^* and λ_{min}^*. The on-time ratio λ_{max}^* is the ratio of a time, during which the switching element S_1 in the DC circuit in the inverter is turned-on for providing an output corresponding to the maximum voltage command v_{max}^*, to one switching period in the switching operation of converting the DC voltages to an AC voltage. While, the on-time ratio λ_{min}^* is the ratio of a time, during which the switching element S_4 in the DC circuit in the inverter is turned-on for providing an output corresponding to the minimum voltage command v_{min}^*, to one switching period in the foregoing switching operation of the conversion:

$$\left.\begin{aligned} \lambda_{max}^* &= v_{max}^*/E_d \\ \lambda_{min}^* &= v_{min}^*/(-E_d) \end{aligned}\right\} \qquad (2)$$

where each of λ_{max}^* and λ_{min}^* has a value between 1 and 0.

[0044] As is apparent from the expressions (2), the on-time ratios λ_{max}^* and λ_{min}^* are proportional to the voltage commands v_{max}^* and v_{min}^*, respectively. Here, the value of λ_{min}^* is provided as a positive one.

[0045] The on-time ratio λ_{mid}^* with respect to the middle voltage command v_{mid}^* with the value thereof being zero is similarly provided as $\lambda_{min}^*=0$.

[0046] Here, consider the on-time ratio in the one switching period of each of switching elements in each phase.

[0047] In the section 1, the maximum voltage command v_{max} is the voltage command v_u^* in the U-phase. Then, the maximum voltage command v_{max}^* after being compensated is the voltage command v_{u0}.Therefore, the on-time ratio of the switching element S_1, which outputs the maximum voltage Ed in the DC circuit with respect to the U-phase in the three-level inverter shown in FIG. 14, is provided as λ_{max}^*. While, the switching element S_3 in the circuit is made to be turned-off while the switching element S_1 is turned-on and is made to be turned-on while the switching element S_1 is turned-off to output a voltage zero. Therefore, the on-time ratio thereof is provided as $1 - \lambda_{max}^*$. Furthermore, the switching element S_2, causing no short circuit in the DC power supply 102 even though it is turned-on, is made to be turned-on through the one switching period to be brought into a free-wheeling mode. The switching element S_4, since the DC circuit with respect to the U-phase outputs no minimum voltage -Ed in the section 1, is made to be turned-off through the one switching period.

[0048] From the foregoing, the respective on-time ratios λ_{maxS1} to λ_{maxS4} of the switching elements S_1 to S_4 for the maximum voltage command v_{max}^* are expressed as the expressions (3):

$$\left.\begin{aligned} \lambda_{maxS1} &= \lambda_{max}^* \\ \lambda_{maxS2} &= 1 \\ \lambda_{maxS3} &= 1 - \lambda_{max}^* \\ \lambda_{maxS4} &= 0 \end{aligned}\right\} . \qquad (3)$$

[0049] Next, in the section 1, the voltage command v_v^* in the V-phase has a middle value. Then, the compensated

middle voltage command v_{mid}^* having the value of zero becomes the voltage command v_{v0} in the V-phase. Therefore, in the DC circuit in the V-phase, on the basis of the on-time ratio $\lambda_{mid}^*(=0)$ for outputting the voltage zero, on-time ratios λ_{midS1} to λ_{midS4} of the switching elements S_1 to S_4, respectively, are provided as those expressed in the expressions (4). This makes the switching elements S_2 and S_3 turned-on and the switching elements S_1 and S_4 turned-off through the one switching period:

$$\left.\begin{aligned} \lambda_{midS1} &= 0 \\ \lambda_{midS2} &= 1 \\ \lambda_{midS3} &= 1 \\ \lambda_{midS4} &= 0 \end{aligned}\right\} . \qquad (4)$$

[0050] As is apparent from the expressions (4), for outputting the voltage zero according to the middle voltage command, each of the switching element S_2 and S_3 is fixed in a turned-on state and each of the switching element S_1 and S_4 is fixed in a turned-off state without carrying out switching operation in the one switching period.

[0051] Furthermore, in the section 1, the minimum voltage command v_{min} is the voltage command v_w^* in the W-phase. Then, the minimum voltage command v_{min}^* after being compensated is the voltage command v_{w0}. Therefore, the on-time ratio of the switching element S_4, which outputs the minimum voltage -Ed in the DC circuit with respect to the W-phase, equivalent to the DC circuit with respect to the U-phase in the three-level inverter shown in FIG. 14, is provided as λ_{min}^*. While, the switching element S_2 in the circuit is made to be turned-off while the switching element S_4 is turned-on and is made to be turned-on while the switching element S_4 is turned-off to output a voltage zero. Therefore, the on-time ratio thereof is provided as $1 - \lambda_{min}^*$. Furthermore, the switching element S_3, causing no short circuit in the DC power supply 101 even though it is turned-on, is made to be turned-on through the one switching period to be brought into a free-wheeling mode. The switching element S_1, since the DC circuit with respect to the W-phase outputs no maximum voltage Ed in the section 1, is made to be turned-off through the one switching period.

[0052] From the foregoing, the respective on-time ratios λ_{minS1} to λ_{minS4} of the switching elements S_1 to S_4 for the minimum voltage command v_{min}^* are expressed as the expressions (5):

$$\left.\begin{aligned} \lambda_{minS1} &= 0 \\ \lambda_{minS2} &= 1 - \lambda_{min}^* \\ \lambda_{minS3} &= 1 \\ \lambda_{minS4} &= \lambda_{min}^* \end{aligned}\right\} . \qquad (5)$$

[0053] The on-time ratio operating means 30 shown in FIG. 1 outputs the on-time ratios λ_{max}^*, λ_{mid}^* and λ_{min}^* obtained from the inputted maximum voltage command v_{max}^*, middle voltage command v_{mid}^* (=0) and minimum voltage command v_{min}^*, respectively, inputted in each section.

[0054] A by-phase on-time ratio operating means 40 converts the on-time ratios λ_{max}^*, λ_{mid}^* and λ_{min}^* in each of the foregoing sections, which ratios are inputted to the means 40 while being classified by value, into on-time ratios λ_u, λ_v and λ_w classified by phase of the U, V and W. As was explained in the foregoing, the on-time ratios λ_{max}^* and λ_{min}^* are proportional to the maximum voltage command v_{max} and v_{min}^*, respectively, and the value of the on-time ratio λ_{mid}^* is zero in correspondence with the value of the middle voltage command v_{mid}^* being zero. Therefore, the waveforms of the on-time ratios λ_u, λ_v and λ_w are geometrically similar to the waveforms of the voltage commands v_{u0}, v_{v0} and v_{w0} shown in FIG. 3, respectively. However, the on-time ratios corresponding to the negative voltage commands become positive.

[0055] A triangular wave comparing means 50 as a carrier comparison means compares the waveforms of the on-time ratios λ_u, λ_v and λ_w in their respective U-, V- and W-phases with a triangular wave as a carrier to obtain on-off commands for the switching elements in the DC circuit of the inverter in each of the U-, V- and W-phases from the result of the comparison and outputs the obtained commands. In FIG. 1, signs S_{u1} to S_{w4} designate on-off commands outputted from the triangular wave comparing means 50. Of the on-off commands S_{u1} to S_{w4}, the on-off commands S_{u1} to S_{u4} are

the on-off commands to four switching elements (corresponding to the switching elements S_1 to S_4 shown in FIG. 14) in the DC circuit in the U-phase, the on-off commands S_{v1} to S_{v4} are the on-off commands to four switching elements in the DC circuit in the V-phase not shown, and the on-off commands S_{w1} to S_{w4} are the on-off commands to four switching elements in the DC circuit in the W-phase not shown.

[0056] FIGURE 4 is a waveform diagram showing the operation of the triangular wave comparing means 50 according to the first embodiment in a part of the section 1 with (a) showing the waveforms of the on-time ratios λ_u, λ_v, λ_w in the U-, V- and W-phases, respectively, together with the waveform of the triangular wave as a carrier, (b) showing the waveforms of the on-off commands S_{u1} to S_{u4} to the switching elements in the inverter in the U-phase, (c) showing the waveforms of the on-off commands S_{v1} to S_{v4} to the switching elements in the inverter in the V-phase, (d) showing the waveforms of the on-off commands S_{w1} to S_{w4} to the switching elements in the inverter in the W-phase. That is, (b), (c) and (d) of FIG. 4 show the turned-on and -off states of the switching elements in the U-, V- and W-phases, respectively. Here, "a part of the section 1" is the part from 0.3 to 0.32 in the section 1 when letting the length (time length) of the section 1 shown in FIG. 2 and FIG. 3 be unity. In the following explanations, the reference signs of the on-off commands S_{u1} to S_{u4}, S_{v1} to S_{v4} and S_w to S_{w4} are to be also used as the reference signs of the switching elements.

[0057] By using an up-down counter contained in a device such as a microcomputer, a carrier of a triangular wave is formed which moves between 0 and 1 as is shown in (a) of FIG. 4. The time length from the time at which the carrier initiates an increase from zero to the time at which the carrier returns to zero again after reaching 1 and then turning back therefrom becomes the one switching period.

[0058] The triangular wave comparing means 50 shown in FIG. 1 is formed by using a comparator contained in a device such as a microcomputer, with which means the values of the on-time ratios λ_u, λ_v and λ_w, corresponding to the values of the waveforms of the voltage commands λ_{u0}, v_{v0}, v_{w0} in the U-, V- and W-phases shown in FIG. 3, respectively, are compared with the value of the triangular wave as a carrier as is shown in (a) of FIG. 4. The period of the triangular wave is equivalent to the one switching period of the switching element.

[0059] In the part of the section 1 shown in (a) of FIG. 4, the on-time ratios λ_u, λ_v and λ_w are shown as the on-time ratio λ_{max}* corresponding to the voltage command v_{u0} as the maximum voltage command v_{max}*, the on-time ratio λ_{mid}* corresponding to the voltage command v_{v0} as the middle voltage command λ_{mid}* and the on-time ratio λ_{min}* corresponding to the voltage command v_{w0} as the minimum voltage command v_{min}*, respectively. Here, however, the on-time ratio λ_w, shown as the on-time ratio λ_{min}* corresponding to the voltage command v_{w0} as the negative minimum voltage command λ_{min}*, is shown as being positive according to the expressions (2).

[0060] By the comparison between the value of the on-time ratio and the value of the carrier as the triangular wave, the time during which the value of the on-time ratio is equal to or more than the value of the triangular wave in the period of the triangular wave, i.e. the one switching period of a switching element, is determined as the time during which the switching element is made turned-on with the on-time ratio by an on-off command.

[0061] This can be explained by considering a triangle with the vertex thereof put on the horizontal axis in (a) of FIG. 4. The triangle is formed by the triangular wave and a straight line intersecting the triangular wave and representing, for example, the on-time ratio λ_u in the U-phase as the on-time ratio λ_{max}*. The triangle is one with the straight line that represents the on-time ratio $\lambda_u(\lambda_{max}$*) forming a base and the on-time ratio $\lambda_u(\lambda_{max}$*) therefore being the height thereof. Since the length of a base of a triangle is proportional to the height to the vertex opposite to the base, the ratio of the time, during which the value of the on-time ratio $\lambda_u(\lambda_{max}$*) is equal to or more than the value of the carrier, to the one switching period is the on-time ratio λ_{max}*. The time in the rest of the one period of the carrier, during which the value of the on-time ratio $\lambda_u(\lambda_{max}$*) is less than the value of the carrier, is proportional to the on-time ratio 1 - λ_{max}*.

[0062] The same is true for the on-time ratio λ_w in the W-phase shown as the on-time ratio λ_{min}*.

[0063] The on-time ratio λ_v in the V-phase shown as the on-time ratio λ_{mid}*(=0) is 0 on the basis of the same consideration as that in the foregoing.

[0064] In this way, by using one carrier signal of a triangular wave, on-off commands, each having a determined on-time ratio, are formed with respect to each of the phases as is shown in (b), (c) and (d) of FIG. 4.

[0065] In the section 1, as was explained in the foregoing, the voltage command v_{u0} in the U-phase is the maximum voltage command λ_{max}*. Therefore, in (b) of FIG. 4, waveforms of the on-off commands S_{u1} to S_{u4}, which are for carrying out switching of the switching elements S_{u1} to S_{u4} in the U-phase with the on-time ratios λ_{maxS1} to λ_{maxS4}, respectively, being provided by the expressions (3), are shown in the part of the section 1.

[0066] At the beginning of the one switching period, the value of the on-off command S_{u1} becomes 1 from 0 with the on-time ratio λ_{maxS1} provided as λ_{max}* as the on-time ratio λ_u by the expressions (3). Simultaneously with this, the value of the on-off command S_{u3} becomes 0 from 1.

[0067] Thereafter, the value of the on-off commands S_{u1} becomes 0. Simultaneously with this, the on-off commands S_{u3} becomes to have the value of 1 with the on-time ratio λ_{maxS3} provided as 1 - λ_{max}* by the expressions (3) and becomes to have the value 0 again at the end of the one switching period, i.e. at the beginning of the next one switching period. Simultaneously with this, the value of the on-off command S_{u1} becomes 1 again from 0.

[0068] This makes each of the switching elements S_{u1} and S_{u3} carry out two times of switching, four times in total of

both, in the one switching period (the switching elements S_{u1} is made to be turned-on, then turned-off and then turned-on and the switching element S_{u3} is made to be turned-off, then turned-on and then turned-off).

[0069] Compared with this, the on-time ratio λ_{maxS2} of the on-off command S_{u2} is left at 1 according to the expression $\lambda_{maxS2} = 1$ provided by the expressions (3) and the on-time ratio λ_{maxS4} of the on-off command S_{u4} is left at 0 according to the expression $\lambda_{maxS4} = 0$ provided by the expressions (3). That is, the switching elements S_{u2} and S_{u4} carry out no switching (turning-on and -off) .

[0070] Moreover, in the section 1, as was explained in the foregoing, the voltage command v_{v0} in the V-phase is the middle voltage command v_{mid}^* (=0). In correspondence with this, the on-time ratio λ_v of the on-off command is the on-time ratio λ_{mid}^*(=0). On the basis of this, in (c) of FIG. 4, waveforms of the on-off commands S_{v1} to S_{v4}, which are for carrying out switching of the switching elements S_{v1} to S_{v4} in the V-phase with the on-time ratios λ_{midS1} to λ_{midS4}, respectively, being provided by the expressions (4), are shown in the part of the section 1.

[0071] Namely, the on-time ratios λ_{midS2} and λ_{midS3} of the on-off commands S_{v2} and S_{v3} are left at 1 according to the expressions $\lambda_{midS2} = 1$ and $\lambda_{midS3} = 1$, respectively, which are provided by the expressions (4) and the on-time ratios λ_{midS1} and λ_{midS4} of the on-off commands S_{v1} and S_{v4} are left at 0 according to the expressions $\lambda_{midS1} = 0$ and $\lambda_{midS4} = 0$, respectively, which are provided by the expressions (4). This makes the switching elements S_{w2} and S_{w3} left turned-on and the switching elements S_{v1} and S_{v4} left turned-off. In this way, in the v-phase, all of the switching elements S_{v1} to S_{v4} carry out no switching (turning-on and -off) with the number of switching in the one switching period being zero.

[0072] Moreover, in the section 1, as was explained in the foregoing, the voltage command v_{v0} in the V-phase is the middle voltage command v_{mid}^* (=0). In correspondence with this, the on-time ratio λ_v of the on-off command is the on-time ratio λ_{mid}^*(=0). On the basis of this, in (c) of FIG. 4, waveforms of the on-off commands S_{v1} to S_{v4}, which are for carrying out switching of the switching elements S_{v1} to S_{v4} in the V-phase with the on-time ratios λ_{midS1} to λ_{midS4}, respectively, being provided by the expressions (4), are shown in the part of the section 1.

[0073] Namely, the on-time ratios λ_{midS2} and λ_{midS3} of the on-off commands S_{v2} and S_{v3} are left at 1 according to the expressions $\lambda_{midS2} = 1$ and $\lambda_{midS3} = 1$, respectively, which are provided by the expressions (4) and the on-time ratios λ_{midS1} and λ_{midS4} of the on-off commands S_{v1} and S_{v4} are left at 0 according to the expressions $\lambda_{midS1} = 0$ and $\lambda_{midS4} = 0$, respectively, which are provided by the expressions (4). This makes the switching elements S_{w2} and S_{w3} left turned-on and the switching elements S_{v1} and S_{v4} left turned-off. In this way, in the v-phase, all of the switching elements S_{v1} to S_{v4} carry out no switching (turning-on and -off) with the number of switching in the one switching period being zero.

[0074] Here, in (c) of FIG. 4, the waveforms (characteristic lines) of the on-off commands S_{v3} and S_{v2} to their respective switching elements S_{v3} and S_{v2} coincide with each other and the waveforms (characteristic lines) of the on-off commands S_{v4} and S_{v1} to their respective switching elements S_{v4} and S_{v1} coincide with each other. Thus, the characteristic lines are shown as those for the switching elements S_{v3} and S_{v4} only.

[0075] Furthermore, in the section 1, as was explained in the foregoing, the voltage command v_{w0} in the W-phase is the minimum voltage command v_{min}^*. Therefore, in (d) of FIG. 4, waveforms of the on-off commands S_{w1} to S_{w4}, which are for carrying out switching of the switching elements S_{w1} to S_{w4} in the W-phase with the on-time ratios λ_{minS1} to λ_{minS4}, respectively, being provided by the expressions (5), are shown in the part of the section 1.

[0076] At the beginning of the one switching period, the value of the on-off command S_{w4} becomes 1 from 0 with the on-time ratio λ_{minS4} provided as λ_{min}^* as the on-time ratio λ_w by the expressions (5). Simultaneously with this, the value of the on-off command S_{w2} becomes 0 from 1.

[0077] Thereafter, the value of the on-off commands S_{w4} becomes 0. Simultaneously with this, the on-off commands S_{w2} becomes to have the value of 1 with the on-time ratio λ_{minS2} provided as $1 - \lambda_{min}^*$ by the expressions (5) and becomes to have the value 0 again at the end of the one switching period, i.e. at the beginning of the next one switching period. Simultaneously with this, the value of the on-off command S_{w2} becomes 1 again from 0.

[0078] This makes each of the switching elements S_{w2} and S_{w4} carry out two times of switching, four times in total of both, in the one switching period like the switching elements S_{u1} and S_{u3} in the U-phase.

[0079] Compared with this, the on-time ratio λ_{minS1} of the on-off command S_{w1} is left at 0 according to the expression $\lambda_{minS1} = 0$ provided by the expressions (5) and the on-time ratio λ_{minS3} of the on-off command S_{w3} is left at 1 according to the expression $\lambda_{minS3} = 1$ provided by the expressions (5). That is, the switching elements S_{w1} and S_{w3} carry out no switching (turning-on and -off) .

[0080] By the switching operation like in the foregoing, a train of rectangular waves each with an on-time ratio changing with time, that is, a train of rectangular waves each with a width proportional to the value of the compensated voltage command changing with time, are formed with respect to each of three phases of the U-, V- and W-phases. The train of the rectangular waves are subjected to known demodulating processing to be converted into a three-level AC voltage.

[0081] As is explained in the foregoing, according to the first embodiment, the three-level inverter can be controlled by carrying out switching of eight times per switching period.

[0082] Moreover, the carrier of the triangular wave, which is used for outputting the on-off commands in the U- V- and W-phases with the predetermined on-time ratios λ_u, λ_v and λ_w, respectively, in each section, can be produced by an up-down counter contained in a device such as a common microcomputer. This requires no high performance and high

expensive operation device to make it possible to avoid an increase in cost.

[0083] In the foregoing inverter according to the first embodiment, it is possible to reduce switching losses by reducing the number of times of switching and, along with this, to lower the cost of the control system with the use of an inexpensive device such as a microcomputer.

[0084] The control system according to the first embodiment, however, has the following problem. Namely, the voltage command after being compensated and shown in FIG. 3 has an amplitude ($\pm$0.75 in the embodiment) larger than the amplitude ($\pm$0. 5 in the embodiment) of the voltage command shown in FIG. 2 which is inputted to the control system. Therefore, when the amplitude of the inputted voltage command becomes large, the value of the maximum voltage command v_{max}* after being compensated and the absolute value of the minimum voltage command v_{mm}* after being compensated are sometimes calculated as being larger than the absolute value E_d of the power supply voltage to cause the values of the on-time ratios λ_{max}* and λ_{min}* to exceed 1. Since this is not permitted, the values of the on-time ratios λ_{max}* and λ_{min}* are restricted to 1. This results in saturation in the inverted output voltages to make it impossible to output correct voltages according to commands to thereby restrict the values of voltages that can be normally outputted.

[0085] Accordingly, in the following second embodiment, a control system is actualized in which the range of the voltage that can be normally outputted is expanded with the number of times of switching equal to that in the first embodiment.

[0086] FIGURE 5 is a functional block diagram showing a configuration of a control system according to a second embodiment (corresponding to the fourth to the sixth aspects) of the invention. The control system, like the control system according to the first embodiment, is formed with hardware and software of a microcomputer system. Also the embodiment will be explained as a control system of the three-level inverter shown in FIG. 14. The embodiment, however, can be of course applied also to the control of the three-level inverter shown in FIG. 13.

[0087] FIGURE 6 is a waveform diagram showing the waveforms of three-phase output voltage commands v_u*, v_v* and v_w* in the control system according to the second embodiment.

[0088] In FIG. 5, constituents with similar functions to those of constituents shown in FIG. 1 will be denoted with similar reference numerals and signs. In the following, explanations will be made with particular emphasis on parts different from those shown in FIG. 1.

[0089] In FIG. 5, reference numeral 60 denotes a maximum, middle and minimum voltage command operating means, to which three-phase AC output voltage commands v_u*, v_v* and v_w* shown in FIG. 6 are inputted like in the first embodiment.

[0090] In each of sections to be explained later, from the inputted three-phase AC output voltage commands v_u*, v_v* and v_w*, an absolute maximum value command discriminating means 70 detects a voltage command having an absolute maximum value as an absolute maximum voltage command v_{max}. From the detected absolute maximum voltage command v_{max}* and the polarity (sign) thereof, the absolute maximum value command discriminating means 70 further obtains an absolute maximum voltage command v_0* as a compensation value to be explained later and output it to the maximum, middle and minimum voltage command operating means 60.

[0091] As is shown in FIG. 6, the one period of each of the voltage commands is divided into six, from the section 1 to the section 6. With respect to each section, the maximum, middle and minimum voltage command operating means 60, according to a selection table given as Table 2, determines a phase with stopped switching and a voltage level produced in the phase before carrying out operations for obtaining v_{max}*, v_{mid}* and v_{mm}* as being maximum, middle and minimum voltage commands, respectively, which will be explained later.

Table 2

SECTION	ABSOLUTE MAX. VOLTAGE COMMAND v_{max}	SIGN OF v_{MAX} Sign	PHASE WITH STOPPED SWITCHING AND VOLTAGE LEVEL PRODUCED IN THE PHASE
1	v_u*	+	U-PHASE, Ed
2	v_w*	-	W-PHASE, -Ed
3	v_v*	+	V-PHASE, Ed
4	v_u*	-	U-PHASE, -Ed
5	v_w*	+	W-PHASE, Ed
6	v_v*	-	V-PHASE, -Ed

[0092] For example, in the section 1 shown in FIG. 6, the voltage command v_u^* in the U-phase has the maximum value with the absolute value thereof also being maximum compared with the voltage command v_v^* in the V-phase and the voltage command v_w^* in the W-phase. Therefore, of the switching elements connected to the U-phase output terminal in the DC circuit shown in FIG. 14, the switching element S_1 between the U-phase output terminal and the DC high voltage E_d is made to be turned-on over one switching period to thereby produce the voltage E_d at the U-phase output terminal. At this time, the switching elements S_3 and S_4 are made to be turned-off for preventing the DC power supply from being short-circuited and the switching element S_2 is made to be turned-on for being brought into a fly-wheeling mode.

[0093] In the section 2 shown in FIG. 6, the voltage command v_w^* in the W-phase has the minimum value with the absolute value thereof being maximum compared with the voltage command v_u^* in the U-phase and the voltage command v_v^* in the V-phase. Therefore, of the switching elements connected to the W-phase output terminal in the DC circuit shown in FIG. 14, the switching element S_4 between the W-phase output terminal and the low DC voltage $-E_d$ (Although FIG. 14 shows the DC circuit in the U-phase, the DC circuit in the W-phase has a configuration identical to the DC circuit shown in FIG. 14. Therefore, the switching element is to be denoted as S_4 here) is made to be turned-on over one switching period to thereby produce the voltage $-E_d$ at the W-phase output terminal. At this time, the switching elements S_1 and S_2 are made to be turned-off for preventing the DC power supply from being short-circuited and the switching element S_3 is made to be turned-on for being brought into a fly-wheeling mode.

[0094] The operations of the absolute maximum value command discriminating means 70 and the maximum, middle and minimum voltage command operating means 60 will be further explained as follows.

[0095] The absolute maximum value command discriminating means 70 obtains the absolute maximum voltage command v_0^* as a compensation value by the expression (6):

$$v_0^* = \mathrm{sign}(v_{max})E_d - v_{max} \qquad (6)$$

where sign (v_{max}) represents the polarity of the voltage command v_{max} with the absolute value thereof becoming maximum, which becomes 1 when v_{max} is positive and becomes -1 when v_{max} is negative. Therefore, when v_{max} is positive, v_0^* is provided as $v_0^* = E_d - v_{max}$ and, when v_{max} is negative, v_0^* is provided as $v_0^* = -(|E_d| - |v_{max}|)$.

[0096] Next to this, the maximum, middle and minimum voltage command operating means 60 classifies the original output voltage commands v_u^*, v_v^* and v_w^* by value into an absolute maximum voltage command v_{max}, a middle voltage command v_{mid} and a minimum voltage command v_{min} in each section like in the first embodiment. With respect to thus classified voltage commands, the maximum, middle and minimum voltage command operating means 60 carries out operations of compensating them with the absolute maximum voltage command v_0^* obtained by the expression (6) as are expressed by the following expressions (7) to obtain a maximum voltage command v_{max}^*, a middle voltage command v_{mid}^* and a minimum voltage command v_{min}^*. With the absolute maximum voltage command v_0^* obtained by the expression (6), the maximum voltage command v_{max}^* in the expressions (7) becomes E_d or $-E_d$:

$$\left.\begin{aligned} v_{max}^* &= v_{max} + v_0^* = \mathrm{sign}(v_{max})E_d \\ v_{mid}^* &= v_{mid} + v_0^* \\ v_{min}^* &= v_{min} + v_0^* \end{aligned}\right\}. \qquad (7)$$

[0097] FIGURE 7 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 2 are compensated according to the expressions (7). For easy understanding, the waveforms of the voltage commands v_{u0}, v_{v0} and v_{w0} shown in FIG. 7 are shown in FIG. 8A, FIG. 8B and FIG. 8C, respectively. In addition, FIG. 8D shows only a zero-phase voltage command 3w shown in FIG. 7. The zero-phase voltage command 3w, when expressed according to the expressions (7), becomes as $0 + v_0^* = v_0^*$, which is equivalent to the absolute maximum voltage command v_0^* given by the expression (6).

[0098] However, since the zero-phase voltage is the reference voltage for a voltage in each phase, then, in a line-to-line voltage as a difference between a voltage in a certain phase and a voltage in another phase, the zero-phase voltages with respect to their respective voltages cancel out each other. Therefore, in each of the voltage commands v_{u0}, v_{v0} and v_{w0} which is provided as the difference between the voltage command in a certain phase and the voltage command in another phase as is expressed in the expressions (7), the zero-phase voltage commands 3w cancel out each other. Thus, the control of an output voltage according to each of the voltage commands v_{u0}, v_{v0} and v_{w0} will be unaffected by the zero-phase voltage command 3w.

[0099] As is apparent from FIG. 7 and FIGS. 8A to 8C, in the section 1 to section 6, in a phase in which the absolute value of a voltage command is maximum (hereinafter referred to as an "absolute maximum value phase"), the value of the maximum voltage command v_{max}^* is 1 or -1 when letting the value of the voltage E_d be 1. For example, as the maximum voltage command v_{max}^*, the voltage command v_{u0} with the value 1 in the U-phase is outputted in the section 1, the voltage command v_{w0} with the value -1 in the W-phase is outputted in the section 2 and the voltage command v_{v0} with the value 1 in the V-phase is outputted in the section 3.

[0100] That is, by fixing the value of the voltage command in a phase with the absolute value of the voltage command being maximum in each section at 1 or -1, as was shown in the foregoing Table 2, the switching operation in the phase is stopped, by which the DC high voltage Ed or the low DC voltage -Ed is to be continuously outputted.

[0101] Subsequent to this, as is shown in FIG. 5, to an on-time ratio operating means 30, the maximum voltage command v_{max}^*, middle voltage command v_{mid}^* and minimum voltage command v_{min}^* in each section are inputted which are those after being compensated. The on-time ratio operating means 30 carries out operations by the following expressions (8) with the values of the middle voltage command v_{mid}^* and minimum voltage command v_{min}^* of the voltage commands and the values of the DC voltages Ed and -Ed in the DC circuit of the inverter to obtain on-time ratios λ_{mid}^* and λ_{min}^*. The on-time ratio λ_{mid}^* is the ratio of a time, during which the switching element in a phase with the absolute value of the middle voltage command v_{mid}^* being a middle value (hereinafter referred to as an "absolute middle value phase") is turned-on, to the one switching period. While, the on-time ratio λ_{min}^* is the ratio of a time, during which the switching element in a phase with the absolute value of the minimum voltage command v_{min}^* being a minimum value (hereinafter referred to as an "absolute minimum value phase") is turned-on, to the one switching period:

$$\left.\begin{aligned} \lambda_{mid}^* &= v_{mid}^*/E_d \\ \lambda_{min}^* &= v_{min}^*/E_d \end{aligned}\right\} \quad (8)$$

where each of λ_{max}^* and λ_{min}^* has a positive value between 1 and 0. As is apparent from the expressions (8), the on-time ratios λ_{max}^* and λ_{min}^* are proportional to the absolute value of the middle voltage command v_{max}^* and the absolute value of the minimum voltage command v_{min}^*, respectively. In addition, in a phase with the maximum voltage command v_{max}^*, the on-time ratio λ_{max}^* becomes 1 when the maximum voltage command v_{max}^* is positive, with which the switching element S_1 is made to be turned-on, and becomes 0 when the maximum voltage command v_{max}^* is negative, with which the switching element S_4 is made to be turned-on.

[0102] Here, consider the on-time ratio in the one switching period of each of switching elements in each phase.

[0103] In the section 1, as is shown in FIG. 8A, the voltage command v_{u0} in the U-phase is the maximum voltage command v_{max}^* with the absolute value thereof being maximum. Thus, the on-time ratio of the switching element S_1 becomes 1 in the DC circuit with respect to the U-phase in an inverter shown in FIG.14. In this case, as was explained in the foregoing, the on-time ratios of the switching elements S_3 and S_4 become zero and the on-time ratio of the switching element S_2 becomes 1. From the foregoing, the respective on-time ratios λ_{uS1} to λ_{uS4} of the switching elements S_1 to S_4 in the U-phase as the absolute maximum value phase are expressed as the expressions (9):

$$\left.\begin{aligned} \lambda_{uS1} &= 1 \\ \lambda_{uS2} &= 1 \\ \lambda_{uS3} &= 0 \\ \lambda_{uS4} &= 0 \end{aligned}\right\}. \quad (9)$$

[0104] In the section 2, as is shown in FIG. 8C, the voltage command v_{w0} in the W-phase is the maximum voltage command v_{max}^* in the absolute maximum value phase with the polarity thereof being negative. Thus, the respective on-time ratios λ_{wS1} to λ_{wS4} of the switching elements S_1 to S_4 in the W-phase as the absolute maximum value phase are expressed as the expressions (10) :

$$\left.\begin{aligned} \lambda_{wS1} &= 0 \\ \lambda_{wS2} &= 0 \\ \lambda_{wS3} &= 1 \\ \lambda_{wS4} &= 1 \end{aligned}\right\} \quad (10)$$

[0105] In addition, in the section 1, as is shown in FIGS. 8B and 8C, the middle voltage command v_{mid}^* in the absolute middle value phase shifts from the voltage command v_{w0} in the W-phase to the voltage command v_{v0} in the V-phase with the polarities thereof being positive. Therefore, switching is carried out between the DC high voltage E_d and the DC middle voltage, i.e. zero voltage. For such switching, the respective on-time ratios λ_{midS1} to λ_{midS4} of the switching elements S_1 to S_4 in the DC circuit in each of the W-phase and the V-phase as the absolute middle value phase are expressed as the expressions (11):

$$\left.\begin{aligned} \lambda_{midS1} &= \lambda_{mid}^* \\ \lambda_{midS2} &= 1 \\ \lambda_{midS3} &= 1 - \lambda_{mid}^* \\ \lambda_{midS4} &= 0 \end{aligned}\right\} \quad (11)$$

[0106] Furthermore, in the section 1, as is also shown in FIGS. 8B and 8C, the minimum voltage command v_{min}^* in the absolute minimum value phase shifts from the voltage command v_{v0} in the V-phase to the voltage command v_{w0} in the W-phase with the polarities thereof being negative. Therefore, switching is carried out between the DC middle voltage, i.e. zero voltage and the DC low voltage $-E_d$. For such switching, the respective on-time ratios λ_{minS1} to λ_{minS4} of the switching elements S_1 to S_4 in the DC circuit in each of the V-phase and the W-phase as the absolute minimum value phase are expressed as the expressions (12):

$$\left.\begin{aligned} \lambda_{minS1} &= 0 \\ \lambda_{minS2} &= 1 - \lambda_{min}^* \\ \lambda_{minS3} &= 1 \\ \lambda_{minS4} &= \lambda_{min}^* \end{aligned}\right\} \quad (12)$$

[0107] The on-time ratio operating means 30 shown in FIG. 5 outputs the on-time ratios λ_{max}^*, λ_{mid}^* and λ_{min}^* obtained from the inputted maximum voltage command v_{max}^*, middle voltage command v_{mid}^* and minimum voltage command v_{min}^*, respectively.

[0108] A by-phase on-time ratio operating means 40 converts the on-time ratios λ_{max}^*, λ_{mid}^* and λ_{min}^* in each of the foregoing sections, which ratios are inputted to the means 40 while being classified by value, into on-time ratios λ_u, λ_v and λ_w classified by phase of the U, V and W. As was explained in the foregoing, the on-time ratios λ_{mid}^* and λ_{min}^* are proportional to the middle voltage command v_{mid}^* and the minimum voltage command v_{min}^*, respectively, and the value of the on-time ratio λ_{max}^* is 1 or zero. Therefore, the waveforms of the on-time ratios λ_u, λ_v and λ_w are geometrically similar to the waveforms of the voltage commands v_{u0}, v_{v0} and v_{w0} shown in FIGS. 8A, 8B and 8C, respectively. However, the on-time ratios corresponding to the negative voltage commands become positive.

[0109] A triangular wave comparison means 50 as a carrier comparison means compares the waveforms of the on-time ratios λ_u, λ_v and λ_w in their respective U-, V- and W-phases with a triangular wave as a carrier to obtain on-off commands for the switching elements in the DC circuit of the inverter in each of the U-, V- and W-phases from the result of the comparison and outputs the obtained commands. Like in FIG. 1 showing the configuration of the control system

according to the first embodiment, signs S_{u1} to S_{w4} designate on-off commands outputted from the triangular wave comparison means 50. Of the on-off commands S_{u1} to S_{w4}, the on-off commands S_{u1} to S_{u4} are the on-off commands to four switching elements (corresponding to the switching elements S_1 to S_4 shown in FIG. 14) in the DC circuit in the U-phase, the on-off commands S_{v1} to S_{v4} are the on-off commands to four switching elements in the DC circuit in the V-phase not shown, and the on-off commands S_{w1} to S_{w4} are the on-off commands to four switching elements in the DC circuit in the V-phase not shown.

[0110] FIGURE 9 is a waveform diagram showing the operation of the triangular wave comparing means 50 according to the second embodiment in a part of the section 1 with (a) showing the waveforms of the on-time ratios λ_u, λ_v, λ_w in the U-, V- and W-phases, respectively, together with the waveform of the triangular wave as a carrier, (b) showing the waveforms of the on-off commands S_{u1} to S_{u4} to the switching elements in the inverter in the U-phase, (c) showing the waveforms of the on-off commands S_{v1} to S_{v4} to the switching elements in the inverter in the V-phase, (d) showing the waveforms of the on-off commands S_{w1} to S_{w4} to the switching elements in the inverter in the W-phase. That is, (b), (c) and (d) of FIG. 9 show the turned-on and -off states of the switching elements in the U-, V- and W-phases, respectively. Here, "a part of the section 1" is the part from 0 to 0. 02 in the section 1 when letting the length (time length) of the section 1 shown in FIG. 6 to FIG. 8D be unity. In the following explanations, the reference signs of the on-off commands S_{u1} to S_{u4}, S_{v1} to S_{v4} and S_{w1} to S_{w4} are to be also used as the reference signs of the switching elements.

[0111] Like in the first embodiment, by using an up-down counter, a carrier of a triangular wave is formed which moves between 0 and 1 as is shown in (a) of FIG. 9. The time length from the time at which the carrier initiates an increase from zero to the time at which the carrier returns to zero again after reaching 1 and then turning back therefrom becomes the one switching period.

[0112] Like in the first embodiment, the triangular wave comparison means 50 shown in FIG. 5 is also formed by using a comparator contained in a device such as a microcomputer, with which means the values of the on-time ratios λ_u, λ_v and λ_w, corresponding to the values of the waveforms of the voltage commands v_{u0}, v_{v0}, v_{w0} in the U-, V- and W-phases shown in FIGS. 8A to 8C, respectively, are compared with the value of the triangular wave as a carrier as is shown in (a) of FIG. 9. The period of the triangular wave is equivalent to the one switching period of the switching element.

[0113] In the part of the section 1 shown in (a) of FIG. 9, the on-time ratio λ_u is shown as the on-time ratio λ_{max}^* (=1) corresponding to the voltage command v_{u0} as the maximum voltage command v_{max}^* (=1). The on-time ratio λ_v is shown as the on-time ratio λ_{min}^* corresponding to the voltage command v_{v0} as the minimum voltage command v_{min}^* before the voltage command v_{v0} is shifted to the middle voltage command v_{mid}^*, and the on-time ratio λ_w is shown as the on-time ratio λ_{mid}^* corresponding to the voltage command v_{w0} as the minimum voltage command v_{mid}^* before the voltage command v_{w0} is shifted to the minimum voltage command v_{min}^*. Here, however, the on-time ratio λ_v as the on-time ratio λ_{min}^* corresponding to the voltage command v_{v0} being the negative minimum voltage command v_{min}^*, is shown as being positive according to the expressions (8).

[0114] In addition, the part of the section 1 shown in FIG. 9 is the part from 0 to 0.02 to the 1 as the length of the section 1, i.e. a very short part of only 2% of the section 1. Therefore, in such a short part, the waveform of the on-time ratio can be regarded as a straight line approximately representing a constant value and in parallel to the horizontal axis.

[0115] Like in the first embodiment, by the comparison between the value of the on-time ratio and the value of the carrier as the triangular wave, the time during which the value of the on-time ratio is equal to or more than the value of the carrier in the one switching period of the carrier, i.e. the one switching period of a switching element, is determined as the time during which the switching element is made turned-on with the on-time ratio by an on-off command.

[0116] In this way, by using one carrier signal of a triangular wave, on-off commands, each having a determined on-time ratio, are formed with respect to each of the phases as is shown in (b), (c) and (d) of FIG. 9.

[0117] As is shown in (a) of FIG. 9, in the section 1, the on-time ratio λ_u has the maximum value. Therefore, in (b) of FIG. 9, waveforms of the on-off commands S_{u1} to S_{u4}, which are for carrying out switching of the switching elements S_{u1} to S_{u4} in the V-phase with the on-time ratios λ_{uS1} to λ_{uS4}, respectively, being provided by the expressions (9), are shown in the part of the section 1.

[0118] Namely, the on-time ratios λ_{uS1} and λ_{uS2} of the on-off commands S_{u1} and S_{u2} are left at 1 according to the expressions $\lambda_{uS1} = 1$ and $\lambda_{uS2} = 1$, respectively, which are provided by the expressions (9) and the on-time ratios λ_{uS3} and λ_{uS4} of the on-off commands S_{u3} and S_{u4} are left at 0 according to the expressions $\lambda_{uS3} = 0$ and $\lambda_{uS4} = 0$, respectively, which are provided by the expressions (9). This makes the switching elements S_{ui} and S_{u2} left turned-on and the switching elements S_{u3} and S_{u4} left turned-off. In this way, in the U-phase, all of the switching elements S_{u1} to S_{u4} carry out no switching with the number of switching in the one switching period being zero.

[0119] Here, in (b) of FIG. 9, the waveforms (characteristic lines) of the on-off commands S_{u1} and S_{u2} to their respective switching elements S_{u1} and S_{u2} coincide with each other and the waveforms (characteristic lines) of the on-off commands S_{u3} and S_{u4} to their respective switching elements S_{u3} and S_{u4} coincide with each other.

[0120] In (c) of FIG. 9, waveforms of the on-off commands S_{v1} to S_{v4}, which are for carrying out switching of the switching elements S_{v1} to S_{v4} in the V-phase with the on-time ratios λ_{midS1} to λ_{midS4}, respectively, being provided by the expressions (11), are shown in the part of the section 1.

[0121] This makes each of the switching elements S_{v1} and S_{v3} carry out two times of switching, four times in total of both, in the one switching period.

[0122] Compared with this, the on-time ratio λ_{midS2} of the on-off command S_{v2} is left at 1 according to the expression $\lambda_{midS2} = 1$ provided by the expressions (11) and the on-time ratio λ_{midS4} of the on-off command S_{v4} is left at 0 according to the expression $\lambda_{midS4} = 0$ provided by the expressions (11). That is, the switching elements S_{v2} and S_{v4} carry out no switching.

[0123] In (d) of FIG. 9, waveforms of the on-off commands S_{w1} to S_{w4}, which are for carrying out switching of the switching elements S_{w1} to S_{w4} in the W-phase with the on-time ratios λ_{minS1} to λ_{minS4}, respectively, being provided by the expressions (12), are shown in the part of the section 1.

[0124] This makes each of the switching elements S_{w2} and S_{w4} carry out two times of switching, four times in total of both, in the one switching period like the switching elements S_{u1} and S_{u3} in the U-phase.

[0125] Compared with this, the on-time ratio λ_{minS1} of the on-off command S_{w1} is left at 0 according to the expression $\lambda_{minS1} = 0$ provided by the expressions (12) and the on-time ratio λ_{minS3} of the on-off command S_{w3} is left at 1 according to the expression $\lambda_{minS3} = 1$ provided by the expressions (12). That is, the switching elements S_{w1} and S_{w3} carry out no switching.

[0126] By the switching operation like in the foregoing, a train of rectangular waves each with an on-time ratio changing with time, that is, a train of rectangular waves each with a width proportional to the value of the compensated voltage command changing with time, are formed with respect to each of three phases of the U-, V- and W-phases. The train of the rectangular waves are subjected to known demodulating processing to be converted into a three-level AC voltage.

[0127] Therefore, also in the first embodiment, like in the first embodiment, the three-level inverter can be controlled by carrying out switching of eight times per switching period.

[0128] Moreover, the carrier of the triangular wave can be easily produced to make it possible to form the control device at a low cost.

[0129] Furthermore, in the second embodiment, no restriction is imposed on the amplitude of a voltage command, namely the value of a voltage that can be outputted from a three-level inverter.

[0130] FIGURE 10 is a waveform diagram showing the waveforms of the voltage commands v_{u0}, v_{v0} and v_{w0} after the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 2 are compensated with their respective amplitudes increased from illustrated 0.5 to 0.8 (letting the DC voltage be 1, from 50% to 80% to the DC voltage) in the first embodiment. FIGURE 11 is a waveform diagram showing the waveforms of voltage commands v_{u0}, v_{v0} and v_{w0} after the compensation according to the second embodiment is carried out with respect to the output voltage commands v_u^*, v_v^* and v_w^* shown in FIG. 6 with their respective amplitudes similarly increased from illustrated 0.5 to 0.8.

[0131] As is apparent from FIG. 10, in the first embodiment, some parts of each of the voltage commands v_{u0}, v_{v0} and v_{w0} are outside the range of -1 to 1, that is, outside the DC power supply voltage ranging from $-E_d$ to E_d. Since the inverter cannot outputs a voltage with the absolute value thereof being larger than the power supply voltage E_d, the part of the voltage command with the value thereof exceeding 1 or -1 cannot produce voltages according to the command. This means that the output voltages are saturated to be distorted. This is because the compensation in the first embodiment is carried out so as to add a middle voltage command in the phase with the middle voltage command to a voltage commands in other phases as is expressed in the expressions (1) with the switching made stopped in the phase with the middle voltage command. That is, this is because in the phase with the maximum voltage command, an increased amplitude of the voltage command sometimes causes the value of the voltage command after the compensation to become larger than the value of the original maximum voltage command and exceed 1 by the addition.

[0132] Compared with this, in the second embodiment, with the value of the DC power supply voltage taken as 1, control is carried out so that the compensated value of the voltage command, the absolute value of which is maximum in each phase, becomes 1. Therefore, no voltage commands in the other phases exceed 1 to make it possible to output voltages while being limited to the value of the DC power supply voltage, by which there is no possibility of causing distortions in the output voltages.

[0133] In the first embodiment, in a region in which the amplitude of the voltage command is small, the value of the zero-phase voltage command 3w is smaller than that in the second embodiment, which provides the advantage of small potential variations in the zero-phase as a common mode that cause small noises.

[0134] Therefore, it is preferable to make use of the respective merits of the first embodiment and the second embodiment to distinguish between the use of the first embodiment and the use of the second embodiment according to the ratio of the amplitude of the voltage command to the DC power supply voltage.

[0135] Namely, as is explained in the seventh aspect of the invention and shown in FIG. 12, an explanatory diagram showing the discrimination for switching between the control according to the first embodiment and the control according to the second embodiment, a discriminating means is provided for carrying out switching so that, with respect to the region in which the ratio of the amplitude as the maximum value of the voltage command to the DC power supply voltage is equal to or less than 0.6, the control of output voltages is carried out with the on-time ratios determined by the operations according to the first embodiment and, with respect to the region in which the ratio is more than 0.6, the control of output

voltages is carried out with the on-time ratios determined by the operations according to the second embodiment.

[0136] The foregoing ratio 0.6 is a rough measure, which can be corrected with the voltage drops in the semiconductor switching elements and errors in detection circuits in detection circuits taken into consideration.

[0137] The switching between control according to the first embodiment and the control according to the second embodiment switches the operation procedures of the voltage commands. Then, operations of the voltages commands according to both of the embodiments are not simultaneously carried out in parallel to cause no fear of increasing the burden of operational processing in a microcomputer. Furthermore, since the foregoing switching is carried out only by switching between voltage commands to be compared with the carrier, no shock due to pulses is generated at switching.

[0138] While the present invention has been particularly shown and described with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details can be made therein without departing from the spirit and scope of the present invention.

Claims

1. A method for controlling a three-level inverter in a configuration in which three three-level inverters are connected in parallel to each other, the method comprising:

the three three-level inverters carrying out turning-on and -off of a plurality of semiconductor switching elements, wherein
at least one semiconductor switching element is connected between a high voltage point of a DC circuit and one output terminal,
at least one semiconductor switching element is connected between a middle voltage point of the DC circuit and the output terminal, and
at least one semiconductor switching element is connected between a low voltage point of the DC circuit and the output terminal, and
enabling any one out of the three voltage levels of a DC high voltage, DC middle voltage, and DC low voltage as the base of an AC voltage for one phase to be outputted from the output terminal,
the method makes a plurality of the semiconductor switching elements in each of the three three-level inverters turned-on and -off on the basis of output voltage commands of three-phase AC voltages to thereby make the three-phase AC voltage outputted,
the method comprising the steps of:

carrying out operations for obtaining on-time ratios of a plurality of the semiconductor switching elements in each of the three three-level inverters on the basis of the output voltage commands of the three-phase AC voltages;
dividing the one period of the output voltage command of the three-phase AC voltage into a plurality of sections; and
in each of the sections,
making the three-level inverter for one phase alternately turn-on and-off the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC high voltage and the DC middle voltage;
along with this, making the three-level inverter for one other phase fix the at least one switching element connected between the middle voltage point and the output terminal in a turned-on state to output the DC middle voltage; and
along with this, further making the three-level inverter for the remaining one phase alternately turn-on and -off the at least one semiconductor switching element connected between the middle voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal with their respective operated on-time ratios in the one switching period to alternately output the DC middle voltage and the DC low voltage.

2. The method for controlling a three-level inverter according to claim 1, further comprising the steps of:

in each of the sections,
with respect to a phase with the value of the output voltage command being a maximum value, carrying out compensation of subtracting a middle value of the output voltage command in another phase from the maximum

value to provide thus compensated value as the value of a maximum voltage command in the phase in the section;
with respect to the phase with the value of the output voltage command being the middle value, carrying out compensation of providing 0 as the value of a middle voltage command in the phase in the section;
with respect to the rest phase with the value of the output voltage command being a minimum value, carrying out compensation of subtracting the middle value of the output voltage command from the minimum value to provide thus compensated value as the value of a minimum voltage command in the phase in the section;
with respect to the phase with the value of the output voltage command being the minimum value, carrying out an operation of dividing the value of the maximum voltage command by the value of the DC high voltage to provide the on-time ratio of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the three-level inverter on the basis of the result of the division;
with respect to the phase with the value of the output voltage commandbeing the middle value, carrying out an operation of providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the turned-on state in the three-level inverter in the phase on the basis of the value 0; and
with respect to the phase with the value of the output voltage command being the minimum value, carrying out an operation of dividing the value of the minimum voltage command by the value of the DC low voltage to provide the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the three-level inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal in the three-level inverter on the basis of the result of the division.

3. A system for controlling a three-level inverter for carrying out the method according to claim 1 or 2 comprising:

a middle phase selecting means (20) configured for selecting, in each of the sections, an output voltage command of a phase with the value thereof being a middle value from the output voltage commands of the three-phase AC voltage;
a maximum, middle and minimum voltage command operating means (10) configured for classifying, in each of the sections, the output voltage commands of the three-phase AC voltage by value into a voltage command of a phase with the value thereof being a maximum value, the selected voltage command of the phase with the value thereof being the middle value and a voltage command of a phase with the value thereof being a minimum value, and carrying out the compensation of subtracting the selected middle value from each of the classified output voltage commands to output the compensated results as a maximum voltage command, a middle voltage command with zero value and a minimum voltage command;
an on-time ratio operating means (30) configured for carrying out, in each of the sections, an operation of dividing the value of the inputted maximum voltage command by the value of the DC high voltage to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between the high voltage point of the DC circuit and the one output terminal, carrying out an operation of converting the value 0 of the inputted middle voltage command into value 1 to output the value 1 as an operated value of the on-time ratio of fixing the at least one semiconductor switching element connected between the middle voltage point of the DC circuit and the one output terminal in the turned-on state, and carrying out an operation of dividing the value of the inputted minimum voltage command by the value of the DC low voltage to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between the low voltage point of the DC circuit and the one output terminal;
a by-phase on-time ratio operating means (40) configured for classifying by phase, in each of the sections, the operated values of the on-time ratios, which are classified by values, and outputting the operated values classified by phase as voltages with the values thereof corresponding to the on-time ratios; and
a carrier comparing means (50) configured for making, in each of the sections, the voltages, inputted by phase with the values thereof corresponding to the on-time ratios, compared with a carrier, which converts the compared voltage into an on-off command with an on-time ratio corresponding to the compared voltage, to produce on-off commands with the on-time ratios by phase and provide the on-off commands as those for a plurality of the semiconductor switching elements in each of the three three-level inverters.

4. A method for controlling a three-level inverter in a configuration in which three three-level inverters are connected in parallel to each other, the method comprising
the three three-level inverters carrying out turning-on and -off of a plurality of semiconductor switching elements, wherein

at least one semiconductor switching element is connected between a high voltage point of a DC circuit and one output terminal,
at least one semiconductor switching element is connected between a middle voltage point of the DC circuit and the output terminal, and
at least one semiconductor switching element is connected between a low voltage point of the DC circuit and the output terminal, and
enabling any one out of three voltage levels of a DC high voltage, DC middle voltage and DC low voltage as the base of an AC voltage for one phase to be outputted from the output terminal,
the method makes a plurality of the semiconductor switching elements in each of the three three-level inverters turned-on and -off on the basis of output voltage commands of three-phase AC voltages to thereby make the three-phase AC voltage outputted,
the method comprising the steps of:

carrying out operations for obtaining on-time ratios of a plurality of the semiconductor switching elements in each of the three three-level inverters on the basis of the output voltage commands of the three-phase AC voltages;
dividing the one period of the output voltage command of the three-phase AC voltage into a plurality of sections; and
in each of the sections,
making the three-level inverter for one phase fix one of the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal in a turned-on state to output one of the DC high voltage and the DC low voltage;
along with this, making the three-level inverter for one other phase alternately turn-on and -off one of the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the low voltage point and the output terminal with the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output one of the DC high voltage and the DC low voltage with the DC middle voltage; and
along with this, when making the three-level inverter for the remaining one phase output the DC high voltage, further making the three-level inverter for the remaining one phase alternately turn-on and -off the at least one semiconductor switching element connected between the low voltage point and the output terminal and the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC low voltage with the DC middle voltage; and
when making the three-level inverter for the one other phase output the DC low voltage, further making the three-level inverter for the remaining one phase alternately turn-on and -off the at least one semiconductor switching element connected between the high voltage point and the output terminal and the at least one semiconductor switching element connected between the middle voltage point and the output terminal with their respective operated on-time ratios in one switching period of the semiconductor switching element to alternately output the DC high voltage with the DC middle voltage.

5. The method for controlling a three-level inverter according to claim 4 comprising the steps of:

in each of the sections,
when the output voltage command has the positive polarity and the absolute value of the maximum value,
with respect to a phase with the output voltage command having the positive polarity and the absolute value of the maximum value,
making the value of the DC high voltage as the maximum value of the compensated voltage command, providing the value of the DC high voltage as the maximum voltage command in the phase in the section, carrying out an operation of dividing the maximum voltage command by the value of the DC high voltage and, on the basis of the result of the division, providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the low voltage point and the output terminal in the turned-on state in the three-level inverter in the phase;
with respect to a phase with the value of the output voltage command being a middle value,
carrying out compensation of adding the difference between the value of the DC high voltage and the maximum value of the output voltage command to the middle value of the voltage command, providing the value of the

compensated voltage command as the value of the middle voltage command in the phase in the section, carrying out an operation of dividing the value of the middle voltage command by the value of the DC high voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the inverter in the phase;

with respect to a phase with the value of the output voltage command being a minimum value,

carrying out compensation of adding the difference between the value of the DC high voltage and the maximum value of the output voltage command to the minimum value of the voltage command, providing the value of the compensated voltage command as the value of the minimum voltage command in the phase in the section, carrying out an operation of dividing the value of the minimum voltage command by the value of the DC high voltage and, on the basis of the result of the division and the polarity of the minimum voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the high voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal in the inverter in the phase;

when the output voltage command has the negative polarity and the absolute value of the maximum value,

with respect to a phase with the output voltage command having the negative polarity and the absolute value of the maximum value,

making the absolute value of the DC low voltage as the maximum value of the compensated voltage command, providing the absolute value of the DC low voltage as the maximum voltage command in the phase in the section, carrying out an operation of dividing the absolute value of the maximum voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division, providing 1 as the on-time ratio of fixing the at least one semiconductor switching element connected between the low voltage point and the output terminal in the turned-on state in the three-level inverter in the phase;

with respect to a phase with the value of the output voltage command being a middle value,

carrying out compensation of subtracting the difference between the absolute value of the DC low voltage and the maximum value of the output voltage command from the middle value of the voltage command, providing the value of the compensated voltage command as the value of the middle voltage command in the phase in the section, carrying out an operation of dividing the value of the middle voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the middle voltage point and the output terminal in the inverter in the phase; and

with respect to a phase with the value of the output voltage command being a minimum value,

carrying out compensation of subtracting the difference between the absolute value of the DC low voltage and the maximum value of the output voltage command to the minimum value of the voltage command, providing the value of the compensated voltage command as the value of the minimum voltage command in the phase in the section, carrying out an operation of dividing the value of the minimum voltage command by the absolute value of the DC low voltage and, on the basis of the result of the division and the polarity of the middle voltage command, providing the on-time ratio of one of the at least one semiconductor switching element connected between the high voltage point and the output terminal in the three-level inverter in the phase and the at least one semiconductor switching element connected between the low voltage point and the output terminal in the inverter in the phase and the on-time ratio of the at least one semiconductor switching element connected between the minimum voltage point and the output terminal.

6. A system for controlling a three-level inverter for carrying out the method according to claim 4 or 5 comprising:

an absolute maximum value command discriminating means (70) configured for detecting, in each of the sections, an output voltage command of a phase with an absolute value of the maximum value from the output voltage commands of the three-phase AC voltage and carrying out an operation for providing a compensation value for the output voltage commands on the basis of the maximum value and the polarity thereof;

a maximum, middle and minimum voltage command operating means (10) configured for classifying, in each

of the sections, the output voltage commands of the three-phase AC voltage by value into a voltage command of a phase with the value thereof being a maximum value, a voltage command of the phase with the value thereof being the middle value and a voltage command of a phase with the value thereof being a minimum value, carrying out the compensation of adding the compensation value when the polarity of the maximum value is positive and subtracting the compensation value when the polarity of the maximum value is negative, and outputting the compensated results as a maximum voltage command with the value thereof being one of the value of the DC high voltage and the absolute value of the DC low voltage, a middle voltage command and a minimum voltage command;

an on-time ratio operating means (30) configured for carrying out, in each of the sections, an operation of dividing the value of the inputted maximum voltage command by the value of one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to convert the value of the inputted maximum voltage command to 1 to output the result of the operation as an operated value of the on-time ratio of fixing the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point and the one output terminal in the turned-on state, carrying out an operation of dividing the value of the inputted middle voltage command by one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point of the DC circuit and the one output terminal, and carrying out an operation of dividing the value of the inputted minimum voltage command by one of the value of the DC high voltage and the absolute value of the DC low voltage on the basis of the polarity of the maximum value to output the result of the operation as an operated value of the on-time ratio of the at least one semiconductor switching element connected between one of the high voltage point and the low voltage point of the DC circuit and the one output terminal;

a by-phase on-time ratio operating means (40) configured for classifying by phase, in each of the sections, the operated values of the on-time ratios, which are classified by values, and outputting the operated values classified by phase as voltages with the values thereof corresponding to the on-time ratios; and

a carrier comparing means (50) configured for making, in each of the sections, the voltages, inputted by phase with the values thereof corresponding to the on-time ratios, compared with a carrier, which converts the compared voltage into an on-off command with an on-time ratio corresponding to the compared voltage, to produce on-off commands with the on-time ratios by phase and provide the on-off commands as those for a plurality of the semiconductor switching elements in each of the three three-level inverters.

7. The control method of a three-level inverter carried out as the method according to claim 1 or 2 when the amplitude of a three-phase output voltage command is equal to or less than a specified value and carried out as the method according to claim 4 or 5 when the amplitude of the three-phase output voltage command is equal to or more than the specified value.

8. The system for controlling a three-level inverter according to claim 3 or 6, wherein the carrier is a triangular wave.

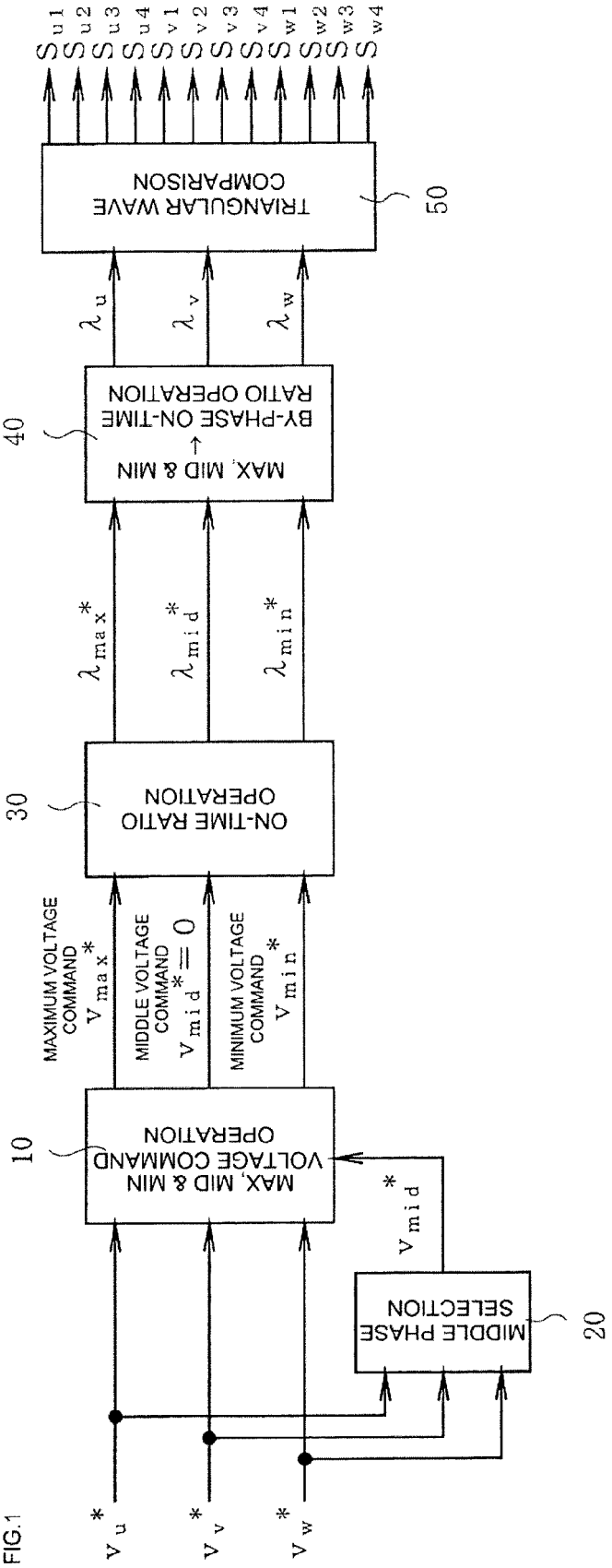

Su1 Su2 Su3 Su4 Sv1 Sv2 Sv3 Sv4 Sw1 Sw2 Sw3 Sw4
TRIANGULAR WAVE COMPARISON
50
λu λv λw
MAX, MID & MIN
BY-PHASE ON-TIME RATIO OPERATION
40
λmax* λmid* λmin*
ON-TIME RATIO OPERATION
30
MAXIMUM VOLTAGE COMMAND Vmax*
MIDDLE VOLTAGE COMMAND Vmid* = 0
MINIMUM VOLTAGE COMMAND Vmin*
MAX, MID & MIN VOLTAGE COMMAND OPERATION
10
Vmid*
MIDDLE PHASE SELECTION
20
Vu* Vv* Vw*

FIG.1

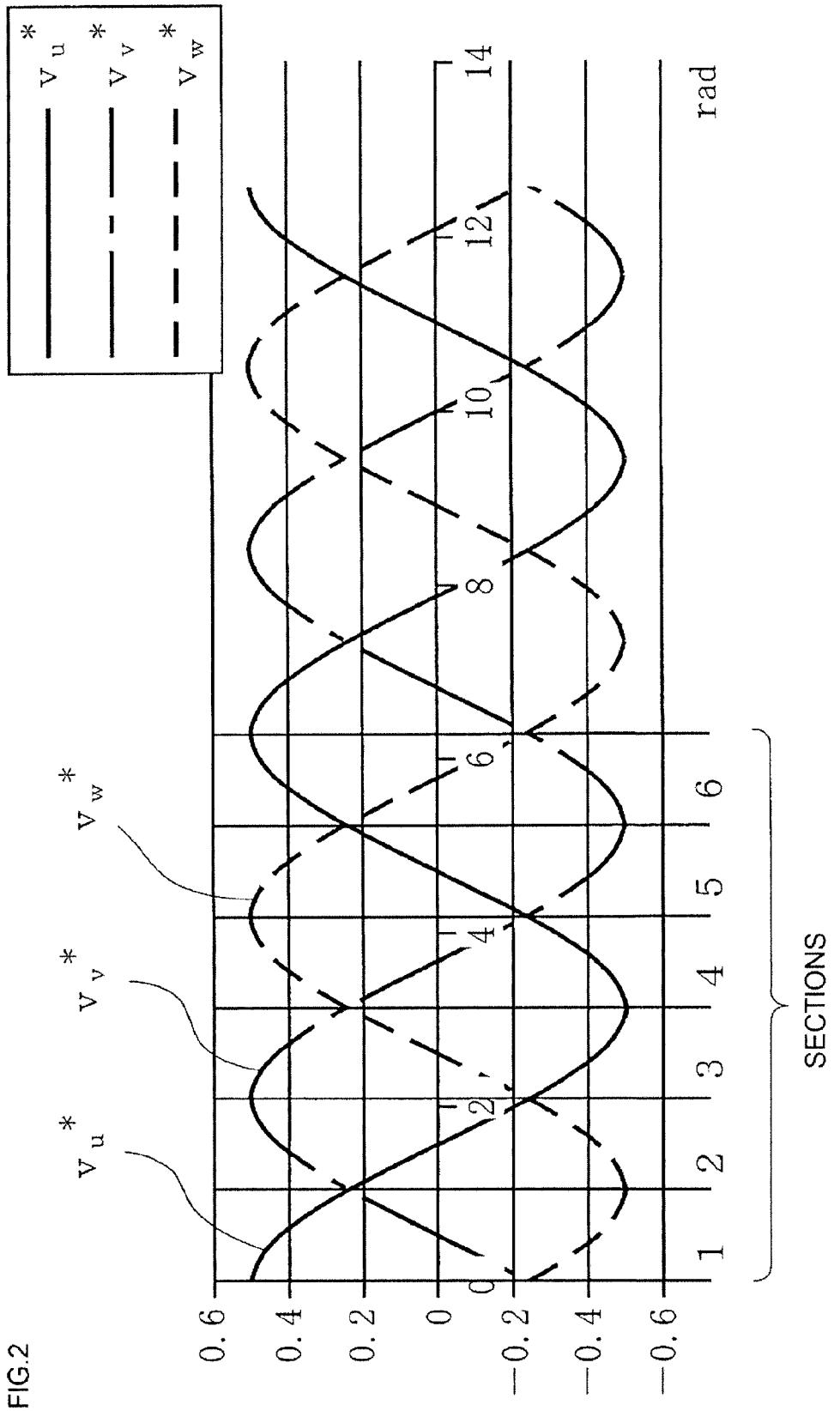


FIG.2

FIG.3

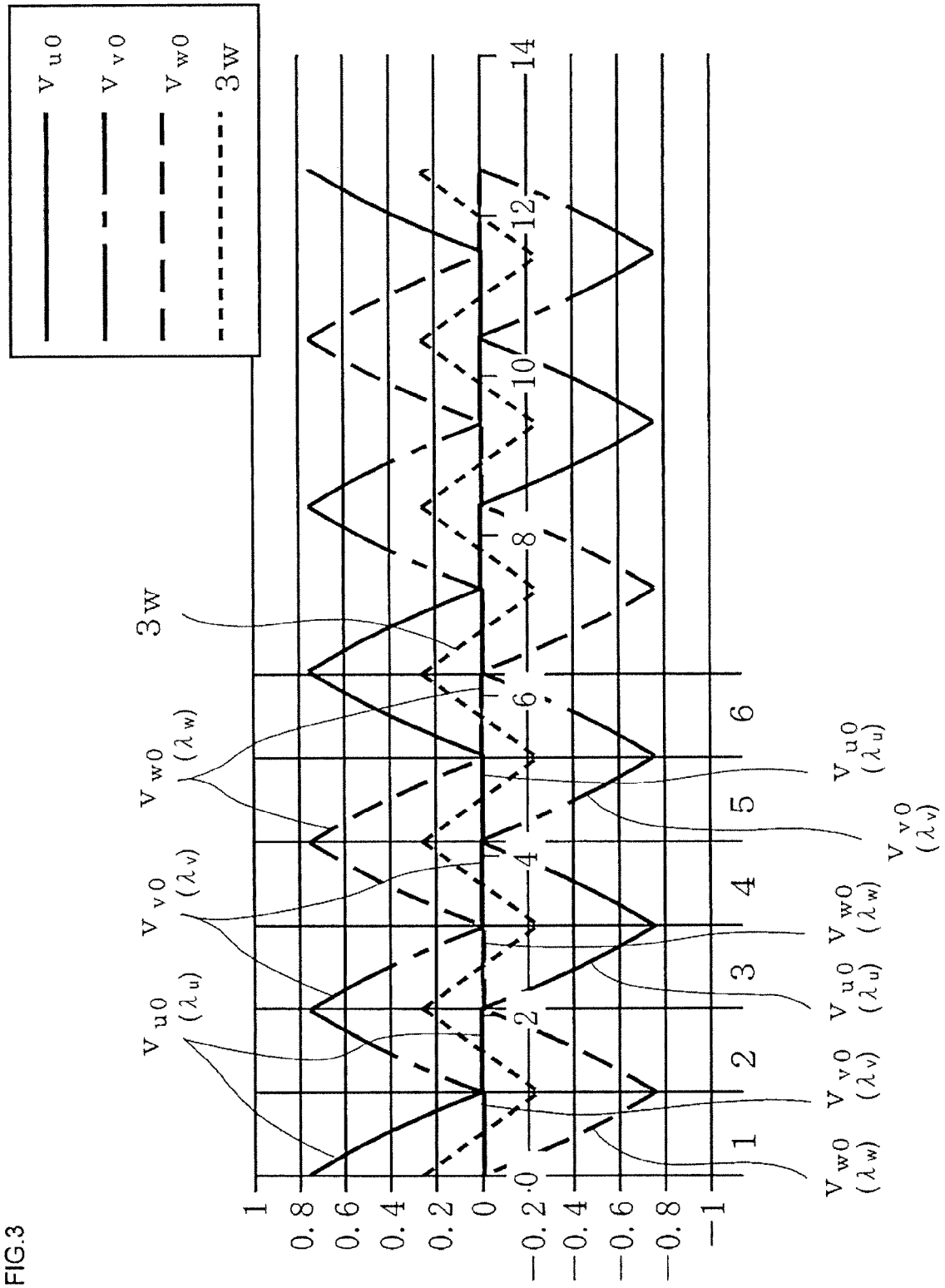

V_{u0}
V_{v0}
V_{w0}
3w
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
0
2
4
6
8
10
12
14
1
2
3
4
5
6
V_{u0} (λ_u)
V_{v0} (λ_v)
V_{w0} (λ_w)
3w
V_{w0} (λ_w)
V_{v0} (λ_v)
V_{u0} (λ_u)
V_{u0} (λ_u)
V_{v0} (λ_v)
V_{w0} (λ_w)
V_{v0} (λ_v)
V_{u0} (λ_u)
V_{w0} (λ_w)

FIG.4A

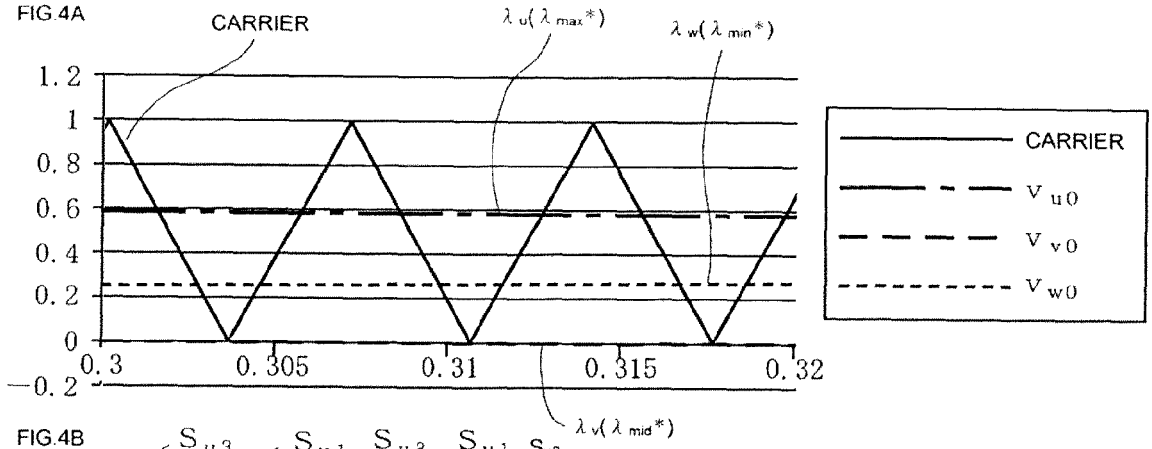


FIG.4B

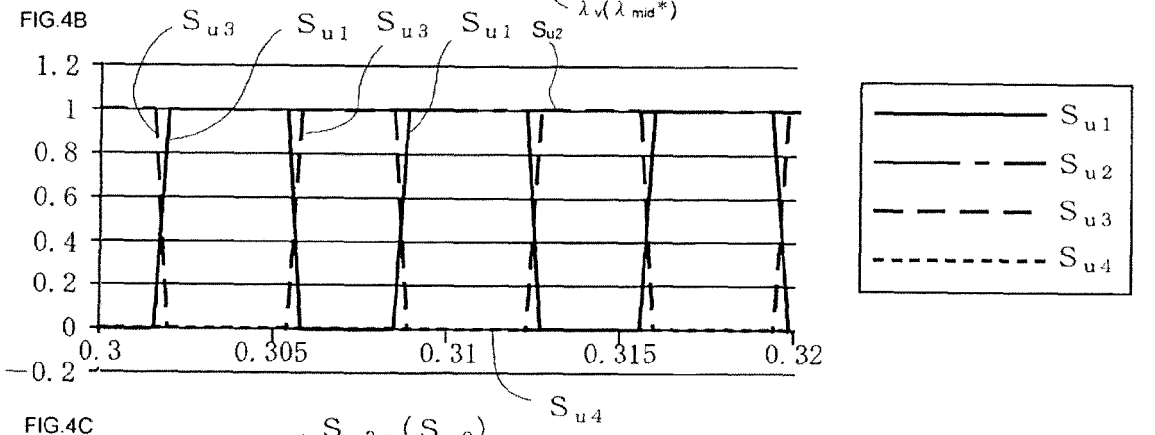


FIG.4C

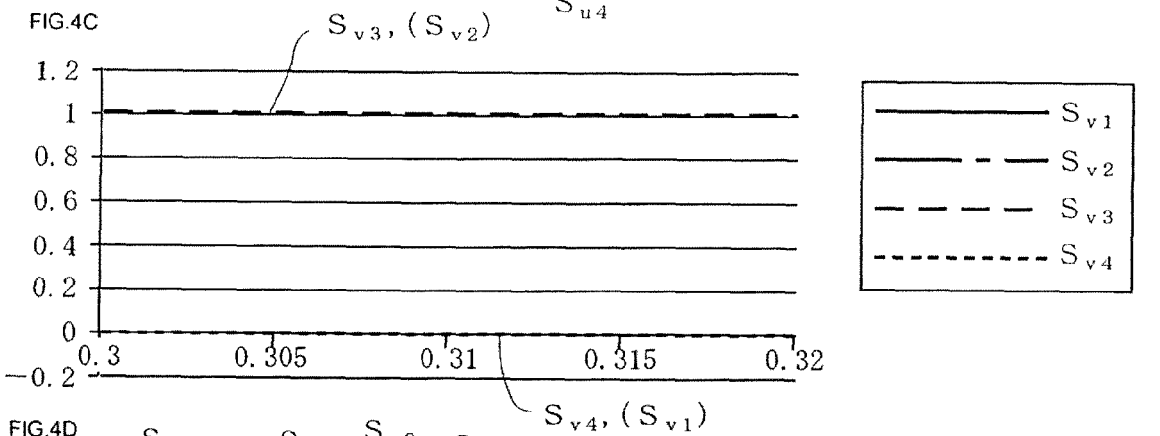
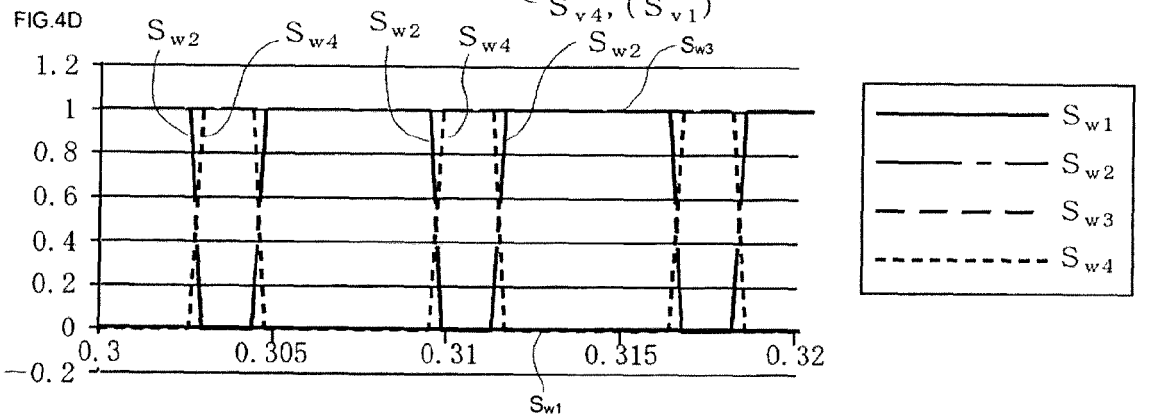


FIG.4D



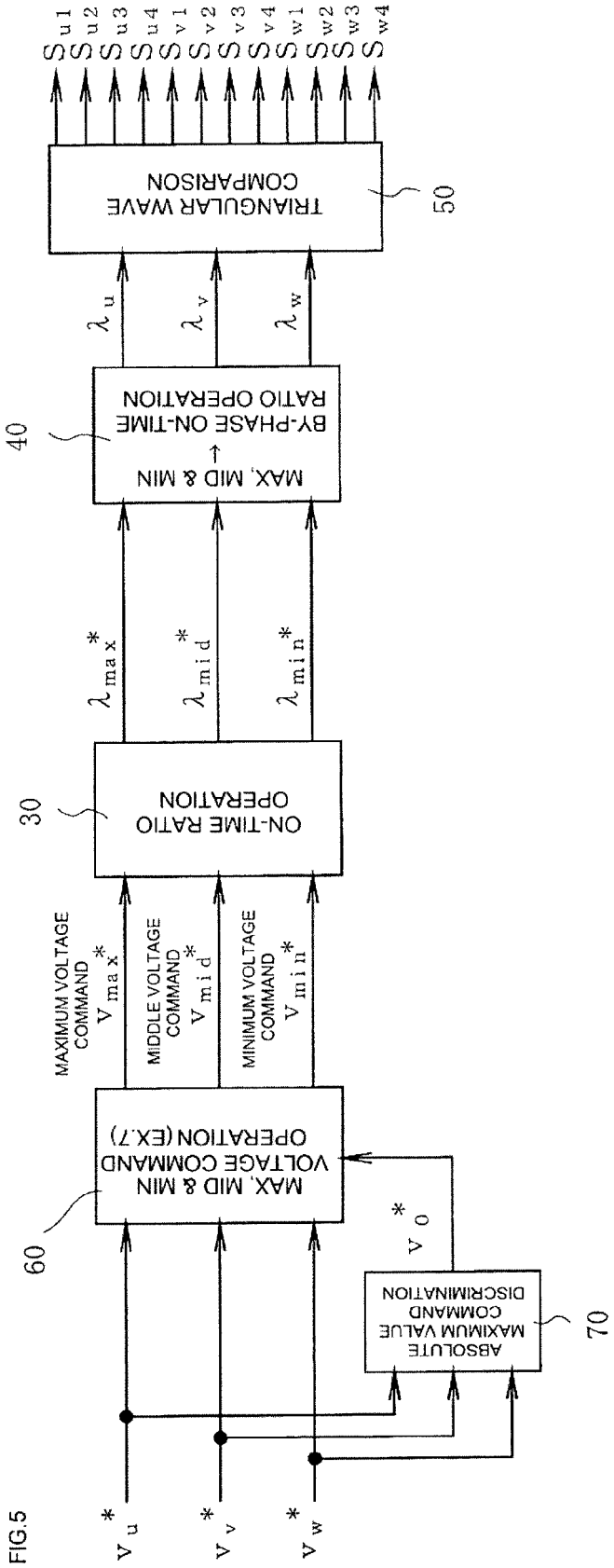

Su1 Su2 Su3 Su4 Sv1 Sv2 Sv3 Sv4 Sw1 Sw2 Sw3 Sw4
TRIANGULAR WAVE COMPARISON
50
λu λv λw
MAX, MID & MIN
↓
BY-PHASE ON-TIME RATIO OPERATION
40
λmax* λmid* λmin*
ON-TIME RATIO OPERATION
30
MAXIMUM VOLTAGE COMMAND Vmax*
MIDDLE VOLTAGE COMMAND Vmid*
MINIMUM VOLTAGE COMMAND Vmin*
MAX, MID & MIN VOLTAGE COMMAND OPERATION (EX.7)
60
V0*
ABSOLUTE MAXIMUM VALUE COMMAND DISCRIMINATION
70
Vu* Vv* Vw*

FIG.5

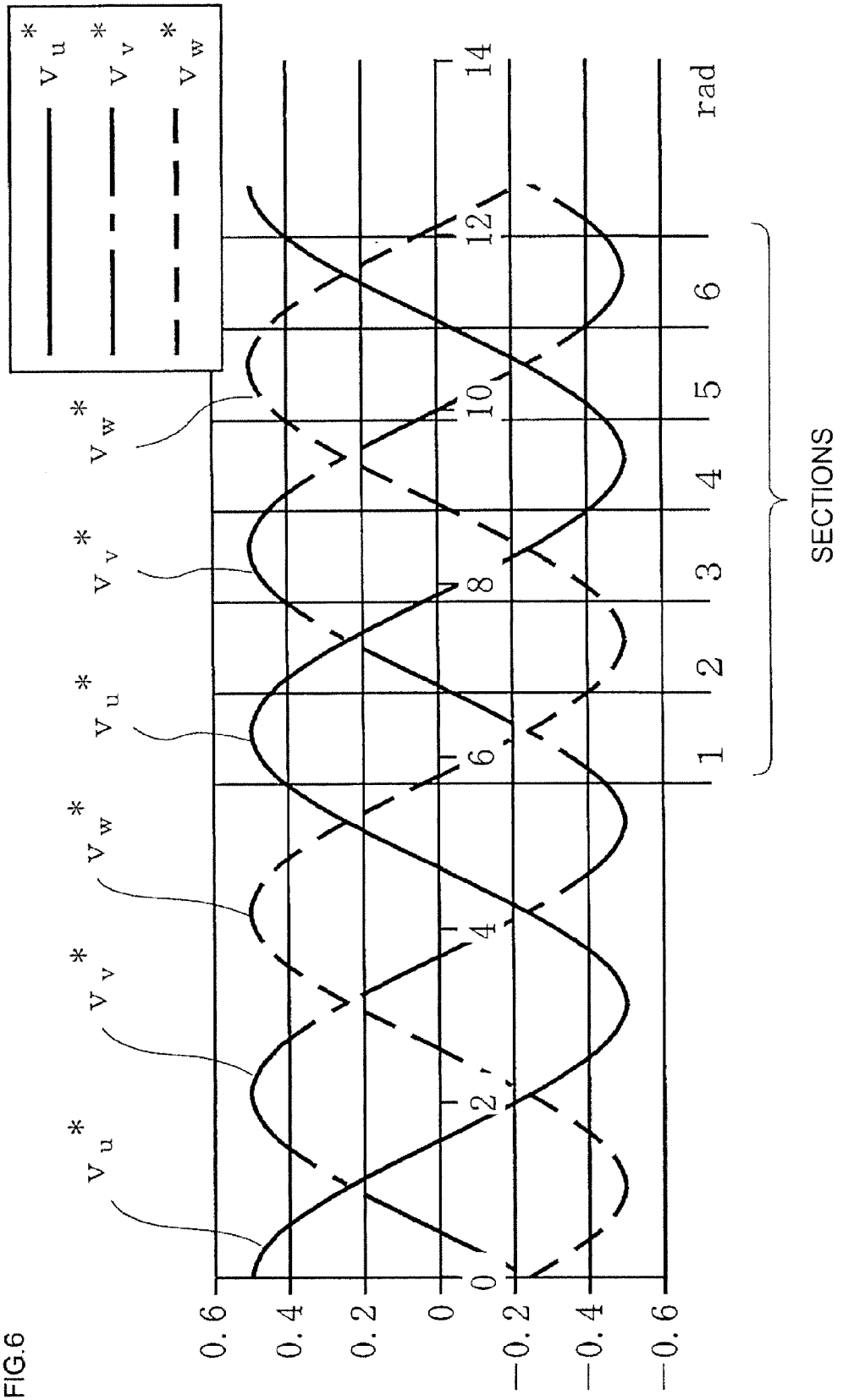


FIG.6

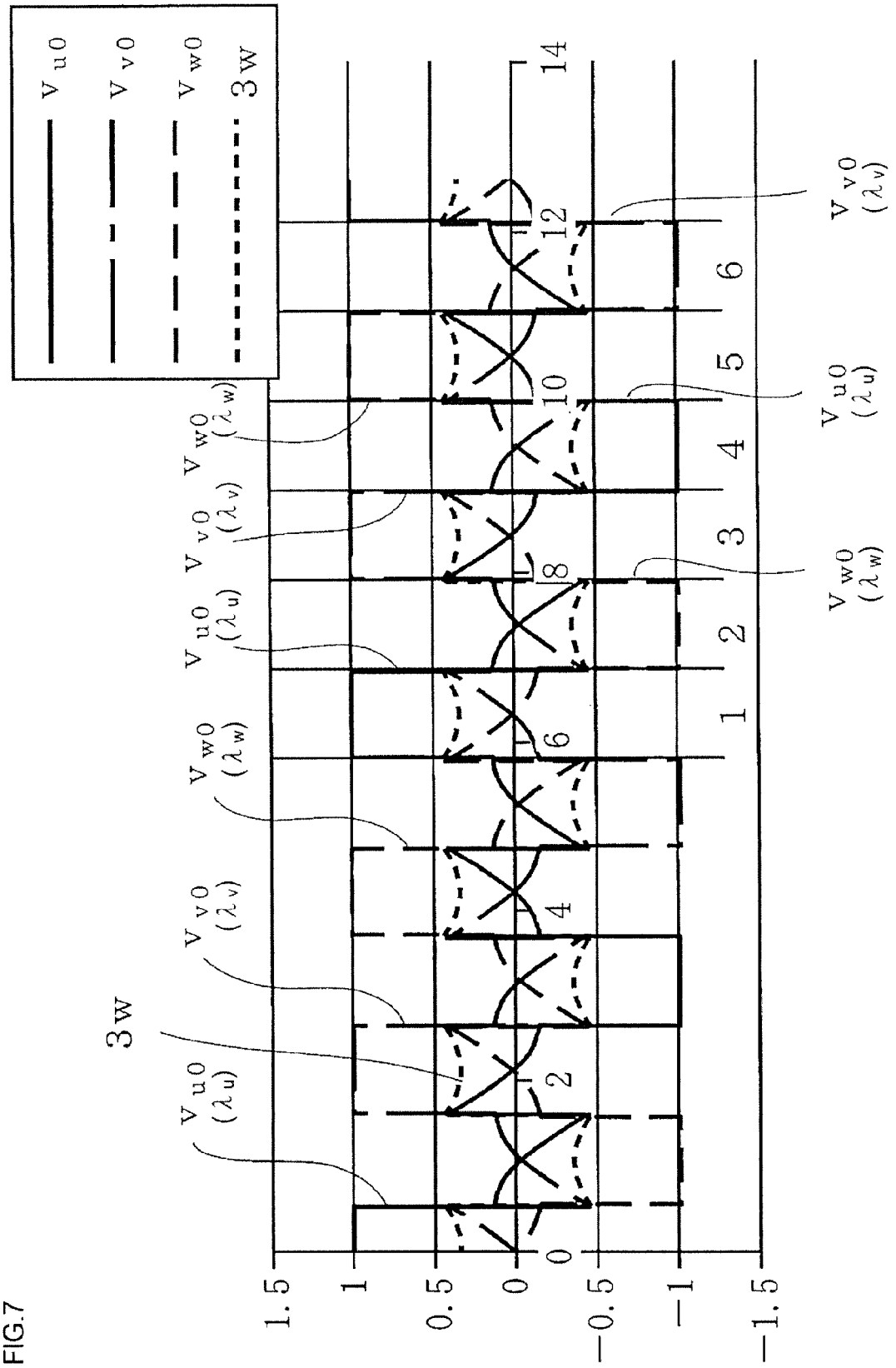

V u0
V v0
V w0
3W
1.5
1
0.5
0
−0.5
−1
−1.5
0
2
4
6
8
10
12
14
1
2
3
4
5
6
V u0 (λu)
V v0 (λv)
V w0 (λw)

FIG.7

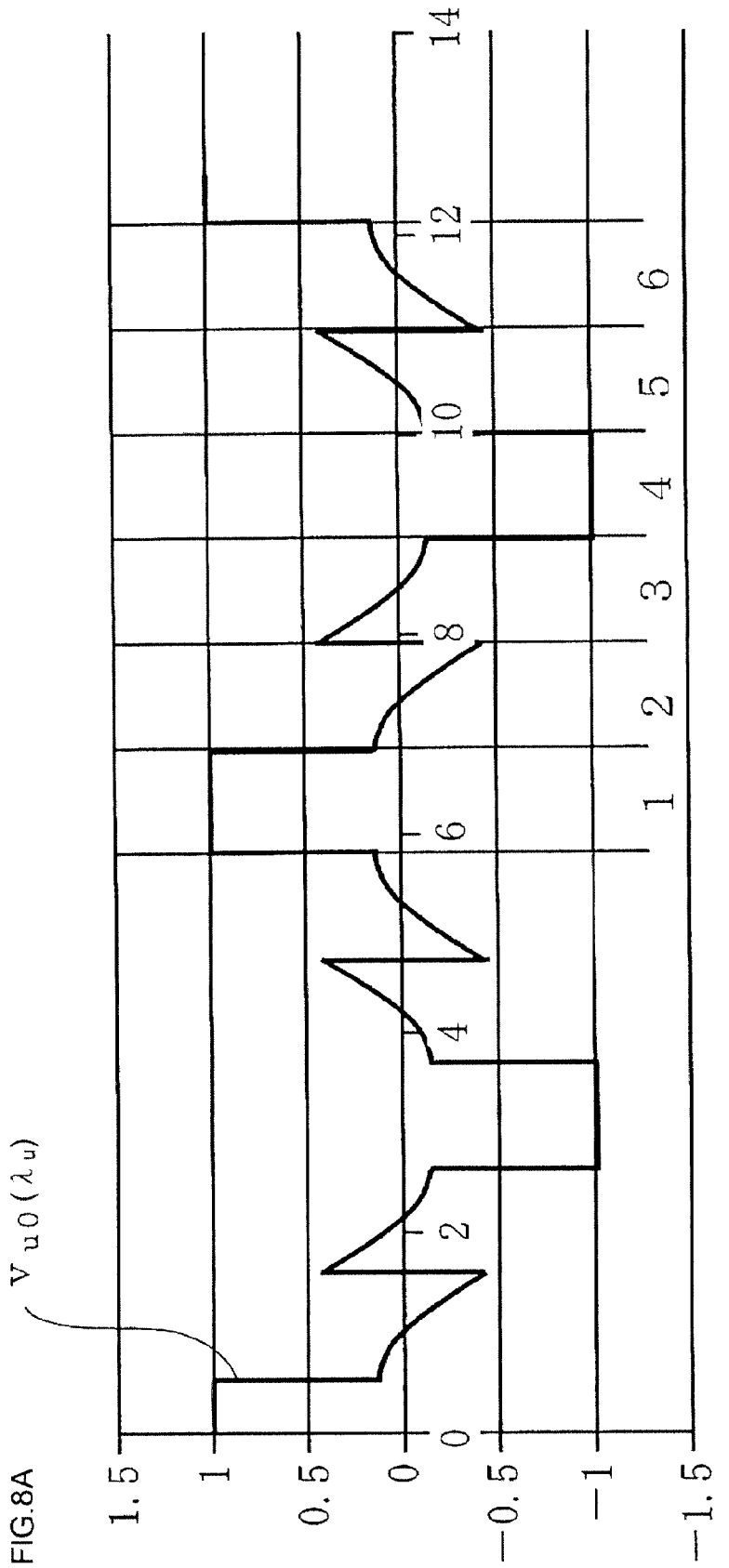


FIG.8A

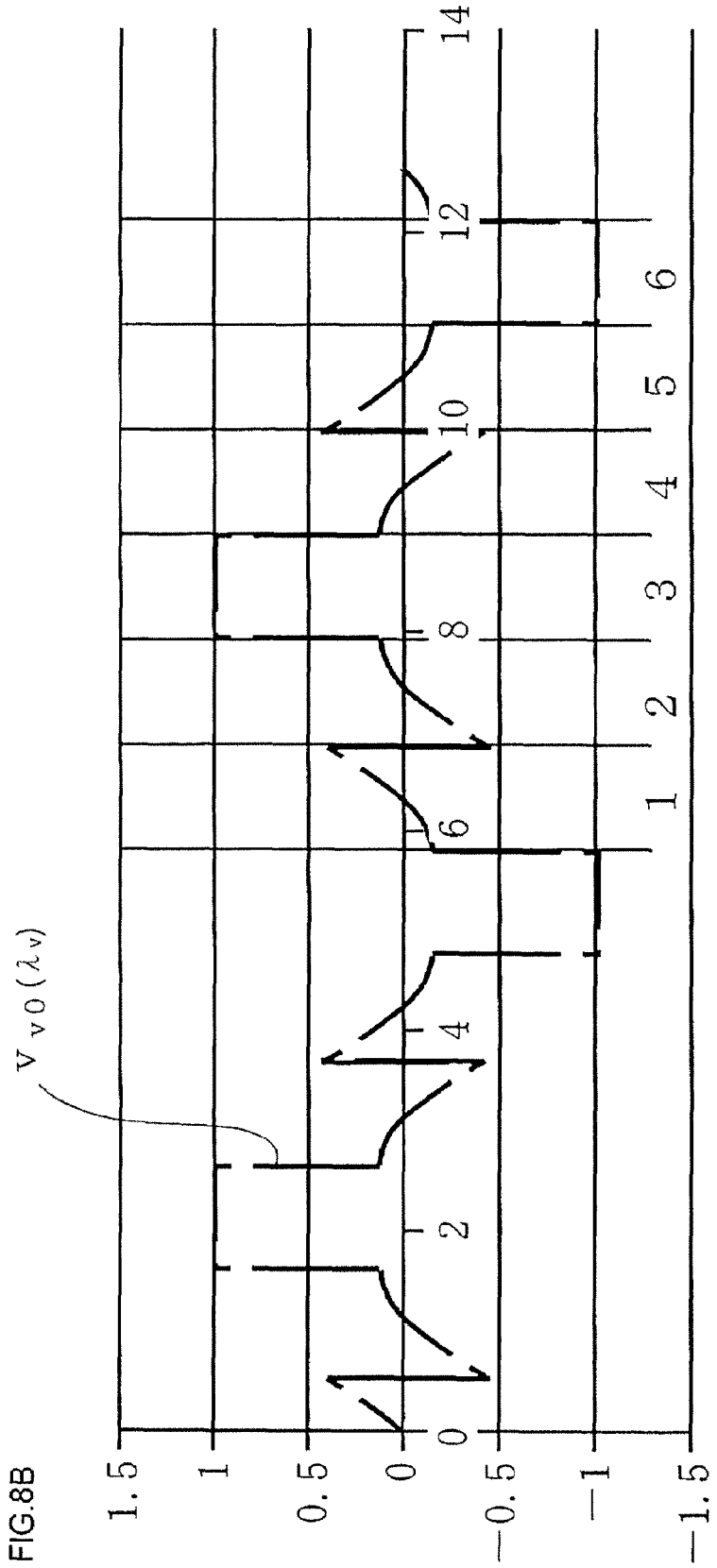


FIG.8B

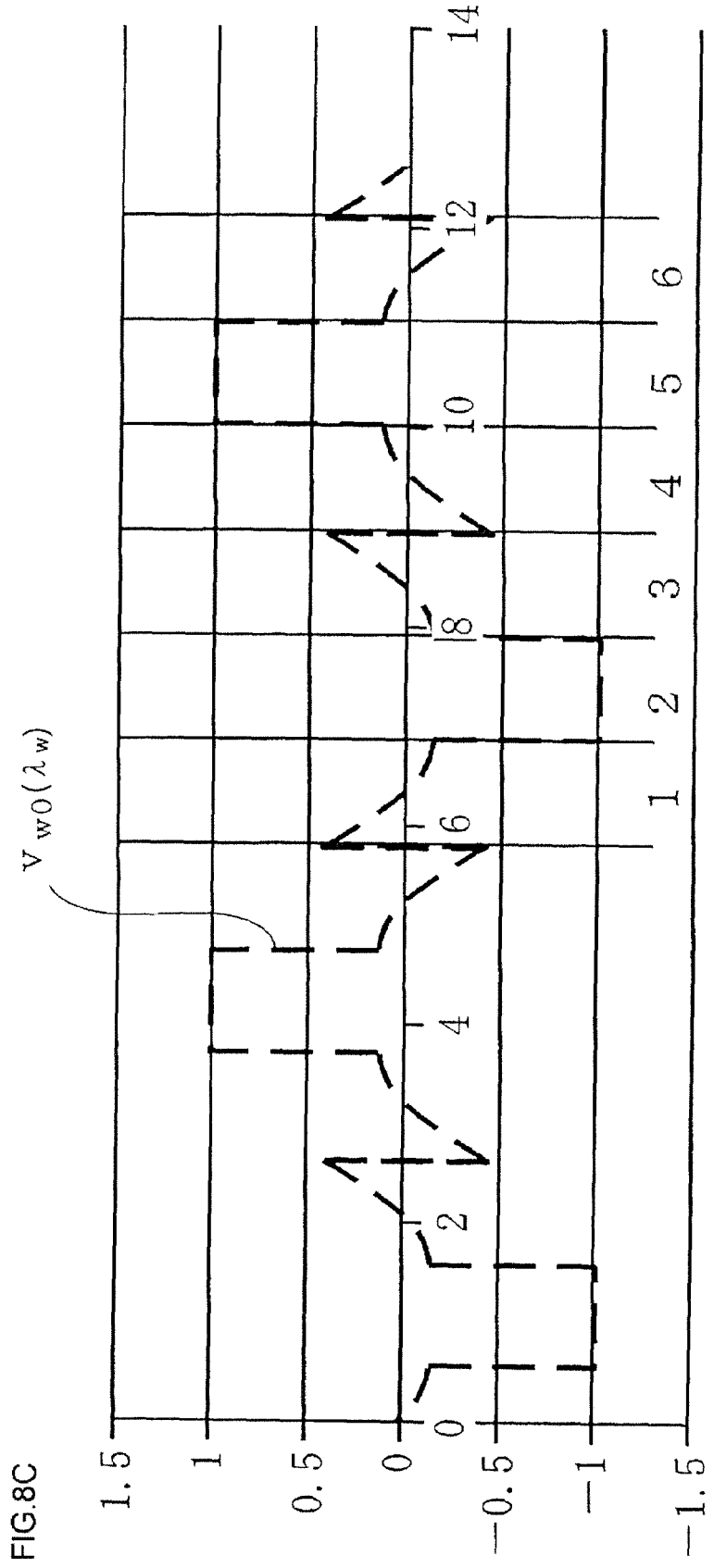


FIG.8C

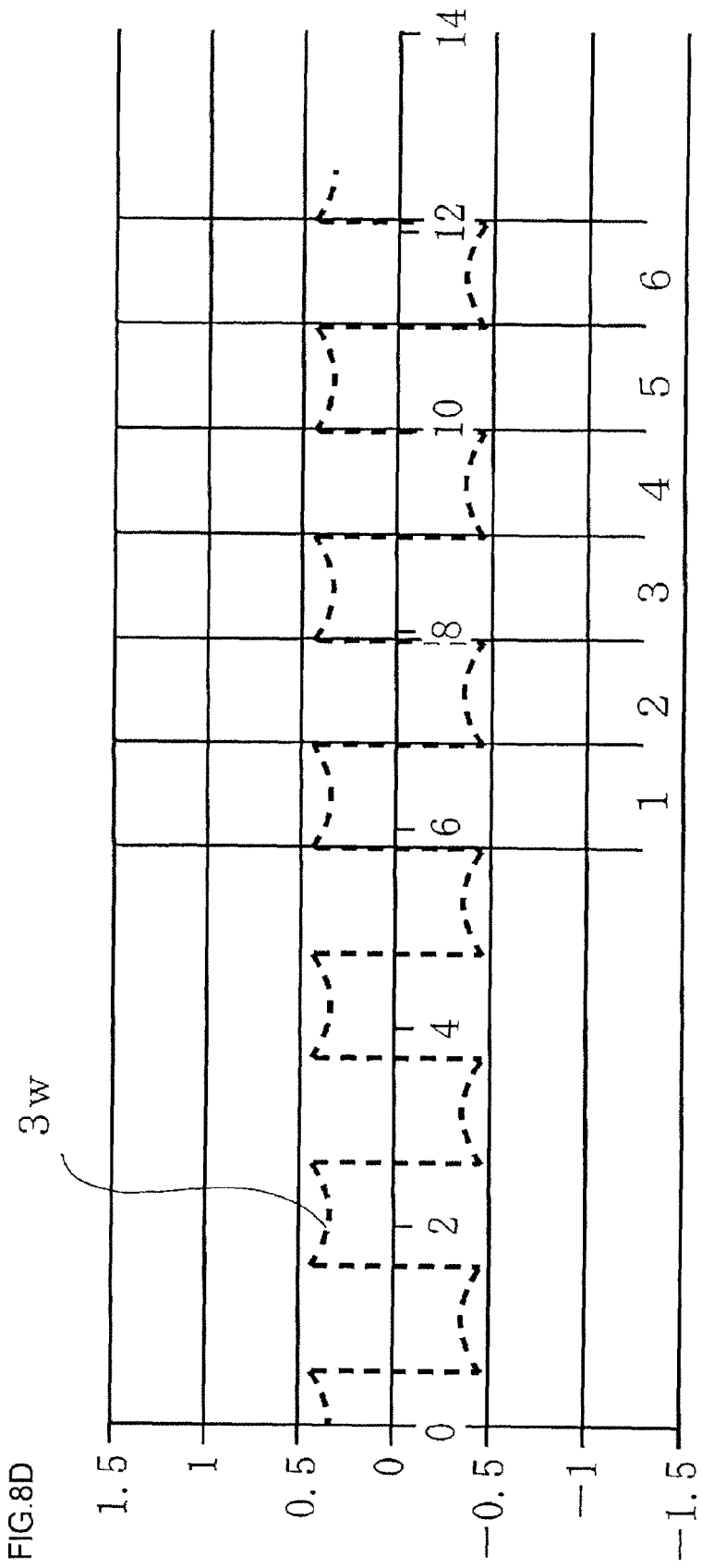


FIG.8D

FIG.9A

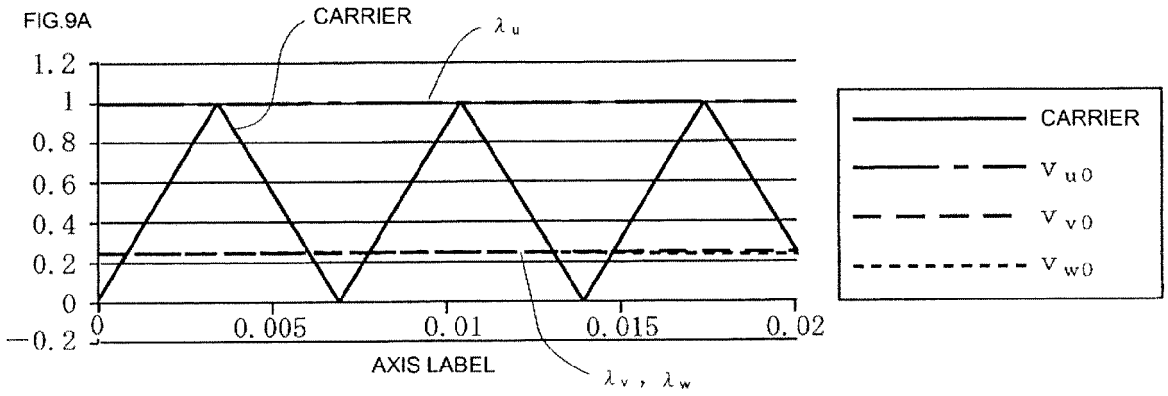


FIG.9B

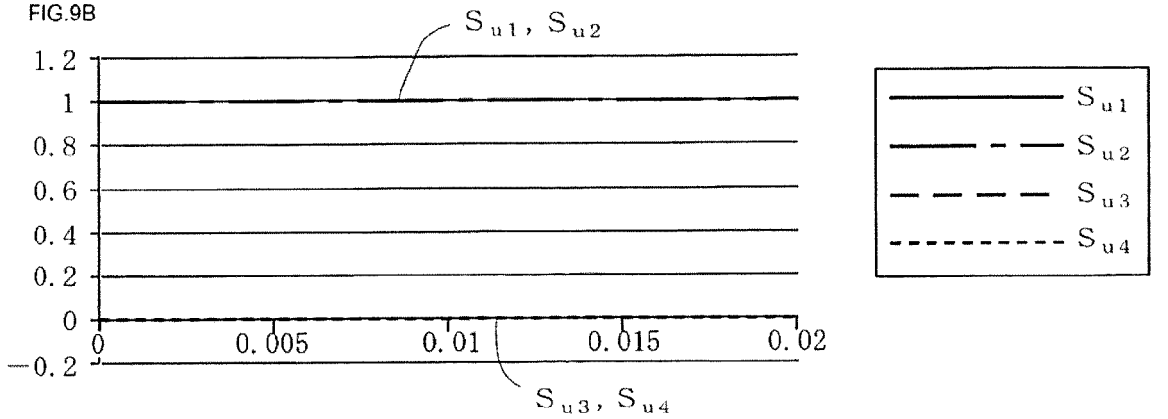


FIG.9C

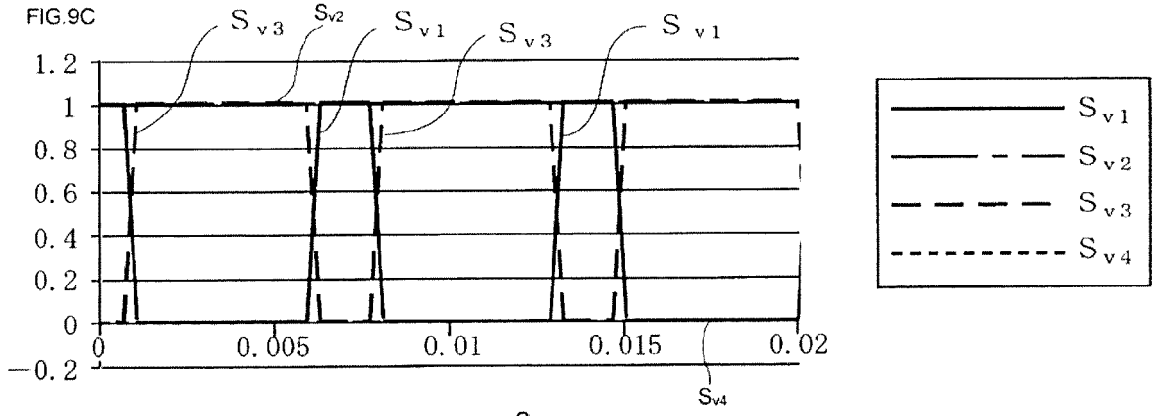
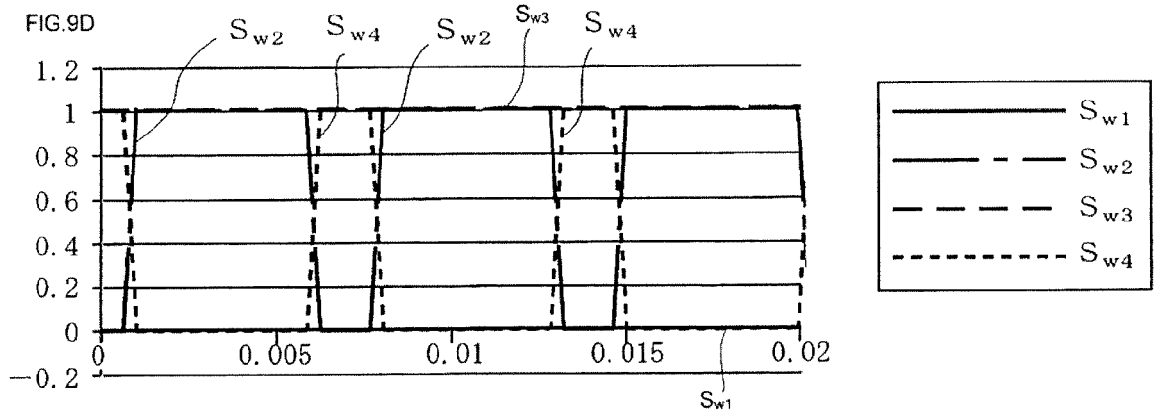


FIG.9D



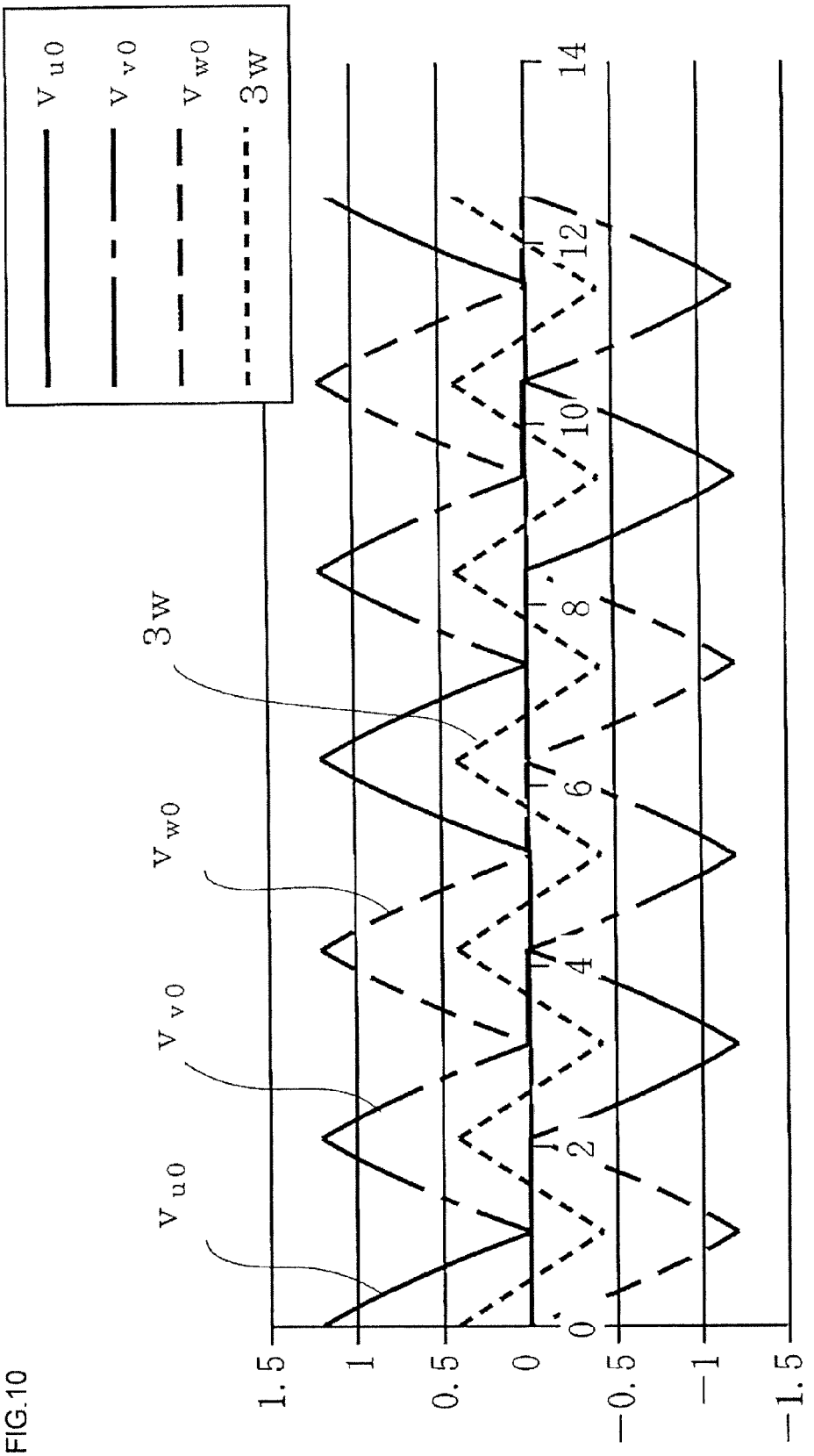


FIG.10

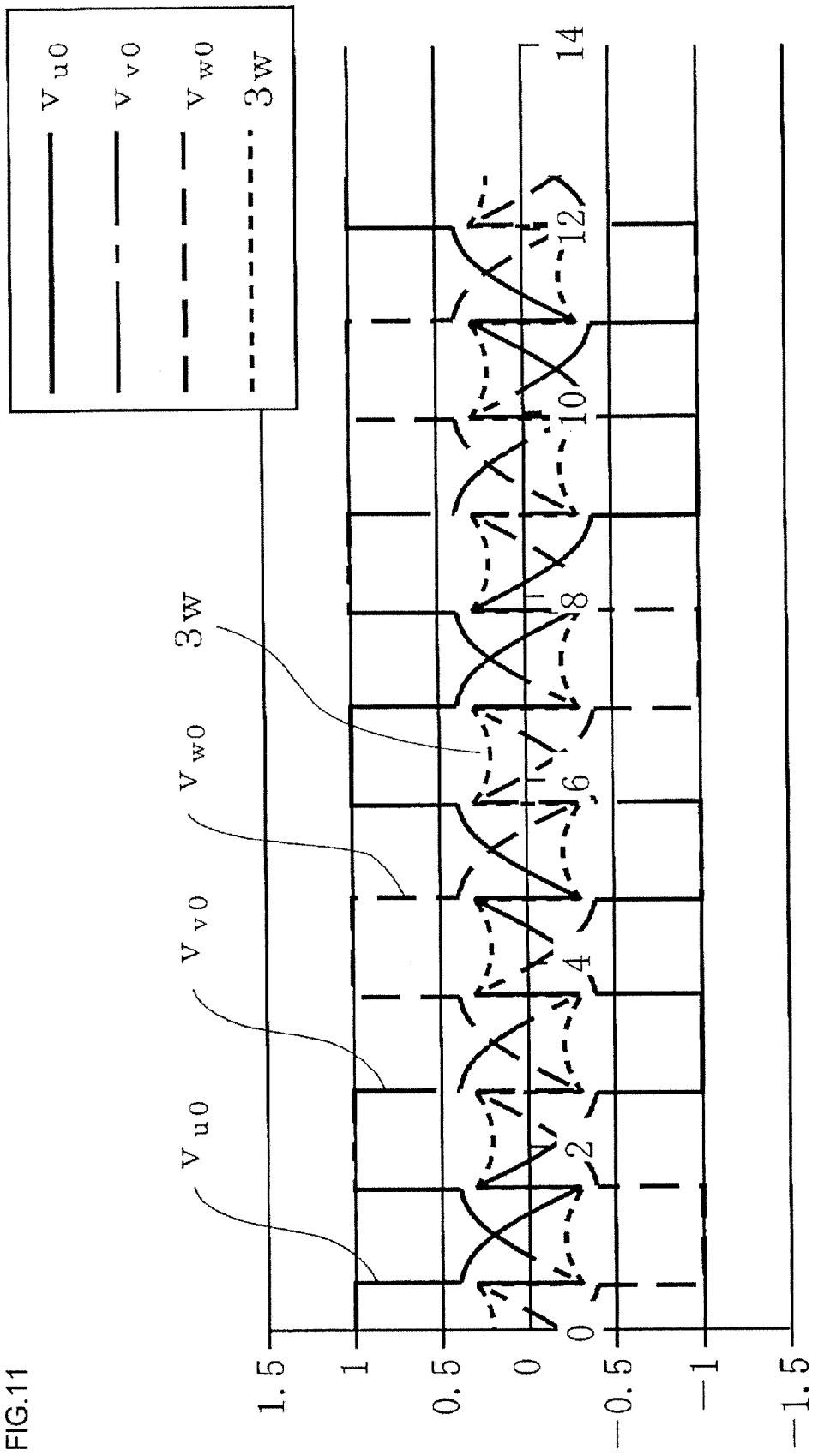


FIG.11

FIG.12

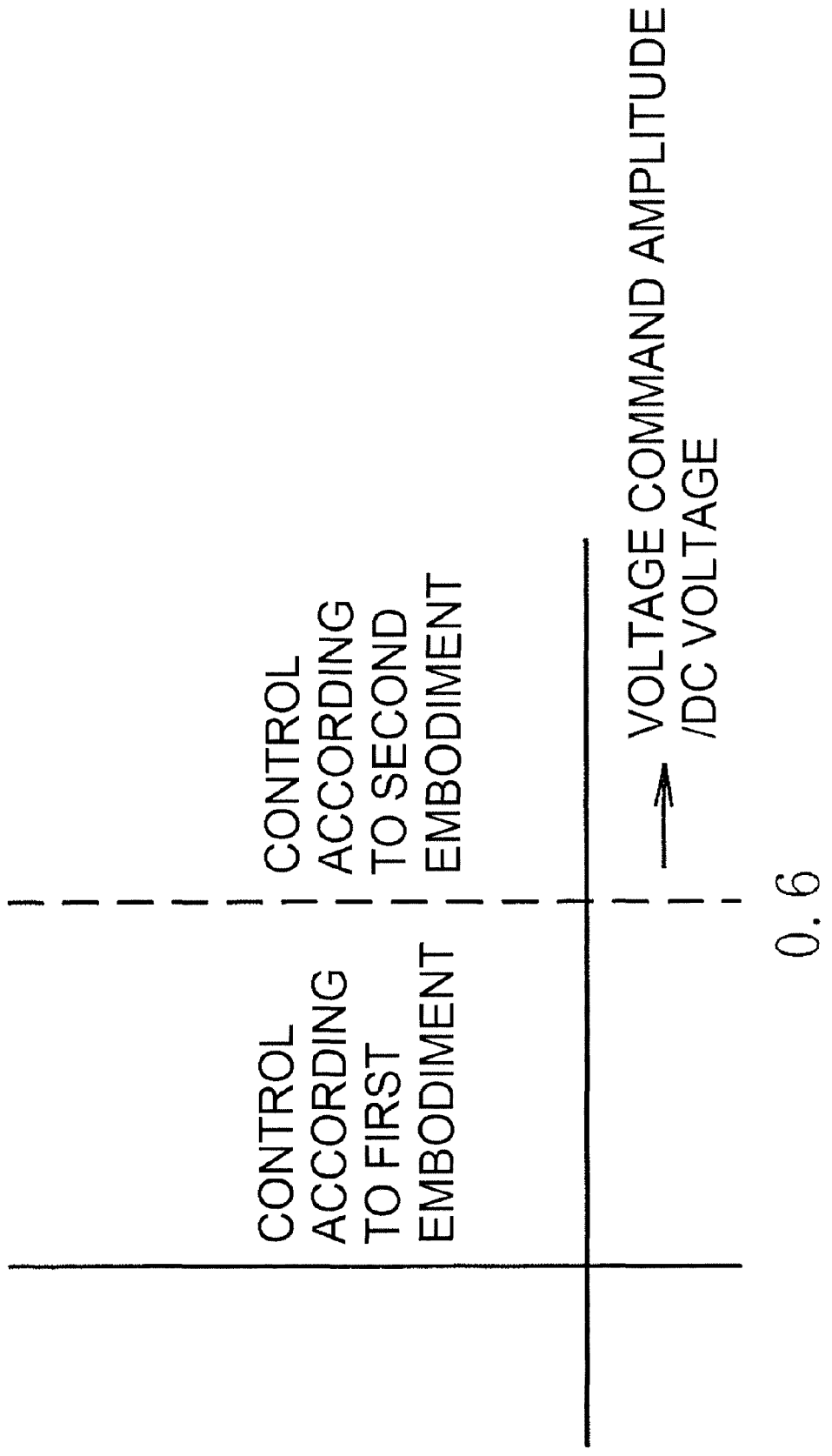

CONTROL ACCORDING TO FIRST EMBODIMENT
CONTROL ACCORDING TO SECOND EMBODIMENT
VOLTAGE COMMAND AMPLITUDE /DC VOLTAGE
0.6

FIG.13

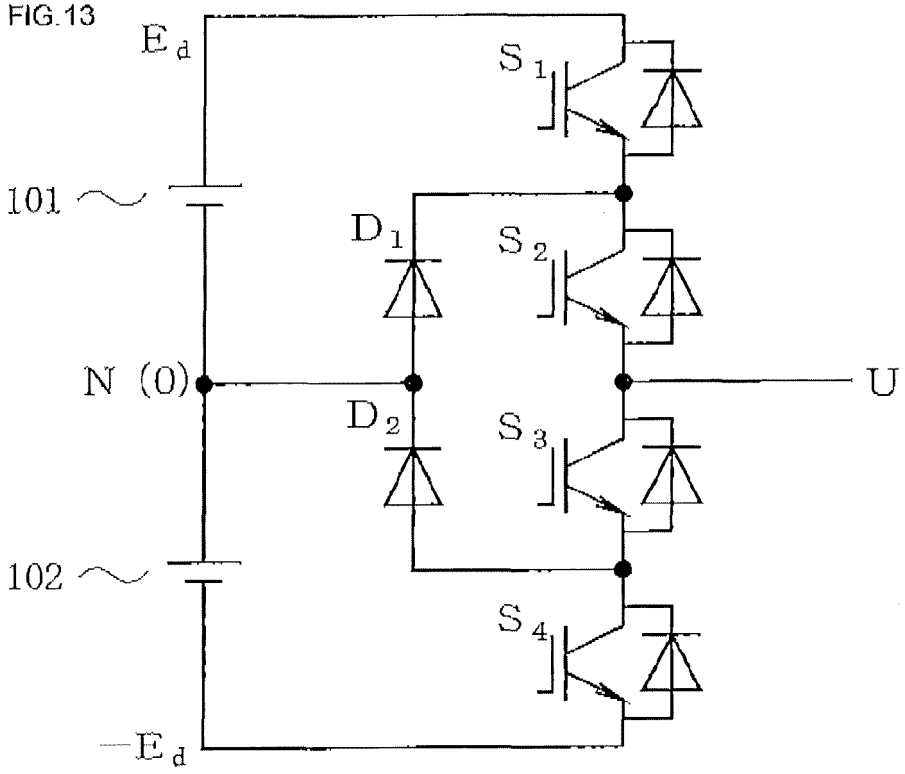
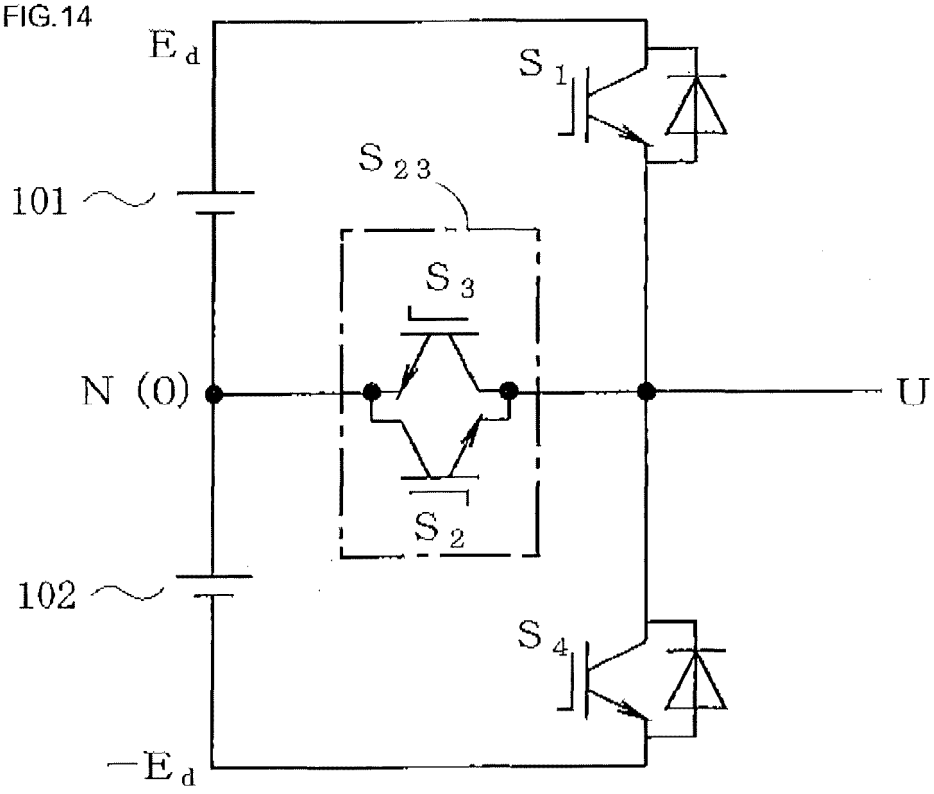


FIG.14



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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