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(54) **CURRENT ZERO-CROSS DETECTION DEVICE, SIGNAL ACQUISITION CIRCUIT, AND CIRCUIT SYSTEM**

NULLSTROMERKENNUNGSVORRICHTUNG, SIGNALERFASSUNGSSCHALTUNG UND SCHALTUNGSSYSTEM

DISPOSITIF DE DÉTECTION DE PASSAGE PAR ZÉRO DE COURANT, CIRCUIT D'ACQUISITION DE SIGNAL, ET SYSTÈME DE CIRCUIT

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(56) References cited:
CN-A- 1 855 658
CN-A- 101 707 441
CN-A- 101 707 441
CN-A- 101 728 964
CN-A- 102 520 232
CN-A- 102 545 582
CN-A- 102 647 099
US-A- 5 521 807
US-A1- 2003 080 723
US-A1- 2012 293 141

EP 2 995 963 B1

Description

Technical Field

[0001] The present invention relates to the field of power supply, and more particularly, to a current zero-cross detection device, a zero-cross current signal acquisition circuit and a totem pole bridgeless circuit system.

Background of the Related Art

[0002] Research on single-phase Power Factor Correction (PFC) technology is towards the trend of high efficiency and high power density, and the totem pole bridgeless PFC topology is proposed in responsive to this trend, as shown in FIG. 1. In the totem pole bridgeless boost converter circuit system, a first bridge arm unit, a second bridge arm unit, and a capacitor Co are connected in parallel, with one connected end connected to the ground; the first bridge arm unit has two working frequency switches S1 and S2 connected in series in the same direction; a second bridge arm unit has two switches S3 and S4 connected in series in the same direction; an AC power supply Vin and an inductor L are connected between the connection point of two diodes and the connection point of two switches.

[0003] In the abovementioned totem pole bridgeless PFC circuit system, due to constraints of the topology itself, the totem pole PFC cannot use the fast recovery diode characteristics to improve EMI (Electro Magnetic Interference) as the two-way switch bridgeless PFC does, meanwhile the hard switching characteristics of the CCM (Continuous Conduction Mode) mode cannot meet the growing demand for high efficiency in the industry, therefore the totem pole bridgeless PFC control policy described in this application is based on the TCM (triangular current mode) mode, according to the simple topology of the totem pole, the high power density and high efficiency requirements can be met simultaneously if it is to control to achieve zero voltage switching (ZVS) or valley switching (VS) feature in full input voltage and full load range in the TCM mode.

[0004] However, during the process of practicing and studying the abovementioned control policy, the applicants of the present application found that: in the relevant totem pole conversion circuit system, based on the above control idea, it needs to timely and accurately detect the inductor current zero-cross signal of the PFC to achieve the timing control of working frequency switches S1 and S2 and high frequency switches S3 and S4, so as to achieve the ZVS or VS control in the full input voltage and full load range in the TCM mode.

[0005] The document CN 101707441 A discloses a totem-pole bridgeless circuit system and a current sampling device, and is applied in the technical field of electricity supply. The circuit system comprises a switch control unit, a second bridge arm unit and two current sampling units added in the bridge unit, wherein the switching on/off of a first switching tube and a second switching tube in the second bridge arm unit are respectively controlled by the current sampled by the switch control unit through a first current sampling unit and a second current sampling unit.

[0006] The document US 2012/293141 A1 discloses a bridgeless PFC converter, comprising: input terminals configured to receive an input AC power supply; an output terminal configured to provide power supply; a high frequency bridge arm comprising a first switch and a third switch coupled between the output terminal and a ground node; a low frequency bridge arm comprising a second switch and a fourth switch coupled between the output terminal and the ground node; an inductor coupled between the input AC power supply and the high frequency bridge arm; and a control circuit configured to control the switching of switches in the high frequency bridge arm and the low frequency bridge arm.

[0007] The document US 2003/080723 A1 discloses that the control switch is referenced to the ground, and therefore floating drive for the series switch in the prior art is not necessary. The peak current signal is always available regardless of the status of the control switch. By separating the peak and average current signals, the converter can be better controlled and both peak current mode control and current sharing control can be optimized. Referencing the peak current and average current signals to the different grounds provides freedom to implement different control schemes.

Summary of the Invention

[0008] To resolve the technical problem that it is difficult to control the timing of a totem pole bridgeless circuit system, a current zero-cross detection device, a zero-cross current signal acquisition circuit and a totem pole bridgeless circuit system according to independent claims are provided. Further improvements and embodiments are provided in the dependent claims.

[0009] Also provided is a current zero-cross detection device which comprises a current transformer, a first sampling switch, a second sampling switch, a sampling resistor and a comparator, and the current transformer comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit to be detected;

two ends of the secondary winding are connected respectively to drain electrodes of the first sampling switch and the second sampling switch;

a source electrode of the first sampling switch is connected to a source electrode of the second sampling switch, and the source electrodes are connected to ground;

two ends of the sampling resistor are respectively connected to the drain electrode and source electrode of the second sampling switch;

a negative input end of the comparator is connected to the drain electrode of the second sampling switch, and a positive input end of the comparator is connected to a reference voltage; and

the first sampling switch and the second sampling switch are in an ON or OFF state.

[0010] Alternatively, the device further comprises a reset resistor, and two ends of the reset resistor are respectively connected to the two ends of the secondary winding.

[0011] Alternatively, the sampling switch is a metal-oxide-semiconductor field effect transistor (Mosfet), an insulated gate bipolar transistor (IGBT), or a bipolar transistor (BJT).

[0012] Also provided is a current zero-cross signal acquisition circuit, wherein, the circuit comprises:

a first current zero-cross detection unit, located in a first circuit branch, and configured to collect a current flowing through the first circuit branch when an alternate current (AC) input voltage is in a positive half cycle, to acquire a current zero-cross signal of the first circuit branch;

a second current zero-cross detection unit, located in a second circuit branch and configured to collect a current flowing through the second circuit branch when the AC input voltage is in a negative half cycle to acquire a current zero-cross signal of the second circuit branch; and

a signal processing circuit, configured to select the current zero-cross signal collected by the first current zero-cross detection unit when the AC input voltage is in the positive half cycle; and select the current zero-cross signal collected by the second current zero-cross detection unit when the AC input voltage is in the negative half cycle,

wherein the first current zero-cross detection unit and the second current zero-cross detection unit have an identical structure, comprising a current transformer, a first sampling switch, a second sampling switch, a sampling resistor and a comparator, and the current transformer comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit to be detected;

two ends of the secondary winding are respectively connected to drain electrodes of the first sampling switch and the second sampling switch;

a source electrode of the first sampling switch is connected to a source electrode of the second sampling switch, and the source electrodes are connected to ground;

two ends of the sampling resistor are respectively connected to the drain electrode and the source electrode of the second sampling switch; and

a negative input end of the comparator is connected to the drain electrode of the second sampling switch, and a positive input end of the comparator is connected to a reference voltage.

[0013] Alternatively, the signal processing circuit comprises: a first AND gate, a second AND gate and an OR gate, an input end of the first AND gate is connected to an output end of the first current zero-cross detection unit and a first working frequency signal representing polarity of the AC input voltage; an input end of the second AND gate is connected to an output end of the second current zero-cross detection unit and a second working frequency signal representing polarity of the AC input voltage; an input end of the OR gate is connected to output ends of the first AND gate and the second AND gate.

[0014] Alternatively, the first current zero-cross detection unit and the second current zero-cross detection unit further comprise reset resistors, and two ends of the reset resistor are respectively connected to the two ends of the secondary winding.

[0015] Also provided is a totem pole bridgeless circuit system, wherein the system comprises: a first bridge arm unit and a second bridge arm unit, wherein the first bridge arm unit and the second bridge arm unit are connected in parallel between a first parallel connection point and a second parallel connection point, the first bridge arm unit comprises a first switch and a second switch connected in series in the same direction; the second bridge arm unit comprises a third switch and a fourth switch connected in series in the same direction; a power supply and an inductor are connected between a first connection point between the first switch and the second switch and a second connection point between the third switch and the fourth switch, and the second bridge arm unit further comprises:

a first current zero-cross detection unit, a second current zero-cross detection unit and a signal processing circuit, wherein the first current zero-cross detection unit and the third switch are connected in series between the first parallel connection point and the second connection point; the second current zero-cross detection unit and the fourth switch are connected in series between the second

parallel connection point and the second connection point; the signal processing circuit is connected to the first current zero-cross detection unit and the second current zero-cross detection unit;

the first current zero-cross detection unit is configured to, when an AC input voltage is in a positive half cycle and a body diode of the third switch is conducted, collect a current flowing through the third switch, and obtain a current zero-cross signal of the current flowing through the third switch;

the second current zero-cross detection unit is configured to, when the AC input voltage is in a negative half cycle and a body diode of the fourth switch is conducted, collect a current flowing through the fourth switch and obtain a current zero-cross signal of the current flowing through the fourth switch;

the signal processing circuit is configured to select the current zero-cross signal collected by the first current zero-cross detection unit when the AC input voltage is in the positive half axle; select the current zero-cross signal collected by the second current zero-cross detection unit when the AC input voltage is in the negative half cycle; and

a switching control unit, connected to the signal processing circuit as well as the third switch and the fourth switch, and is configured to control ON or OFF of the third switch and the fourth switch according to a signal output by the signal processing circuit,

wherein structures of the first current zero-cross detection unit and the second current zero-cross detection unit respectively comprise a current transformer, a first sampling switch, a second sampling switch, a sampling resistor and a comparator, and the current transformer comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit to be detected;

two ends of the secondary winding are respectively connected to drain electrodes of the first sampling switch and the second sampling switch;

a source electrode of the first sampling switch is connected to a source electrode of the second sampling switch, and the source electrodes are connected to ground;

two ends of the sampling resistor are respectively connected to the drain electrode and the source electrode of the second sampling switch; and

a negative input end of the comparator is connected to the drain electrode of the second sampling switch, and a positive input end thereof is connected to a reference voltage.

[0016] Alternatively, the signal processing circuit comprises: a first AND gate, a second AND gate and an OR gate, an input end of the first AND gate is connected to an output end of the first current zero-cross detection unit and a first working frequency signal representing polarity of the AC input voltage and output by the switching control unit; an input end of the second AND gate is connected to an output end of the second current zero-cross detection unit and a second working frequency signal representing polarity of the AC input voltage and output by the switching control unit; an input end of the OR gate is connected to output ends of the first AND gate and the second AND gate.

[0017] Alternatively, the first current zero-cross detection unit and the second current zero-cross detection unit further comprise reset resistors, and two ends of the reset resistor are respectively connected to the two ends of the secondary winding.

[0018] The current zero-cross detection device, current zero-cross signal acquisition circuit and totem pole bridgeless circuit system in accordance with the embodiment of the present invention control the ON and OFF state of a switch by collecting the current zero-cross signal to achieve the ZVS or VS control in the full input voltage and full load range under the TCM mode, and to improve the efficiency of the totem pole bridgeless PFC system.

Brief Description of Drawings

[0019]

FIG. 1 is a schematic diagram of the structure of a totem pole bridgeless PFC system in the related art;

FIG. 2 is a schematic diagram of the structure of a totem pole bridgeless PFC system provided in an embodiment of the present invention;

FIG. 3 is a circuit diagram of a current zero-cross detection system of the totem pole bridgeless PFC system provided in an embodiment of the present invention;

FIG. 4 is a circuit diagram of a current zero-cross detection unit in the totem pole bridgeless PFC system working in an AC positive half cycle provided in an embodiment of the present invention;

FIG. 5 is a circuit diagram of the current zero-cross detection unit in the totem pole bridgeless PFC system provided working in the AC negative half axle in the embodiment of the present invention;

FIG. 6 is a working waveform diagram of the current zero-cross detection unit in the totem pole bridgeless PFC system provided in an embodiment of the present invention;

FIG. 7 is a working waveform diagram of a signal processing circuit in the totem pole bridgeless PFC system provided in an embodiment of the present invention.

Preferred Embodiments of the Invention

[0020] Hereinafter in conjunction with the accompanying drawings in the embodiments of the present invention, the technical scheme in the embodiments of the present invention will be described clearly and completely. Based on the embodiments of the present invention, all other embodiments obtained by those with ordinary skill in the art without creative efforts should be within the protection scope of the present invention. It should be noted that, in the case of no conflict, embodiments and features in the embodiments in the present application may be arbitrarily combined with each other.

[0021] The schematic diagram of the structure of the totem Pole bridgeless PFC circuit system according to the embodiment of the present invention is shown in FIG. 2, comprising:

the first bridge arm unit 10 and the second bridge arm unit 20 connected in parallel between the first parallel connection point 1 and the second parallel connection point 2, wherein the first bridge arm unit 10 comprises the first switch 110 and the second switch 120 connected in series in the same direction; the second bridge arm unit 20 comprises the third switch 211 and the fourth switch 220 connected in series in the same direction; the power supply Vin and the inductor L are connected between the first connection point 4 between the first switch 110 and the second switch 120 and the second connection point 3 between the third switch 211 and the fourth switch 220, and the second bridge arm unit 20 further comprises:

the first and second current zero cross detection units 210 and 221 and the signal processing circuit 230, wherein the first current zero-cross detection unit 210 and the third switch 211 in the two switches are connected in series between the first parallel connection point 1 and the second connection point 3; the second current zero-cross detection unit 221 and the fourth switch 220 in the two switches are connected in series between the second parallel connection point 2 and the second connection point 3; the signal processing circuit 230 is connected to the first current zero-cross detection unit 210 and the second current zero-cross detection unit 221;

the first current zero-cross detection unit 210 is configured to collect the current flowing through the body diode of the third switch 211 and obtain its current zero cross signal when the AC input voltage is in the positive half cycle and the body diode of the third switch 211 is conducted, and release the energy collected by the first current zero-cross detection unit 210 when the body diode of the third switch 211 is cut off;

the second current zero-cross detection unit is configured to collect the current flowing through the body diode of the fourth switch 220 and obtain its current zero-cross signal when the AC input voltage is in the negative half cycle and the body diode of the fourth switch 220 is conducted; release the energy collected by the second current zero-cross detection unit 221 when the fourth switch 220 is switched off;

the signal processing circuit 230 is configured to select the current zero-cross signal collected by the first current zero-cross detection unit 210 when the AC input voltage is in the positive half axis; select the current zero-cross signal collected by the second current zero-cross detection unit 220 when the AC input voltage is in the negative half cycle; and

a switching control unit 30, connected to the first switch 120 and the second switch 110, and is configured to provide two working frequency signals which represent the AC input voltage polarities and are complementary, to control the ON or OFF of the first switch 110 and the second switch 120; it is connected to the signal processing circuit 230, the third switch 211 and the fourth switch 220, and controls the ON and OFF of the third switch 211 or the fourth switch 221 according to the signal output by the signal processing circuit 230.

[0022] Accordingly, the current signal output ends of the first current zero-cross detection unit 210 and the second current zero-cross detection unit 221 are connected to the input end of the signal processing circuit 230; and two control output ends of the switching control unit 30 provides the signal processing circuit 230 with two working frequency signals representing the AC input voltage polarities, these two control output ends are also directly connected with the first switch 110 and the second switch 220, the other two control outputs are connected with the third switch 211 and the fourth switch 221, so that when the AC input voltage is in the positive half cycle, the second switch 120 is always conducted, and when the body diode of the third switch 211 is conducted or cut off, the first current zero-cross detection unit 210 correspondingly collects current or releases energy, meanwhile, when in the negative half cycle, the first switch 110 is always conducted, while when the body diode of the fourth switch 220 is conducted or cut off, the

second current zero-cross detection unit 221 correspondingly collects current or releases energy.

[0023] Thus, after the current zero-cross signals of the first current zero-cross detection unit 210 and the second current zero-cross detection unit 221 are signal-selected by the signal processing circuit 230 in different polarities of the AC input voltage, the signals are sent to the control input end of the switching control unit 30, the switching control unit 30 controls the ON and OFF of the switch, if the AC input voltage works in the positive half cycle, the switching control unit 30 controls the second switch 120 to be conducted, and meanwhile obtains the current zero-cross signal of the first current zero-cross detection unit 210 according to the selection of the signal processing circuit 230, then adds a preset delay to control the on of the fourth switch 220 on the basis of the signal.

[0024] Accordingly, the preset delay is set according to the reverse recovery time and resonance time of the selected MOS transistor.

[0025] The first current zero-cross detection unit 210 and the second current zero-cross detection unit 221 may be implemented with the same method, such as implemented with components such as the current transformer. Therefore, when the AC input power suppler is in the positive half cycle, the second switch 120 and the fourth switch 220 are switched on, and the third switch 211 is switched off, then the inductor L, the fourth switch 220, the second switch 120 and the second current zero-cross detection unit 221 form a energy storage circuit, while the second current zero-cross detection unit 221 does not collect the current zero-cross signal of the fourth switch 220, the secondary winding of the current transformer is directly short by the sampling switch; when the energy storage of the inductor L completes, the second switch 120 and the third switch 211 are switched on, while the fourth switch 220 is switched off, then the inductor L, the third switch 211, the second switch 120 and the first current zero-cross detection unit 210 form a continuing current circuit and release the energy in the inductor L, at this time, the first current zero-cross detection unit 210 will collect the forward current zero-cross signal of the third switch 211, and the secondary winding of the current transformer in the second current zero-cross detection unit 221 is still in the short-circuit state.

[0026] When the AC input power supply is in the negative half cycle, the first switch 110 and the third switch 211 are switched on, and the fourth switch 220 is switched off, at this time, the third switch 211, the first switch 110, the inductor L and the first current zero-cross detection unit 210 form a energy storage circuit, and at this time, the first current zero-cross detection unit 210 does not collect the current zero-cross signal of the third switch 211, the secondary winding of its current transformer is directly short by the sampling switch; When the energy storage of the inductor L completes, the first switch 110 and the fourth switch 220 are switched on, and the third switch 211 is switched off, at this time, the fourth switch 220, the first switch 110, the inductor L and the second current zero-cross detection unit 221 form a continuing current circuit and release the energy in the inductor L, now the second current zero-cross detection unit 221 collects the forward current zero-cross signal of the fourth switch 220, and the secondary winding of the current transformer in the first current zero-cross detection unit 210 is still in the short-circuit state.

[0027] Thus, in the entire working frequency cycle, it only needs to sample the forward current zero-cross signal flowing through the switch or switch body diode in the continuing current circuit. That is, when the AC input power supply is in the positive half cycle, it only needs the first current zero-cross detection unit 210 to collect the forward current zero-cross signal of the third switch 211; when the AC input power supply is in the negative half cycle, it only needs the second current zero-cross detection unit 221 to collect the forward current zero-cross signal of the fourth switch 220.

[0028] As can be seen from the control principle of the abovementioned circuit system, when the AC input power supply is in the positive half cycle, it needs to control the first current zero-cross detection unit 210 to sample to obtain the forward current zero-cross signal of the third switch 211, while the second current zero cross detection unit 221 does not sample the zero current signal; similarly, in the negative half cycle, the second current zero-cross detection unit 221 samples to obtain the forward current zero-cross signal of the fourth switch 220, while the first current zero-cross detection unit 210 does not sample the zero current signal.

[0029] With reference to FIG. 3, FIG. 4 and FIG. 5, in one specific embodiment, the first current zero-cross detection unit 210 and the second current zero-cross detection unit 221 are implemented in the same manner.

[0030] Wherein the first current zero-cross detection unit 210 comprises:

A current transformer CT1, two sampling switches S11 and S12, a sampling resistor R2 and a comparator T1, wherein the current transformer CT1 comprises a primary winding and a secondary winding; an optional reset resistor R1 is connected in parallel to the two ends of the secondary winding of the current transformer CT1, but it should be noted that, the R1 may not be included.

[0031] The two sampling switches S11 and S12 are connected in series and then connected in parallel with the secondary winding of the current transformer; wherein the drain electrode of the first sampling switch S11 is connected to one end of the secondary winding, the source electrode of the first sampling switch S11 is connected to the drain electrode of the second sampling switch S12, the source electrode of the second sampling switch S12 is connected to the other end of the secondary winding; the sampling resistor R2 is connected in parallel with the source electrode and the drain electrode of the second sampling switch S12.

[0032] The second current zero-cross detection unit 221 comprises:

A current transformer CT2, two sampling switches S21

and S22, a sampling resistor R4, and a comparator T2, the current transformer CT2 comprises a primary winding and a secondary winding; an optional reset impedance R3, which is connected in parallel with both ends of the secondary winding of the current transformer CT1, it should be noted that, the R3 may not be included.

[0033] The two sampling switches S21 and S22 are connected in series and then connected in parallel with the secondary winding of the current transformer; wherein the drain electrode of the first sampling switch S21 is connected to one end of the secondary winding, the source electrode of the first sampling switch S21 is connected to the drain electrode of the second sampling switch S22, the source electrode of the second sampling switch S22 is connected to the other end of the secondary winding; the sampling resistor R4 is connected in parallel with the source electrode and the drain electrode of the second sampling switch S22.

[0034] The abovementioned comparators T1 and T2 are connected to the signal processing circuit 230, when the AC input power is in the positive half cycle, the output end of the comparator T1 is the forward current zero-cross signal sampled by the first current zero-cross detection unit 210; when the AC input power supply is in the negative half cycle, the output end of the comparator T2 is the forward current zero-cross signal sampled by the second current zero-cross detection unit 221.

[0035] In general, the sampling switch comprises a body diode and a parasitic capacitor, wherein the parasitic capacitor is used to reset to achieve the volt-second balance.

[0036] The signal processing circuit 230 comprises the first and second AND gates Z1 and Z2, and an OR gate Z3. The input end of the first AND gate Z1 is connected to the output end of the first current zero-cross detection unit 210 as well as the first working frequency signal representing the AC input voltage polarity and output by the switching control unit 30; the output end of the second AND gate Z2 is connected to the output end of the second current zero-cross detection unit 221 as well as the second working frequency signal representing the AC input voltage polarity and output by the switching control unit 30; the input end of the OR gate Z3 is connected to the output ends of the first AND gate Z1 and the second AND gate Z2.

[0037] Accordingly, when the AC input voltage is respectively in the positive and negative half cycles, the switching control unit provides two working frequency signals representing the AC input voltage polarities, the two working frequency signals are respectively AND with the zero-cross signal obtained by the corresponding current zero-cross detection unit to obtain effective current zero-cross signals in the positive and negative half cycles, and then they are superimposed through the OR gate to obtain the current zero-cross detection signal over the full input voltage range.

[0038] When the current zero-cross detection unit in the present embodiment works in the positive half cycle of the AC input voltage, it is shown as FIG. 4(a), 4(b) and 4(c).

[0039] The working principle of the current zero-cross detection unit in the third switch is as follows: in the positive half cycle of the entire AC input voltage, it is to control to switch off the sampling switches S11 and S12 corresponding to the third switch, and conduct the sampling switches S21 and S22 corresponding to the fourth switch. At this time, when the body diode of the third switch is conducted, that is, when the current shown in FIG. 4 (a) flows through the primary winding of the current transformer CT1, the secondary winding of current transformer CT1 induces the current shown in FIG. 4(a), the secondary winding of the current transformer CT1, the sampling resistor R2 and the body diode of the sampling switch S11 form a sampling circuit, i.e., the solid circuit in FIG. 4(a), and collect the current flowing through the connected third switch in the arrow direction shown in FIG. 4(a); in the period when the third switch is switched off, energy stored in the magnetizing inductor of the current transformer CT1 is reset via the parasitic capacitor of the sampling switch S11, as shown in FIG. 4(b). When the secondary winding of the CT1 is connected in parallel with the optional reset resistor R1 shown in FIG. 3, the energy stored in the magnetizing inductor can also be reset via the R1, which will not be described in detail herein.

[0040] In the positive half cycle, the current transformer CT2 does not need to collect the current, the secondary winding of the current transformer CT2 is directly short by the sampling switches S21 and S22, and its working state is as shown in FIG. 4(c).

[0041] When the current zero-cross detection unit works in the negative half cycle of the AC input voltage in the present embodiment, it is as shown in FIG. 5 (a), 5 (b) and 5 (c).

[0042] The working principle of the current zero-cross detection unit in the fourth switch is as follows: in the negative half cycle of the entire AC input voltage, it is to control to switch off the sampling switches S21 and S22 corresponding to the fourth switch, and conduct the sampling switches S11 and S12 corresponding to the third switch. At this time, the body diode of the fourth switch is conducted, that is, when the current shown in FIG. 5(a) flows through the primary winding of the current transformer CT2, the secondary winding of current transformer CT2 induces the current shown in the FIG. 5(a), the secondary winding of the current transformer CT2, the sampling resistor R4 and the body diode of the sampling switch S21 form a sampling circuit, i.e., the solid circuit in FIG. 5(a), and collect the current flowing through the connected fourth switch in the arrow direction shown in FIG. 5(a); in the period when the fourth switch is switched off, energy stored in the magnetizing inductor of the current transformers CT2 is reset via the parasitic capacitor of the switch S21, as shown in FIG. 5(b). When the secondary winding of the CT2 is connected in parallel with the optional reset resistor R3 shown in FIG. 3, the energy

stored in the magnetizing inductor can also be reset via the R3, which will not be described in detail herein.

[0043] In the negative half cycle, the current transformer CT2 does not need to collect the current, the secondary winding of the current transformer CT2 is directly short by the sampling switches S11 and S12, and its working state is as shown in FIG. 5(c).

[0044] According to the above analysis, it can be seen that, when the totem pole bridgeless PFC works in the TCM working mode, the current transformer only samples the current flowing through the switch in its continuing current circuit, that is, it only samples the current in the segment where the inductor current falls, and hereby obtains the current zero-cross signal, its working waveform is shown in FIG. 6. V_{CT1} is the voltage of the sampling resistor R2 in the working frequency positive half cycle, and V_{CT2} is the voltage of the sampling resistor R4 in the working frequency negative half cycle. Comparing the voltage signal with the reference voltage Vth of the comparator, and when the sampled voltage is less than Vth, the comparator inverts and outputs a high level, thus receiving the zero-cross detection signal in the segment where the inductor current falls, and the signal can be used to switch off the corresponding continuing current switch, as well as to add a certain delay on the basis of the signal to switch on the primary switch.

[0045] Wherein, the third switch is a continuing current tube and the fourth switch is the primary switch in the working frequency positive half cycle, and on the contrary, the fourth switch is a continuing current tube and the third switch is the primary switch in the working frequency negative half-cycle.

[0046] The working waveform of the signal processing circuit is shown in FIG. 7: when the AC input voltage Vin is in the positive half cycle, the obtained effective zero current detection signals Vzcd1 and Vzcd2 are invalid signals, on the contrary, when the AC input voltage Vin is in the negative half-cycle, the effective zero current detection signal Vzcd2 is obtained, while the Vzcd1 is an invalid signal. Thus, a switching control unit is used to provide working frequency signals VPos and VNeg representing the positive half cycle and the negative half cycle, that is, these two signals are used to control the ON or OFF of the first switch and the second switch in the first bridge arm, and also used to obtain the effective zero current detection signal Vzcd in both positive and negative half cycles after respectively shielding the unwanted signals in the positive and negative half cycles.

[0047] In summary, the totem pole bridgeless PFC circuit in the embodiment of the present invention comprises a signal processing circuit and a switching control unit, two current zero-cross detection units are added in the second bridge arm unit, the forward current zero-cross signals collected by the switching control unit via the first current zero-cross detection unit and the second current zero-cross detection unit are signal-processed by the signal processing circuit to obtain the current zero-cross signals which are respectively used for controlling the ON or OFF of the third switch and the fourth switch in the second bridge arm unit. Compared to the totem pole bridgeless PFC circuit system in the related art, the system in accordance with the embodiment of the present invention controls the ON and OFF of the switch by sampling the current zero signal of the inductor, to achieve the ZVS or VS control within the full input voltage and full load range under the TCM mode, so as to effectively realize the timing control of the totem pole bridgeless circuit system and improve the efficiency of the totem pole bridgeless PFC system.

[0048] The embodiment of the present invention further provides a current zero-cross detection device, as shown in FIG. 3, the device comprises a current transformer, a first sampling switch, a second sampling switch, a sampling resistor and a comparator, wherein the current transformer comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit to be detected;

two ends of the secondary winding are respectively connected to the drain electrodes of the first sampling switch and the second sampling switch;

the source electrode of the first sampling switch is connected to the source electrode of the second sampling switch, and the source electrodes are connected to ground;

two ends of the sampling resistor are respectively connected to the drain electrode and the source electrode of the second sampling switch;

the negative input end of the comparator is connected to the drain electrode of the second sampling switch, and the positive input end of the comparator is connected to a reference voltage;

the first and second sampling switches are in an ON or OFF state.

[0049] Alternatively, the device further comprises a reset resistor, and two ends of the reset resistor are respectively connected to two ends of the secondary winding.

[0050] The sampling switch is a metal-oxide-semiconductor field effect transistor (Mosfet), an insulated gate bipolar transistor (IGBT), or a bipolar transistor (BJT).

[0051] Furthermore, the present invention further provides a current zero-cross signal acquisition circuit, wherein, the circuit comprises:

a first current zero-cross detection unit, located in a first circuit branch, and configured to collect a current flowing through the first circuit branch when an alternate current (AC) input voltage is in a positive half

cycle, to acquire a current zero-cross signal of the first circuit branch;

a second current zero-cross detection unit, located in a second circuit branch and configured to collect a current flowing through the second circuit branch when the AC input voltage is in a negative half cycle, to acquire a current zero-cross signal of the second circuit branch; and

a signal processing circuit, configured to select the current zero-cross signal collected by the first current zero-cross detection unit when the AC input voltage is in the positive half cycle; and select the current zero-cross signal collected by the second current zero-cross detection unit when the AC input voltage is in the negative half cycle.

[0052] The first and second current zero-cross detection units have an identical structure, comprising a current transformer, a first sampling switch, a second sampling switch, a sampling resistor and a comparator, wherein the current transformer comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit to be detected;
two ends of the secondary winding are respectively connected to drain electrodes of the first sampling switch and the second sampling switch;
a source electrode of the first sampling switch is connected to a source electrode of the second sampling switch, and the source electrodes are connected to ground;
two ends of the sampling resistor are respectively connected to the drain electrode and the source electrode of the second sampling switch;
the negative input end of the comparator is connected to the drain electrode of the second sampling switch, and the positive input end of the comparator is connected to a reference voltage;
alternatively, the signal processing circuit comprises: a first AND gate, a second AND gate and an OR gate, the input end of the first AND gate is connected to the output end of the first current zero-cross detection unit and a first working frequency signal representing the AC input voltage polarity; the input end of the second AND gate is connected to the output end of the second current zero-cross detection unit and a second working frequency signal representing the AC input voltage polarity; the input end of the OR gate is connected to the output ends of the first AND gate and the second AND gate.

[0053] The first and second current zero-cross detection units further comprise reset resistors, and two ends of the reset resistor are respectively connected to two ends of the secondary winding.

[0054] The current zero-cross detection unit in accordance with the embodiment of the present invention can collect the AC current zero-cross signal, i.e., collecting the current zero-cross signal via a energy storage circuit consisting of the secondary winding of the current transformer, two sampling switches, one sampling resistor and one comparator.

Industrial Applicability

[0055] The current zero-cross detection device, current zero-cross signal acquisition circuit and totem pole bridgeless circuit system in accordance with the embodiment of the present invention control the ON and OFF state of a switch by collecting the current zero-cross signal to achieve the ZVS or VS control in the full input voltage and full load range under the TCM mode, and to improve the efficiency of the totem pole bridgeless PFC system.

Claims

1. A current zero-cross detection device (210, 221), comprising a current transformer (CT1, CT2), a first sampling switch (S11, S21), a second sampling switch (S12, S22), a sampling resistor (R2, R4) and a comparator (T1, T2), wherein the current transformer (CT1, CT2) comprises a primary winding and a secondary winding; wherein:

the primary winding is configured to be connected with a circuit for detecting a current through the circuit;
two ends of the secondary winding are connected respectively to drain electrodes of the first sampling switch (S11, S21) and the second sampling switch (S12, S22);
a source electrode of the first sampling switch (S11, S21) is connected to a source electrode of the second sampling switch (S12, S22), and the source electrodes are connected to ground;
two ends of the sampling resistor (R2, R4) are respectively connected to the drain electrode and source electrode of the second sampling switch (S12, S22);
a negative input end of the comparator (T1, T2) is connected to the drain electrode of the second sampling switch (S12, S22), and a positive input end of the comparator (T1, T2) is connected to a reference voltage; and
the first sampling switch (S11, S21) and the second sampling switch (S12, S22) are in an ON or OFF state,
characterized in that, current flowing through the current transformer (CT1, CT2) is sampled via the first sampling switch (S11, S21) and the sampling resistor (R2, R4), and energy stored

in the current transformer (CT1, CT2) is reset via a parasitic capacitor of the first sampling switch (S11, S21) and the sampling resistor (R2, R4),
wherein voltage of the sampling resistor (R2, R4) is compared with the reference voltage of the comparator (T1, T2), and when the voltage of the sampling resistor (R2, R4) is less than the reference voltage of the comparator (T1, T2), the comparator (T1, T2) is configured to invert and output a high level, thus the current zero-cross is detected.

2. The device of claim 1, wherein, the device further comprises a reset resistor (R1, R3), and two ends of the reset resistor (R1, R3) are respectively connected to the two ends of the secondary winding.

3. The device of claim 1, wherein, the sampling switch (S11, S12) is a metal-oxide-semiconductor field effect transistor (Mosfet), an insulated gate bipolar transistor (IGBT), or a bipolar transistor (BJT).

4. A current zero-cross signal acquisition circuit, comprising:

a first current zero-cross detection unit (210), located in a first circuit branch, and configured to collect a current flowing through the first circuit branch when an alternate current (AC) input voltage is in a positive half cycle, to acquire a current zero-cross signal of the first circuit branch;
a second current zero-cross detection unit (221), located in a second circuit branch and configured to collect a current flowing through the second circuit branch when the AC input voltage is in a negative half cycle, to acquire a current zero-cross signal of the second circuit branch; and
a signal processing circuit (230), configured to select the current zero-cross signal collected by the first current zero-cross detection unit (210) when the AC input voltage is in the positive half cycle; and select the current zero-cross signal collected by the second current zero-cross detection unit (221) when the AC input voltage is in the negative half cycle,
wherein, the first current zero-cross detection unit (210) and the second current zero-cross detection unit (221) have an identical structure, comprising a current transformer (CT1, CT2), a first sampling switch (S11, S21), a second sampling switch (S12, S22), a sampling resistor (R2, R4) and a comparator (T1, T2), and the current transformer (CT1, CT2) comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit for detecting a current through the circuit;
two ends of the secondary winding are respectively connected to drain electrodes of the first sampling switch (S11, S21) and the second sampling switch (S12, S22);
a source electrode of the first sampling switch (S11, S21) is connected to a source electrode of the second sampling switch (S12, S22), and the source electrodes are connected to ground;
two ends of the sampling resistor (R2, R4) are respectively connected to the drain electrode and the source electrode of the second sampling switch (S12, S22); and
a negative input end of the comparator (T1, T2) is connected to the drain electrode of the second sampling switch (S12, S22), and a positive input end of the comparator (T1, T2) is connected to a reference voltage,
characterized in that, current flowing through the current transformer (CT1, CT2) is sampled via the first sampling switch (S11, S21) and the sampling resistor (R2, R4), and energy stored in the current transformer (CT1, CT2) is reset via a parasitic capacitor of the first sampling switch (S11, S21) and the sampling resistor (R2, R4)

wherein voltage of the sampling resistor (R2, R4) is compared with the reference voltage of the comparator (T1, T2), and when the voltage of the sampling resistor (R2, R4) is less than the reference voltage of the comparator (T1, T2), the comparator (T1, T2) inverts and outputs a high level, thus the current zero-cross is detected.

5. The circuit of claim 4, wherein, the signal processing circuit (230) comprises: a first AND gate (Z1), a second AND gate (Z2) and an OR gate (Z3), an input end of the first AND gate (Z1) is connected to an output end of the first current zero-cross detection unit (210) and a first working frequency signal representing polarity of the AC input voltage; an input end of the second AND gate (Z2) is connected to an output end of the second current zero-cross detection unit (221) and a second working frequency signal representing polarity of the AC input voltage; an input end of the OR gate (Z3) is connected to output ends of the first AND gate (Z1) and the second AND gate (Z2).

6. The circuit of claim 4, wherein, the first current zero-cross detection unit (210) and the second current zero-cross detection unit (221) further comprise reset resistors (R1, R3), and two ends of the reset resistor are respectively connected to the two ends of

the secondary winding.

7. A totem pole bridgeless circuit system, comprising: a first bridge arm unit (10) and a second bridge arm unit (20),
wherein the first bridge arm unit (10) and the second bridge arm unit (20) are connected in parallel between a first parallel connection point (1) and a second parallel connection point (2), the first bridge arm unit (10) comprises a first switch (110) and a second switch (120) connected in series in the same direction; the second bridge arm unit (20) comprises a third switch (211) and a fourth switch (220) connected in series in the same direction; a power supply (Vin) and an inductor (L) are connected between a first connection point (4) between the first switch (110) and the second switch (120) and a second connection point (3) between the third switch (211) and the fourth switch (220), and the second bridge arm unit (20) further comprises:

a first current zero-cross detection unit (210), a second current zero-cross detection unit (221) and a signal processing circuit (230), wherein the first current zero-cross detection unit (210) and the third switch (211) are connected in series between the first parallel connection point (1) and the second connection point (3); the second current zero-cross detection unit (221) and the fourth switch (220) are connected in series between the second parallel connection point (2) and the second connection point (3); the signal processing circuit (230) is connected to the first current zero-cross detection unit (210) and the second current zero-cross detection unit (221);
the first current zero-cross detection unit (210) is configured to, when an AC input voltage is in a positive half cycle and a body diode of the third switch (211) is conducted, collect a current flowing through the third switch (211), and obtain a current zero-cross signal of the current flowing through the third switch (211);
the second current zero-cross detection unit (221) is configured to, when the AC input voltage is in a negative half cycle and a body diode of the fourth switch (220) is conducted, collect a current flowing through the fourth switch (220) and obtain a current zero-cross signal of the current flowing through the fourth switch (220);
the signal processing circuit (230) is configured to select the current zero-cross signal collected by the first current zero-cross detection unit (210) when the AC input voltage is in the positive half axle; select the current zero-cross signal collected by the second current zero-cross detection unit (220) when the AC input voltage is in the negative half cycle; and

a switching control unit (30), connected to the signal processing circuit (230) as well as the third switch (211) and the fourth switch (220), and is configured to control ON or OFF of the third switch (211) and the fourth switch (220) according to a signal output by the signal processing circuit (230),
wherein, structures of the first current zero-cross detection unit (210) and the second current zero-cross detection unit (221) respectively comprise a current transformer (CT1, CT2), a first sampling switch (S11, S21), a second sampling switch (S12, S22), a sampling resistor (R2, R4) and a comparator (T1, T2), and the current transformer (CT1, CT2) comprises a primary winding and a secondary winding; wherein:

the primary winding is connected with a circuit for detecting a current through the circuit;
two ends of the secondary winding are respectively connected to drain electrodes of the first sampling switch (S11, S21) and the second sampling switch (S12, S22);
a source electrode of the first sampling switch (S11, S21) is connected to a source electrode of the second sampling switch (S12, S22), and the source electrodes are connected to ground;
two ends of the sampling resistor (R2, R4) are respectively connected to the drain electrode and the source electrode of the second sampling switch (S12, S22); and
a negative input end of the comparator (T1, T2) is connected to the drain electrode of the second sampling switch (S12, S22), and a positive input end thereof is connected to a reference voltage,
characterized in that, current flowing through the current transformer (CT1, CT2) is sampled via the first sampling switch (S11, S21) and the sampling resistor (R2, R4), and energy stored in the current transformer (CT1, CT2) is reset via a parasitic capacitor of the first sampling switch (S11, S21) and the sampling resistor (R2, R4)

wherein voltage of the sampling resistor (R2, R4) is compared with the reference voltage of the comparator (T1, T2), and when the voltage of the sampling resistor (R2, R4) is less than the reference voltage of the comparator (T1, T2), the comparator (T1, T2) inverts and outputs a high level, thus the current zero-cross is detected.

8. The circuit system of claim 7, wherein, the signal processing circuit (230) comprises:
a first AND gate (Z1), a second AND gate (Z2) and

an OR gate (Z3), an input end of the first AND gate (Z1) is connected to an output end of the first current zero-cross detection unit (210) and a first working frequency signal representing polarity of the AC input voltage and output by the switching control unit (30); an input end of the second AND gate (Z2) is connected to an output end of the second current zero-cross detection unit (221) and a second working frequency signal representing polarity of the AC input voltage and output by the switching control unit (30); an input end of the OR gate (Z3) is connected to output ends of the first AND gate (Z1) and the second AND gate (Z2).

9. The circuit system of claim 7, wherein, the first current zero-cross detection unit (210) and the second current zero-cross detection unit (221) further comprise reset resistors, and two ends of the reset resistor (R1, R3) are respectively connected to the two ends of the secondary winding.

Patentansprüche

1. Nullstromerkennungsvorrichtung (210, 221), die einen Stromwandler (CT1, CT2), einen ersten Abtastschalter (S11, S21), einen zweiten Abtastschalter (S12, S22), einen Abtastwiderstand (R2, R4) und einen Komparator (T1, T2) umfasst, wobei der Stromwandler (CT1, CT2) eine primäre Wicklung und eine sekundäre Wicklung umfasst; wobei:

die primäre Wicklung dazu konfiguriert ist, mit einer Schaltung zum Erkennen eines Stroms durch die Schaltung verbunden zu sein;
zwei Enden der sekundären Wicklung jeweils mit Drainelektroden des ersten Abtastschalters (S11, S21) und des zweiten Abtastschalters (S12, S22) verbunden sind;
eine Quellenelektrode des ersten Abtastschalters (S11, S21) mit einer Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und die Quellenelektroden geerdet sind;
zwei Enden des Abtastwiderstands (R2, R4) jeweils mit der Drainelektrode und der Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden sind;
ein negatives Eingangsende des Komparators (T1, T2) mit der Drainelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und ein positives Eingangsende des Komparators (T1, T2) mit einer Bezugsspannung verbunden ist; und
der erste Abtastschalter (S11, S21) und der zweite Abtastschalter (S12, S22) sich in einem AN- oder AUS-Zustand befinden,
dadurch gekennzeichnet, dass Strom, der durch den Stromwandler (CT1, CT2) fließt, über den ersten Abtastschalter (S11, S21) und den Abtastwiderstand (R2, R4) abgetastet wird und Energie, die in dem Stromwandler (CT1, CT2) gespeichert ist, über einen parasitären Kondensator des ersten Abtastschalters (S11, S21) und den Abtastwiderstand (R2, R4) zurückgesetzt wird,
wobei Spannung des Abtastwiderstands (R2, R4) mit der Bezugsspannung des Komparators (T1, T2) verglichen wird, und wenn die Spannung des Abtastwiderstands (R2, R4) geringer als die Bezugsspannung des Komparators (T1, T2) ist, ist der Komparator (T1, T2) dazu konfiguriert, zu invertieren und einen hohen Pegel auszugeben, wodurch der Nullstrom erkannt wird.

2. Vorrichtung nach Anspruch 1, wobei die Vorrichtung ferner einen Rücksetzwiderstand (R1, R3) umfasst und zwei Enden des Rücksetzwiderstands (R1, R3) jeweils mit den zwei Enden der sekundären Wicklung verbunden sind.

3. Vorrichtung nach Anspruch 1, wobei der Abtastschalter (S11, S12) ein Metalloxid-Halbleiter-Feldeffekttransistor (Mosfet), ein Bipolartransistor mit isolierter Gate-Elektrode (insulated gate bipolar transistor - IGBT) oder ein Bipolartransistor (bipolar transistor - BJT) ist.

4. Nullstromsignalerfassungsschaltung, umfassend:

eine erste Nullstromerkennungseinheit (210), die sich in einem ersten Schaltungszweig befindet und die dazu konfiguriert ist, einen Strom zu sammeln, der durch den ersten Schaltungszweig fließt, wenn eine Wechselstrom (alternate current - AC)-Eingangsspannung in einem positiven Halbzyklus vorliegt, zum Erfassen eines Nullstromsignals des ersten Schaltungszweigs;
eine zweite Nullstromerkennungseinheit (221), die sich in einem zweiten Schaltungszweig befindet und die dazu konfiguriert ist, einen Strom zu sammeln, der durch den zweiten Schaltungszweig fließt, wenn die AC-Eingangsspannung in einem negativen Halbzyklus vorliegt, zum Erfassen eines Nullstromsignals des zweiten Schaltungszweigs; und
eine Signalverarbeitungsschaltung (230), die dazu konfiguriert ist, das Nullstromsignal auszuwählen, das von der ersten Nullstromerkennungseinheit (210) gesammelt wird, wenn die AC-Eingangsspannung in dem positiven Halbzyklus vorliegt; und das Nullstromsignal auszuwählen, das von der zweiten Nullstromerkennungseinheit (221) gesammelt wird, wenn die AC-Eingangsspannung in dem negativen Halbzyklus vorliegt,

wobei die erste Nullstromerkennungseinheit (210) und die zweite Nullstromerkennungseinheit (221) eine identische Struktur aufweisen, die einen Stromwandler (CT1, CT2), einen ersten Abtastschalter (S11, S21), einen zweiten Abtastschalter (S12, S22), einen Abtastwiderstand (R2, R4) und einen Komparator (T1, T2) umfasst, und wobei der Stromwandler (CT1, CT2) eine primäre Wicklung und eine sekundäre Wicklung umfasst; wobei:

die primäre Wicklung mit einer Schaltung zum Erkennen eines Stroms durch die Schaltung verbunden ist;
zwei Enden der sekundären Wicklung jeweils mit Drainelektroden des ersten Abtastschalters (S11, S21) und des zweiten Abtastschalters (S12, S22) verbunden sind;
eine Quellenelektrode des ersten Abtastschalters (S11, S21) mit einer Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und die Quellenelektroden geerdet sind;
zwei Enden des Abtastwiderstands (R2, R4) jeweils mit der Drainelektrode und der Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden sind; und
ein negatives Eingangsende des Komparators (T1, T2) mit der Drainelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und ein positives Eingangsende des Komparators (T1, T2) mit einer Bezugsspannung verbunden ist,
dadurch gekennzeichnet, dass Strom, der durch den Stromwandler (CT1, CT2) fließt, über den ersten Abtastschalter (S11, S21) und den Abtastwiderstand (R2, R4) abgetastet wird und Energie, die in dem Stromwandler (CT1, CT2) gespeichert ist, über einen parasitären Kondensator des ersten Abtastschalters (S11, S21) und den Abtastwiderstand (R2, R4) zurückgesetzt wird,
wobei Spannung des Abtastwiderstands (R2, R4) mit der Bezugsspannung des Komparators (T1, T2) verglichen wird, und wenn die Spannung des Abtastwiderstands (R2, R4) geringer als die Bezugsspannung des Komparators (T1, T2) ist, invertiert der Komparator (T1, T2) und gibt einen hohen Pegel aus, wodurch der Nullstrom erkannt wird.

5. Schaltung nach Anspruch 4, wobei die Signalverarbeitungsschaltung (230) Folgendes umfasst: ein erstes UND-Gatter (Z1), ein zweites UND-Gatter (Z2) und ein ODER-Gatter (Z3), wobei ein Eingangsende des ersten UND-Gatters (Z1) mit einem Ausgangsende der ersten Nullstromerkennungseinheit (210) verbunden ist und wobei ein erstes Arbeitsfrequenzsignal eine Polarität der AC-Eingangsspannung darstellt; wobei ein Eingangsende des zweiten UND-Gatters (Z2) mit einem Ausgangsende der zweiten Nullstromerkennungseinheit (221) verbunden ist und wobei ein zweites Arbeitsfrequenzsignal eine Polarität der AC-Eingangsspannung darstellt; wobei ein Eingangsende des ODER-Gatters (Z3) mit Ausgangsenden des ersten UND-Gatters (Z1) und des zweiten UND-Gatters (Z2) verbunden ist.

6. Schaltung nach Anspruch 4, wobei die erste Nullstromerkennungseinheit (210) und die zweite Nullstromerkennungseinheit (221) ferner Rücksetzwiderstände (R1, R3) umfassen und zwei Enden des Rücksetzwiderstands jeweils mit den zwei Enden der sekundären Wicklung verbunden sind.

7. Totem-Pole-Schaltungssystem ohne Brücke, umfassend: eine erste Brückenzweigeinheit (10) und eine zweite Brückenzweigeinheit (20),
wobei die erste Brückenzweigeinheit (10) und die zweite Brückenzweigeinheit (20) parallel zwischen einem ersten parallelen Verbindungspunkt (1) und einem zweiten parallelen Verbindungspunkt (2) verbunden sind, die erste Brückenzweigeinheit (10) einen ersten Schalter (110) und einen zweiten Schalter (120) umfasst, die in der gleichen Richtung in Reihe geschaltet sind; wobei die zweite Brückenzweigeinheit (20) einen dritten Schalter (211) und einen vierten Schalter (220) umfasst, die in die gleiche Richtung in Reihe geschaltet sind; wobei eine Leistungszufuhr (Vin) und ein Induktor (L) zwischen einem ersten Verbindungspunkt (4) zwischen dem ersten Schalter (110) und dem zweiten Schalter (120) und einem zweiten Verbindungspunkt (3) zwischen dem dritten Schalter (211) und dem vierten Schalter (220) verbunden sind, und wobei die zweite Brückenzweigeinheit (20) ferner Folgendes umfasst:

eine erste Nullstromerkennungseinheit (210), eine zweite Nullstromerkennungseinheit (221) und eine Signalverarbeitungsschaltung (230), wobei die erste Nullstromerkennungseinheit (210) und der dritte Schalter (211) zwischen dem ersten parallelen Verbindungspunkt (1) und dem zweiten Verbindungspunkt (3) in Reihe geschaltet sind; wobei die zweite Nullstromerkennungseinheit (221) und der vierte Schalter (220) zwischen dem zweiten parallelen Verbindungspunkt (2) und dem zweiten Verbindungspunkt (3) in Reihe geschaltet sind; wobei die Signalverarbeitungsschaltung (230) mit der ersten Nullstromerkennungseinheit (210) und der zweiten Nullstromerkennungseinheit (221) verbunden ist;

wobei die erste Nullstromerkennungseinheit (210) dazu konfiguriert ist, wenn eine AC-Eingangsspannung in einem positiven Halbzyklus vorliegt und eine Substratdiode des dritten Schalters (211) ausgeführt wird, einen Strom zu sammeln, der durch den dritten Schalter (211) fließt, und ein Nullstromsignal des Stroms zu erhalten, der durch den dritten Schalter (211) fließt;

wobei die zweite Nullstromerkennungseinheit (221) dazu konfiguriert ist, wenn die AC-Eingangsspannung in einem negativen Halbzyklus vorliegt und eine Substratdiode des vierten Schalters (220) ausgeführt wird, einen Strom zu sammeln, der durch den vierten Schalter (220) fließt, und ein Nullstromsignal des Stroms zu erhalten, der durch den vierten Schalter (220) fließt;

wobei die Signalverarbeitungsschaltung (230) dazu konfiguriert ist, das Nullstromsignal auszuwählen, das von der ersten Nullstromerkennungseinheit (210) gesammelt wird, wenn die AC-Eingangsspannung in dem positiven Halbzyklus vorliegt; das Nullstromsignal auszuwählen, das von der zweiten Nullstromerkennungseinheit (220) gesammelt wird, wenn die AC-Eingangsspannung in dem negativen Halbzyklus vorliegt; und

eine Schaltsteuereinheit (30), die mit der Signalverarbeitungsschaltung (230) wie auch mit dem dritten Schalter (211) und dem vierten Schalter (220) verbunden ist und dazu konfiguriert ist, ein AN oder AUS des dritten Schalters (211) und des vierten Schalters (220) gemäß einer Signalausgabe durch die Signalverarbeitungsschaltung (230) zu steuern,

wobei Strukturen der ersten Nullstromerkennungseinheit (210) und der zweiten Nullstromerkennungseinheit (221) jeweils einen Stromwandler (CT1, CT2), einen ersten Abtastschalter (S11, S21), einen zweiten Abtastschalter (S12, S22), einen Abtastwiderstand (R2, R4) und einen Komparator (T1, T2) umfassen und der Stromwandler (CT1, CT2) eine primäre Wicklung und eine sekundäre Wicklung umfasst; wobei:

die primäre Wicklung mit einer Schaltung zum Erkennen eines Stroms durch die Schaltung verbunden ist;

zwei Enden der sekundären Wicklung jeweils mit Drainelektroden des ersten Abtastschalters (S11, S21) und des zweiten Abtastschalters (S12, S22) verbunden sind;

eine Quellenelektrode des ersten Abtastschalters (S11, S21) mit einer Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und die Quellenelektroden geerdet sind;

zwei Enden des Abtastwiderstands (R2, R4) jeweils mit der Drainelektrode und der Quellenelektrode des zweiten Abtastschalters (S12, S22) verbunden sind; und

ein negatives Eingangsende des Komparators (T1, T2) mit der Drainelektrode des zweiten Abtastschalters (S12, S22) verbunden ist und ein positives Eingangsende desselben mit einer Bezugsspannung verbunden ist,

dadurch gekennzeichnet, dass Strom, der durch den Stromwandler (CT1, CT2) fließt, über den ersten Abtastschalter (S11, S21) und den Abtastwiderstand (R2, R4) abgetastet wird und Energie, die in dem Stromwandler (CT1, CT2) gespeichert ist, über einen parasitären Kondensator des ersten Abtastschalters (S11, S21) und den Abtastwiderstand (R2, R4) zurückgesetzt wird,

wobei Spannung des Abtastwiderstands (R2, R4) mit der Bezugsspannung des Komparators (T1, T2) verglichen wird, und wenn die Spannung des Abtastwiderstands (R2, R4) geringer als die Bezugsspannung des Komparators (T1, T2) ist, invertiert der Komparator (T1, T2) und gibt einen hohen Pegel aus, wodurch der Nullstrom erkannt wird.

8. Schaltungssystem nach Anspruch 7, wobei die Signalverarbeitungsschaltung (230) Folgendes umfasst:

ein erstes UND-Gatter (Z1), ein zweites UND-Gatter (Z2) und ein ODER-Gatter (Z3), wobei ein Eingangsende des ersten UND-Gatters (Z1) mit einem Ausgangsende der ersten Nullstromerkennungseinheit (210) verbunden ist und wobei ein erstes Arbeitsfrequenzsignal eine Polarität der AC-Eingangsspannung darstellt und von der Schaltsteuereinheit (30) ausgegeben wird; wobei ein Eingangsende des zweiten UND-Gatters (Z2) mit einem Ausgangsende der zweiten Nullstromerkennungseinheit (221) verbunden ist und wobei ein zweites Arbeitsfrequenzsignal eine Polarität der AC-Eingangsspannung darstellt und von der Schaltsteuereinheit (30) ausgegeben wird; wobei ein Eingangsende des ODER-Gatters (Z3) mit Ausgangsenden des ersten UND-Gatters (Z1) und des zweiten UND-Gatters (Z2) verbunden ist.

9. Schaltungssystem nach Anspruch 7, wobei die erste Nullstromerkennungseinheit (210) und die zweite Nullstromerkennungseinheit (221) ferner Rücksetzwiderstände umfassen und zwei Enden des Rücksetzwiderstands (R1, R3) jeweils mit den zwei Enden der sekundären Wicklung verbunden sind.

Revendications

1. Dispositif de détection de passage à zéro de courant (210, 221), comprenant un transformateur de courant (CT1, CT2), un premier commutateur d'échantillonnage (S11, S21), un deuxième commutateur d'échantillonnage (S12, S22), une résistance d'échantillonnage (R2, R4) et un comparateur (T1, T2), où le transformateur de courant (CT1, CT2) comprend un enroulement primaire et un enroulement secondaire ; où :

l'enroulement primaire est configuré pour être relié à un circuit de détection d'un courant traversant le circuit ;
deux extrémités de l'enroulement secondaire sont reliées respectivement à des électrodes de drain du premier commutateur d'échantillonnage (S11, S21) et du deuxième commutateur d'échantillonnage (S12, S22) ;
une électrode de source du premier commutateur d'échantillonnage (S11, S21) est reliée à une électrode de source du deuxième commutateur d'échantillonnage (S12, S22), et les électrodes de source sont reliées à la masse ;
deux extrémités de la résistance d'échantillonnage (R2, R4) sont respectivement reliées à l'électrode de drain et à l'électrode de source du deuxième commutateur d'échantillonnage (S12, S22) ;
une extrémité d'entrée négative du comparateur (T1, T2) est reliée à l'électrode de drain du deuxième commutateur d'échantillonnage (S12, S22), et une extrémité d'entrée positive du comparateur (T1, T2) est reliée à une tension de référence ; et
le premier commutateur d'échantillonnage (S11, S21) et le deuxième commutateur d'échantillonnage (S12, S22) sont dans un état activé ou désactivé,
caractérisé en ce qu'un courant circulant à travers le transformateur de courant (CT1, CT2) est échantillonné par l'intermédiaire du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4), et une énergie stockée dans le transformateur de courant (CT1, CT2) est réinitialisée par l'intermédiaire d'un condensateur parasite du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4),
dans lequel une tension de la résistance d'échantillonnage (R2, R4) est comparée à la tension de référence du comparateur (T1, T2) et, lorsque la tension de la résistance d'échantillonnage (R2, R4) est inférieure à la tension de référence du comparateur (T1, T2), le comparateur (T1, T2) est configuré pour inverser et délivrer en sortie un niveau élevé, ainsi le passage à zéro de courant est détecté.

2. Dispositif de la revendication 1, dans lequel le dispositif comprend en outre une résistance de réinitialisation (R1, R3), et deux extrémités de la résistance de réinitialisation (R1, R3) sont respectivement reliées aux deux extrémités de l'enroulement secondaire.

3. Dispositif de la revendication 1, dans lequel le commutateur d'échantillonnage (S11, S12) est un transistor à effet de champ à semiconducteur à oxyde métallique (Mosfet), un transistor bipolaire à porte isolée (IGBT) ou un transistor bipolaire (BJT).

4. Circuit d'acquisition de signal de passage à zéro de courant, comprenant :

une première unité de détection de passage à zéro de courant (210), située dans une première branche de circuit et configurée pour recueillir un courant circulant à travers la première branche de circuit lorsqu'une tension d'entrée de courant alternatif (CA) se trouve dans un demi-cycle positif, pour acquérir un signal de passage à zéro de courant de la première branche de circuit ;
une deuxième unité de détection de passage à zéro de courant (221), située dans une deuxième branche de circuit et configurée pour recueillir un courant circulant à travers la deuxième branche de circuit lorsque la tension d'entrée CA se trouve dans un demi-cycle négatif, pour acquérir un signal de passage à zéro de courant de la deuxième branche de circuit ; et
un circuit de traitement de signal (230), configuré pour sélectionner le signal de passage à zéro de courant recueilli par la première unité de détection de passage à zéro de courant (210) lorsque la tension d'entrée CA se trouve dans le demi-cycle positif ; et pour sélectionner le signal de passage à zéro de courant recueilli par la deuxième unité de détection de passage à zéro de courant (221) lorsque la tension d'entrée CA se trouve dans le demi-cycle négatif,
dans lequel, la première unité de détection de passage à zéro de courant (210) et la deuxième unité de détection de passage à zéro de courant (221) ont une structure identique, comprenant un transformateur de courant (CT1, CT2), un premier commutateur d'échantillonnage (S11, S21), un deuxième commutateur d'échantillonnage (S12, S22), une résistance d'échantillonnage (R2, R4) et un comparateur (T1, T2), et le transformateur de courant (CT1, CT2) comprend un enroulement primaire et un enroulement secondaire ; où :

l'enroulement primaire est relié à un circuit de détection d'un courant traversant le circuit ;
deux extrémités de l'enroulement secondaire sont respectivement reliées à des électrodes de drain du premier commutateur d'échantillonnage (S11, S21) et du deuxième commutateur d'échantillonnage (S12, S22) ;
une électrode de source du premier commutateur d'échantillonnage (S11, S21) est reliée à une électrode de source du deuxième commutateur d'échantillonnage (S12, S22), et les électrodes de source sont reliées à la masse ;
deux extrémités de la résistance d'échantillonnage (R2, R4) sont respectivement reliées à l'électrode de drain et à l'électrode de source du deuxième commutateur d'échantillonnage (S12, S22) ; et
une extrémité d'entrée négative du comparateur (T1, T2) est reliée à l'électrode de drain du deuxième commutateur d'échantillonnage (S12, S22), et une extrémité d'entrée positive du comparateur (T1, T2) est reliée à une tension de référence,
caractérisé en ce qu'un courant circulant à travers le transformateur de courant (CT1, CT2) est échantillonné par l'intermédiaire du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4), et une énergie stockée dans le transformateur de courant (CT1, CT2) est réinitialisée par l'intermédiaire d'un condensateur parasite du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4),
dans lequel une tension de la résistance d'échantillonnage (R2, R4) est comparée à la tension de référence du comparateur (T1, T2) et, lorsque la tension de la résistance d'échantillonnage (R2, R4) est inférieure à la tension de référence du comparateur (T1, T2), le comparateur (T1, T2) inverse et délivre en sortie un niveau élevé, ainsi le passage à zéro de courant est détecté.

5. Circuit de la revendication 4, dans lequel le circuit de traitement de signal (230) comprend : une première porte ET (Z1), une deuxième porte ET (Z2) et une porte OU (Z3), une extrémité d'entrée de la première porte ET (Z1) est reliée à une extrémité de sortie de la première unité de détection de passage à zéro de courant (210) et à un premier signal de fréquence de travail représentant une polarité de la tension d'entrée CA ; une extrémité d'entrée de la deuxième porte ET (Z2) est reliée à une extrémité de sortie de la deuxième unité de détection de passage à zéro de courant (221) et à un deuxième signal de fréquence de travail représentant une polarité de la tension d'entrée CA ; une extrémité d'entrée de la porte OU (Z3) est reliée à des extrémités de sortie de la première porte ET (Z1) et de la deuxième porte ET (Z2).

6. Circuit de la revendication 4, dans lequel la première unité de détection de passage à zéro de courant (210) et la deuxième unité de détection de passage à zéro de courant (221) comprennent en outre des résistances de réinitialisation (R1, R3) et deux extrémités de la résistance de réinitialisation sont respectivement reliées aux deux extrémités de l'enroulement secondaire.

7. Système de circuit sans pont totem-pôle, comprenant : une première unité de bras de pont (10) et une deuxième unité de bras de pont (20),
dans lequel la première unité de bras de pont (10) et la deuxième unité de bras de pont (20) sont reliées en parallèle entre un premier point de liaison parallèle (1) et un deuxième point de liaison en parallèle (2), la première unité de bras de pont (10) comprend un premier commutateur (110) et un deuxième commutateur (120) reliés en série dans la même direction ; la deuxième unité de bras de pont (20) comprend un troisième commutateur (211) et un quatrième commutateur (220) reliés en série dans la même direction ; un bloc d'alimentation (Vin) et une bobine d'induction (L) sont reliés entre un premier point de liaison (4) entre le premier commutateur (110) et le deuxième commutateur (120) et un deuxième point de liaison (3) entre le troisième commutateur (211) et le quatrième commutateur (220), et la deuxième unité de bras de pont (20) comprend en outre :

une première unité de détection de passage à zéro de courant (210), une deuxième unité de détection de passage à zéro de courant (221) et un circuit de traitement de signal (230), où la première unité de détection de passage à zéro de courant (210) et le troisième commutateur (211) sont reliés en série entre le premier point de liaison parallèle (1) et le deuxième point de liaison (3); la deuxième unité de détection de passage à zéro de courant (221) et le quatrième commutateur (220) sont reliés en série entre le deuxième point de liaison parallèle (2) et le deuxième point de liaison (3) ; le circuit de traitement de signal (230) est relié à la première unité de détection de passage à zéro de courant (210) et à la deuxième unité de détection de passage à zéro de courant (221) ;
la première unité de détection de passage à zéro de courant (210) est configurée, lorsqu'une tension d'entrée CA se trouve dans un demi-cycle

positif et qu'une diode de corps du troisième commutateur (211) est passante, pour recueillir un courant circulant à travers le troisième commutateur (211) et pour obtenir un signal de passage à zéro de courant du courant circulant à travers le troisième commutateur (211) ;
la deuxième unité de détection de passage à zéro de courant (221) est configurée, lorsque la tension d'entrée CA se trouve dans un demi-cycle négatif et qu'une diode de corps du quatrième commutateur (220) est passante, pour recueillir un courant circulant à travers le quatrième commutateur (220) et pour obtenir un signal de passage à zéro de courant du courant circulant à travers le quatrième commutateur (220) ;
le circuit de traitement de signal (230) est configuré pour sélectionner le signal de passage à zéro de courant recueilli par la première unité de détection de passage à zéro de courant (210) lorsque la tension d'entrée CA se trouve dans le demi-cycle positif ; pour sélectionner le signal de passage à zéro de courant recueilli par la deuxième unité de détection de passage à zéro de courant (220) lorsque la tension d'entrée CA se trouve dans le demi-cycle négatif ; et
une unité de commande de commutation (30), reliée au circuit de traitement de signal (230) ainsi qu'au troisième commutateur (211) et au quatrième commutateur (220), et est configurée pour commander l'activation ou la désactivation du troisième commutateur (211) et du quatrième commutateur (220) en fonction d'un signal délivré en sortie par le circuit de traitement de signal (230),
dans lequel les structures de la première unité de détection de passage à zéro de courant (210) et de la deuxième unité de détection de passage à zéro de courant (221) comprennent respectivement un transformateur de courant (CT1, CT2), un premier commutateur d'échantillonnage (S11, S21), un deuxième commutateur d'échantillonnage (S12, S22), une résistance d'échantillonnage (R2, R4) et un comparateur (T1, T2), et le transformateur de courant (CT1, CT2) comprend un enroulement primaire et un enroulement secondaire ; où :

l'enroulement primaire est relié à un circuit de détection d'un courant traversant le circuit ;
deux extrémités de l'enroulement secondaire sont respectivement reliées à des électrodes de drain du premier commutateur d'échantillonnage (S11, S21) et du deuxième commutateur d'échantillonnage (S12, S22) ;
une électrode de source du premier commutateur d'échantillonnage (S11, S21) est reliée à une électrode de source du deuxième commutateur d'échantillonnage (S12, S22), et les électrodes de source sont reliées à la masse ;
deux extrémités de la résistance d'échantillonnage (R2, R4) sont respectivement reliées à l'électrode de drain et à l'électrode de source du deuxième commutateur d'échantillonnage (S12, S22) ; et
une extrémité d'entrée négative du comparateur (T1, T2) est reliée à l'électrode de drain du deuxième commutateur d'échantillonnage (S12, S22), et une extrémité d'entrée positive de celui-ci est reliée à une tension de référence,
caractérisé en ce qu'un courant circulant à travers le transformateur de courant (CT1, CT2) est échantillonné par l'intermédiaire du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4), et une énergie stockée dans le transformateur de courant (CT1, CT2) est réinitialisée par l'intermédiaire d'un condensateur parasite du premier commutateur d'échantillonnage (S11, S21) et de la résistance d'échantillonnage (R2, R4),
dans lequel une tension de la résistance d'échantillonnage (R2, R4) est comparée à la tension de référence du comparateur (T1, T2) et, lorsque la tension de la résistance d'échantillonnage (R2, R4) est inférieure à la tension de référence du comparateur (T1, T2), le comparateur (T1, T2) inverse et délivre en sortie un niveau élevé, ainsi le passage à zéro de courant est détecté.

8. Système de circuit de la revendication 7, dans lequel le circuit de traitement de signal (230) comprend : une première porte ET (Z1), une deuxième porte ET (Z2) et une porte OU (Z3), une extrémité d'entrée de la première porte ET (Z1) est reliée à une extrémité de sortie de la première unité de détection de passage à zéro de courant (210) et à un premier signal de fréquence de travail représentant une polarité de la tension d'entrée CA et délivré en sortie par l'unité de commande de commutation (30) ; une extrémité d'entrée de la deuxième porte ET (Z2) est reliée à une extrémité de sortie de la deuxième unité de détection de passage à zéro de courant (221) et à un deuxième signal de fréquence de travail représentant une polarité de la tension d'entrée CA et délivré en sortie par l'unité de commande de commutation (30) ; une extrémité d'entrée de la porte OU (Z3) est reliée à des extrémités de sortie de la première porte ET (Z1) et de la deuxième porte ET (Z2).

9. Système de circuit de la revendication 7, dans lequel

la première unité de détection de passage à zéro de courant (210) et la deuxième unité de détection de passage à zéro de courant (221) comprennent en outre des résistances de réinitialisation et deux extrémités de la résistance de réinitialisation (R1, R3) sont respectivement reliées aux deux extrémités de l'enroulement secondaire.

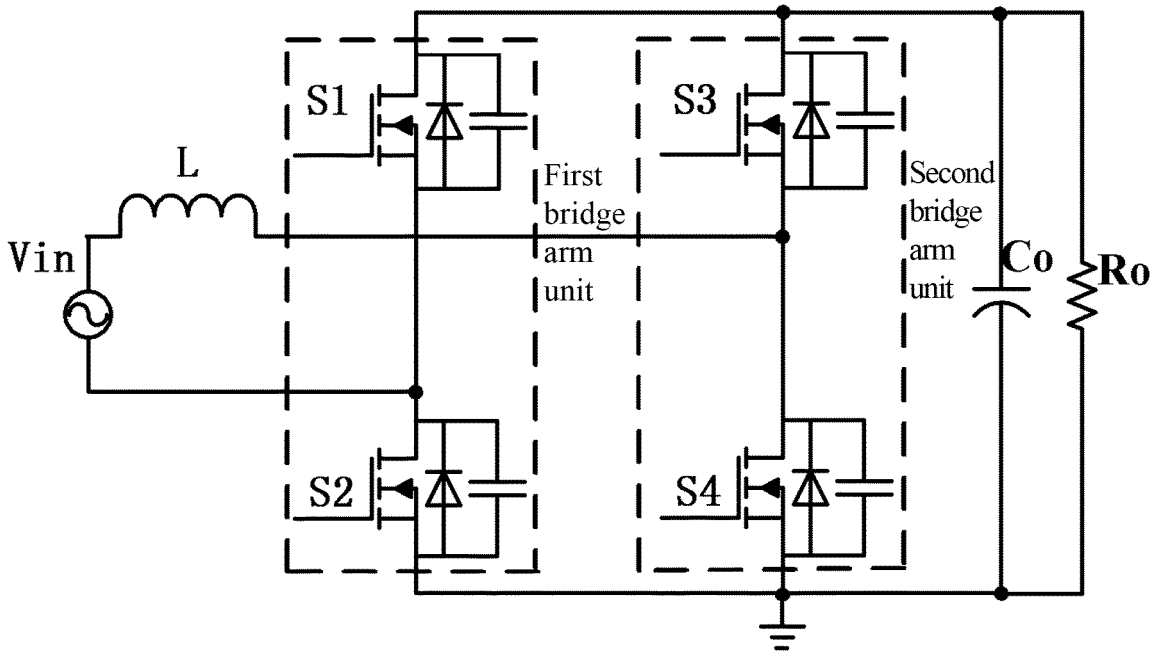

S1
S3
L
Vin
First bridge arm unit
Second bridge arm unit
Co
Ro
S2
S4

FIG. 1

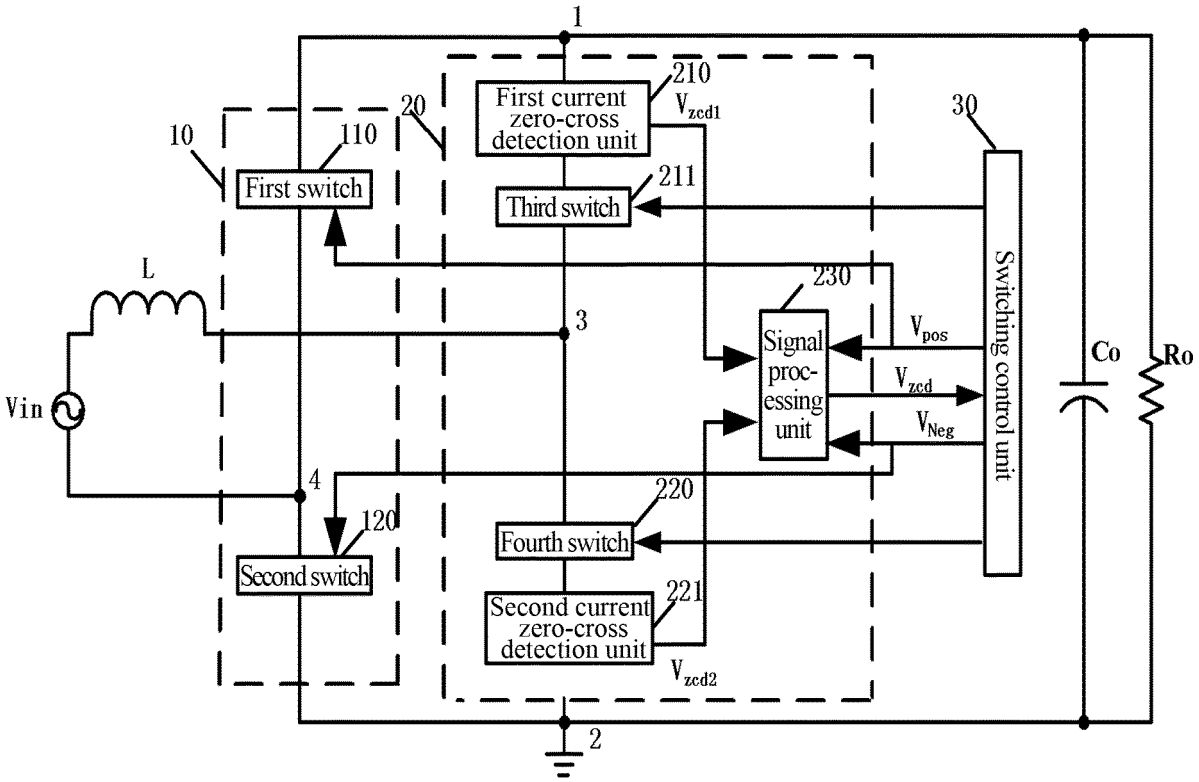

1
210
First current zero-cross detection unit
V_{zcd1}
20
30
10
110
First switch
211
Third switch
L
230
3
Signal proc-essing unit
V_{pos}
V_{zcd}
V_{Neg}
Switching control unit
Co
Ro
Vin
4
220
120
Fourth switch
Second switch
221
Second current zero-cross detection unit
V_{zcd2}
2

FIG. 2

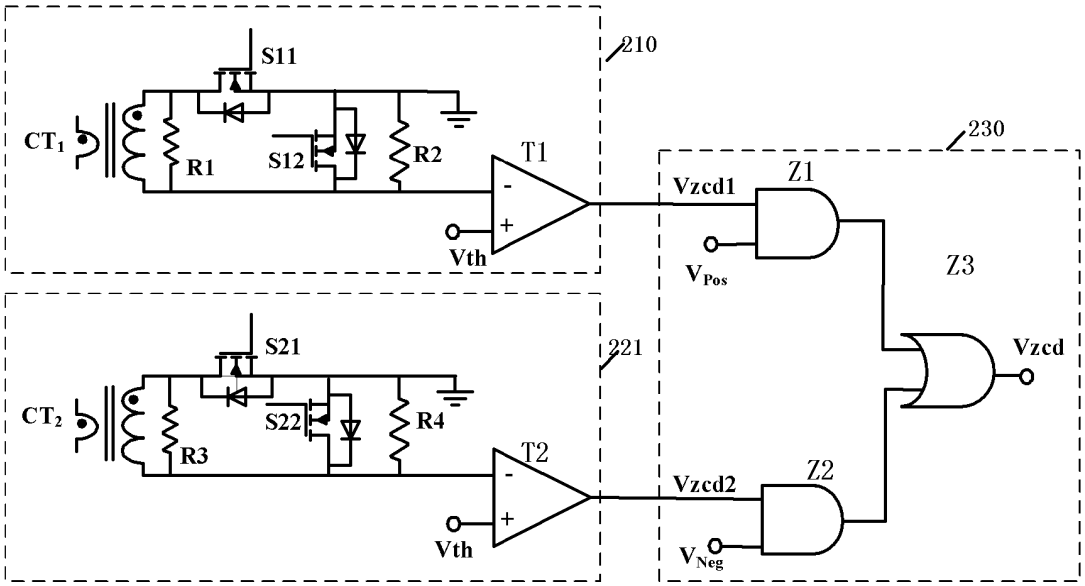
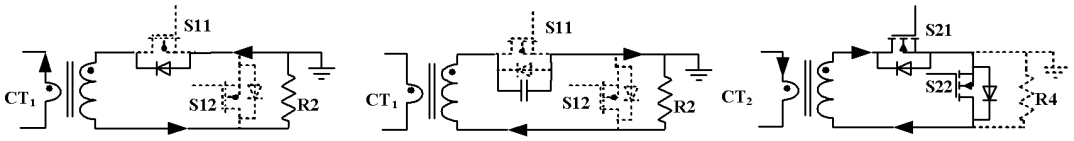
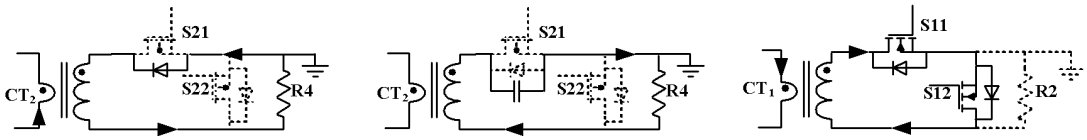


FIG. 3



4（a） 4（b） 4（c）

FIG. 4



5（a） 5（b） 5（c）

FIG. 5

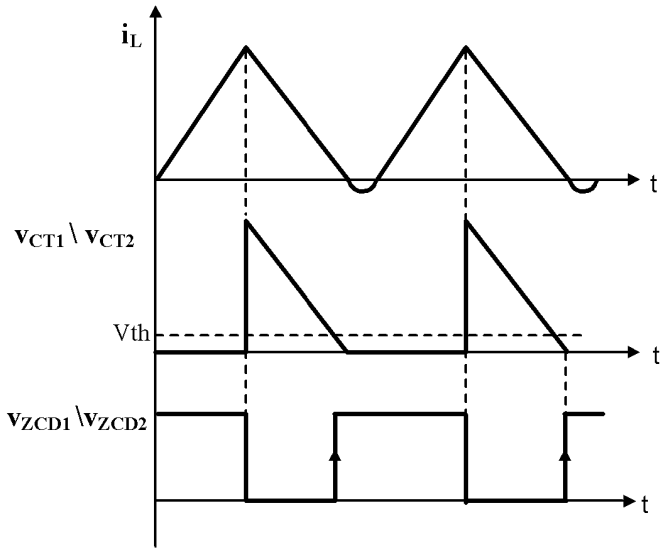


FIG. 6

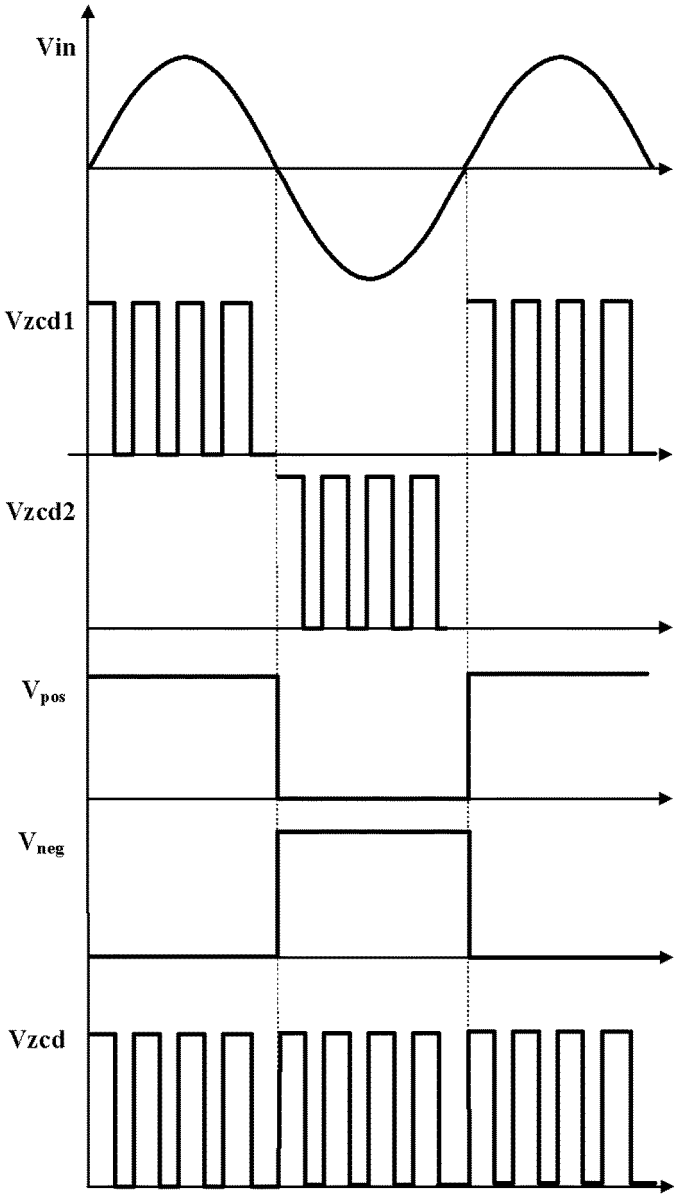


FIG. 7

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 101707441 A **[0005]**
- US 2012293141 A1 **[0006]**
- US 2003080723 A1 **[0007]**