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**(54) Voltage reference source and method for generating a reference voltage**

Spannungsreferenzquelle und Verfahren zur Erzeugung einer Referenzspannung

Source de tension de référence et un procédé permettant de générer une tension de référence

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## Description

**[0001]** The present invention is related to a voltage reference source and a method for generating a reference voltage.

**[0002]** Integrated circuits often comprise a voltage reference source which generates a reference voltage. The reference voltage can be a signal with a low temperature dependency. The reference voltage should be realized as a low noise voltage.

**[0003]** Document US 7,242,240 B1 describes a low noise bandgap circuit. The bandgap circuit comprises a plurality of cells. Each cell is formed of a plurality of bipolar transistors which form an amplifier. The amplifier generates a voltage that is proportional to the absolute temperature, abbreviated as PTAT. The plurality of cells is sequentially connected to add the voltages generated by each cell.

**[0004]** Document US 2014/0103900 A1 is related to a low-power reference generator circuit. A band-gap voltage generator comprises a circuit with two PMOS transistors and two NMOS transistors, a resistor coupled to said circuit, a reference output, a first and a second PMOS mirror transistor forming a current mirror and a series connection of a further resistor and a bipolar transistor. The circuit comprising the two PMOS transistors and the two NMOS transistors has a terminal connected to the resistor, a terminal connected to a reference potential terminal and two terminals connected to the first PMOS mirror transistor.

**[0005]** Document US 2006/0250178 A1 describes a low noise band-gap circuit. A cell comprises two cross-coupled transistors and two transistors arranged as a current mirror. An output voltage is tapped across a resistor that couples one of the cross-coupled transistors to a reference potential terminal.

**[0006]** Document US 2013/0106391 A1 refers to a low voltage, low power bandgap circuit comprising an operational amplifier that receives inputs from a current mirror.

**[0007]** It is an object of the present application to provide a voltage reference source and a method for generating a reference voltage with low power consumption.

**[0008]** This object is solved by a voltage reference source and a method for generating a reference voltage according to the independent claims. Preferred embodiments are presented in the respective dependent claims.

**[0009]** In an embodiment, a voltage reference source comprises a source block and a first resistor that comprises a first terminal coupled to a first terminal of the source block. A reference output of the voltage reference source is designed for providing a reference voltage. Moreover, the voltage reference source comprises a first and a second mirror transistor forming a first current mirror. The first mirror transistor couples a second terminal of the source block to a supply voltage terminal and the second mirror transistor couples the reference output to the supply voltage terminal. Furthermore, the voltage reference source comprises a series connection of a second resistor and a diode. The series connection is arranged between the reference output and the first terminal of the first resistor such that a mirror current flows through the second mirror transistor and the series connection to the first terminal of the first resistor.

**[0010]** It is an advantage of the voltage reference source that a low number of current paths between the supply voltage terminal and the reference potential terminal are required. Thus, the power consumption is low. The first resistor has a high contribution to the noise of the reference voltage. The noise of the resistor increases with its resistance value. Since the mirror current is fed back to the first resistor, the value of the first resistor can be small resulting in a low output noise of the reference voltage.

**[0011]** In an embodiment, the first resistor comprises a second terminal coupled to a reference potential terminal.

**[0012]** In an embodiment, the first and the second mirror transistor are both implemented as field-effect transistors or are both implemented as bipolar transistors. The first and the second mirror transistor are of the same transistor type. The first and the second mirror transistor may differ only in their current driving capability.

**[0013]** In an embodiment, a current driving capability of the second mirror transistor is the P-fold of a current driving capability of the first mirror transistor. The factor P is larger than 1. Thus, the mirror current is the P-fold of a second signal.

**[0014]** In an embodiment, a control terminal of the first mirror transistor is directly connected to a control terminal of the second mirror transistor. The control terminal of the first mirror transistor may be directly connected to a first terminal of the first mirror transistor. The first terminal of the first mirror transistor may be directly connected to the second terminal of the source block. The first terminal of the second mirror transistor may be directly connected to the reference output. Each second terminal of the first and the second mirror transistor may be directly connected to the supply voltage terminal.

**[0015]** In an embodiment, the reference voltage is a constant voltage. The reference voltage may have a low temperature coefficient. Preferably, the reference voltage may have a very low temperature dependency. The mirror current may be realized as a current proportional to the absolute temperature, abbreviated IPTAT. The flow of the mirror current through the second resistor may generate a voltage with positive temperature coefficient which compensates the negative temperature coefficient of the voltage generated by the flow of the mirror current through the diode.

**[0016]** In an embodiment, the reference voltage has a predetermined temperature coefficient. The coefficient may be non-zero. The coefficient may be positive or negative. The coefficient mainly may be a function of the resistance value of the second resistor.

**[0017]** In an embodiment, the source block provides a first signal at the first terminal that is implemented as a voltage.

The first signal may be realized as a voltage proportional to the absolute temperature. Thus, the first signal is a voltage that drops across the first resistor. The first signal is the voltage between the first terminal of the first resistor and the second terminal of the first resistor.

**[0018]** In an embodiment, the source block provides the second signal at the second terminal that is implemented as a current and flows through the second terminal of the source block. The current may be proportional to the absolute temperature. The second signal is realized as a current that is mirrored by the first current mirror into the mirror current. Thus, the current which flows through the series connection of the second resistor and the diode to the first terminal of the first resistor depends on the second signal.

**[0019]** In an embodiment, the second signal that is implemented as a current not only flows through the second terminal of the source block but also through the first terminal of the source block.

**[0020]** In an embodiment, the source block comprises a first current path between the first and the second terminal of the source block. The second signal may flow through the first current path.

**[0021]** In an embodiment, the source block comprises a third terminal that is coupled to the reference potential terminal. The source block may comprise a second current path between the third and the second terminal of the source block.

**[0022]** In an embodiment, the source block comprises a fourth terminal that is coupled to the supply voltage terminal. The source block may comprise a second current path between the third and the fourth terminal of the source block.

**[0023]** In an embodiment, the voltage reference source comprises a current source which couples the fourth terminal of the source block to the supply voltage terminal.

**[0024]** In an embodiment, the current source is realized by a source resistor. The current source may be implemented without a transistor. Thus, the current source consists of only one circuit part. The current source may require only a low area on a semiconductor body that comprises the voltage reference source.

**[0025]** In an alternative embodiment, the current source comprises a source transistor. The current source may be implemented by a circuit comprising the source transistor and the source resistor. The source transistor and the source resistor may be serially connected between the supply voltage terminal and the fourth terminal of the source block. Thus, the current source is able to reduce influence of fluctuations in a supply voltage provided at the supply voltage terminal.

**[0026]** In an embodiment, the source block comprises a cross coupled transistor pair.

**[0027]** In an embodiment, the source block comprises the cross coupled transistor pair and a second current mirror.

**[0028]** In an embodiment, the source block comprises a first and a second transistor that are cross coupled. The cross coupled transistor pair is realized by the first and the second transistor. The first transistor is arranged between the first terminal of the source block and the second terminal of the source block. The second transistor is arranged between the third terminal of the source block and the fourth terminal of the source block. Each of the first and the second transistor has a first terminal, a second terminal and a control terminal. The first and the second transistor are cross-coupled by a connection of the first terminal of the first transistor to the control terminal of the second transistor and correspondingly by a connection of the first terminal of the second transistor to the control terminal of the first transistor.

**[0029]** In an embodiment, the first and the second transistor are realized as bipolar transistors. The first and the second transistor may be implemented as npn bipolar transistors. Thus, the first terminals of the first and the second transistor are realized as collector and the second terminals of the first and the second transistor are implemented as emitter. The control terminals of the first and the second transistor are implemented as base. The collector of the first transistor may be connected to the base of the second transistor and the collector of the second transistor may be connected to the base of the first transistor.

**[0030]** In an embodiment, a current driving capability of the first transistor is the N-fold of a current driving capability of the second transistor. The factor N may be larger than 1.

**[0031]** In an embodiment, the source block comprises a third and a fourth mirror transistor. The second current mirror is realized by the third and the fourth mirror transistor. The third mirror transistor is arranged in series to the first transistor and the fourth mirror transistor is arranged in series to the second transistor. Thus, a controlled section of the first transistor and a controlled section of the third mirror transistor are arranged in series and couple the second terminal of the source block to the first terminal of the source block. Similarly, a controlled section of the second transistor and a controlled section of the fourth mirror transistor are connected in series and couple the fourth terminal of the source block to the third terminal of the source block.

**[0032]** In an embodiment, the first transistor is connected to the first terminal of the source block and the third mirror transistor is connected to the second terminal of the source block. Moreover, the second transistor is connected to the third terminal of the source block, whereas the fourth mirror transistor is connected to the fourth terminal of the source block. The third and the fourth mirror transistor each have a first terminal, a second terminal and a control terminal. The control terminal of the third mirror transistor is connected to the control terminal of the fourth mirror transistor. Moreover, the control terminal of the fourth mirror transistor may be connected to the first terminal of the fourth mirror transistor.

**[0033]** In an embodiment, the third and the fourth mirror transistor are implemented as bipolar transistors. The third and the fourth mirror transistor may be realized as npn-bipolar transistors. Each of the third and the fourth mirror transistor has an emitter, a collector and a base. A base of the fourth mirror transistor is connected to a base of the third mirror

transistor. The base of the fourth mirror transistor may be connected to an emitter of the fourth mirror transistor or an emitter of the third mirror transistor.

**[0034]** In an embodiment, a current driving capability of the fourth mirror transistor is the M-fold of a current driving capability of the third mirror transistor. The factor M may be larger than 1.

**[0035]** In an embodiment, the current source provides a source current. The source current flows through the second current path that is the series connection of the second transistor and the fourth mirror transistor. Thus, the source block is supplied by the current source and the first mirror transistor. The source block may exclusively be supplied by the current source and the first mirror transistor. The voltage reference source may have only two DC current paths between the supply voltage terminal and the source block which are implemented by the current source and the first mirror transistor. The voltage reference source may be free of a third DC current path between the supply voltage terminal and the source block.

**[0036]** In an embodiment, the voltage reference source comprises a capacitor that is arranged between the second terminal of the source block and the supply voltage terminal. The capacitor reduces variations of a voltage across the first and the second terminal of the first mirror transistor. Thus, a current flowing through the first mirror transistor and, consequently, the mirror current is stabilized by means of the capacitor. The mirror current has a larger value in comparison to the current flowing through the first terminal of the source block. A voltage drop across the first resistor is mainly caused by the mirror current. Thus, the reference voltage is stabilized by means of the capacitor.

**[0037]** In an embodiment, the source block comprises a first series circuit comprising a first diode and a first series transistor and connecting the first terminal of the source block to the second terminal of the source block.

**[0038]** In a further development, the source block comprises a second series circuit comprising a second diode and a second series transistor and connecting the third terminal of the source block to the second terminal of the source block. The first and the second diode are connected to the first and to the third terminal of the source block. The first and the second series transistor are connected to the second terminal of the source block. The first and the second series transistor are realized as field-effect transistors.

**[0039]** In an embodiment, the source block comprises an amplifier coupled on its input side to a node between the first diode and the first series transistor and to a node between the second diode and the second series transistor. The amplifier is coupled on its output side to a control terminal of the first series transistor and to a control terminal of the second series transistor. Thus, the supply voltage terminal may be connected twice to the source block, namely via the first mirror transistor and via a connection of the supply voltage terminal to a supply input of the amplifier.

**[0040]** In an embodiment, the voltage reference source is realized as a low noise voltage reference based on a cross-coupled quad of bipolar transistors. The cross-coupled quad of bipolar transistors comprises the second current mirror and the cross coupled transistor pair. It has an improved noise performance for the same supply current when compared with another Bandgap architecture. Another name for the cross-coupled quad is translinear loop, abbreviated as TL.

**[0041]** In an embodiment, a method for generating a reference voltage comprises providing a first signal at a first terminal of a source block. The first terminal of the source block is coupled to a first terminal of a first resistor. Moreover, a second signal that is implemented as a current is provided at a second terminal of a source block. The second signal is mirrored into a mirror current by a first current mirror comprising a first and a second mirror transistor. The first mirror transistor couples the second terminal of the source block to a supply voltage terminal and the second mirror transistor couples a reference output to the supply voltage terminal. Furthermore, the mirror current is provided via a series connection of a second resistor and a diode to the first terminal of the first resistor. The reference voltage is provided at the reference output.

**[0042]** Advantageously, only a small number of current paths and devices is required for generating the reference voltage. Thus, a power consumption is kept low. The reference voltage is generated with a low noise, since a small value of the resistance of the first resistor can be selected.

**[0043]** The following description of figures of exemplary embodiments may further illustrate and explain the invention. Circuit parts, devices and circuit blocks with the same structure and the same effect, respectively, appear with equivalent reference symbols. In so far as circuit parts, devices or circuit blocks correspond to one another in terms of their function in different figures, the description thereof is not repeated for each of the following figures.

Figures 1, 2, 3A, 3B, and 4 show exemplary embodiments of a voltage reference source.

Figures 5A and 5B show exemplary embodiments of a diode of the voltage reference source.

Figure 6 shows an exemplary characteristic of a current flowing in a voltage reference source.

**[0044]** Figure 1 shows an exemplary embodiment of a voltage reference source 10 comprising a first and a second mirror transistor 11, 12 which form a first current mirror 13. Moreover, the voltage reference source 10 comprises a supply voltage terminal 14 and a reference output 15. The first current mirror 13 couples the supply voltage terminal 14

to the reference output 15. A controlled section of the second mirror transistor 12 is arranged between the supply voltage terminal 14 and the reference output 15.

**[0045]** Moreover, the voltage reference source 10 comprises a first resistor 16 having a first and a second terminal. The voltage reference source 10 comprises a series connection 17 of a second resistor 18 and a diode 19. The series connection 17 is connected on the one side to the reference output 15 and on the other side to the first terminal of the first resistor 16. The second terminal of the first resistor 16 is directly connected to a reference potential terminal 20. The diode 19 is connected to the reference output 15, whereas the second resistor 18 is connected to the first terminal of the first resistor 16.

**[0046]** Furthermore, the voltage reference source 10 comprises a source block 21 having a first and a second terminal 22, 23. The first terminal 22 of the source block 21 is connected to the first terminal of the first resistor 16. The second terminal 23 of the source block 21 is connected to the first current mirror 13. Thus, a controlled section of the first mirror transistor 11 is arranged between the supply voltage terminal 14 and the second terminal 23 of the source block 21. Additionally, the source block 21 comprises a third terminal 24 that is connected to the reference potential terminal 20. A fourth terminal 25 of the source block 21 is coupled to the supply voltage terminal 14.

**[0047]** A control terminal of the first mirror transistor 11 is connected to a control terminal of the second mirror transistor 12. The first and the second mirror transistor 11, 12 are implemented as field-effect transistors. The first and the second mirror transistor 11, 12 may be realized as p-channel metal-oxide-semiconductor field-effect transistors. The control terminal of the first mirror transistor 11 is connected to a first terminal of the first mirror transistor 11 and thus to the second terminal 23 of the source block 21.

**[0048]** A first signal S1 is provided at the first terminal 22 of the source block 21. A second signal S2 is provided at the second terminal 23 of the source block 21. The first signal S1 is realized as a voltage. The voltage is implemented as a voltage proportional to the absolute temperature, abbreviated VPTAT. The first signal S1 drops across the first resistor 16.

**[0049]** The second signal S2 is implemented as a current. The second signal S2 may be realized as a current proportional to the absolute temperature, abbreviated IPTAT. The second signal S2 is mirrored by the first current mirror 13 into a mirror current S3. A current driving capability of the second mirror transistor 12 is a P-fold of a current driving capability of the first mirror transistor 11. The factor P may be larger than 1. The factor P may be also named current mirror ratio of the first current mirror 13. Thus, the mirror current S3 can be calculated by means of the following equation:

$$S3 = S2 \cdot P,$$

wherein S2 is the second signal that is realized as a current. The mirror current S3 flows through the series connection 17. Thus, the mirror current S3 and an output current S4 flowing through the first terminal 22 of the source block 21 flow through the first resistor 16 to the reference potential terminal 20. A resistor current S5 can be calculated according to the following equation:

$$S5 = S3 + S4 = P \cdot S2 + S4$$

**[0050]** The resistor current S5 is also a current proportional to the absolute temperature, abbreviated IPTAT. The first signal S1 can be calculated according to the following equation:

$$S1 = R1 \cdot S5 = (S4 + P \cdot S2) \cdot R1$$

**[0051]** A reference voltage S6 can be tapped at the reference output 15. The reference voltage S6 drops across the series circuit of the series connection 17 and the first resistor 16. A supply voltage VDD is applied to the supply voltage terminal 14.

**[0052]** The diode 19 may be fabricated as a single pn-junction. Alternatively, the diode 19 may be realized as a bipolar transistor 60 as shown in Figures 5A and 5B. The diode 19 may be realized by using a pn-junction of the bipolar transistor 60.

**[0053]** In an alternative embodiment, not shown, the diode 19 is connected to the first terminal of the first resistor 16, whereas the second resistor 18 is connected to the reference output 15.

**[0054]** In an alternative embodiment, not shown, the first and the second mirror transistor 11, 12 are implemented as bipolar transistors.

**[0055]** Figure 2 shows an alternative embodiment of the voltage reference source 10 which is a further development

of the embodiment shown in Figure 1 and merely serves an illustrative purpose. The source block 21 comprises a first and a second series circuit 30, 31. The first series circuit 30 connects the second terminal 23 of the source block 21 to the first terminal 22 of the source block 21. The second series circuit 31 connects the second terminal 23 of the source block 21 to the third terminal 24 of the source block 21. The first series circuit 30 comprises a first diode 32 and a first series transistor 33. The first series transistor 33 is connected to the second terminal 23 of the source block 21, whereas the first diode 32 is connected to the first terminal 22 of the source block 21. Correspondingly, the second series circuit 31 comprises a second diode 34 and a second series transistor 35. Whereas the second series transistor 35 is connected to the second terminal 23 of the source block 21, the second diode 34 is connected to the third terminal 24 of the source block 21.

**[0056]** Moreover, the source block 21 comprises an amplifier 36 having a first and a second input. The first input of the amplifier 36 is coupled to a node between the first diode 32 and the first series transistor 33. Similarly, the second input of the amplifier 36 is connected to a node between the second diode 34 and the second series transistor 35. The first input is realized as a non-inverting input and the second input is realized as an inverting input of the amplifier 36. An output of the amplifier 36 is connected to a control terminal of the first series transistor 33 and to a control terminal of the second series transistor 35. A supply input of the amplifier 36 is coupled via the fourth terminal 25 of the source block 21 to the supply voltage terminal 14. The first and the second series transistor 33, 35 are realized as field-effect transistors. Both transistors 33, 35 may be implemented as p-channel metal-oxide-semiconductor field-effect transistors. **[0057]** In an alternative embodiment, not shown, the first and the second series transistor 33, 35 are realized as bipolar transistors.

**[0058]** Figure 3A shows an alternative exemplary embodiment of the voltage reference source 10 which is a further development of the embodiments shown in Figures 1 and 2. The voltage reference source 10 comprises a capacitor 40 that is coupled to the first current mirror 13. The capacitor 40 connects a first terminal of the first mirror transistor 11 to a second terminal of the first mirror transistor 11. Thus, the capacitor 40 stabilizes a voltage across the controlled section of the first mirror transistor 11. Consequently, the capacitor 40 stabilizes the second signal S2 that flows as a current through the first mirror transistor 11 and, therefore, also the mirror current S3 flowing through the second mirror transistor 12.

**[0059]** Additionally, the voltage reference source 10 comprises a current source 41. The current source 41 is arranged between the fourth terminal 25 of the source block 21 and the supply voltage terminal 14. The current source 41 may be realized by a not shown source resistor 50.

**[0060]** The source block 21 is implemented as a cross coupled quad. Quad means that the source block 21 comprises four transistors 42 - 45. The source block 21 may not comprise more transistors than four transistors. The source block 21 may be implemented as a cross coupled quad of bipolar transistors 42 - 45. The source block 21 comprises the first and the second series circuit 30, 31. The first series circuit 30 is arranged between the second terminal 23 and the first terminal 22 of the source block 21. The second series circuit 31 is arranged between the fourth terminal 25 and the third terminal 24 of the source block 21. The source block 21 comprises a first and a second transistor 42, 43 that are cross-coupled. The first and the second transistor 42, 43 form a cross coupled transistor pair 46. The first series circuit 30 comprises the first transistor 42, whereas the second series circuit 31 comprises the second transistor 43. A control terminal of the first transistor 42 is connected to a first terminal of the second transistor 43. Correspondingly, a control terminal of the second transistor 43 is connected to a first terminal of the first transistor 42.

**[0061]** Moreover, the source block 21 comprises a third and a fourth mirror transistor 44, 45 forming a second current mirror 47. The third mirror transistor 44 is comprised by the first series circuit 30, whereas the fourth mirror transistor 45 is comprised by the second series circuit 31. The first transistor 42 is connected to the first terminal 22 of the source block 21, whereas the third mirror transistor 44 is connected to the second terminal 23 of the source block 21. Correspondingly, the second transistor 43 is connected to the third terminal 24 of the source block 21, whereas the fourth mirror transistor 45 is connected to the fourth terminal 25 of the source block 21. A control terminal of the third mirror transistor 44 is connected to a control terminal of the fourth mirror transistor 45. The control terminal of the fourth mirror transistor 45 is also connected to a first terminal of the fourth mirror transistor 45 and thus to the fourth terminal 25 of the source block 21.

**[0062]** The first and the second transistor 42, 43 and the third and the fourth mirror transistor 44, 45 are implemented as bipolar transistors. Said four transistors 42 - 45 may be implemented as npn bipolar transistors.

**[0063]** In an alternative, not shown, embodiment, the first and the second transistor 42, 43 and/or the third and the fourth mirror transistor 44, 45 are implemented as field-effect transistors.

**[0064]** Figure 3B shows an alternative embodiment of the voltage reference source 10 which is a further development of the embodiments shown in Figures 1, 2 and 3A. The capacitor 40 as shown in Figure 3A is omitted. Thus, the capacitor 40 is an optional device of the voltage reference source 10.

**[0065]** The current source 41 comprises the source resistor 50 that is arranged between the fourth terminal 25 of the source block 21 and the supply voltage terminal 14. Moreover, the current source 41 comprises a source transistor 51 that is arranged in series to the source resistor 50. Moreover, the current source 41 comprises a current path 52 that

couples the supply voltage terminal 14 to the reference potential terminal 20. A node of the current path 52 is connected to a control terminal of the source transistor 51. The source transistor 51 is connected to the fourth terminal 25 of the source block 21 and the source resistor 50 is connected to the supply voltage terminal 14.

**[0066]** The current path 52 comprises a further source resistor 53 and a further source transistor 54 that are connected in series. The further source transistor 54 is connected to the supply voltage terminal 14, whereas the further source resistor 53 is connected to the reference potential terminal 20. A node between the further source resistor 53 and the further source transistor 54 is connected to the control terminal of the source transistor 51. A node between the controlled section of the source transistor 51 and the source resistor 50 is connected to a control terminal of the further source transistor 54. Thus, the current source 41 is implemented with a small number of devices. The current source 41 increases the power supply rejection ratio. The current source 41 may be implemented also by other current source circuits.

**[0067]** Furthermore, the voltage reference source 10 comprises a buffer 55 that is connected on its input side to the reference output 15. At an output of the buffer 55, a buffered reference voltage S8 is provided.

**[0068]** The voltage reference source 10 uses a cross-coupled quad of bipolar transistors 42 - 45 for generating the first signal S1. The first signal S1 is a PTAT voltage across the first resistor 16. Contrary to the voltage reference source 10 shown in Figure 4, the branch with the diode 19 and the second resistor 18 is not connected to the reference potential terminal 20, said branch is fed back to the first resistor 16. A current signal S7 that is a current I1 through the second series circuit 31 of the transistors 43, 45 is generated by the current source 41. The current source 41 as shown in Figure 3B performs an improved power supply rejection.

**[0069]** In the following equations, the base currents of the transistors 42 - 45 are neglected because it is assumed that the current gain  $\beta$  of these transistors 42 - 45 is large ( $\beta \gg 1$ ):

$$V_{BE45} + V_{BE42} + V_{R1} = V_{BE44} + V_{BE43}$$

$$V_T \cdot \ln\left(\frac{I_1}{M \cdot I_S}\right) + V_T \cdot \ln\left(\frac{I_2}{N \cdot I_S}\right) + R_1 \cdot I_2 \cdot (1 + P) = V_T \cdot \ln\left(\frac{I_2}{I_S}\right) + V_T \cdot \ln\left(\frac{I_1}{I_S}\right)$$

$$I_2 = \frac{V_T}{(1 + P) \cdot R_1} \cdot \ln(M \cdot N) \quad (= \text{PTAT current})$$

wherein VBE45 is a base-emitter voltage of the fourth mirror transistor 45, VBE42 is a base-emitter voltage of the first transistor 42, VR1 is a voltage value of the first signal S1, VBE44 is a base-emitter voltage of the third mirror transistor 44, VBE43 is a base-emitter voltage of the second transistor 43, VT is a thermal voltage, I1 is a value of the current signal S7 flowing through the second transistor 43, M is a factor, IS is a reverse bias saturation current, N is a factor, R1 is a resistance value of the first resistor 16 and P is a factor. The voltage value VR1 of the first signal S1 is equal to the voltage drop across the first resistor 16. I2 is a current value of the second signal S2 flowing through the second terminal 23 of the source block 21 and is also equal to the output current S4 flowing through the first terminal 22 of the source block 21.

**[0070]** The factor M is defined such that a current driving capability of the fourth mirror transistor 45 is the M-fold of a current driving capability of the third mirror transistor 44. The factor M may be also named current mirror ratio of the second current mirror 47. The factor M may be larger than 1. The factor N is defined such that a current driving capability of the first transistor 42 is the N-fold of a current driving capability of the second transistor 43. The factor N may be larger than 1. The factor N may be also named cross coupled transistor ratio.

**[0071]** The reference voltage S6 that is also named Bandgap voltage VBG can be calculated as

$$S6 = V_{BG} = V_D + V_{R2} + V_{R1}$$

$$S6 = V_{BG} = V_D + P \cdot I_2 \cdot R_2 + (P + 1) \cdot I_2 \cdot R_1$$

$$S6 = V_{BG} = V_D + V_T \cdot \ln(M \cdot N) \cdot \left(1 + \frac{P}{P + 1} \cdot \frac{R_2}{R_1}\right)$$

wherein VD is a diode forward voltage of the diode 19, VR2 is a voltage drop across the second resistor 18 and R2 is a resistance value of the second resistor 18.

**[0072]** In the voltage reference source 10, the output branch comprising the diode 19 and the second resistor 18 is fed back into a node between the first resistor 16 and the first transistor 42. The mirror current S3 that is realized as a fed back current is a multiple of the collector current of the third mirror transistor 44 (current mirror ratio P).

**[0073]** In the voltage reference source 10, the noise gain for the noise from the first resistor 16 is the same as in the circuit shown in Figure 4, if the current mirror ratio P is large. But due to the mirror current S3, the value of the first resistor 16 can be smaller especially for the same supply current and, therefore, the output noise of the reference voltage S6 is lower.

**[0074]** The source block 21 is realized as the cross coupled quad and is designed for generation of the second signal S2 that is a PTAT current. By connecting the series connection 17 to the first terminal of the first resistor 16, a feedback of the output branch of the voltage reference source 10 is realized.

**[0075]** Figure 4 shows an alternative embodiment of the voltage reference source 10 which is a further development of the embodiments shown in Figures 1, 2, 3A and 3B and merely serves an illustrative purpose. The current source 51 is implemented by the source resistor 50. Thus, the current source 51 is free of any transistor. The series connection 17 is arranged between the reference output 15 and the reference potential terminal 20. Thus, the series connection 17 does not couple the reference output 15 to the first terminal of the first resistor 16. Consequently, the mirror current S3 flows through the series connection 17 directly to the reference potential terminal 20. The diode 19 is connected to the reference potential terminal 20, whereas the second resistor 18 is connected to the reference output 15.

**[0076]** In an alternative embodiment, not shown, the diode 19 is connected to the reference output 15 and the second resistor 18 is connected to the reference potential terminal 20.

**[0077]** The voltage reference source 10, as shown in Figures 3A, 3B and 4, is implemented as a Bandgap circuit. The voltage reference source 10 uses a cross-coupled quad of bipolar transistors 42-45 for generating a PTAT voltage across the first resistor 16. Another name for the cross-coupled quad is translinear loop TL. The cross-coupled quad is used for a PTAT current generator. Used in a Bandgap circuit, the PTAT current is mirrored into the output branch that comprises the diode 19 and the second resistor 18 by the first current mirror 13. The mirror current S3 realized as PTAT current through the second resistor 18 generates a voltage with positive temperature coefficient for compensating the negative temperature coefficient of the diode 19.

**[0078]** The voltage reference source 10 implemented as a Bandgap and based on the cross-coupled quad has the following properties: No startup circuit is needed. The voltage reference source 10 only has a single stable operating point and is free of a startup circuit. Moreover, the first signal S1 that is a PTAT voltage is large due to the stacked transistor arrangement:  $S1 = V_{PTAT} = V_T \cdot \ln(M \cdot N)$ . The voltage reference source 10 as shown in one of the Figures above multiplies the PTAT voltage.

**[0079]** Figures 5A and 5B show exemplary embodiments of the diode 19. The diode 19 is implemented by a bipolar transistor 60. As shown in Figure 5A, the diode 19 is realized by an npn-bipolar transistor. The base and the collector of the bipolar transistor 60 are connected together. Thus, the diode 19 is formed by the base-emitter junction of the bipolar transistor 60.

**[0080]** As shown in Figure 5B, the diode 19 is realized by a pnp-bipolar transistor. The base of the bipolar transistor 60 is connected to the collector of the bipolar transistor 60. Thus, the diode 19 is formed by the base-collector junction of the bipolar transistor 60.

**[0081]** Figure 6 shows an exemplary characteristic of the voltage reference source 10. A base noise current is shown depending on the frequency and the current value. As shown at the lower frequency values, a 1/f noise occurs. The flicker noise exponent AFN has a value of 1.8.

**[0082]** For good low frequency noise performance the current through the bipolar transistors 42 - 45 should be kept low due to their 1/f behavior. In Figure 6, the noise of the base current of an npn transistor is depicted. The white noise current only increases with the square root of the emitter current, while the 1/f noise current increases almost proportional to the emitter current. For minimizing the 1/f noise, the current through the transistors 42, 44 of the first series circuit 30 should be kept small, while for good white noise performance the current through the first resistor 16 should be large, resulting in a small resistance value for the first resistor 16. This can be accomplished in the voltage reference source 10 as shown in Figures 1, 2, 3A and 3B by choosing a large current mirror ratio of the first current mirror 14 ( $P > 1$ ).

**[0083]** Further, the added feedback loop leads to the following improved circuit properties: the noise of the first transistor 42 and of the third mirror transistor 44 may be attenuated. The noise of the third and the fourth mirror transistors 44, 45 may be attenuated. The noise of the first and the second mirror transistors 11, 12 may be attenuated. Therefore, the first to the fourth current mirror transistor 11, 12, 44, 45 can be kept small without increasing the 1/f noise level of the reference voltage S6.

**[0084]** The matching requirement of the first current mirror 13 may be reduced. Also the matching requirement of the second current mirror 47 may be reduced.

**[0085]** The reference output 15 at which the reference voltage S6 is tapped has a lower impedance.

**[0086]** First simulation runs of the voltage reference source 10 led to the following simulated noise values: White noise: 29nV/VHz and 1/f noise: 49nV/ $\sqrt{\text{Hz}}$  at a frequency  $f = 10 \text{ Hz}$ .

**[0087]** Advantageously, the voltage reference source 10 as shown in the Figures 3A, 3B and 4 implements a low noise voltage reference with cross-coupled quad bipolar transistors 42-45.

5

Reference Numerals

**[0088]**

|    |     |                               |
|----|-----|-------------------------------|
| 10 | 10  | voltage reference source      |
|    | 11  | first mirror transistor       |
|    | 12  | second mirror transistor      |
|    | 13  | first current mirror          |
|    | 14  | supply voltage terminal       |
| 15 | 15  | reference output              |
|    | 16  | first resistor                |
|    | 17  | series connection             |
|    | 18  | second resistor               |
|    | 19  | diode                         |
| 20 | 20  | reference potential terminal  |
|    | 21  | source block                  |
|    | 22  | first terminal                |
|    | 23  | second terminal               |
|    | 24  | third terminal                |
| 25 | 25  | fourth terminal               |
|    | 30  | first series circuit          |
|    | 31  | second series circuit         |
|    | 32  | first diode                   |
|    | 33  | first series transistor       |
| 30 | 34  | second diode                  |
|    | 35  | second series transistor      |
|    | 36  | amplifier                     |
|    | 40  | capacitor                     |
|    | 41  | current source                |
| 35 | 42  | first transistor              |
|    | 43  | second transistor             |
|    | 44  | third mirror transistor       |
|    | 45  | fourth mirror transistor      |
|    | 46  | cross coupled transistor pair |
| 40 | 47  | second current mirror         |
|    | 50  | source resistor               |
|    | 51  | source transistor             |
|    | 52  | current path                  |
|    | 53  | further source resistor       |
| 45 | 54  | further source transistor     |
|    | 55  | buffer                        |
|    | 60  | bipolar transistor            |
|    | S1  | first signal                  |
|    | S2  | second signal                 |
| 50 | S3  | mirror current                |
|    | S4  | output current                |
|    | S5  | resistor current              |
|    | S6  | reference voltage             |
|    | S7  | current signal                |
| 55 | S8  | buffered reference voltage    |
|    | VBE | base-emitter voltage          |
|    | VDD | supply voltage                |

## Claims

## 1. Voltage reference source, comprising:

- a source block (21),
- a first resistor (16) having a first terminal coupled to a first terminal (22) of the source block (21) and a second terminal coupled to a reference potential terminal (20),
- a reference output (15) for providing a reference voltage (S6),
- a first and a second mirror transistor (11, 12) forming a first current mirror (13), wherein the first mirror transistor (11) couples a second terminal (23) of the source block (21) to a supply voltage terminal (14) and the second mirror transistor (12) couples the reference output (15) to the supply voltage terminal (14), and
- a series connection (17) of a second resistor (18) and a diode (19) that is arranged between the reference output (15) and the first terminal of the first resistor (16) such that a mirror current (S3) flows through the second mirror transistor (12) and the series connection (17) to the first terminal of the first resistor (16),

wherein the source block (21) comprises a third terminal (24) that is coupled to the reference potential terminal (20), and

wherein the source block (21) comprises a first and a second transistor (42, 43) such that the first transistor (42) is arranged between the first terminal (22) of the source block (21) and the second terminal (23) of the source block (21) and the second transistor (43) is arranged between the third terminal (24) of the source block (21) and a fourth terminal (25) of the source block (21),

**characterized in**

**that** the fourth terminal (25) of the source block (21) is coupled to the supply voltage terminal (14), wherein the first and the second transistor (42, 43) of the source block (21) are cross coupled.

## 2. Voltage reference source according to claim 1,

wherein the source block (21) is configured to provide a first signal (S1) at the first terminal (22) of the source block (21) that is implemented as a voltage proportional to the absolute temperature.

## 3. Voltage reference source according to claim 1 or 2,

wherein the source block (21) is configured to provide a second signal (S2) at the second terminal (23) of the source block (21) that is implemented as a current proportional to the absolute temperature and flows through the second terminal (23) of the source block (21).

## 4. Voltage reference source according to one of claims 1 to 3,

wherein a current driving capability of the second mirror transistor (13) is the P-fold of a current driving capability of the first mirror transistor (12) and the factor P is larger than 1.

## 5. Voltage reference source according to one of claims 1 to 4,

wherein a control terminal of the first mirror transistor (11) is directly connected to a control terminal of the second mirror transistor (12).

## 6. Voltage reference source according to one of claims 1 to 5,

wherein the first and the second mirror transistor (11, 12) are both implemented as field-effect transistors or are both implemented as bipolar transistors.

## 7. Voltage reference source according to one of claims 1 to 6,

comprising a current source (41) which couples the fourth terminal (25) of the source block (21) to the supply voltage terminal (14).

## 8. Voltage reference source according to claim 7,

wherein the current source (41) comprises a source resistor (50) that is arranged between the fourth terminal (25) of the source block (21) and the supply voltage terminal (14).

## 9. Voltage reference source according to one of claims 1 to 8,

wherein a current driving capability of the first transistor (42) is the N-fold of a current driving capability of the second transistor (43) and the factor N is larger than 1.

10. Voltage reference source according to claim 8 or 9,  
wherein the source block (21) comprises a third and a fourth mirror transistor (44, 45) forming a second current mirror (47), as well as the third mirror transistor (44) is arranged in series to the first transistor (42) and the fourth mirror transistor (45) is arranged in series to the second transistor (43).

11. Voltage reference source according to claim 10,  
wherein a current driving capability of the fourth mirror transistor (45) is the M-fold of a current driving capability of the third mirror transistor (44) and the factor M is larger than 1.

12. Method for generating a reference voltage, comprising:

- providing a first signal (S1) at a first terminal (22) of a source block (21), wherein the first terminal (22) of the source block (21) is coupled to a first terminal of a first resistor (16) and a second terminal of the first resistor (16) is coupled to a reference potential terminal (20),
- providing a second signal (S2) implemented as a current at a second terminal (23) of the source block (21),
- mirroring the second signal (S2) into a mirror current (S3) by a first current mirror (13) comprising a first and a second mirror transistor (11, 12) such that the first mirror transistor (11) couples the second terminal (23) of the source block (21) to a supply voltage terminal (14) and the second mirror transistor (12) couples a reference output (15) to the supply voltage terminal (14),
- providing the mirror current (S3) via a series connection (17) of a second resistor (18) and a diode (19) to the first terminal of the first resistor (16), and
- providing the reference voltage (S6) at the reference output (15),

wherein the source block (21) comprises a third terminal (24) that is coupled to the reference potential terminal (20), and

wherein the source block (21) comprises a first and a second transistor (42, 43) such that the first transistor (42) is arranged between the first terminal (22) of the source block (21) and the second terminal (23) of the source block (21) and the second transistor (43) is arranged between the third terminal (24) of the source block (21) and a fourth terminal (25) of the source block (21),

**characterized in**

**that** the fourth terminal (25) of the source block (21) is coupled to the supply voltage terminal (14), wherein the first and the second transistor (42, 43) of the source block (21) are cross coupled.

## Patentansprüche

1. Spannungsreferenzquelle, umfassend:

- einen Quellenblock (21),
- einen ersten Widerstand (16) mit einem ersten Anschluss, der an einen ersten Anschluss (22) des Quellenblocks (21) angeschlossen ist, und einem zweiten Anschluss, der an einen Referenzpotentialanschluss (20) angeschlossen ist,
- einen Referenzausgang (15), um eine Referenzspannung (S6) bereitzustellen,
- einen ersten und einen zweiten Spiegeltransistor (11, 12), die einen ersten Stromspiegel (13) bilden, wobei der erste Spiegeltransistor (11) einen zweiten Anschluss (23) des Quellenblocks (21) an einen Versorgungsspannungsanschluss (14) anschließt, und der zweite Spiegeltransistor (12) den Referenzausgang (15) an den Versorgungsspannungsanschluss (14) anschließt, und
- eine Reihenschaltung (17) aus einem zweiten Widerstand (18) und einer Diode (19), die zwischen dem Referenzausgang (15) und dem ersten Anschluss des ersten Widerstands (16) derart angeordnet ist, dass ein Spiegelstrom (S3) durch den zweiten Spiegeltransistor (12) und die Reihenschaltung (17) zum ersten Anschluss des ersten Widerstands (16) fließt,

wobei der Quellenblock (21) einen dritten Anschluss (24) umfasst, der an den Referenzpotentialanschluss (20) angeschlossen ist, und

wobei der Quellenblock (21) einen ersten und einen zweiten Transistor (42, 43) derart umfasst, dass der erste Transistor (42) zwischen dem ersten Anschluss (22) des Quellenblocks (21) und dem zweiten Anschluss (23) des Quellenblocks (21) angeordnet ist, und der zweite Transistor (43) zwischen dem dritten Anschluss (24) des Quellenblocks (21) und einem vierten Anschluss (25) des Quellenblocks (21) angeordnet ist,

**dadurch gekennzeichnet,**

**dass** der vierte Anschluss (25) des Quellenblocks (21) an den Versorgungsspannungsanschluss (14) angeschlossen ist, wobei der erste und der zweite Transistor (42, 43) des Quellenblocks (21) kreuzgekoppelt sind.

- 5     **2.** Spannungsreferenzquelle nach Anspruch 1,  
wobei der Quellenblock (21) dazu konfiguriert ist, ein erstes Signal (S1) am ersten Anschluss (22) des Quellenblocks (21) bereitzustellen, das als Spannung implementiert ist, die proportional zur absoluten Temperatur ist.
- 10    **3.** Spannungsreferenzquelle nach Anspruch 1 oder 2,  
wobei der Quellenblock (21) dazu konfiguriert ist, ein zweites Signal (S2) am zweiten Anschluss (23) des Quellenblocks (21) bereitzustellen, das als Strom implementiert ist, der proportional zur absoluten Temperatur ist und durch den zweiten Anschluss (23) des Quellenblocks (21) fließt.
- 15    **4.** Spannungsreferenzquelle nach einem der Ansprüche 1 bis 3,  
wobei eine Stromantriebsfähigkeit des zweiten Spiegeltransistors (13) das P-fache einer Stromantriebsfähigkeit des ersten Spiegeltransistors (12) beträgt und der Faktor P größer als 1 ist.
- 20    **5.** Spannungsreferenzquelle nach einem der Ansprüche 1 bis 4,  
wobei ein Steueranschluss des ersten Spiegeltransistors (11) direkt mit einem Steueranschluss des zweiten Spiegeltransistors (12) verbunden ist.
- 25    **6.** Spannungsreferenzquelle nach einem der Ansprüche 1 bis 5,  
wobei der erste und der zweite Spiegeltransistor (11, 12) beide als Feldeffekttransistoren implementiert sind, oder beide als Bipolartransistoren implementiert sind.
- 30    **7.** Spannungsreferenzquelle nach einem der Ansprüche 1 bis 6, eine Stromquelle (41) umfassend, die den vierten Anschluss (25) des Quellenblocks (21) an den Versorgungsspannungsanschluss (14) anschließt.
- 35    **8.** Spannungsreferenzquelle nach Anspruch 7,  
wobei die Stromquelle (41) einen Quellenwiderstand (50) umfasst, der zwischen dem vierten Anschluss (25) des Quellenblocks (21) und dem Versorgungsspannungsanschluss (14) angeordnet ist.
- 40    **9.** Spannungsreferenzquelle nach einem der Ansprüche 1 bis 8,  
wobei eine Stromantriebsfähigkeit des ersten Transistors (42) das N-fache einer Stromantriebsfähigkeit des zweiten Transistors (43) beträgt und der Faktor N größer als 1 ist.
- 45    **10.** Spannungsreferenzquelle nach Anspruch 8 oder 9,  
wobei der Quellenblock (21) einen dritten und einen vierten Spiegeltransistor (44, 45) umfasst, die einen zweiten Stromspiegel (47) bilden, und der dritte Spiegeltransistor (44) in Reihe zum ersten Transistor (42) angeordnet ist, und der vierte Spiegeltransistor (45) in Reihe zum zweiten Transistor (43) angeordnet ist.
- 50    **11.** Spannungsreferenzquelle nach Anspruch 10,  
wobei eine Stromantriebsfähigkeit des vierten Spiegeltransistors (45) das M-fache einer Stromantriebsfähigkeit des dritten Spiegeltransistors (44) beträgt und der Faktor M größer als 1 ist.
- 55    **12.** Verfahren zum Generieren einer Referenzspannung, umfassend:
  - Bereitstellen eines ersten Signals (S1) an einem ersten Anschluss (22) eines Quellenblocks (21), wobei der erste Anschluss (22) des Quellenblocks (21) an einen ersten Anschluss eines ersten Widerstands (16) angeschlossen ist, und ein zweiter Anschluss des ersten Widerstands (16) an einen Referenzpotentialanschluss (20) angeschlossen ist,
  - Bereitstellen eines als Strom implementierten zweiten Signals (S2) an einem zweiten Anschluss (23) des Quellenblocks (21),
  - Spiegeln des zweiten Signals (S2) in einen Spiegelstrom (S3) durch einen ersten Stromspiegel (13), der einen ersten und einen zweiten Spiegeltransistor (11, 12) umfasst, und zwar derart, dass der erste Spiegeltransistor (11) den zweiten Anschluss (23) des Quellenblocks (21) an einen Versorgungsspannungsanschluss (14) anschließt, und der zweite Spiegeltransistor (12) einen Referenz Ausgang (15) an den Versorgungsspannungsanschluss (14) anschließt,

- Bereitstellen des Spiegelstroms (S3) über eine Reihenschaltung (17) aus einem zweiten Widerstand (18) und einer Diode (19) an den ersten Anschluss des ersten Widerstands (16), und
- Bereitstellen der Referenzspannung (S6) am Referenzausgang (15),

wobei der Quellenblock (21) einen dritten Anschluss (24) umfasst, der an den Referenzpotentialanschluss (20) angeschlossen ist, und

wobei der Quellenblock (21) einen ersten und einen zweiten Transistor (42, 43) derart umfasst, dass der erste Transistor (42) zwischen dem ersten Anschluss (22) des Quellenblocks (21) und dem zweiten Anschluss (23) des Quellenblocks (21) angeordnet ist, und der zweite Transistor (43) zwischen dem dritten Anschluss (24) des Quellenblocks (21) und einem vierten Anschluss (25) des Quellenblocks (21) angeordnet ist,

**dadurch gekennzeichnet,**

**dass** der vierte Anschluss (25) des Quellenblocks (21) an den Versorgungsspannungsanschluss (14) angeschlossen ist, wobei der erste und der zweite Transistor (42, 43) des Quellenblocks (21) kreuzgekoppelt sind.

## Revendications

### 1. Source de référence de tension, comprenant:

- un bloc de source (21),
- une première résistance (16) présentant une première borne couplée à une première borne (22) du bloc de source (21) et une deuxième borne couplée à une borne de potentiel de référence (20),
- une sortie de référence (15) destinée à fournir une tension de référence (S6),
- un premier et un deuxième transistor miroir (11, 12) formant un premier miroir de courant (13), sachant que le premier transistor miroir (11) couple une deuxième borne (23) du bloc de source (21) à une borne de tension d'alimentation (14) et le deuxième transistor miroir (12) couple la sortie de référence (15) à la borne de tension d'alimentation (14), et
- une connexion série (17) d'une deuxième résistance (18) et d'une diode (19) qui est agencée entre la sortie de référence (15) et la première borne de la première résistance (16) de telle sorte qu'un courant miroir (S3) passe par le deuxième transistor miroir (12) et la connexion série (17) vers la première borne de la première résistance (16),

sachant que le bloc de source (21) comprend une troisième borne (24) qui est couplée à la borne de potentiel de référence (20), et

sachant que le bloc de source (21) comprend un premier et un deuxième transistor (42, 43) de telle sorte que le premier transistor (42) soit agencé entre la première borne (22) du bloc de source (21) et la deuxième borne (23) du bloc de source (21) et le deuxième transistor (43) soit agencé entre la troisième borne (24) du bloc de source (21) et une quatrième borne (25) du bloc de source (21),

**caractérisée en ce que**

la quatrième borne (25) du bloc de source (21) est couplée à la borne de tension d'alimentation (14), sachant que le premier et le deuxième transistor (42, 43) du bloc de source (21) sont couplés de manière croisée.

### 2. Source de référence de tension selon la revendication 1,

sachant que le bloc de source (21) est configuré pour fournir au niveau de la première borne (22) du bloc de source (21) un premier signal (S1) qui est implémenté comme tension proportionnelle à la température absolue.

### 3. Source de référence de tension selon la revendication 1 ou 2,

sachant que le bloc de source (21) est configuré pour fournir au niveau de la deuxième borne (23) du bloc de source (21) un deuxième signal (S2) qui est implémenté comme courant proportionnel à la température absolue qui passe par la deuxième borne (23) du bloc de source (21).

### 4. Source de référence de tension selon l'une des revendications 1 à 3,

sachant qu'une capacité d'attaque en courant du deuxième transistor miroir (13) est égale à P fois une capacité d'attaque en courant du premier transistor miroir (12) et le facteur P est supérieur à 1.

### 5. Source de référence de tension selon l'une des revendications 1 à 4,

sachant qu'une borne de commande du premier transistor miroir (11) est directement connectée à une borne de commande du deuxième transistor miroir (12).

6. Source de référence de tension selon l'une des revendications 1 à 5, sachant que le premier et le deuxième transistor miroir (11, 12) sont tous deux implémentés comme transistors à effet de champ ou sont tous deux implémentés comme transistors bipolaires.

7. Source de référence de tension selon l'une des revendications 1 à 6, comprenant une source de courant (41) qui couple la quatrième borne (25) du bloc de source (21) à la borne de tension d'alimentation (14).

8. Source de référence de tension selon la revendication 7, sachant que la source de courant (41) comprend une résistance de source (50) qui est agencée entre la quatrième borne (25) du bloc de source (21) et la borne de tension d'alimentation (14).

9. Source de référence de tension selon l'une des revendications 1 à 8, sachant qu'une capacité d'attaque en courant du premier transistor (42) est égale à N fois une capacité d'attaque en courant du deuxième transistor (43) et le facteur N est supérieur à 1.

10. Source de référence de tension selon la revendication 8 ou 9, sachant que le bloc de source (21) comprend un troisième et un quatrième transistor miroir (44, 45) formant un deuxième miroir de courant (47), et sachant que le troisième transistor miroir (44) est agencé en série par rapport au premier transistor (42) et le quatrième transistor miroir (45) est agencé en série par rapport au deuxième transistor (43).

11. Source de référence de tension selon la revendication 10, sachant qu'une capacité d'attaque en courant du quatrième transistor miroir (45) est égale à M fois une capacité d'attaque en courant du troisième transistor miroir (44) et le facteur M est supérieur à 1.

12. Procédé de génération d'une tension de référence, comprenant:

- la mise à disposition d'un premier signal (S1) au niveau d'une première borne (22) d'un bloc de source (21), sachant que la première borne (22) du bloc de source (21) est couplée à une première borne d'une première résistance (16) et une deuxième borne de la première résistance (16) est couplée à une borne de potentiel de référence (20),

- la mise à disposition d'un deuxième signal (S2) implémenté comme courant au niveau d'une deuxième borne (23) du bloc de source (21),

- la mise en miroir du deuxième signal (S2) en un courant miroir (S3) par un premier miroir de courant (13) comprenant un premier et un deuxième transistor miroir (11, 12) de telle sorte que le premier transistor miroir (11) couple la deuxième borne (23) du bloc de source (21) à une borne de tension d'alimentation (14) et le deuxième transistor miroir (12) couple une sortie de référence (15) à la borne de tension d'alimentation (14),

- la mise à disposition du courant miroir (S3) via une connexion série (17) d'une deuxième résistance (18) et d'une diode (19) à la première borne de la première résistance (16), et

- la mise à disposition de la tension de référence (S6) au niveau de la sortie de référence (15),

sachant que le bloc de source (21) comprend une troisième borne (24) qui est couplée à la borne de potentiel de référence (20), et

sachant que le bloc de source (21) comprend un premier et un deuxième transistor (42, 43) de telle sorte que le premier transistor (42) soit agencé entre la première borne (22) du bloc de source (21) et la deuxième borne (23) du bloc de source (21) et le deuxième transistor (43) soit agencé entre la troisième borne (24) du bloc de source (21) et une quatrième borne (25) du bloc de source (21),

**caractérisé en ce que**

la quatrième borne (25) du bloc de source (21) est couplée à la borne de tension d'alimentation (14),

sachant que le premier et le deuxième transistor (42, 43) du bloc de source (21) sont couplés de manière croisée.

FIG 1

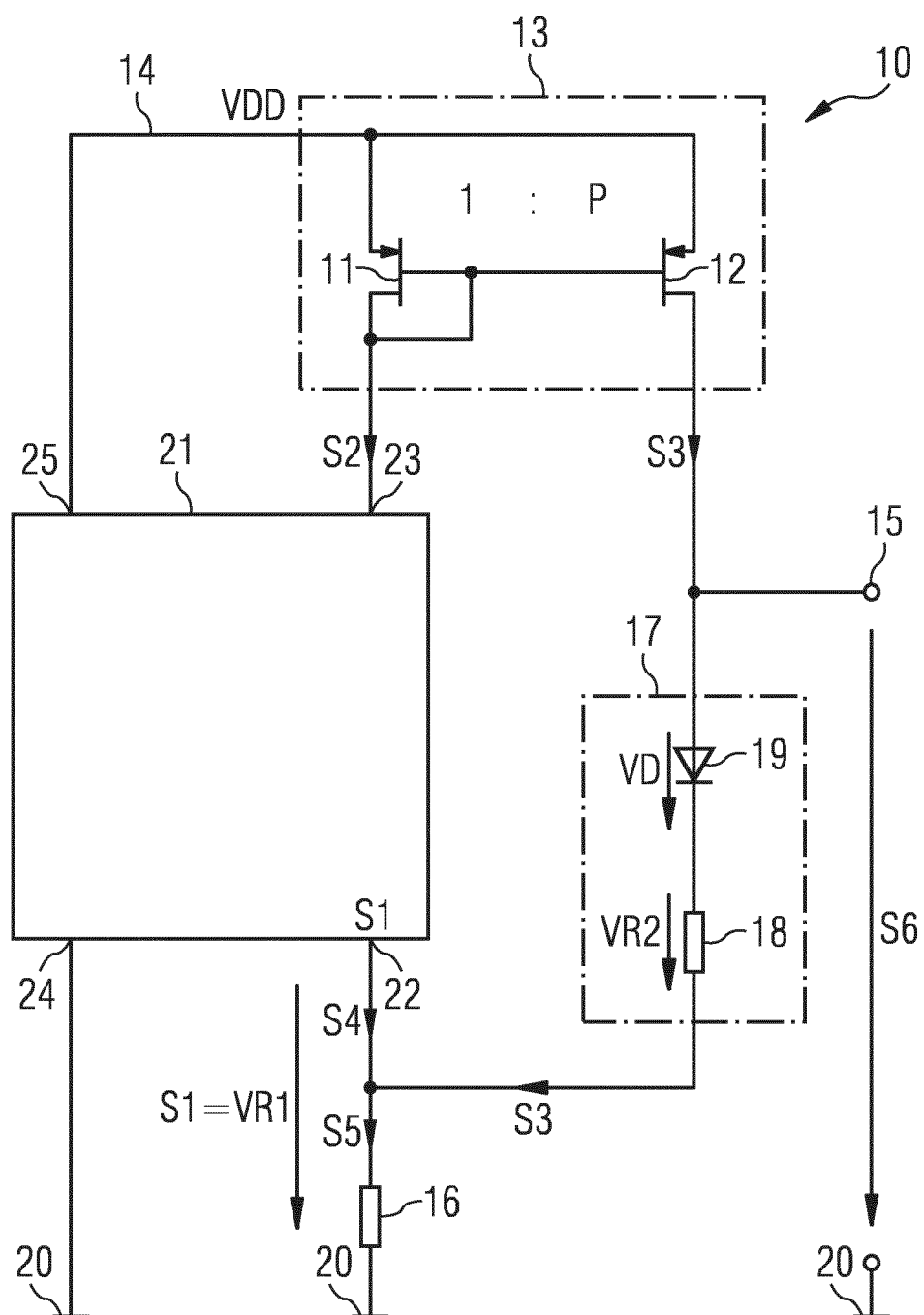


FIG 2

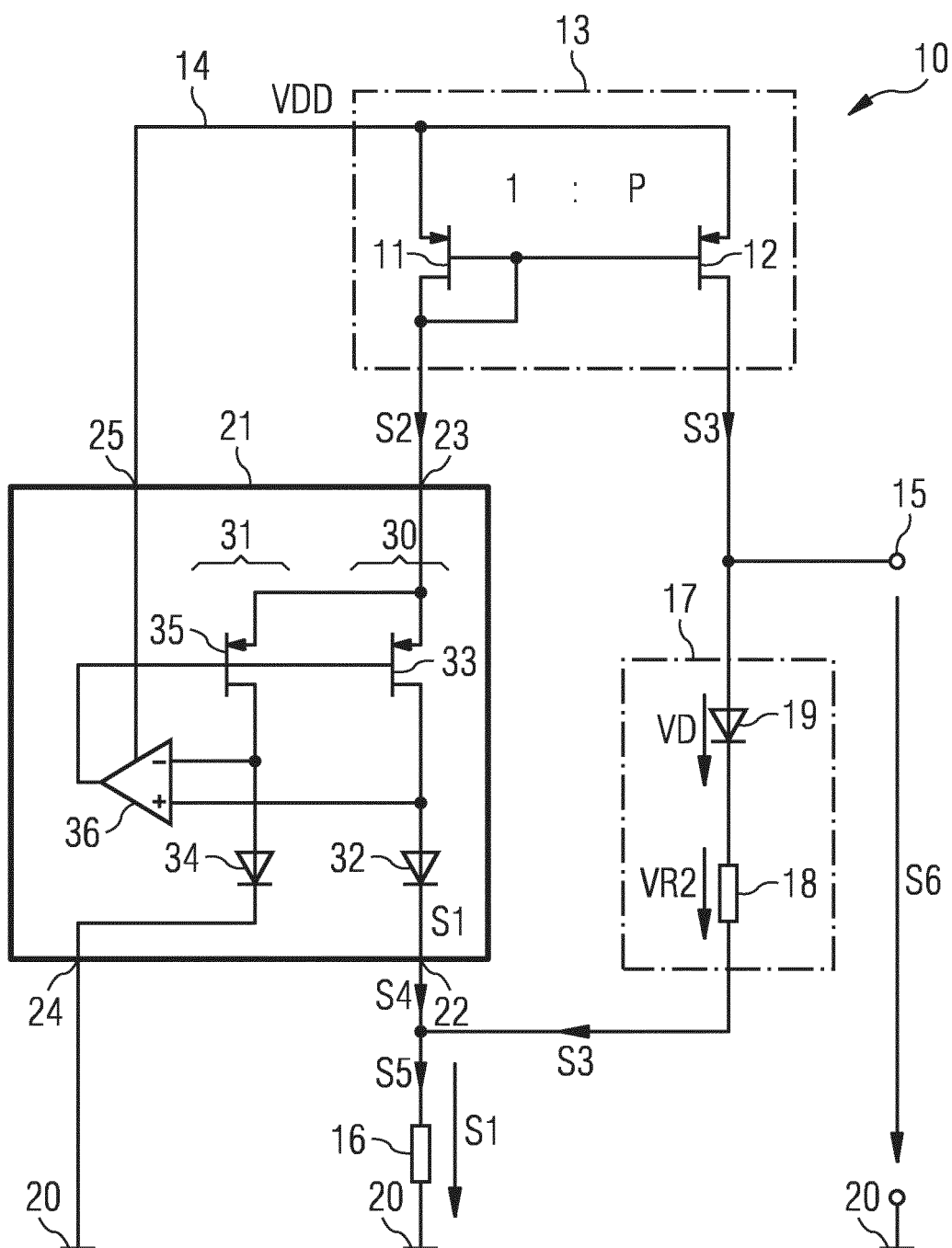
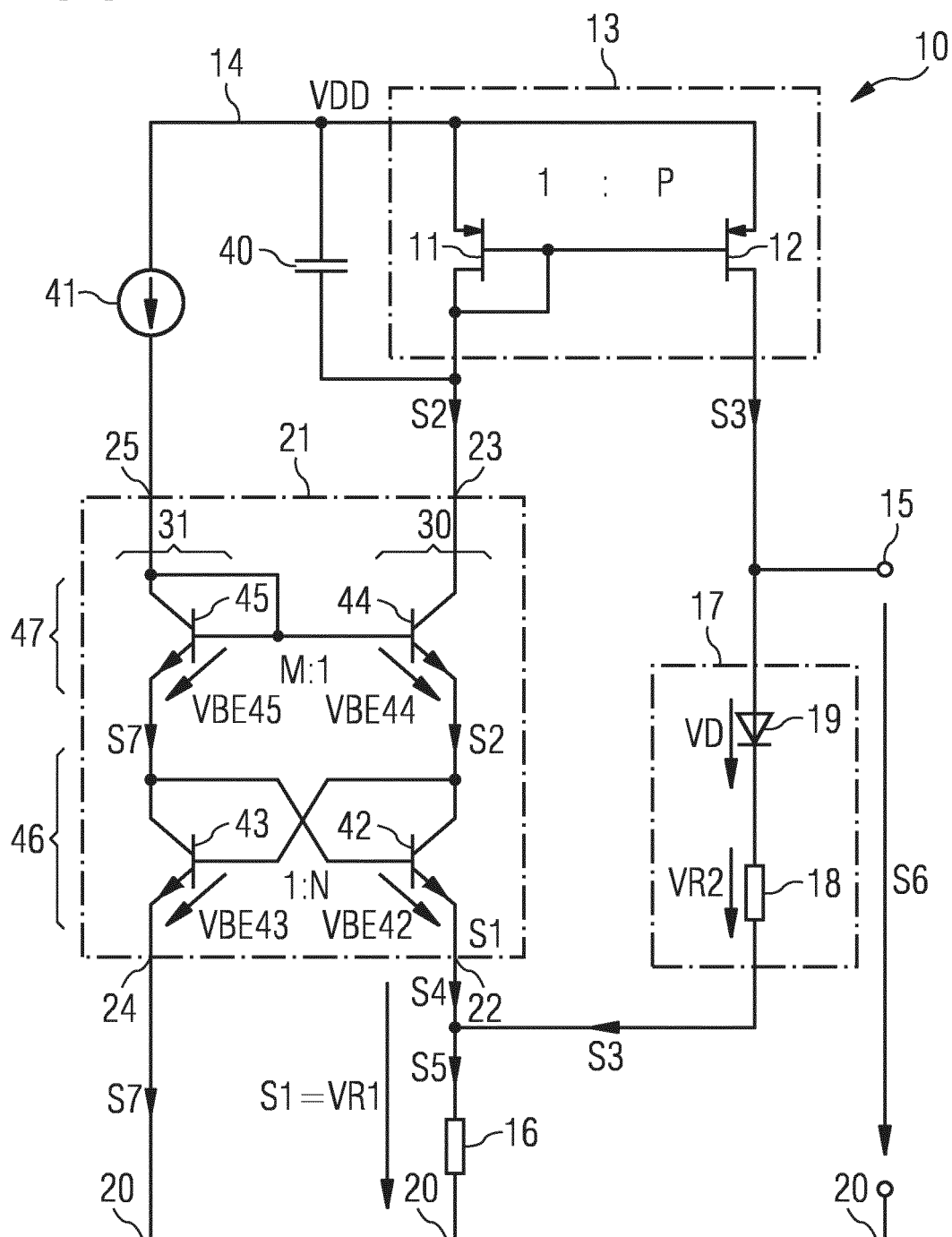


FIG 3A



**FIG 3B**

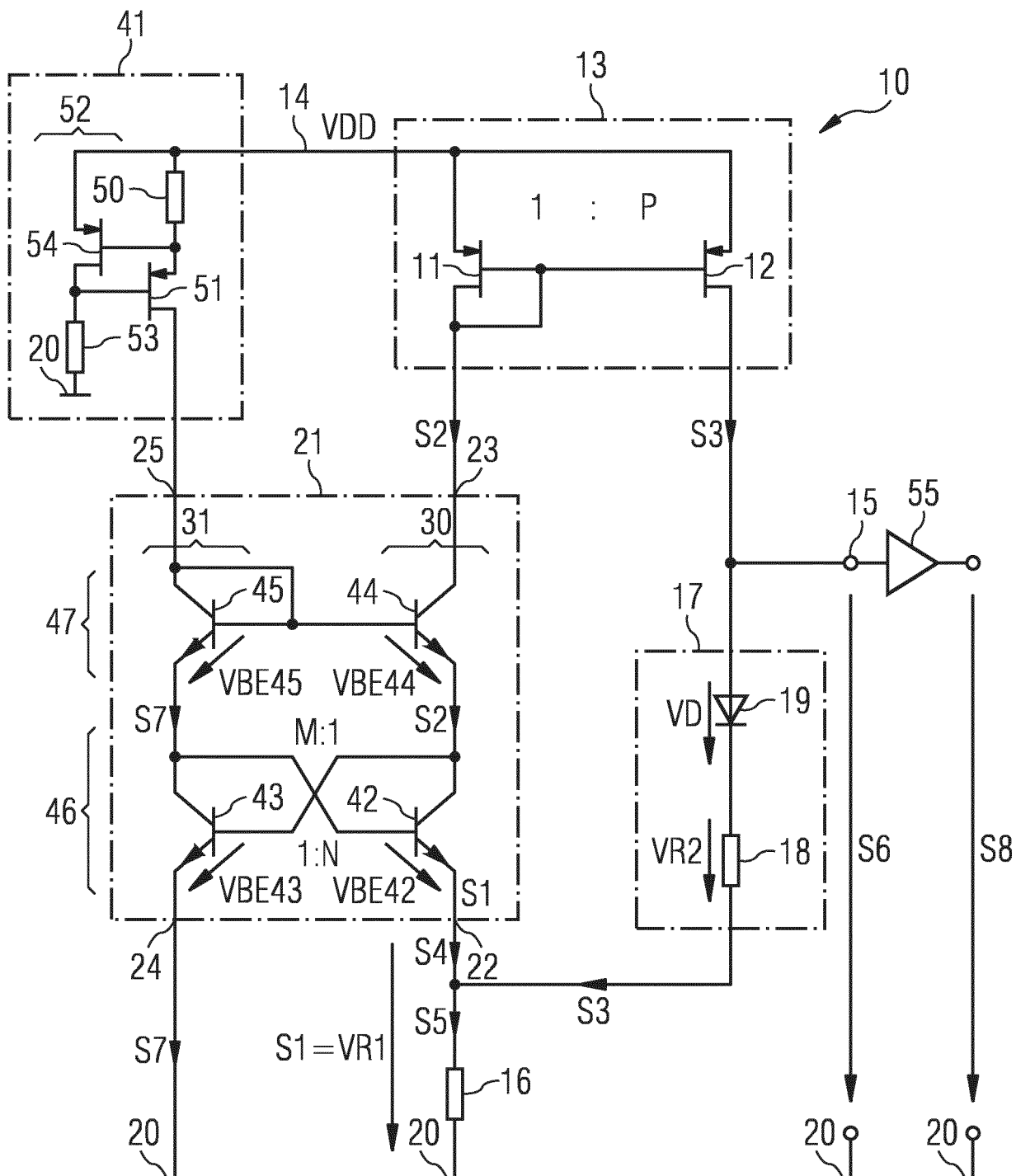


FIG 4

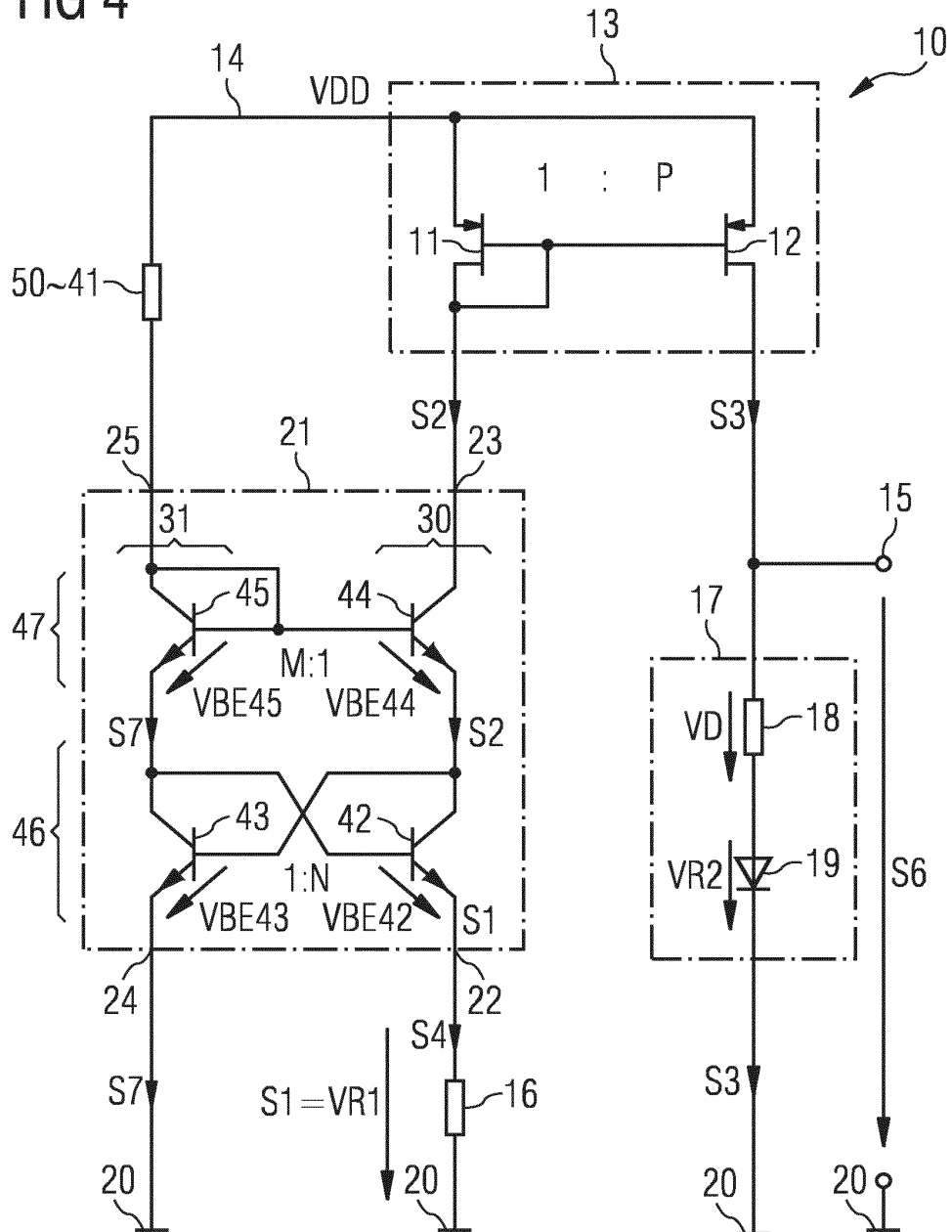


FIG 5A

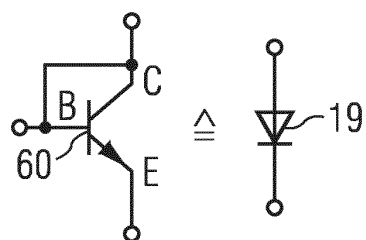


FIG 5B

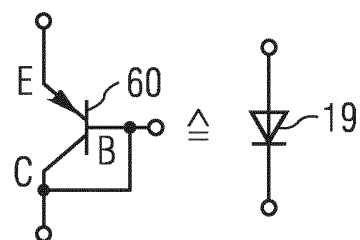
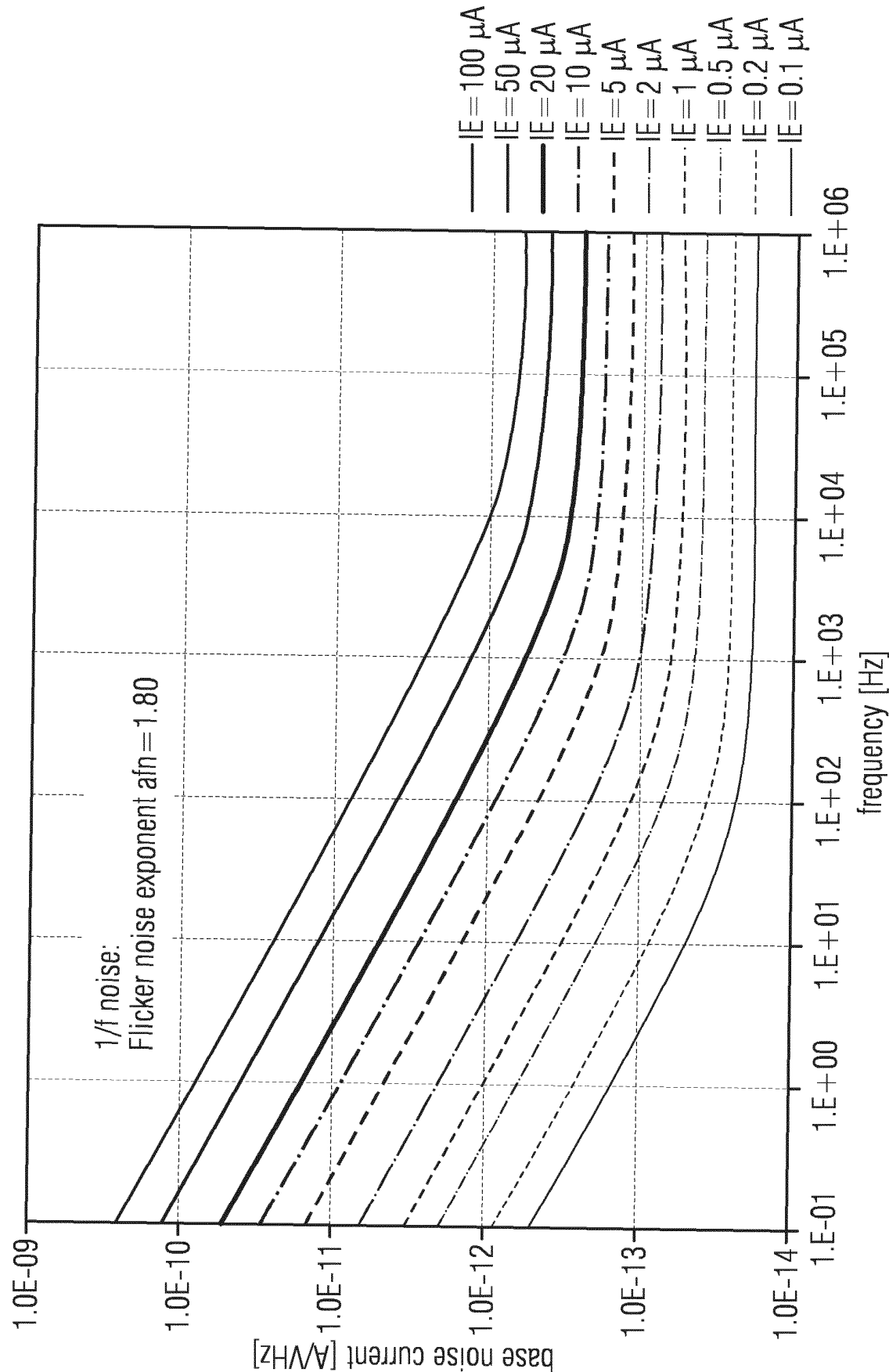


FIG 6



**REFERENCES CITED IN THE DESCRIPTION**

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