

## (11) EP 3 093 917 A1

(12)

### **EUROPEAN PATENT APPLICATION**

(43) Date of publication:

16.11.2016 Bulletin 2016/46

(51) Int Cl.:

H01P 3/00 (2006.01) H01P 11/00 (2006.01) H01P 3/08 (2006.01)

(21) Application number: 15167192.2

(22) Date of filing: 11.05.2015

(84) Designated Contracting States:

AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

**Designated Extension States:** 

**BA ME** 

**Designated Validation States:** 

MA

(71) Applicant: Nokia Technologies Oy 02610 Espoo (FI)

(72) Inventor: Haque, Md Samiul Cambridge, CB4 1GN (GB)

(74) Representative: Potter Clarkson LLP

The Belgrave Centre
Talbot Street
Nottingham NG1 5GG (GB)

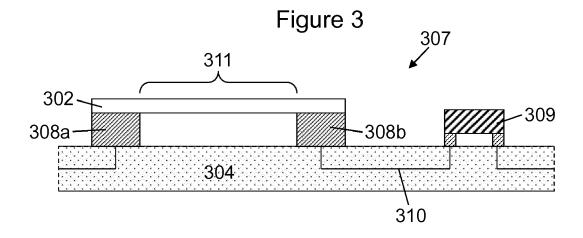
# (54) A SUSPENDED 2D SIGNAL LINE FOR CIRCUITS, AND ASSOCIATED APPARATUS AND METHODS

(57) An apparatus comprising: a two-dimensional signal line;

first and second electrodes configured to enable the transmission of an electrical signal from the first electrode through the two-dimensional signal line to the second electrode; and

a component interconnect substrate configured to support the two-dimensional signal line and the first and second electrodes to allow transmission of the electrical signal through the component interconnect substrate to/from one or more components on the substrate via the first and/or second electrode,

wherein the two-dimensional signal line is attached to the first and second electrodes such that a portion of the two-dimensional signal line is suspended by the first and second electrodes over the component interconnect substrate to reduce electromagnetic interactions between the component interconnect substrate and the suspended portion to facilitate transmission of the electrical signal.



EP 3 093 917 A1

15

25

#### Acknowledgement

**[0001]** The research leading to these results has received funding from the European Union Seventh Framework Programme under grant agreement no. 604391 Graphene Flagship.

1

#### **Technical Field**

[0002] The present disclosure relates particularly to the field of transmission lines for integrated circuits, associated methods and apparatus, and specifically concerns an apparatus comprising a two-dimensional signal line suspended over a component interconnect substrate by first and second electrodes to reduce electromagnetic interactions between the component interconnect substrate and the signal line to facilitate transmission of an electrical signal to/from one or more components on the substrate. Certain disclosed example aspects/embodiments relate to portable electronic devices, in particular, so-called hand-portable electronic devices which may be hand-held in use (although they may be placed in a cradle in use). Such hand-portable electronic devices include so-called Personal Digital Assistants (PDAs) and tablet PCs.

[0003] The portable electronic devices/apparatus according to one or more disclosed example aspects/embodiments may provide one or more audio/text/video communication functions (e.g. tele-communication, video-communication, and/or text transmission, Short Message Service (SMS)/ Multimedia Message Service (MMS)/emailing functions, interactive/non-interactive viewing functions (e.g. web-browsing, navigation, TV/program viewing functions), music recording/playing functions (e.g. MP3 or other format and/or (FM/AM) radio broadcast recording/playing), downloading/sending of data functions, image capture function (e.g. using a (e.g. in-built) digital camera), and gaming functions.

#### Background

**[0004]** Research is currently being done to develop new integrated circuits with improved physical and electrical properties for use in a variety of applications.

**[0005]** The listing or discussion of a prior-published document or any background in this specification should not necessarily be taken as an acknowledgement that the document or background is part of the state of the art or is common general knowledge.

#### **Summary**

**[0006]** According to a first aspect, there is provided an apparatus comprising:

a two-dimensional signal line;

first and second electrodes configured to enable the transmission of an electrical signal from the first electrode through the two-dimensional signal line to the second electrode; and

a component interconnect substrate configured to support the two-dimensional signal line and the first and second electrodes to allow transmission of the electrical signal through the component interconnect substrate to/from one or more components on the substrate via the first and/or second electrode, wherein the two-dimensional signal line is attached to the first and second electrodes such that a portion of the two-dimensional signal line is suspended by the first and second electrodes over the component interconnect substrate to reduce electromagnetic interactions between the component interconnect substrate and the suspended portion to facilitate transmission of the electrical signal.

**[0007]** The two-dimensional signal line may be positioned between, and spaced apart from, a pair of coplanar ground lines to form a ground-signal-ground configuration on the component interconnect substrate.

**[0008]** Each ground line may be attached to a respective pair of first and second electrodes such that a portion of the ground line is suspended by the first and second electrodes over the component interconnect substrate.

**[0009]** The two-dimensional signal line may be spaced apart from each ground line on the component interconnect substrate by an in-plane distance of  $1-100\mu m$ .

**[0010]** One or more of the two-dimensional signal line and ground lines may have a length of between 100nm and 10mm.

**[0011]** The two-dimensional signal line may comprise between 1 and 5 monolayers of conductive two-dimensional material. In certain embodiments, the two-dimensional signal line may be up to around 10nm thick, for example.

[0012] The conductive two-dimensional material may comprise one or more of graphene and reduced graphene oxide or a combination of graphene-doped graphene or other 2D materials such as MOS<sub>2</sub>, hBN (hexagonal boronitride as encapsulants). The structure may comprise different 2D materials forming a suspended heterostructure. In such a situation, the additional layers of 2D materials may be of the same order of thickness as the underlying 2D layer such that the overall thickness of the heterostructure may be up to around 20nm, for example. Such a heterostructure can still be considered to be a 2D signal line. In certain embodiments, respective 2D materials forming the signal line may be separated by a layer to provide stacked respective 2D signal lines separated by the layer. For example, if the separating later is hBN (hexagonal boronitride), the layer could be insulating (which might induce capacitive behaviour between the layers). In other embodiments, the separating layer could

[0013] The conductive two-dimensional material may

15

20

25

40

45

comprise one or more dopants configured to reduce the sheet resistance of the two-dimensional signal line.

**[0014]** The one or more dopants may comprise molybdenum oxide  $(MoO_3)$  or  $FeCl_3$ .

**[0015]** The ground lines may comprise one or more of a metal, a conductive two-dimensional material, copper, gold, silver, aluminium, nickel, graphene and reduced graphene oxide.

**[0016]** The first and second electrodes may comprise one or more of a metal, a doped semiconductor, copper, gold, silver, aluminium, nickel, germanium carbide and silicon carbide.

**[0017]** The apparatus may be configured to enable the transmission of AC electrical signals in the frequency range of 10kHz to 1THz.

**[0018]** The component interconnect substrate may be one or more of a rigid, reversibly flexible and reversibly stretchable substrate.

**[0019]** The apparatus may be one or more of an electronic device, a portable electronic device, a portable telecommunications device, a mobile phone, a personal digital assistant, a tablet, a phablet, a desktop computer, a laptop computer, a server, a smartphone, a smartwatch, smart eyewear, a circuit board, a transmission line, a microstrip, a coplanar waveguide, a filter circuit, an electronic oscillator, and a module for one or more of the same.

**[0020]** According to a further aspect, there is provided a method comprising:

forming a two-dimensional signal line and first and second electrodes for provision on a component interconnect substrate such that a portion of the twodimensional signal line is suspended over the component interconnect substrate by the first and second electrodes to reduce electromagnetic interactions between the component interconnect substrate and the suspended portion, wherein the first and second electrodes are configured to enable the transmission of an electrical signal from the first electrode through the two-dimensional signal line to the second electrode, and wherein the first and/or second electrode is configured to connect the two-dimensional signal line to the component interconnect substrate to allow transmission of the electrical signal through the component interconnect substrate to/from one or more components on the substrate.

**[0021]** Forming the two-dimensional signal line and first and second electrodes may comprise:

forming a layer of conductive two-dimensional material on top of a layer of electrode material; selectively etching the layer of conductive two-dimensional material to define the two-dimensional signal line; and selectively etching the layer of electrode material to

define the first and second electrodes.

**[0022]** Forming the layer of conductive two-dimensional material on top of the layer of electrode material may comprise growing the layer of conductive two-dimensional material via chemical vapour deposition using the layer of electrode material as a seed layer.

**[0023]** The method may comprise transferring the twodimensional signal line and first and second electrodes onto the component interconnect substrate by:

depositing a layer of transfer material on top of the layers of conductive two-dimensional and electrode material;

transferring the layers of conductive two-dimensional and electrode material onto the component interconnect substrate using the layer of transfer material; and

removing the layer of transfer material.

**[0024]** The layer of transfer material may comprise poly(methyl methacrylate).

**[0025]** Forming the two-dimensional signal line and first and second electrodes may comprise:

forming the first and second electrodes on top of the component interconnect substrate; and depositing a preformed two-dimensional signal line on top of the first and second electrodes.

[0026] The steps of any method disclosed herein do not have to be performed in the exact order disclosed, unless explicitly stated or understood by the skilled person

**[0027]** Throughout the present specification, descriptors relating to relative orientation and position, such as "top", "bottom", "upper", "lower", "above" and "below", as well as any adjective and adverb derivatives thereof, are used in the sense of the orientation of the apparatus as presented in the drawings. However, such descriptors are not intended to be in any way limiting to an intended use of the described or claimed invention.

**[0028]** Corresponding computer programs for implementing one or more steps of the methods disclosed herein are also within the present disclosure and are encompassed by one or more of the described example embodiments.

[0029] One or more of the computer programs may, when run on a computer, cause the computer to configure any apparatus, including a battery, circuit, controller, or device disclosed herein or perform any method disclosed herein. One or more of the computer programs may be software implementations, and the computer may be considered as any appropriate hardware, including a digital signal processor, a microcontroller, and an implementation in read only memory (ROM), erasable programmable read only memory (EPROM) or electronically erasable programmable read only memory (EEPROM), as non-limiting examples. The software may be an assembly program.

40

**[0030]** One or more of the computer programs may be provided on a computer readable medium, which may be a physical computer readable medium such as a disc or a memory device, or may be embodied as a transient signal. Such a transient signal may be a network download, including an internet download.

**[0031]** The present disclosure includes one or more corresponding aspects, example embodiments or features in isolation or in various combinations whether or not specifically stated (including claimed) in that combination or in isolation. Corresponding means for performing one or more of the discussed functions are also within the present disclosure.

[0032] The above summary is intended to be merely exemplary and non-limiting.

#### **Brief Description of the Figures**

**[0033]** A description is now given, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 shows a conventional microstrip transmission line (perspective view);

Figure 2 shows a conventional coplanar waveguide (perspective view);

Figure 3 shows one example of the present apparatus (cross-section);

Figure 4 shows another example of the present apparatus (plan view);

Figures 5a-f show a method of making the present apparatus (schematic);

Figures 6a-b show another method of making the present apparatus (schematic);

Figure 7 shows another example of the present apparatus (schematic);

Figure 8 shows a method of making the present apparatus (flow chart).

Figure 9 shows another method of making the present apparatus (flow chart); and

Figure 10 shows a computer-readable medium comprising a computer program configured to perform, control or enable a method described herein (schematic).

#### **Description of Specific Aspects/Embodiments**

[0034] As mentioned previously, the apparatus and associated methods described herein relate to transmission lines for integrated circuits, and in particular, transmission lines comprising two-dimensional (2D) signal lines. Generally speaking, a transmission line is an electrical conductor for carrying radio and microwave frequency AC signals to and from the various components of a printed circuit board (e.g. in a filter circuit or electronic oscillator). Standard wires and traces are not suitable for transmitting such high frequency signals because the energy tends to radiate off the conductor as radio/micro

waves causing power losses. In addition, radio and microwave frequency currents tend to reflect from discontinuities in the wire/trace (such as connectors and joints) and travel back down the conductor towards the source.

This can prevent the signal from reaching its destination. Transmission lines use special configurations and impedance matching to carry electromagnetic signals with fewer reflections and power losses. Common types of transmission line in modern circuits include the microstrip transmission line and the coplanar waveguide.

[0035] Figure 1 shows a microstrip transmission line 101 in perspective view. It consists of a conductive strip 102 (signal line) of length "I", width "w" and thickness "t" separated from a ground plane 103 by a dielectric substrate 104 of thickness "h". The electromagnetic wave carried by a microstrip transmission line 101 exists partly in the dielectric substrate 104 and partly in the air above it. The width "w" of the signal line 102 together with the thickness "h" and dielectric constant of the substrate 104 determine the characteristic impedance of the microstrip 101.

[0036] Figure 2 shows a coplanar waveguide 205 in perspective view. It consists of a conductive strip 202 (signal line) of length "I", width "w" and thickness "t" fabricated between a pair of coplanar ground lines 206a,b on the surface of a dielectric substrate 204 of thickness "h" to form a ground-signal-ground configuration. The signal line 202 is separated from each ground line 206a, b by an in-plane gap "g" which has a constant width along the length of the coplanar waveguide 205. Like the microstrip transmission line 101 shown in Figure 1, the electromagnetic wave carried by a coplanar waveguide 205 exists partly in the dielectric substrate 204 and partly in the air above it. The signal can, however, be more closely confined to the dielectric substrate 204 by using a substrate thickness "h" of at least twice the width "w" of the signal line 202. Coplanar waveguides 205 use the signal line width "w" and the gap "g" between the signal 202 and ground 206a,b lines to control the characteristic impedance.

[0037] Signal transmission using the above-mentioned transmission lines 101, 205 has been found to be limited by electromagnetic interactions between the dielectric substrate 104, 204 and the signal line 101, 201. This effect increases with the frequency of the signal which can inhibit operation in high-speed circuits. However, at higher frequencies, surfaces waves dominate. i. e. specially at higher frequencies in the tera - hertz range 1-100THz, where the surface wave interaction is most prominent, a suspended structure can provide a better solution in terms of architecture and implementation. There will now be described an apparatus and associated methods that may or may not provide a solution to this issue.

[0038] Figure 3 shows one example of the present apparatus 307 in cross-section. The apparatus 307 comprises a two-dimensional signal line 302, and first 308a and second 308b electrodes configured to enable the

25

40

45

50

55

transmission of an electrical signal from the first electrode 308a through the two-dimensional signal line 302 to the second electrode 308b. In addition, a component interconnect substrate 304 is configured to support the twodimensional signal line 302 and the first 308a and second 308b electrodes to allow transmission of the electrical signal through the component interconnect substrate 304 to/from one or more components 309 on the substrate 304 via the first 308a and/or second 308b electrode. As can be seen in this figure, the component interconnect substrate 304 comprises one or more traces 310 therein/thereon for electrical connection of the components 309. Furthermore, the two-dimensional signal line 302 is attached to the first 308a and second 308b electrodes such that a portion 311 of the two-dimensional signal line 302 is suspended by the first 308a and second 308b electrodes over the component interconnect substrate 304 to reduce electromagnetic interactions between the component interconnect substrate 304 and the suspended portion 311 to facilitate transmission of the electrical signal.

[0039] With the present apparatus 307, therefore, the first 308a and second 308b electrodes perform multiple functions. As well as being used to control the flow of electrical signals through the signal line 302, the electrodes 308a,b suspend a portion 311 of the signal line 302 over the component interconnect substrate 304 to reduce the electromagnetic interactions therebetween, and are also used as bonding pads for attachment of the signal line 302 to the component interconnect substrate 304. Furthermore, as will be described layer, the conductive material used to form the electrodes 308a,b may also be used in the fabrication of the two-dimensional signal line 302. The multiple uses of the first 308a and second 308b electrodes help to reduce the cost and complexity of the present apparatus 307.

**[0040]** The term "two-dimensional" with respect to the signal line 302 may be taken to mean that the signal line 302 is formed from a conductive two-dimensional material typically comprising a single layer of atoms or molecules, examples of which include graphene and reduced graphene oxide. Measurements have shown that two-dimensional materials are able to conduct electrical signals at higher frequencies than the materials used in conventional signal lines 302. Furthermore, the sheet resistance of these materials may be reduced to less than  $5\Omega$ /sq by using a few monolayers (e.g. 2-5 layers) and/or introducing one or more dopants (such as MoO<sub>3</sub>).

[0041] The two-dimensional signal line 302 described herein may serve as the signal line 102, 202 of a microstrip transmission line 101 or coplanar waveguide 205 configured to enable the transmission of AC electrical signals in the frequency range of 10kHz to 1THz. In some cases the frequency range can in the 1-100THz. When used in a microstrip transmission line 101, the component interconnect substrate 304 would normally comprise a layer of electrically conductive material on its lower surface, similar to the ground plane 103 shown in Figure 1.

[0042] Figure 4 shows another example of the present apparatus 407 (in plan view) configured for use as a coplanar waveguide. In this example, the two-dimensional signal line 402 is positioned between, and spaced apart from, a pair of coplanar ground lines 406a,b to form a ground-signal-ground configuration on the component interconnect substrate 404 (similar to that shown in Figure 2). The two-dimensional signal line 402 may be spaced apart from each ground line 406a,b by an in-plane distance of 1-100  $\mu \text{m}.$  Furthermore, like the signal line 402, each ground line 406a,b is attached to a respective pair of first 408a and second 408b electrodes such that a portion 411 of the ground line 406a,b is suspended by the first 408a and second 408b electrodes over the component interconnect substrate 404. In other examples, however, the ground lines 406a,b may not be suspended. [0043] One or more of the signal 402 and ground 406a, b lines described above may have a length of between 100nm (or even 10nm, particularly in the future) and 10mm, and may be formed from any conductive material such as a metal (e.g. copper, gold, silver, aluminium, nickel or alloys thereof) or conductive two-dimensional material (e.g. graphene or reduced graphene oxide). Similarly, the first 408a and second 408b electrodes may be formed from a metal (e.g. copper, gold, silver, aluminium, nickel or alloys thereof) or doped semiconductor (e. g. germanium carbide or silicon carbide).

**[0044]** The component interconnect substrate 404 may be one or more of a rigid, reversibly flexible and reversibly stretchable substrate. Whilst rigid substrates (e.g. FR-4) are more traditional, flexible and stretchable substrates are becoming more common in device applications due to new form factors and size constraints. In this respect, the component interconnect substrate 404 may comprise one or more flexible materials (e.g. polyimide or polyester) and/or stretchable materials (e.g. polyurethane or polydimethylsiloxane).

**[0045]** Figures 5a-f illustrate schematically one method of making the present apparatus. In this example, the apparatus is a co-planar waveguide, but the same process may be used to form a microstrip transmission line by omitting the ground lines. Cross-section, top and bottom views of the structure are shown in these figures to aid visualisation of the apparatus following each step of the process.

[0046] First, a layer of conductive two-dimensional material 512 is formed on top of a layer of electrode material 513 (Figure 5a). This may be achieved by growing the layer of conductive two-dimensional material 512 (e.g. graphene) via chemical vapour deposition using the layer of electrode material 513 (e.g. copper) as a seed layer. Formation of the layer of two-dimensional material 512 in this way helps to ensure good physical and electrical contact with the layer of electrode material 513 (and therefore between the signal or ground lines and their respective electrodes). The layer of conductive two-dimensional material 512 is then selectively etched to define the two-dimensional signal line 502 and ground lines

20

25

40

45

50

506a,b (Figure 5b). Once the signal 502 and ground 506a,b lines have been formed, a layer of transfer material 514 (e.g. PMMA) is deposited on top of the layers of conductive two-dimensional 512 and electrode 513 material (Figure 5c) and then the layer of electrode material 513 is selectively etched to define the first 508a and second 508b electrode pairs (Figure 5d). At this stage the layer of transfer material 514 helps to hold the signal line 502, ground lines 506a,b and their respective electrode pairs 508a,b in position following the etching processes. The layer of transfer material 514 is then used to transfer the layers of conductive two-dimensional 512 (i. e. signal 502 and ground 506a,b lines) and electrode 513 (i.e. first 508a and second 508b electrode pairs) material onto a component interconnect substrate 504 (Figure 5e). As can be seen in this figure, the first 508a and second 508b electrodes serve as bonding pads to attach the respective signal 502 and ground 506a,b lines to the component interconnect substrate 504. Once the signal line 502, ground lines 506a,b and electrodes 508a,b are in place on the substrate 504, the layer of transfer material 514 can be removed (Figure 5f). Removal of the transfer layer 514 may be performed by stripping or etching away the transfer material 514 (e.g. using acetone for PMMA). [0047] Figures 6a-b illustrate schematically another method of making the present apparatus in which the signal 602 and ground 606a,b lines are formed separately/remotely from the electrodes 608a,b. This time, the electrode pairs 608a,b are formed directly on top of the component interconnect substrate 604 (Figure 6a). This may be achieved using photo or electron beam lithography in combination with sputter coating or evaporation. Once the electrodes 608a,b have been formed, preformed signal 602 and ground 606a,b lines are deposited on top of their respective electrode pairs 608a,b (Figure 6b). Fabrication (not shown) and deposition of the signal 602 and ground 606a,b lines may be achieved respectively using selective etching and transfer procedures similar to those described with reference to Figure 5.

**[0048]** Although the method of Figures 6a-b may be more straightforward than the method of Figures 5a-f by avoiding the need for selective etching of the layer of electrode material 513 (Figure 5d), the resulting physical and electrical contact between the signal 502/ground 506a,b lines and their respective electrodes 508a,b is typically less robust by virtue of the fact that the layer of conductive two-dimensional material 512 is not formed directly on top of the layer of electrode material 513. These fabrication processes can be part of a roll 2 roll production or be used in printed electronics production environment.

**[0049]** Figure 7 illustrates schematically another example of the present apparatus 707. The apparatus 707 may be one or more of an electronic device, a portable electronic device, a portable telecommunications device, a mobile phone, a personal digital assistant, a tablet, a phablet, a desktop computer, a laptop computer, a server, a smartphone, a smartwatch, smart eyewear, a circuit

board, a transmission line, a microstrip, a coplanar waveguide, a filter circuit, an electronic oscillator, and a module for one or more of the same. In the example shown, the apparatus 707 comprises the two-dimensional signal line 702, first 708a and second 708b electrodes and component interconnect substrate 704 described previously, a power source 715, a processor 716 and a storage medium 717, which are electrically connected to one another by a data bus 718.

**[0050]** The processor 716 is configured for general operation of the apparatus 707 by providing signalling to, and receiving signalling from, the other components to manage their operation. The storage medium 717 is configured to store computer code configured to perform, control or enable operation of the apparatus 707. The storage medium 717 may also be configured to store settings for the other components. The processor 716 may access the storage medium 717 to retrieve the component settings in order to manage the operation of the other components.

**[0051]** Under the control of the processor 716, the power source 715 is configured to apply a voltage between the first 708a and second 708b electrodes to enable the transmission of an electrical signal through the two-dimensional signal line 702 to/from one or more components on the component interconnect substrate 704.

**[0052]** The processor 716 may be a microprocessor, including an Application Specific Integrated Circuit (ASIC). The storage medium 717 may be a temporary storage medium such as a volatile random access memory. On the other hand, the storage medium 717 may be a permanent storage medium 717 such as a hard disk drive, a flash memory, or a non-volatile random access memory. The power source 715 may comprise one or more of a primary battery, a secondary battery, a capacitor, a supercapacitor and a battery-capacitor hybrid.

[0053] Figure 8 shows the main steps 819-824 of a method of making the apparatus described herein in the form of a flow chart. The method is consistent with the schematic diagrams in Figures 5a-f, and generally comprises: forming a layer of conductive two-dimensional material on top of a layer of electrode material 819; selectively etching the layer of conductive two-dimensional material to define the two-dimensional signal line 820; depositing a layer of transfer material on top of the layers of conductive two-dimensional and electrode material 821; selectively etching the layer of electrode material to define the first and second electrodes 822; transferring the layers of conductive two-dimensional and electrode material onto the component interconnect substrate using the layer of transfer material 823; and removing the layer of transfer material 824.

**[0054]** Figure 9 shows the main steps 925-926 of another method of making the apparatus described herein in the form of a flow chart. The method is consistent with the schematic diagrams in Figures 6a-b, and generally comprises: forming the first and second electrodes on top of the component interconnect substrate 925; and

depositing a preformed two-dimensional signal line on top of the first and second electrodes 926.

**[0055]** Figure 10 illustrates schematically a computer/processor readable medium 1027 providing a computer program according to one embodiment. The computer program may comprise computer code configured to perform, control or enable one or more of the method steps 819-824, 925-926 of Figure 8 and/or 9. Additionally or alternatively, the computer program may comprise computer code configured to apply a voltage between the first and second electrodes to enable the transmission of an electrical signal through the two-dimensional signal line to/from one or more components on the component interconnect substrate.

**[0056]** In this example, the computer/processor readable medium 1027 is a disc such as a digital versatile disc (DVD) or a compact disc (CD). In other embodiments, the computer/processor readable medium 1027 may be any medium that has been programmed in such a way as to carry out an inventive function. The computer/processor readable medium 1027 may be a removable memory device such as a memory stick or memory card (SD, mini SD, micro SD or nano SD).

[0057] Other embodiments depicted in the figures have been provided with reference numerals that correspond to similar features of earlier described embodiments. For example, feature number 1 can also correspond to numbers 101, 201, 301 etc. These numbered features may appear in the figures but may not have been directly referred to within the description of these particular embodiments. These have still been provided in the figures to aid understanding of the further embodiments, particularly in relation to the features of similar earlier described embodiments.

[0058] It will be appreciated to the skilled reader that any mentioned apparatus/device and/or other features of particular mentioned apparatus/device may be provided by apparatus arranged such that they become configured to carry out the desired operations only when enabled, e.g. switched on, or the like. In such cases, they may not necessarily have the appropriate software loaded into the active memory in the non-enabled (e.g. switched off state) and only load the appropriate software in the enabled (e.g. on state). The apparatus may comprise hardware circuitry and/or firmware. The apparatus may comprise software loaded onto memory. Such software/computer programs may be recorded on the same memory/processor/functional units and/or on one or more memories/processors/functional units.

[0059] In some embodiments, a particular mentioned apparatus/device may be pre-programmed with the appropriate software to carry out desired operations, and wherein the appropriate software can be enabled for use by a user downloading a "key", for example, to unlock/enable the software and its associated functionality. Advantages associated with such embodiments can include a reduced requirement to download data when further functionality is required for a device, and this can be use-

ful in examples where a device is perceived to have sufficient capacity to store such pre-programmed software for functionality that may not be enabled by a user.

[0060] It will be appreciated that any mentioned apparatus/circuitry/elements/processor may have other functions in addition to the mentioned functions, and that these functions may be performed by the same apparatus/circuitry/elements/processor. One or more disclosed aspects may encompass the electronic distribution of associated computer programs and computer programs (which may be source/transport encoded) recorded on an appropriate carrier (e.g. memory, signal).

**[0061]** It will be appreciated that any "computer" described herein can comprise a collection of one or more individual processors/processing elements that may or may not be located on the same circuit board, or the same region/position of a circuit board or even the same device. In some embodiments one or more of any mentioned processors may be distributed over a plurality of devices. The same or different processor/processing elements may perform one or more functions described herein.

[0062] It will be appreciated that the term "signalling" may refer to one or more signals transmitted as a series of transmitted and/or received signals. The series of signals may comprise one, two, three, four or even more individual signal components or distinct signals to make up said signalling. Some or all of these individual signals may be transmitted/received simultaneously, in sequence, and/or such that they temporally overlap one another.

[0063] With reference to any discussion of any mentioned computer and/or processor and memory (e.g. including ROM, CD-ROM etc), these may comprise a computer processor, Application Specific Integrated Circuit (ASIC), field-programmable gate array (FPGA), and/or other hardware components that have been programmed in such a way to carry out the inventive function. [0064] The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole, in the light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that the disclosed aspects/embodiments may consist of any such individual feature or combination of features. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the disclosure.

**[0065]** While there have been shown and described and pointed out fundamental novel features as applied to different embodiments thereof, it will be understood that various omissions and substitutions and changes in the form and details of the devices and methods described may be made by those skilled in the art without

40

15

20

25

30

35

40

45

50

departing from the spirit of the invention. For example, it is expressly intended that all combinations of those elements and/or method steps which perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Moreover, it should be recognized that structures and/or elements and/or method steps shown and/or described in connection with any disclosed form or embodiment may be incorporated in any other disclosed or described or suggested form or embodiment as a general matter of design choice. Furthermore, in the claims means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents, but also equivalent structures. Thus although a nail and a screw may not be structural equivalents in that a nail employs a cylindrical surface to secure wooden parts together, whereas a screw employs a helical surface, in the environment of fastening wooden parts, a nail and a screw may be equivalent structures.

**Claims** 

1. An apparatus comprising:

a two-dimensional signal line;

first and second electrodes configured to enable the transmission of an electrical signal from the first electrode through the two-dimensional signal line to the second electrode; and

a component interconnect substrate configured to support the two-dimensional signal line and the first and second electrodes to allow transmission of the electrical signal through the component interconnect substrate to/from one or more components on the substrate via the first and/or second electrode.

wherein the two-dimensional signal line is attached to the first and second electrodes such that a portion of the two-dimensional signal line is suspended by the first and second electrodes over the component interconnect substrate to reduce electromagnetic interactions between the component interconnect substrate and the suspended portion to facilitate transmission of the electrical signal.

- 2. The apparatus of claim 1, wherein the two-dimensional signal line is positioned between, and spaced apart from, a pair of coplanar ground lines to form a ground-signal-ground configuration on the component interconnect substrate.
- 3. The apparatus of claim 2, wherein each ground line is attached to a respective pair of first and second electrodes such that a portion of the ground line is suspended by the first and second electrodes over

the component interconnect substrate.

- 4. The apparatus of claim 2 or 3, wherein the two-dimensional signal line is spaced apart from each ground line on the component interconnect substrate by an in-plane distance of 1-100μm.
- The apparatus of any of claims 2 to 4, wherein one or more of the two-dimensional signal line and ground lines have a length of between 10nm and 10mm.
- The apparatus of any preceding claim, wherein the two-dimensional signal line comprises between 1 and 5 monolayers of conductive two-dimensional material.
- 7. The apparatus of claim 6, wherein the conductive two-dimensional material comprises one or more dopants configured to reduce the sheet resistance of the two-dimensional signal line.
- **8.** The apparatus of any preceding claim, wherein the apparatus is configured to enable the transmission of AC electrical signals in the frequency range of 10kHz to 10's of THz.
- The apparatus of any preceding claim, wherein the component interconnect substrate is one or more of a rigid, reversibly flexible and reversibly stretchable substrate.
- 10. The apparatus of any preceding claim, wherein the apparatus is one or more of an electronic device, a portable electronic device, a portable telecommunications device, a mobile phone, a personal digital assistant, a tablet, a phablet, a desktop computer, a laptop computer, a server, a smartphone, a smartwatch, smart eyewear, a circuit board, a transmission line, a microstrip, a coplanar waveguide, a filter circuit, an electronic oscillator, and a module for one or more of the same.

#### 11. A method comprising:

forming a two-dimensional signal line and first and second electrodes for provision on a component interconnect substrate such that a portion of the two-dimensional signal line is suspended over the component interconnect substrate by the first and second electrodes to reduce electromagnetic interactions between the component interconnect substrate and the suspended portion, wherein the first and second electrodes are configured to enable the transmission of an electrical signal from the first electrode through the two-dimensional signal line to the second electrode, and wherein the first

and/or second electrode is configured to connect the two-dimensional signal line to the component interconnect substrate to allow transmission of the electrical signal through the component interconnect substrate to/from one or more components on the substrate.

**12.** The method of claim 11, wherein forming the twodimensional signal line and first and second electrodes comprises:

10

forming a layer of conductive two-dimensional material on top of a layer of electrode material; selectively etching the layer of conductive two-dimensional material to define the two-dimensional signal line; and selectively etching the layer of electrode material to define the first and second electrodes.

15

13. The method of claim 12, wherein forming the layer of conductive two-dimensional material on top of the layer of electrode material comprises growing the layer of conductive two-dimensional material via chemical vapour deposition using the layer of electrode material as a seed layer.

25

**14.** The method of claim 12 or 13, wherein the method comprises transferring the two-dimensional signal line and first and second electrodes onto the component interconnect substrate by:

30

depositing a layer of transfer material on top of the layers of conductive two-dimensional and electrode material;

transferring the layers of conductive two-dimensional and electrode material onto the component interconnect substrate using the layer of transfer material; and

removing the layer of transfer material.

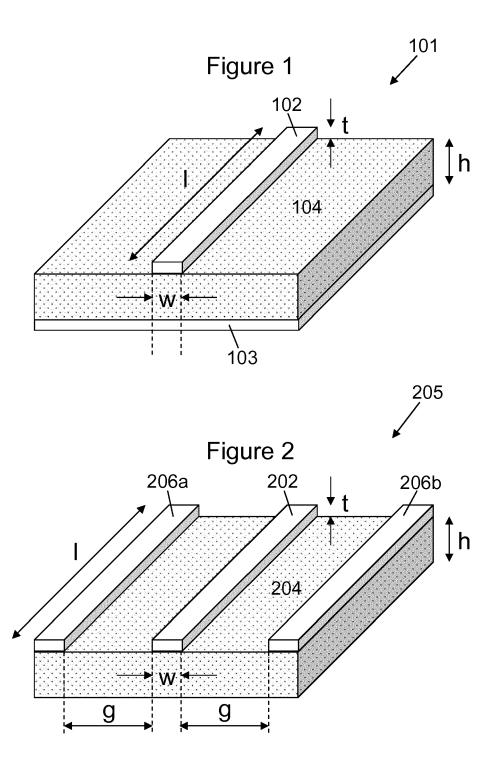
40

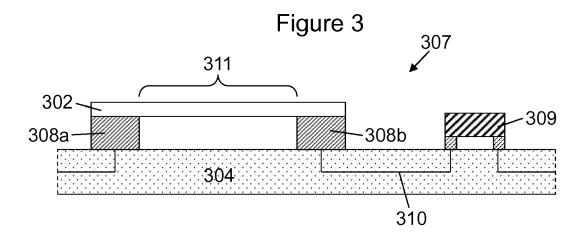
**15.** The method of claim 11, wherein forming the twodimensional signal line and first and second electrodes comprises:

45

forming the first and second electrodes on top of the component interconnect substrate; and depositing a preformed two-dimensional signal line on top of the first and second electrodes.

50





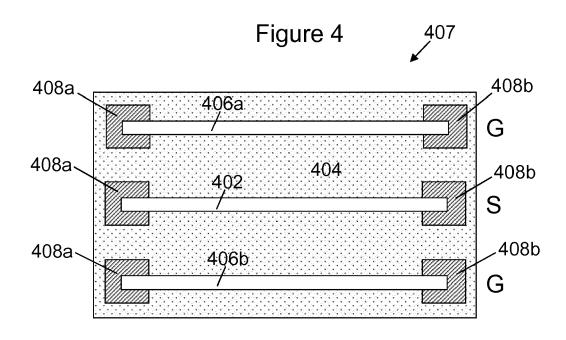
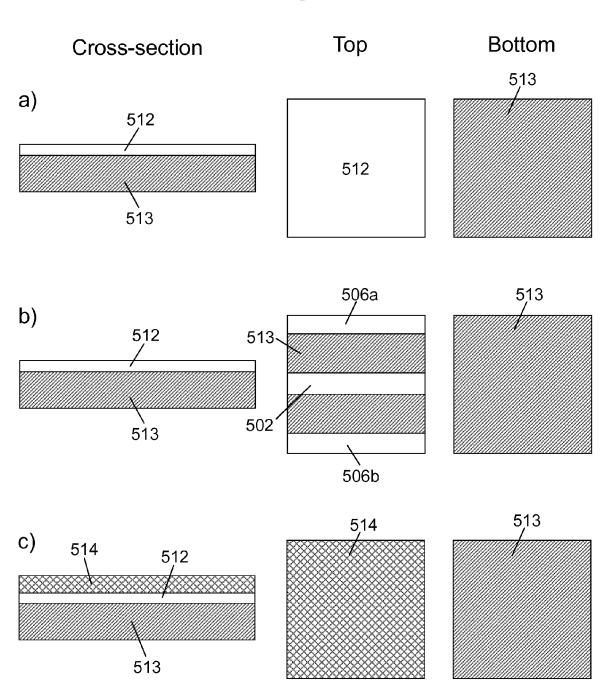
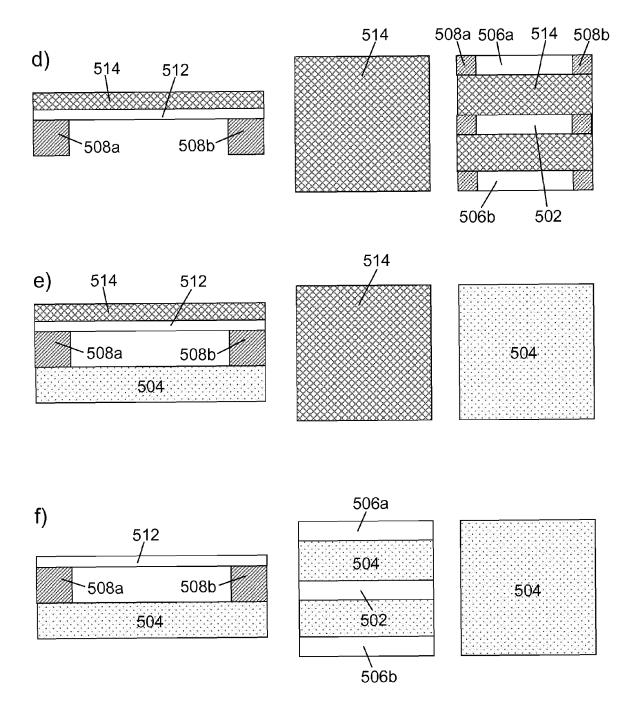


Figure 5





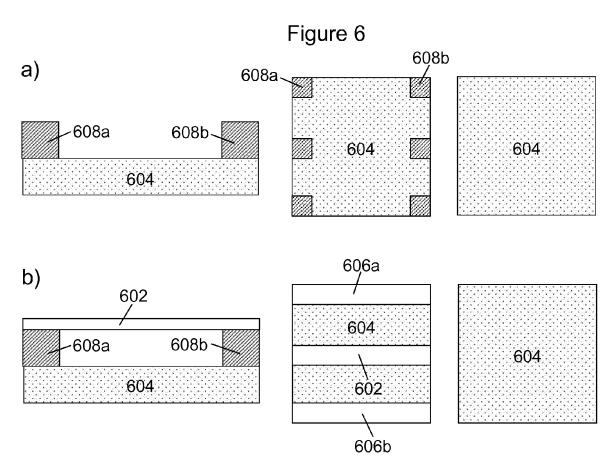
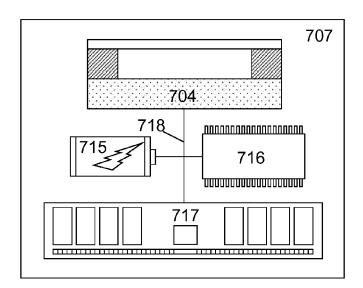


Figure 7



## Figure 8

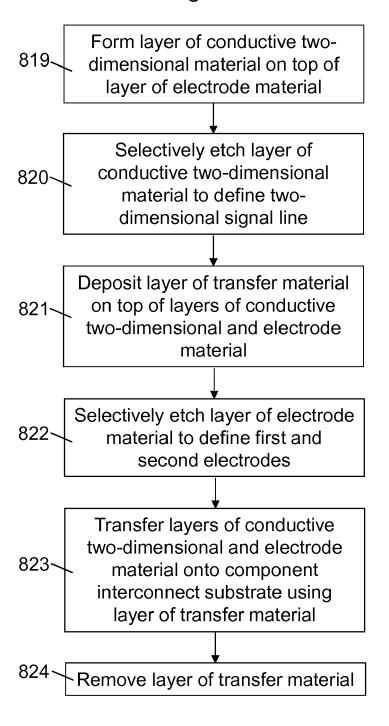


Figure 9

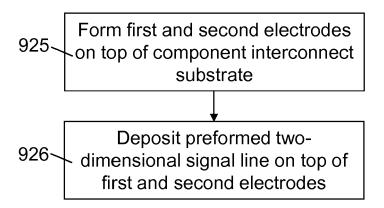
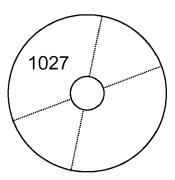


Figure 10





## **EUROPEAN SEARCH REPORT**

Application Number

EP 15 16 7192

10		
15		
20		
25		
30		
35		
40		

45

50

P04C01)	The Hag
03.82 (P	CATEGORY OF
RM 1503 03	X : particularly relevan Y : particularly relevan document of the sa A : technological back

Category	Citation of document with in of relevant pass:		ate,	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	LIM Y ET AL: "Deve carbon nanostructur nanomeshes", 2013 TRANSDUCERS & 17TH INTERNATIONAL SOLID-STATE SENSORS MICROSYSTEMS (TRANS XXVII), IEEE, 16 June 2013 (2013- 1935-1937, XP032499 DOI: 10.1109/TRANSD [retrieved on 2013- * page 1935 - page	EUROSENSORS XXV CONFERENCE ON G, ACTUATORS AND DUCERS & EUROSE -06-16), pages 1802, DUCERS.2013.6627	711: THE 20 ENSORS 2172		INV. H01P3/00 H01P3/08 H01P11/00
X	DANIEL R COOPER ET review of graphene" ARXIV.ORG, CORNELL OLIN LIBRARY CORNEL 14853, 29 October 2011 (20 * Sections 1, 6.3, figure 47 *	UNIVERSITY LIBF L UNIVERSITY IT 011-10-29), XP08	RARY, 201 THACA, NY	,6-11	TECHNICAL FIELDS SEARCHED (IPC)
X	BOLOTIN K I ET AL: mobility in suspend ARXIV.ORG, CORNELL OLIN LIBRARY CORNEL 14853, 17 February 2008 (2 XP080400868, DOI: 10.1016/J.SSC.	led graphene", UNIVERSITY LIBF L UNIVERSITY IT	ARY, 201	.,6,8, .0,11	НО1Р
Υ	* column 1 - column	3; figure 1 *		2-5, 2-14	
	The present search report has	been drawn up for all clair	ms		
	Place of search	Date of completion	n of the search		Examiner
	The Hague	10 Novem	nber 2015	Hue	so González, J
X : part Y : part docu A : tech	ATEGORY OF CITED DOCUMENTS icularly relevant if taken alone icularly relevant if combined with anot ument of the same category incological background	E:6 # her D:0 L:0	heory or principle ur earlier patent docum ifter the filing date document cited in th locument cited for o member of the same	ent, but publis e application ther reasons	hed on, or



## **EUROPEAN SEARCH REPORT**

Application Number EP 15 16 7192

'		ERED TO BE RELEVANT		
Category	Citation of document with in of relevant passa		Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Υ	for MMIC application 2013 IEEE INTERNATION CONFERENCE (RFM), I	GNR transmisson lines ns", ONAL RF AND MICROWAVE EEE, 13-12-09), pages 42-46, 13.6757214 03-05]	2-5, 12-14	
A	AL) 21 June 2012 (20	, [0059] - paragraph	9	
				TECHNICAL FIELDS SEARCHED (IPC)
	The present search report has b	een drawn up for all claims	-	
	Place of search	Date of completion of the search	<u> </u>	Examiner
	The Hague	10 November 2015	5 Hue	eso González, J
X : parti Y : parti docu A : tech	ATEGORY OF CITED DOCUMENTS icularly relevant if taken alone cularly relevant if combined with anoth unent of the same category nological background written disclosure	L : document cited t	cument, but publ te in the application or other reasons	ished on, or

## EP 3 093 917 A1

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 15 16 7192

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

10-11-2015

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012154248 A	21-06-2012	CN 103262343 A EP 2652838 A1 US 2012154248 A1 WO 2012080562 A1	21-08-2013 23-10-2013 21-06-2012 21-06-2012
ORM P0459			

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82