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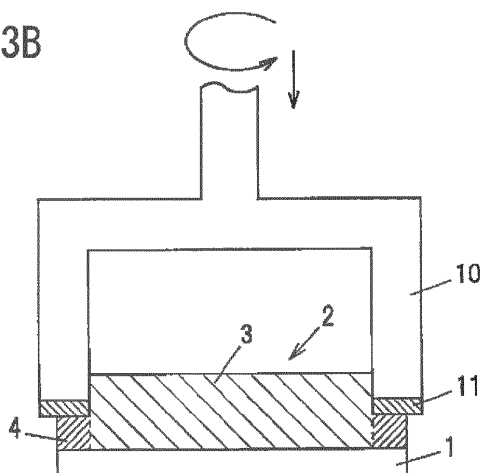
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(54) **SEMICONDUCTOR SUBSTRATE MANUFACTURING METHOD**

(57) [Problem] To provide a semiconductor substrate manufacturing method whereby a semiconductor substrate can be obtained by slicing an epitaxially grown III nitride semiconductor single crystal, while suppressing generation of cracks. [Solution] According to one embodiment of the present invention, a semiconductor substrate manufacturing method includes: a step for epitaxially growing a columnar III nitride semiconductor single crystal (2) on a main surface of a circular substrate (1); a step for removing a cylindrical region (4) on the outer circum-

ferential side of the III nitride semiconductor single crystal (2), and leaving a columnar region (3) on the inner side of the cylindrical region (4) of the III nitride semiconductor single crystal (2); and a step for slicing the columnar region (3) after removing the cylindrical region (4). The cylindrical region (4) is removed such that the shape of the III nitride semiconductor single crystal (2) is constantly axisymmetrical with the center axis of the III nitride semiconductor single crystal (2) as a symmetric axis.

**FIG. 3B**



**Description**

[Technical Field]

**[0001]** The present invention relates to a method for manufacturing a semiconductor substrate.

[Background Art]

**[0002]** A method of slicing a semiconductor substrate from a semiconductor crystal that is epitaxially grown thick on a seed crystal substrate by a method such as HVPE (hydride vapor phase epitaxy) is known as one of a method for manufacturing a group III nitride semiconductor single crystal substrate representing a conventional GaN (gallium nitride) substrate. Such a method partly begins to be practically used.

**[0003]** However, in the method, when beginning to slice the crystal grown on the seed crystal substrate, a problem frequently arises that a crack occurs in the crystal or the crystal is broken. The crack tends to occur according as a dislocation density in the crystal or a defect density such as a polarity reversed region lowers, or according as a crystal property becomes uniform, or according as a diameter of the crystal increases. Thus, it is difficult to slice a superior large crystal (e.g. the diameter is more than 50mm) without the crack.

**[0004]** To solve the problem, a technique is known in which the crystal is cylindrically ground using a grinding stone before the slicing (see e.g., PTL1). PTL1 states that the crack in the crystal during slicing can be prevented by slicing the crystal after removing an outer peripheral edge having a stain in the crystal.

[Prior Art Document]

[Patent Literature]

**[0005]** PTL1: JP-A-2013-60349

[Summary of Invention]

[Technical Problem]

**[0006]** However, even when using the technique disclosed in PTL 1, the cylindrical grinding may often cause the crack in the crystal as soon as it is begun for removing the outer peripheral edge.

**[0007]** It is an object of the invention to provide a method for manufacturing a semiconductor substrate that allows the manufacture of a semiconductor substrate by slicing the epitaxial grown group III nitride semiconductor single crystal while preventing the occurrence of the crack.

[Solution to Problem]

**[0008]** To achieve the object as described above, an

embodiment of the invention provides a method for manufacturing semiconductor substrate set forth in [1] to [24] below.

**[0009]**

[1] A method for manufacturing a semiconductor substrate, comprising:

epitaxially growing a columnar group III nitride semiconductor single crystal on a principal plane of a circular substrate;  
removing a hollow cylindrical region at an outer peripheral edge side of the group III nitride semiconductor single crystal to leave a solid columnar region at an inside of the hollow cylindrical region of the group III nitride semiconductor single crystal; and  
slicing the solid columnar region after removing the hollow cylindrical region,  
wherein the removing of the hollow cylindrical region is carried out such that a shape of the group III nitride semiconductor single crystal always keeps an axial symmetry that a central axis of the semiconductor crystal is defined as a symmetry axis.

[2] The method according to [1] wherein the hollow cylindrical region comprises a region that has a concentration of an impurity that is different from that in the solid columnar region

[3] The method according to [1] or [2], wherein the hollow cylindrical region comprises a region formed by a crystal growth using a plane that has a different orientation from an orientation in an upper surface of the solid columnar region as a growth interface in the epitaxial growth of the group III nitride semiconductor single crystal.

[4] The method according to [1] or [2], wherein the hollow cylindrical region comprises a facet plane having a plane orientation different from that in the upper surface of the hollow cylindrical region.

[5] The method according to [1] or [2], wherein the removing of the hollow cylindrical region is carried out such that a shape of the removed region is always kept into a hollow cylindrical shape with a uniform height.

[6] The method according to [1] or [2], wherein the removing of the hollow cylindrical region is carried out by grinding using a grindstone, ultrasonic processing, electric discharge processing, etching, or laser processing.

[7] The method according to [1] or [2], wherein the group III nitride semiconductor single crystal is a gallium nitride crystal.

[8] The method according to [1] or [2], wherein an upper surface of the solid columnar region is a c-plane of the group III nitride semiconductor single crystal.

[9] The method according to [2] wherein the group III nitride semiconductor single crystal is a gallium nitride crystal epitaxially grown by HVPE method, and the impurity is oxygen.

[10] The method according to [1] or [2], wherein the removing of the hollow cylindrical region is carried out such that a region of the substrate just below the hollow cylindrical region is not removed.

[11] The method according to claim [10], wherein the principal plane of the substrate is ground after slicing the solid columnar region such that the substrate is reused as a seed crystal.

[12] A method for manufacturing a semiconductor substrate, comprising:

epitaxially growing a columnar group III nitride semiconductor single crystal on a principal plane of a circular substrate;

forming a cylindrical cavity in the group III nitride semiconductor single crystal to separate the group III nitride semiconductor single crystal into a hollow cylindrical region at an outer peripheral edge side of the group III nitride semiconductor single crystal and a solid columnar region at an inside of the hollow cylindrical region of the group III nitride semiconductor single crystal; and

slicing the solid columnar region after separating the group III nitride semiconductor single crystal into the hollow cylindrical region and the solid columnar region,

wherein the forming of the cavity is carried out such that a shape of the group III nitride semiconductor single crystal always keeps an axial symmetry that a central axis of the semiconductor crystal is defined as a symmetry axis.

[13] The method according to [12], wherein the hollow cylindrical region comprises a region that has a concentration of an impurity that is different from that in the solid columnar region.

[14] The method according to [12] or [13], wherein the hollow cylindrical region comprises a region formed by a crystal growth using a plane that has a different orientation from an orientation in an upper surface of the solid columnar region as a growth interface in the epitaxial growth of the group III nitride semiconductor single crystal.

[15] The method according to [12] or [13], wherein the hollow cylindrical region comprises a facet plane having a plane orientation different from that in the upper surface of the hollow cylindrical region.

[16] The method according to [12] or [13], wherein the removing of the hollow cylindrical region is carried out such that a shape of the removed region is always kept into a hollow cylindrical shape with a uniform height.

[17] The method according to [12] or [13], wherein

the removing of the hollow cylindrical region is carried out by drilling using a hole saw, grinding using a grindstone, ultrasonic processing, electric discharge processing, or laser processing.

[18] The method according to [12] or [13], wherein the group III nitride semiconductor single crystal is a gallium nitride crystal.

[19] The method according to [12] or [13], wherein an upper surface of the solid columnar region is a c-plane of the group III nitride semiconductor single crystal.

[20] The method according to [13], wherein the group III nitride semiconductor single crystal is a gallium nitride crystal epitaxially grown by HVPE method, and the impurity is oxygen

[21] The method according to [12] or [13], wherein the hollow cylindrical region is removed before slicing the solid columnar region.

[22] The method according to [12] or [13], wherein the solid columnar region is sliced along with the hollow cylindrical region while the hollow cylindrical region remains around the solid columnar region.

[23] The method according to [12] or [13], wherein the forming the cavity is carried out such that a region of the substrate just below the hollow cylindrical region is not removed.

[24] The method according to [23], wherein the principal plane of the substrate is ground after slicing the solid columnar region such that the substrate is reused as a seed crystal.

#### [Advantageous Effects of Invention]

**[0010]** According to the invention, a method for manufacturing a semiconductor substrate can be provided that allows the manufacture of the semiconductor substrate by slicing the epitaxial grown group III nitride semiconductor single crystal while preventing growing the crack.

#### [Brief Description of Drawings]

#### [0011]

##### [FIG.1A]

**FIG.1A** is a vertical cross sectional view showing schematically a step for epitaxially growing a columnar group III nitride semiconductor single crystal on a substrate.

##### [FIG.1B]

**FIG.1B** is a vertical cross sectional view showing schematically a step for epitaxially growing a columnar group III nitride semiconductor single crystal on a substrate.

##### [FIG.1C]

**FIG.1C** is a vertical cross sectional view showing schematically a step for epitaxially growing a columnar group III nitride semiconductor single crystal on

a substrate.

**[FIG.2]**

**FIG.2** is a top view showing a group III nitride semiconductor single crystal epitaxially grown on a c-plane substrate.

**[FIG.3A]**

**FIG.3A** is a vertical cross sectional view showing schematically a step for removing a hollow cylindrical region by grinding using a hollow cylindrical grindstone.

**[FIG.3B]**

**FIG.3B** is a vertical cross sectional view showing schematically a step for removing a hollow cylindrical region by grinding using a hollow cylindrical grindstone.

**[FIG.4A]**

**FIG.4A** is a vertical cross sectional view showing schematically a step for removing a hollow cylindrical region by electric discharging using a hollow cylindrical sinker electric discharge electrode.

**[FIG.4B]**

**FIG.4B** is a vertical cross sectional view showing schematically a step for removing a hollow cylindrical region by electric discharging using a hollow cylindrical sinker electric discharge electrode.

**[FIG.5]**

**FIG.5** is a vertical cross sectional view showing a situation that a hollow cylindrical region is removed from the side of a grown group III nitride semiconductor single crystal and a substrate region is left just below the hollow cylindrical region.

**[FIG.6]**

**FIG.6** is a vertical cross sectional view showing a substrate on which a protective coat for removing a hollow cylindrical region selectively by etching is formed and a group III nitride semiconductor single crystal.

**[FIG.7A]**

**FIG.7A** is a vertical cross sectional view showing schematically a step for slicing a solid columnar region.

**[FIG.7B]**

**FIG.7B** is a vertical cross sectional view showing schematically a step for slicing a solid columnar region.

**[FIG.8A]**

**FIG.8A** is a vertical cross sectional view showing schematically a step for forming a cavity by using a hole saw and separating a hollow cylindrical region from a solid columnar region.

**[FIG.8B]**

**FIG.8B** is a vertical cross sectional view showing schematically a step for forming a cavity by using a hole saw and separating a hollow cylindrical region from a solid columnar region.

**[FIG.9]**

**FIG.9** is a vertical cross sectional view showing a situation of a group III nitride semiconductor single

crystal after being separated from the solid columnar region while remaining the hollow cylindrical region on the substrate.

**[FIG.10]**

**FIG.10** is a vertical cross sectional view showing schematically a configuration of an HVPE growing machine used for crystal growth of a GaN crystal.

[Description of Embodiment]

[First Embodiment]

**[0012]** It is conventionally known that a strain occurs in a hollow cylindrical region at an outer peripheral edge side of a columnar crystal epitaxial grown, and that when slicing the crystal, a crack is caused by the strain. The strain is caused by a difference in the concentration of an impurity which is incorporated in the crystal in the epitaxial growing between the abovementioned hollow cylindrical region and the inner region thereof.

**[0013]** As a result of researching a mechanism for causing the crack earnestly, inventors have found that an immediate cause is the unbalancing of strain distribution in the crystal caused by releasing locally the strain in the hollow cylindrical region that is distributed in axial symmetry in the slicing step, and that the occurrence of the crack can be prevented by conducting the slicing step so as to keep the symmetry of the strain distribution.

**[0014]** The present embodiment is intended to remove the strain in the crystal before conducting the slicing step on the basis of the findings mentioned above, wherein the hollow cylindrical region described above is removed from the crystal while keeping the balance of the strain distribution and the slicing step is subsequently conducted. The details thereof will be described below.

(Growth of a group III nitride semiconductor single crystal)

**[0015]** **FIGS.1A, 1B, and 1C** are vertical cross sectional views showing schematically steps for epitaxially growing a columnar group III nitride semiconductor single crystal 2 on a substrate 1. **FIG.2** is a top view showing the group III nitride semiconductor single crystal 2 epitaxially grown. The group III nitride semiconductor single crystal 2 shown in **FIGS.1A, 1B, 1C** and **FIG.2** is a GaN crystal grown in a c-plane (Ga plane) as an example of the group III nitride semiconductor single crystal 2.

**[0016]** First, as shown in **FIG.1A**, a circular substrate 1 for a seed crystal is provided. The substrate 1 is, for example, a GaN (gallium nitride) substrate whose principal plane 1p is a c-plane. The GaN substrate is suitable for the seed crystal to grow the GaN crystal epitaxially.

**[0017]** Then, as shown in **FIGS.1B and 1C**, the group III nitride semiconductor single crystal 2 grows epitaxially on the principal plane 1p of the substrate 1. The group III nitride semiconductor single crystal 2 grows so as to form columnar in perpendicular to the principal plane 1p

of the substrate **1**. In this epitaxial growth, a growth interface at the outer peripheral edge side of the group III nitride semiconductor single crystal **2** includes a facet plane **4p**. Further, a crystal growth that the growth interface is a specific crystal plane is called facet growth, and the specific crystal plane is called a facet plane.

**[0018]** Herein, at a process described after, in the outer peripheral edge side of the group III nitride semiconductor single crystal **2**, a hollow cylindrical region removed from the group III nitride semiconductor single crystal **2** defines a hollow cylindrical region **4**. A central axis of the hollow cylindrical region **4** is similar to a central axis of the group III nitride semiconductor single crystal **2**, and an inner diameter of the hollow cylindrical region **4** is even. And a solid columnar region arranged at inside of the hollow cylindrical region **4** defines a solid columnar region **3**. The hollow cylindrical region **4** can set a hollow cylindrical region whose upper surface includes the facet plane **4p**.

**[0019]** Plane directions of a plane **3p** that is the upper surface of the solid columnar region **3** and the facet plane **4p** are different. For instance, as the substrate **1** is a GaN substrate whose principal plane **1p** is the c-plane and the group III nitride semiconductor single crystal **2** is the GaN crystal, the plane **3p** of the solid columnar region **3** represents the c-plane. Also, planes **4n** excepting the facet plane **4p** at the upper surface of the hollow cylindrical region **4** are configured by planes having different orientations from the plane **3p** of the solid columnar region **3**.

**[0020]** The growth of the group III nitride semiconductor single crystal **2** is progressed while keeping mostly the shape and size of the facet plane **4p** and the plane **4n**.

**[0021]** As previously described, the concentration of impurities which is incorporated into a predetermined region of the crystal in epitaxial growth depends on an orientation of the growth interface of the region in epitaxial growth. Thus, a region formed by the crystal growth whose growth interfaces are the facet plane **4p** and the plane **4n** is different in the concentration of the impurities incorporated in the epitaxial growth of the group III nitride semiconductor single crystal **2** from a region formed by the crystal growth whose growth interface is the plane **3p**.

**[0022]** The hollow cylindrical region **4** includes entire or substantially entire of the region formed by the crystal growth whose growth interfaces are the facet plane **4p** and the plane **4n**, and the solid columnar region **3** corresponds or substantially corresponds to the region formed by the crystal growth whose growth interface is the plane **3p**. Accordingly, the impurity concentrations of the hollow cylindrical region **4** and the solid columnar region **3** are different.

**[0023]** It is preferable to use the HVPE (hydride vapor phase epitaxy) method which can increase growth speed as a method to grow the group III nitride semiconductor single crystal **2**. In using the HVPE method, the impurity incorporated into the group III nitride semiconductor single crystal **2** during the epitaxial growth and caused of

the strain is often oxygen caused by a quartz member for using a furnace body.

**[0024]** Furthermore, the substrate **1** and the group III nitride semiconductor single crystal **2** may be made of same kind crystal (i.e. a GaN substrate and a GaN crystal), may be made of different kind crystal (i.e. a sapphire substrate and a GaN crystal). As the group III nitride semiconductor single crystal **2** grows homoepitaxially on the substrate **1** which is made of same kind crystal with the group III nitride semiconductor single crystal **2**, for instance, it is preferable to use high uniformity and low-dislocation density substrate made by the VAS (void-assisted separation) method such as disclosed in Japanese patent No. 3631724 as the substrate **1**. As the group III nitride semiconductor single crystal **2** is heteroepitaxially grown on the substrate **1** which is made of different kind crystal from the group III nitride semiconductor single crystal **2**, as thickness of the group III nitride semiconductor single crystal **2** increases, the group III nitride semiconductor single crystal **2** is easy to produce the crack. However, the crack can be suppressed by growing the crystal with intervening something of a strain relaxation layer in the hetero interface. For example, applying the technology shown in Japanese patent No. 3886341, it can decrease a dislocation density and suppress the crack caused by growth of thick film.

**[0025]** The distribution of the impurity concentration in the group III nitride semiconductor single crystal **2** can be confirmed easily as a contrast by observing emission of the group III nitride semiconductor single crystal **2** irradiated with excitation light such as ultraviolet light. Furthermore, the strain in the group III nitride semiconductor single crystal **2** can be detected by photo elasticity measurement or Raman measurement.

**[0026]** The region formed by the crystal growth whose growth interface are the facet plane **4p** and the plane **4n**, thus the region having different impurity concentration in the region formed by the crystal growth whose growth interface is the plane **3p** is often almost similar to a region where the strain arises, however the region where the strain arises is sometimes distributed larger than the region having different impurity concentration in the region formed by the crystal growth whose growth interface is the plane **3p**. In this case, it is preferable to remove the entire region where the strain arises, as obtaining strain field needs to a dedicated equipment, there are problems that a manufacturing process and a manufacturing cost increase.

**[0027]** As long as the method to remove the hollow cylindrical region **4** that is set as a hollow cylindrical region in which the upper surface includes the facet plane **4p** that can observe visually, even not available to remove the entire region having the strain, the strain can be removed even preventing forming the crack by slicing. Thus it can be suppressed to form the crack with short time and low costs.

**[0028]** Furthermore, even a hollow cylindrical region whose value is smallest, which satisfies "a hollow cylin-

dricial region whose upper surface includes the facet plane **4p** in the group III nitride semiconductor single crystal **2**" is set as the hollow cylindrical region **4**, the hollow cylindrical region **4** includes all or almost all region having the strain. Thus, even in this case, all or almost all region having the strain can be removed by removing the hollow cylindrical region **4** from the group III nitride semiconductor single crystal **2**.

[0029] Also, as the thickness of the hollow cylindrical region **4** increases and the hollow cylindrical region **4** includes by a region whose orientation at the upper surface is equal to the plane **3p** in the solid columnar region **3**, the region having the strain can be removed certainly. However, according as the thickness of the hollow cylindrical region **4** increases, the diameter of the solid columnar region **3** decreases and, therefore, a diameter of the semiconductor substrate obtained from the solid columnar region **3** decreases.

[0030] As shown in FIG.2, as the group III nitride semiconductor single crystal **2** is a GaN crystal whose plane **3p** is the c-plane, the facet plane **4p** is a (1-10X) plane (X is natural number), and appears at six-fold symmetrical position whose axis is the central axis of the group III nitride semiconductor single crystal **2** in the outer peripheral edge side of the upper surface of the group III nitride semiconductor single crystal **2**. Further, cross sections shown in FIG.1B and FIG.1C are suitable for a cross section which cut the substrate **1** and the group III nitride semiconductor single crystal **2** along with the A-A line.

[0031] The c-plane of the GaN crystal is the densest plane, and a region which the c-plane becomes the growth interface is characterized substantially poor incorporation of impurities such as oxygen compared with a region whose growth interface has the other orientation.

[0032] Also, as the HVPE method use generally a furnace member made of a quartz member with heating more than 1000 °C, silicon and oxygen which are produced by resolving the quartz are easy to incorporate in the group III nitride semiconductor single crystal **2** as impurity. Here, as the silicon has low dependency for the orientation of the growth interface in the group III nitride semiconductor single crystal **2** and uniformly incorporates as a whole, the silicon is often applied for a dopant to control an electric conductivity of the GaN crystal. Thus the distribution of the strain in the group III nitride semiconductor single crystal **2** caused by the silicon is not non-uniform, the background concentration in the silicon crystal as the impurity seldom occurs.

[0033] In the GaN crystal which is grown in c-plane using the HVPE method, depending on the growth condition, commonly, incorporates oxygen about  $10^{16}$  to  $10^{17}$  cm<sup>-3</sup>. However, in the region growing by the other growth interface excepting c-plane (the facet plane **4p** and the plane **4n**), incorporated is oxygen that the oxygen concentration is about  $10^{18}$  to  $10^{19}$  cm<sup>-3</sup>, which is ten to hundred as much as oxygen incorporated in the GaN crystal whose growth interface is the c-plane. As a result, the one GaN crystal has low oxygen concentration region

and high oxygen concentration region and strain filed appears in the outer peripheral edge side of the crystal.

(Removal of the hollow cylindrical region)

[0034] As described above, the strain in the group III nitride semiconductor single crystal **2** is caused by the distribution of the impurity concentration, the strain is distributed cylindrically in the outer peripheral edge side of the group III nitride semiconductor single crystal **2**, and it is balanced totally. However, in order to process the group III nitride semiconductor single crystal **2** including the strain, when cutting or removing a part of the outer periphery of the group III nitride semiconductor single crystal **2**, a part of the strain is released locally and a balance of the strain in the group III nitride semiconductor single crystal may be unbalanced and may form the crack.

[0035] Due to this, the removal of the hollow cylindrical region **4** is needed to be carried out such that a shape of the group III nitride semiconductor single crystal **2** always keeps an axial symmetry that a central axis of the semiconductor crystal is defined as a symmetrical axis so as not to break the balance of the strain in the group III nitride semiconductor single crystal **2** in removing the hollow cylindrical region **4** from the group III nitride semiconductor single crystal **2**. Herein, the axial symmetry is the same meaning of the rotational symmetry in n th symmetry (n is an arbitrary integer). In this case, removing the hollow cylindrical region **4** is progressed in the direction linear to the growth direction of the group III nitride semiconductor single crystal (the vertical direction of the principal plane **1p** of the substrate **1**).

[0036] For example, in case of removing the hollow cylindrical region **4** by grinding using a hollow cylindrical grindstone described below, ultrasonic processing using a hollow cylindrical ultrasonic processing tool, electric discharge processing using a hollow cylindrical sinker electric discharge electrode, or laser processing, removing the hollow cylindrical region **4** is applied such that a shape of the removed region is always kept into a hollow cylindrical shape with a uniform height.

[0037] A specific example of the method of removing the hollow cylindrical region will be described below.

[0038] FIGS.3A and 3B are vertical cross sectional views showing schematically the step for removing the hollow cylindrical region **4** by grinding using a hollow cylindrical grind stone **10**.

[0039] The hollow cylindrical grindstone **10** has an abrasive grain forming part **11** on an edge (bottom) of the grindstone **10**. The hollow cylindrical region **4** is removed slowly by contacting the grindstone **10** to the group III nitride semiconductor single crystal **2** from an upper side with rotating the abrasive grain with adjusting a rotational axis with the central axis of the group III nitride semiconductor single crystal **2**. According to this method, the hollow cylindrical region **4** can be removed such that the shape of the removed region is always kept into the

hollow cylindrical shape with uniform height. Moreover, a loose abrasive mixed in liquid can be used as the abrasive grain.

**[0040]** FIGS. 4A and 4B are the vertical cross sectional view showing schematically the step for removing a hollow cylindrical region 4 by electric discharge processing using a hollow cylindrical sinker electric discharge electrode 20.

**[0041]** The hollow cylindrical region 4 is removed slowly by rotating the hollow cylindrical sinker electric discharge electrode 20 with adjusting its rotational axis with the central axis of the group III nitride semiconductor single crystal 2, electric discharge processing between the sinker electric discharge electrode 20 and the group III nitride semiconductor single crystal 2, and contacting the sinker electric discharge electrode to the group III nitride semiconductor single crystal 2 from upper side. According to this method, the hollow cylindrical region 4 can be removed such that the shape of the removed region is always kept into the hollow cylindrical shape with uniform height.

**[0042]** Apart from that, the hollow cylindrical region 4 can be removed such that the shape of the removed region is always kept into the hollow cylindrical shape with uniform height using a cylindrical ultrasonic processing tool, or laser processing.

**[0043]** FIGS. 3A, 3B, 4A, and 4B show an example of removing the hollow cylindrical region 4 from the upper side of the group III nitride semiconductor single crystal 2, the hollow cylindrical region 4 may be removed from the side of the substrate 1. However, in this case, as a region of the substrate 1 just below the hollow cylindrical region 4 is also removed, the hollow cylindrical region 4 is needed to be removed from the side of the group III nitride semiconductor single crystal 2 for reusing the substrate 1 as the seed crystal.

**[0044]** FIG. 5 is a vertical cross sectional view showing a situation that a hollow cylindrical region 4 is removed from the side of a grown group III nitride semiconductor single crystal 2 and a region on the substrate 1 just below the hollow cylindrical region 4 is left. This substrate 1 can be reused as the seed crystal with forming semiconductor substrates by slicing the solid columnar region 3 of the remaining group III nitride semiconductor single crystal 2 and then grinding the principal plane 1p.

**[0045]** FIG. 6 is a vertical cross sectional view showing a substrate 1 on which a protective coat 30 for removing the hollow cylindrical region 4 selectively by etching is formed and a group III nitride semiconductor single crystal 2.

**[0046]** First, a protective film 30 made of SiO<sub>2</sub> etc. covers on the plane 3p of the solid columnar region 3 where does not intend to remove, and a region corresponding to the solid columnar region 3 on the opposite surface 1b to the group III nitride semiconductor single crystal 2. Then the hollow cylindrical region 4 is removed by gas phase etching or wet etching. As the gas phase etching, for example, reactive ion etching using BCl (boron trichlo-

ride) gas can be applied. Also as the wet etching, an etching can be used which uses hot phosphoric acid sulfuric acid etchant. By controlling properly condition of the etching, the hollow cylindrical region 4 can be removed such that the shape of the removed region is always kept into the hollow cylindrical shape with uniform height.

(Slicing of the solid columnar region)

**[0047]** Next, the solid columnar region 3 remaining by the removing of the hollow cylindrical region 4 is sliced.

**[0048]** FIGS. 7A and 7B are vertical cross sectional views showing schematically the step for slicing the solid columnar region 3. Herein, the dot-line shows the point of slicing the solid columnar region 3. Existing slicing technologies such as an inner peripheral blade slicer, an outer peripheral blade slicer, wire saw, or electric discharge machine can be used for slicing the solid columnar region 3.

**[0049]** After slicing the solid columnar region 3, the obtained circular semiconductor substrate 5 is beveled along an outer peripheral edge of the circular semiconductor substrate 5, and the front and rear surfaces of the circular semiconductor substrate 5 are ground.

**[0050]** As is clear from the manufacturing process of the semiconductor substrate 5 described above, the diameter of the semiconductor substrate 5 is smaller than the diameter of the substrate 1. Thus it is preferable to determine the diameter of the substrate 1 while considering the diameter of the semiconductor substrate 5 needed and the size of the hollow cylindrical region 4 to remove. Moreover, the diameter of the group III nitride semiconductor single crystal 2 may be reduced by a size smaller than the diameter of the substrate 1 so as to prevent the adhesion of the group III nitride semiconductor single crystal 2 and a growth jig.

[Second embodiment]

**[0051]** The second embodiment is different from the first embodiment in a means for removing the strain in the group III nitride semiconductor single crystal. Meanwhile, the explanation of the same as in the first embodiment is omitted or simplified below.

(Separating of the hollow cylindrical region)

**[0052]** In the present embodiment, the hollow cylindrical region 4 is a region which is separated from the solid columnar region 3 before slicing the solid columnar region 3. By separating the hollow cylindrical region 4 from the solid columnar region 3, as in the case of removing the hollow cylindrical region 4, it is possible to prevent the occurrence of the crack during the slicing of the solid columnar region 3.

**[0053]** The separating of the solid columnar region 3 and the hollow cylindrical region 4 is carried out by forming in the group III nitride semiconductor single crystal 2

a cylindrical cavity having a central axis which is similar to a central axis of the group III nitride semiconductor single crystal **2**. The cavity is preferably formed in a region which passes through a border of the facet plane **4p** and the plane **3p** or inside of the facet plane **4p** so as not to remain a region having high impurity concentration which causes the strain.

**[0054]** As in the case of removing the hollow cylindrical region **4** from the group III nitride semiconductor single crystal **2** in the first embodiment, the forming of the cavity is needed to be carried out such that a shape of the group III nitride semiconductor single crystal **2** always keeps an axial symmetry that the central axis of the group III nitride semiconductor single crystal **2** is defined as the symmetrical axis so as not to break the balance of the strain in the group III nitride semiconductor single crystal **2** as removing the hollow cylindrical region **4** from the solid columnar region **3**. In this case, the forming of the cavity is progressed in the direction of linear to the growth direction of the group III nitride semiconductor single crystal **2** (the vertical direction to the principal plane **1p** in the substrate **1**).

**[0055]** For example, when forming the cavity by drilling using a hole saw, grinding using a hollow cylindrical grindstone, an ultrasonic processing using a hollow cylindrical tool, an electric discharge processing using a hollow cylindrical sinker electric discharge electrode, or laser processing, which are described later, it is more preferable to form the cavity such that the shape of the cavity is always kept into the hollow cylindrical shape with a uniform height.

**[0056]** A specific example of the method of separating the hollow cylindrical region **4** will be described below.

**[0057]** **FIGS. 8A** and **8B** are vertical cross sectional views showing schematically the step for forming a cavity by using a hole saw **40** and separating the hollow cylindrical region **4** from the solid columnar region **3**.

**[0058]** The hole saw **40** has a blade **41** on an edge (bottom) thereof. As the hole saw **40** is rotated adjusting its rotational axis with the central axis of the group III nitride semiconductor single crystal **2**, the cavity is formed slowly while contacting the hole saw **40** with the group III nitride semiconductor single crystal **2**. According to the method, the cavity can be formed such that the shape of the cavity is always kept into the hollow cylindrical shape with a uniform height.

**[0059]** **FIG. 9** is a vertical cross sectional view showing a situation of the group III nitride semiconductor single crystal **2** after separating the hollow cylindrical region **4** from the solid columnar region **3**. The hollow cylindrical region **4** is separated from the solid columnar region **3** through the cavity **6**.

**[0060]** The cavity **6** can be formed by, other than using the hole saw **40**, for example, grinding using a hollow cylindrical grindstone whose thickness is close to the hole saw **40**, ultrasonic processing using a hollow cylindrical tool whose thickness is close to the hole saw **40**, electric discharge processing using a hollow cylindrical electric

discharge electrode whose thickness is close to the hole saw **40**, or laser processing.

**[0061]** After separating the hollow cylindrical region **4** from the solid columnar region **3**, the solid columnar region **3** is sliced after removing the hollow cylindrical region **4** from the substrate **1**. Also, the solid columnar region **3** can be sliced with the hollow cylindrical region **4** while remaining the hollow cylindrical region **4** surrounding the solid columnar region **3**. In this case, although the hollow cylindrical region **4** is broken, the solid columnar region **3** should not be broken.

**[0062]** Also, when reusing the substrate **1** as the seed crystal, as shown in **FIGS. 8A**, **8B**, and **FIG. 9**, the cavity **6** is formed from the side of the group III nitride semiconductor single crystal **2** so as to remain a region on the substrate just below the cavity **6** without removing. Then, after forming the semiconductor substrate by slicing the solid columnar region **3** in the group III nitride semiconductor single crystal **2**, the principal plane **1p** is polished and the substrate **1** is reused as the seed crystal.

(Functions and advantageous effects of the embodiment)

**[0063]** According to the first and second embodiments described above, the strain in the group III nitride semiconductor single crystal epitaxially grown can be removed while preventing the occurrence of the crack, whereby the semiconductor substrate can be obtained by slicing the group III nitride semiconductor single crystal without forming the crack.

**[0064]** Also, as the slicing is carried out after removing the strain in the group III nitride semiconductor single crystal, the strain remaining in the obtained semiconductor substrate can be reduced drastically and a warp of the semiconductor substrate can be reduced. Also, as the warp is reduced, the dispersion of the crystal orientation of the surface of the semiconductor substrate is reduced, and the characteristics dispersion of the device manufactured by the semiconductor substrate can be reduced. Also as the strain remaining in the semiconductor substrate is reduced, when manufacturing the device using the semiconductor substrate, the occurrence of any defect such as break or lack in the semiconductor device can be prevented.

**[0065]** Besides, the first and second embodiments are especially effective in manufacturing the group III nitride single crystal substrate, especially the GaN substrate whose principal plane is the c-plane. As a region whose growth interface is the c-plane in which an arrangement of atoms is dense is hard to incorporate the impurity atoms as compared with a region whose growth interface is the other plane. This is because, in the c-plane grown GaN crystal, the difference of impurity concentration between the region in the outer peripheral edge side that the facet plane is likely to appear and the inner region thereof tends to increase, so that a large strain is likely to accumulate.



**[0066]** Also, the crystal is likely to break according as the caliber increases, the defect density lowers or the crystalline property becomes uniform. This is because there is less defect region such as a dislocation or inversion domain, which has a property of absorbing or relaxing the strain. Thus, the first and second embodiments are especially effective in manufacturing the semiconductor substrate which has a large diameter (for example, a diameter more than **50** mm), less pit or inversion domain, and a low dislocation density (for example, less than  $10^7$  cm<sup>-2</sup>).

**[0067]** Although the first embodiment, as the specific example is explained about the GaN crystal with c-plane growth, if there is a difference between the impurity concentrations in the outer peripheral edge side region and in the inner region thereof in the GaN crystal, it is also effective in the case that the GaN crystal is grown in the different direction than the c-plane. Also, a crystal other than the GaN crystal, such as AlN, AlGaIn, InGaIn, AlInGaIn or a crystal having a laminated structure thereof may be used for manufacturing the semiconductor substrate. Also, the growth orientation of the group III nitride semiconductor single crystal may have an off angle.

#### [Examples]

**[0068]** Examples of semiconductor substrates manufactured based on the embodiments will be described below as well as evaluations thereof.

**[0069]** In the present Examples, as the group III nitride semiconductor single crystal **2** in the embodiment described above, the GaN crystal is epitaxially grown using the HVPE method. First, a step for growing the GaN crystal using the HVPE method will be explained.

**[0070]** **FIG. 10** is a vertical cross sectional view showing schematically a configuration of an HVPE growing machine using for crystal growth of the GaN crystal. The HVPE growing machine **50** comprises a heater that has two zones of a raw material heater **51** heating to about **800** °C in the crystal growth and a crystal growth region heater **52** heating to about **1000**°C, and a reaction tube **53** made of quartz interposed in the heater.

**[0071]** An introducing pipe for material gas is arranged at an upstream side of the quartz reaction tube **53**. Ammonia gas which is a source of group V material is introduced into a furnace through an ammonia gas introducing pipe **57**. Metallic gallium **56** which is a source of group III material is detained in a quartz boat, and mounted in a region where the gallium material heating heater **51**. As the crystal grows, hydrochloric acid gas is flown into the boat through a quartz hydrochloric acid gas introducing pipe **58**. Then gallium chloride gas is generated by the reaction of the metallic gallium **56** and the hydrochloric acid gas, and is sent to the surface of the substrate **1** through a pipe. The gallium chloride and the ammonia reaction on the surface of the substrate **1** heated, and the GaN crystal is grown. For the inside of the furnace, doping gas can be flown through a doping gas introducing

pipe **59**. The substrate **1** which becomes the base of crystal growing is fixed by a substrate holder **54** supported by a rotational axis **55**, and is rotated during the crystal growth. Gas introduced into the reaction pipe is led to detoxicating equipment through a downstream exhaust pipe **80**. Then the gas is exhausted to atmosphere after the detoxification.

#### (Example 1)

**[0072]** A GaN crystal is grown on a GaN substrate as the substrate **1** which is made by the VAS method, and has a c-plane as the principal plane and a diameter of **62** mm, by using the HVPE growing machine **50**. The conditions of gas flow rate in the HVPE growth are **900** sccm for hydrogen gas as carrier gas, **8100** sccm for nitrogen gas, gas **180** sccm for gallium chloride, **500** sccm for ammonium gas. Growth pressure is **100** kPa, a substrate temperature during the growth is **1070** °C, and growth time is **15** hours. The substrate **1** is rotated by **5** rpm during the growth, and is doped with silicon by about  $10^{18}$  cm<sup>-3</sup> by supplying dichlorosilane as a doping material gas toward a substrate region. Consequently, a silicon doped GaN crystal with a thickness of about **4.5** mm is grown on the substrate **1**.

**[0073]** When a fluorescence image is observed by irradiating ultraviolet rays from a mercury lamp toward a surface of thus obtained GaN crystal, a dark ring region with a width of about **3** mm is observed at an outer peripheral edge of the crystal. Also, when the crystal is measured by photo elasticity, a region is observed which has high strain at the outer peripheral edge of the crystal corresponding to the dark region observed by the fluorescence image.

**[0074]** Next, using the hollow cylindrical grindstone **10** shown in **FIGS. 3A, 3B**, the hollow cylindrical region **4** in the GaN crystal is ground slowly, and the solid columnar region **3** with a diameter of **56** mm is thus left. Next, by slicing the solid columnar region **3** of the GaN crystal using the wire saw, five GaN free-standing substrates with a thickness of **630** μm are obtained. Then, the outer peripheral edge of the obtained GaN free-standing substrates is beveled and formed such that they have a diameter of **50.8** mm. After forming an orientation flat and an index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrates is **400** to **450** μm.

**[0075]** During the above processing, any defect such as crack or chipping is not caused in the GaN crystal. Also, the warps (BOW) of the substrates are all within **10** μm. When a dislocation density of one of the obtained GaN free-standing substrate is counted using the cathode luminescence method,  $6.2 \times 10^5$  cm<sup>-2</sup> in averages in the plane is obtained. When a dispersion in inclination of the c-plane in the surface of the substrate is measured using the X-ray diffraction method, it falls within  $\pm 0.05$  ° in the plane for all of the substrates.

(Comparative Example)

[0076] When the GaN crystal grown by the similar method to Example 1 is sliced without removing the hollow cylindrical region 4 by using wire saw, the GaN crystal is broken into two with the crack occurred upon making a cut by wire. Thus, the test process cannot be continued.

(Example 2)

[0077] An undoped GaN layer is grown by 400 nm on a single crystal sapphire substrate which has a c-plane as the principal plane and a diameter of 58 mm, by using the MOCVD method where tri-methyl-gallium and ammonia are used as source materials. Then a titanium metal film is deposited by 20 nm thereon. This substrate as the substrate 1 is put in the HVPE growing machine 50. By thermally treating it in flow of ammonia gas mixed with 20% hydrogen gas at 1050°C for 30 minutes, the titanium metal film on the surface of the substrate 1 is changed into a mesh-like titanium nitride film and a number of microscopic voids are simultaneously generated on the GaN layer. Next, a silicon doped GaN crystal is grown by 7 mm in thickness by using dichlorosilane as dopant while supplying ammonia and gallium chloride onto the substrate 1 in the HVPE growing machine 50. In the crystal growth, hydrogen and nitrogen mixed gas is used as carrier gas and the GaN crystal is embedded in the void of the substrate 1 by optimizing the composition ratio of the gas is adjusted so as not to peel off the GaN crystal from the substrate 1 during the growth.

[0078] According to the fluorescence image obtained by irradiating ultraviolet rays from a mercury lamp toward a surface of thus obtained GaN crystal, a dark ring region with a width of about 3 mm is observed at an outer peripheral edge of the crystal.

[0079] Next, the GaN crystal is separated into the solid columnar region 3 with a diameter of 52 mm and the hollow cylindrical region 4 using a cylindrical grinding stone whose shape is close to the hole saw 8 shown in FIG.8A, 8B. Next, by slicing the solid columnar region 3 of the GaN crystal using the wire saw, eight GaN free-standing substrates with a thickness of 650 μm are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they have a diameter of 50.0 mm. After forming the orientation flat and index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrates is 400 to 450 μm. During the processing described above, any defect such as crack or chipping is not caused in the GaN crystal.

(Example 3)

[0080] A GaN off substrate which the principal plane inclined at 2° from the c-plane forward the m-axis defines the substrate 1, a GaN crystal having inclined crystal ori-

entation is grown as with the method according to the Example 1. Next, the obtained GaN crystal is separated into the solid columnar region 3 with a diameter of 56 mm and the hollow cylindrical region 4 by ultrasonic processing using the ultrasonic machine. The ultrasonic processing is carried out slowly with supplying diamond slurry using a hollow cylindrical cutter whose shape is close to the hole saw 8 shown in FIG.8A, 8B. Next, by slicing the solid columnar region 3 of the GaN crystal using the wire saw, five GaN free-standing substrates with a thickness of 630 μm are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they are 50.8 mm in diameter. After forming the orientation flat and index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrate is 400 to 450 μm.

[0081] During the above processing, any defect such as crack or chipping is not caused in the GaN crystal. Also, when a c-plane off angle and a dispersion of the c-plane off angle in the plane of the obtained GaN free-standing substrates are measured using X-ray diffraction method, they fall within  $2 \pm 0.05^\circ$  in the plane for all of the substrates.

(Example 4)

[0082] By the similar method to Example 1, using as the substrate 1 the GaN substrate which is made by the VAS method, whose principal plane is the c-plane and whose diameter is 62 mm, the silicone doped GaN crystal is grown about 3 mm thick thereon using the HVPE method.

[0083] Next, the hollow cylindrical region 4 of the obtained GaN crystal is removed slowly by the laser processing using the laser processor such that the solid columnar region 3 with a diameter of 55 mm remains. The laser processing is carried out in single mode with a wave length of 532 nm, and at a maximum power of 5w. The hollow cylindrical region 4 is removed by irradiating the laser on the surface of the GaN substrate and rotating it many times at a speed of 10 mm/sec. Next, by slicing the solid columnar region 3 of the GaN crystal using the wire electric discharge processor, three GaN free-standing substrates with a thickness of 680 μm are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they have a diameter of 50.0 mm. After forming the orientation flat and index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrates is 400 to 450 μm. During the above processing, any defect such as crack or chipping is not caused in the GaN crystal.

(Example 5)

**[0084]** By the similar method to Example 1, using as the substrate **1** the GaN substrate which is made by the VAS method, whose principal plane is the c-plane and whose diameter is **62** mm, the silicone doped GaN crystal is grown about **4** mm thick thereon using the HVPE method.

**[0085]** Next, using the hollow cylindrical sinker electric discharge electrode **20** shown in **FIGS.4A, 4B**, the hollow cylindrical region **4** in the GaN crystal is removed slowly such that the solid columnar region **3** with a diameter of **56** mm remains. Then, by slicing the solid columnar region **3** of the GaN crystal using the wire electric discharge processor, five GaN free-standing substrates with a thickness of **630**  $\mu\text{m}$  are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they have a diameter of **50.8** mm. After forming the orientation flat and index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrates is **400** to **450**  $\mu\text{m}$ . During the above processing, any defect such as crack or chipping is not caused in the GaN crystal.

(Example 6)

**[0086]** By the similar method to Example 1, using as the substrate **1** the GaN substrate which is made by the VAS method, whose principal plane is the c-plane and whose diameter is **62** mm, the silicone doped GaN crystal is grown about **3** mm thick thereon using the HVPE method.

**[0087]** Next, the protection film **30** shown in **FIG.6** is formed on the front surface of the obtained GaN crystal and the rear surface of the substrate **1**. The protection film **30** is a film which is made of  $\text{SiO}_2$ , and whose diameter is **58** mm. After forming the protection film **30**, the GaN crystal covered with the protection film **30** is soaked in the mixed liquid including phosphate and sulfuric acid that is heated by **230**  $^{\circ}\text{C}$  in **12** hours. Thereby, the hollow cylindrical region **4** with the front surface and rear surface not covered by the protection film **30** is removed by etching from the side of the rear surface (N-surface). After etching the GaN crystal, the protection film **30** is removed by soaking the GaN crystal in a dilute hydrofluoric acid. Thus, the solid columnar region **3** with a diameter of **56** mm is obtained (the diameter of the solid columnar region **3** reduced by a size smaller than the diameter of the protection film **3**).

**[0088]** Next, by slicing the solid columnar region **3** of the GaN crystal using the wire saw, three GaN free-standing substrates with a thickness of **630**  $\mu\text{m}$  are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they have a diameter of **50.8** mm. After forming the orientation flat and index flat on the substrate, the front and rear surfaces

of the substrate are mirror polished such that the thickness of the substrate is **400** to **450**  $\mu\text{m}$ .

(Example 7)

**[0089]** By the similar method to Example 1, using as the substrate **1** the GaN substrate which is made by the VAS method, whose principal plane is the c-plane and whose diameter is **62** mm, the silicone doped GaN crystal is grown about **4** mm thick thereon using the HVPE method.

**[0090]** Next, using the sinker electric discharge electrode **20** having cylindrical shape shown in **FIGS.4A, 4B**, the hollow cylindrical region **4** in the GaN crystal is removed slowly such that the solid columnar region **3** with a diameter of **56** mm remains. Here, the substrate **1** is not processed by the electric discharging processor, as in the substrate **1** shown in **FIG.5**, the region just below the hollow cylindrical region **4** is left.

**[0091]** Next, by slicing the solid columnar region **3** of the GaN crystal using the wire electric discharge processor, five GaN free-standing substrates with a thickness of **630**  $\mu\text{m}$  are obtained. Then, by beveling the outer peripheral edge of the obtained GaN free-standing substrates, the GaN free-standing substrates are formed such that they have a diameter of **50.8** mm. After forming the orientation flat and index flat on the substrate, the front and rear surfaces of the substrate are mirror polished such that the thickness of the substrates is **400** to **450**  $\mu\text{m}$ . During the above processing, any defect such as crack or chipping is not caused in the GaN crystal.

**[0092]** Then, after the GaN free-standing substrates are obtained, the substrate **1** left is reused as the seeding crystal by planarizing the surface thereof using a grinding machine and mirror polishing it. The same manufacturing method of the GaN free-standing substrate as described above is conducted using the reused substrate **1**. As a result, obtained is the GaN free-standing substrate whose quality is equivalent to that of the original substrate **1**. Thereby, it is confirmed that the GaN substrate can be repeatedly used as the substrate **1**.

**[0093]** Although the embodiments and the Examples have been described, the invention is not to be limited to the embodiments and the Examples. The various kind of modifications can be implemented without departing from the gist of the invention.

**[0094]** Also, the invention is not to be limited to the embodiments and the Examples. Further, it should be noted that all combinations of the features described in the embodiments and the Examples are not necessary to solve the problems of the invention.

[Industrial Applicability]

**[0095]** A method for manufacturing a semiconductor substrate can be provided that allows the manufacture of the semiconductor substrate by slicing the epitaxial grown group III nitride semiconductor single crystal while

preventing growing the crack.

[Reference Signs List]

[0096]

1: SUBSTRATE  
 1p: PRINCIPAL PLANE  
 2: GROUP III NITRIDE SEMICONDUCTOR SINGLE CRYSTAL  
 3: SOLID COLUMNAR REGION  
 3p: PLANE  
 4: HOLLOW CYLINDRICAL REGION  
 4p: FACET PLANE  
 5: SEMICONDUCTOR SUBSTRATE  
 6: CAVITY  
 10: GRINDSTONE  
 20: SINKER ELECTRIC DISCHARGE ELECTRODES  
 30: PROTECTION FILM  
 40: HOLE SAW  
 50: HVPE GROWING MACHINE

#### Claims

1. A method for manufacturing a semiconductor substrate, comprising:

epitaxially growing a columnar group III nitride semiconductor single crystal on a principal plane of a circular substrate;  
 removing a hollow cylindrical region at an outer peripheral edge side of the group III nitride semiconductor single crystal to leave a solid columnar region at an inside of the hollow cylindrical region of the group III nitride semiconductor single crystal; and  
 slicing the solid columnar region after removing the hollow cylindrical region,  
 wherein the removing of the hollow cylindrical region is carried out such that a shape of the group III nitride semiconductor single crystal always keeps an axial symmetry that a central axis of the semiconductor crystal is defined as a symmetry axis.

2. The method according to claim 1, wherein the hollow cylindrical region comprises a region that has a concentration of an impurity that is different from that in the solid columnar region.

3. The method according to claim 1 or 2, wherein the hollow cylindrical region comprises a region formed by a crystal growth using a plane that has a different orientation from an orientation in an upper surface of the solid columnar region as a growth interface in the epitaxial growth of the group III nitride semiconductor single crystal.

4. The method according to claim 1 or 2, wherein the hollow cylindrical region comprises a facet plane having a plane orientation different from that in the upper surface of the hollow cylindrical region.

5. The method according to claim 1 or 2, wherein the removing of the hollow cylindrical region is carried out such that a shape of the removed region is always kept into a hollow cylindrical shape with a uniform height.

6. The method according to claim 1 or 2, wherein the removing of the hollow cylindrical region is carried out by grinding using a grindstone, ultrasonic processing, electric discharge processing, etching, or laser processing.

7. The method according to claim 1 or 2, wherein the group III nitride semiconductor single crystal is a gallium nitride crystal.

8. The method according to claim 1 or 2, wherein an upper surface of the solid columnar region is a c-plane of the group III nitride semiconductor single crystal.

9. The method according to claim 2, wherein the group III nitride semiconductor single crystal is a gallium nitride crystal epitaxially grown by HVPE method, and the impurity is oxygen.

10. The method according to claim 1 or 2, wherein the removing of the hollow cylindrical region is carried out such that a region of the substrate just below the hollow cylindrical region is not removed.

11. The method according to claim 10, wherein the principal plane of the substrate is ground after slicing the solid columnar region such that the substrate is re-used as a seed crystal.

12. A method for manufacturing a semiconductor substrate, comprising:

epitaxially growing a columnar group III nitride semiconductor single crystal on a principal plane of a circular substrate;  
 forming a cylindrical cavity in the group III nitride semiconductor single crystal to separate the group III nitride semiconductor single crystal into a hollow cylindrical region at an outer peripheral edge side of the group III nitride semiconductor single crystal and a solid columnar region at an inside of the hollow cylindrical region of the group III nitride semiconductor single crystal; and  
 slicing the solid columnar region after separating the group III nitride semiconductor single crystal

into the hollow cylindrical region and the solid columnar region,  
wherein the forming of the cavity is carried out such that a shape of the group III nitride semiconductor single crystal always keeps an axial symmetry that a central axis of the semiconductor crystal is defined as a symmetry axis.

13. The method according to claim 12, wherein the hollow cylindrical region comprises a region that has a concentration of an impurity that is different from that in the solid columnar region. 10
14. The method according to claim 12 or 13, wherein the hollow cylindrical region comprises a region formed by a crystal growth using a plane that has a different orientation from an orientation in an upper surface of the solid columnar region as a growth interface in the epitaxial growth of the group III nitride semiconductor single crystal. 15 20
15. The method according to claim 12 or 13, wherein the hollow cylindrical region comprises a facet plane having a plane orientation different from that in the upper surface of the hollow cylindrical region. 25
16. The method according to claim 12 or 13, wherein the removing of the hollow cylindrical region is carried out such that a shape of the removed region is always kept into a hollow cylindrical shape with a uniform height. 30
17. The method according to claim 12 or 13, wherein the removing of the hollow cylindrical region is carried out by drilling using a hole saw, grinding using a grindstone, ultrasonic processing, electric discharge processing, or laser processing. 35
18. The method according to claim 12 or 13, wherein the group III nitride semiconductor single crystal is a gallium nitride crystal. 40
19. The method according to claim 12 or 13, wherein an upper surface of the solid columnar region is a c-plane of the group III nitride semiconductor single crystal. 45
20. The method according to claim 13, wherein the group III nitride semiconductor single crystal is a gallium nitride crystal epitaxially grown by HVPE method, and the impurity is oxygen. 50
21. The method according to claim 12 or 13, wherein the hollow cylindrical region is removed before slicing the solid columnar region. 55
22. The method according to claim 12 or 13, wherein the solid columnar region is sliced along with the hollow

cylindrical region while the hollow cylindrical region remains around the solid columnar region.

23. The method according to claim 12 or 13, wherein the forming of the cavity is carried out such that a region of the substrate just below the hollow cylindrical region is not removed.
24. The method according to claim 23, wherein the principal plane of the substrate is ground after slicing the solid columnar region such that the substrate is re-used as a seed crystal.

FIG. 1A



FIG. 1B

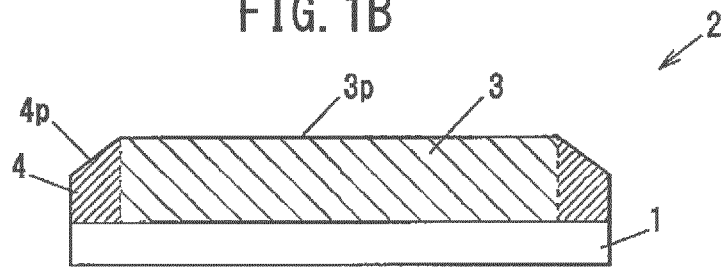


FIG. 1C

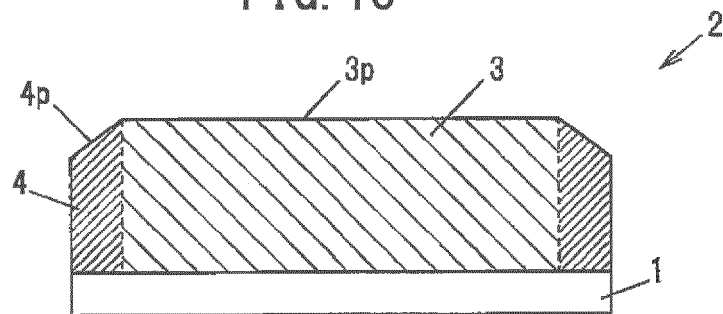


FIG. 2

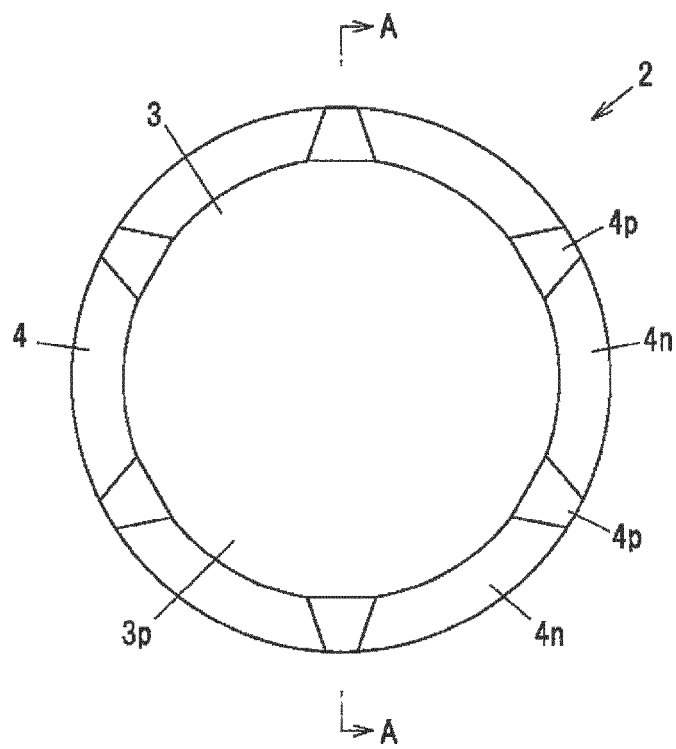


FIG. 3A

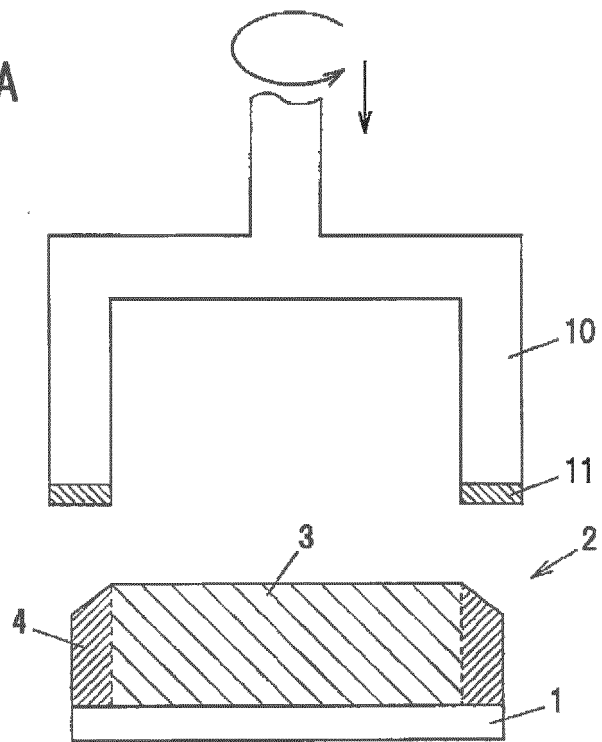


FIG. 3B

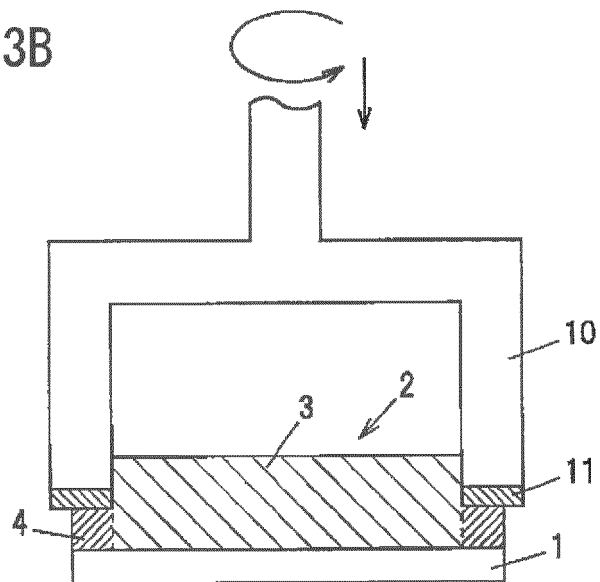




FIG. 4A

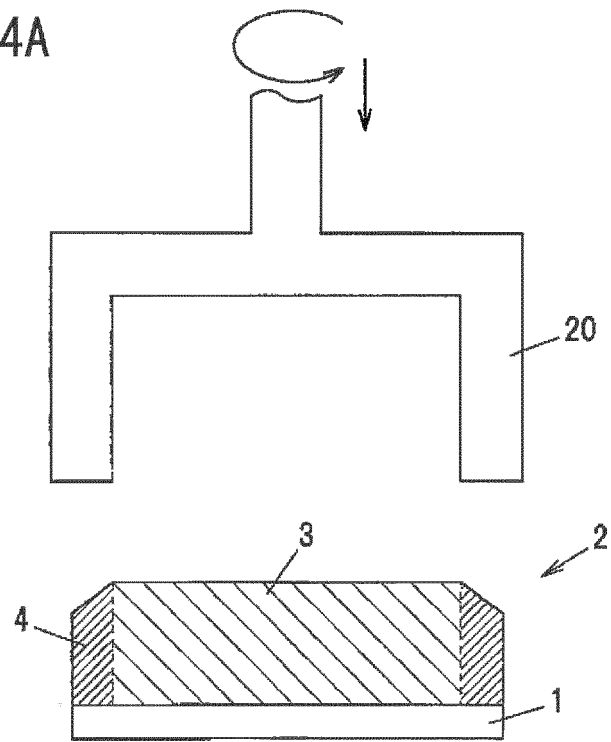


FIG. 4B

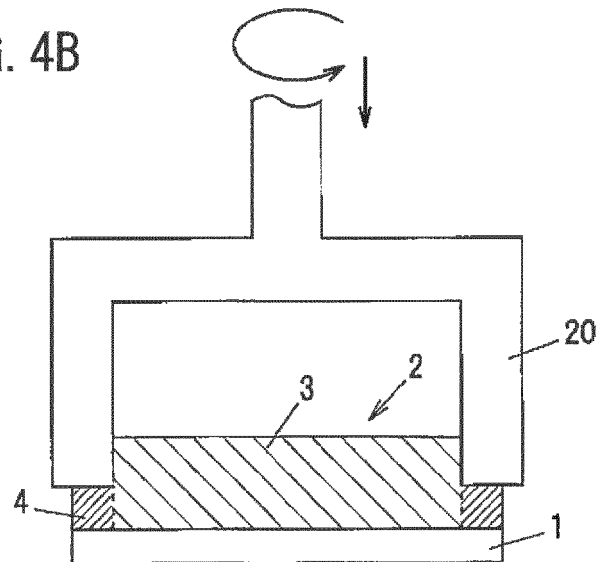


FIG. 5

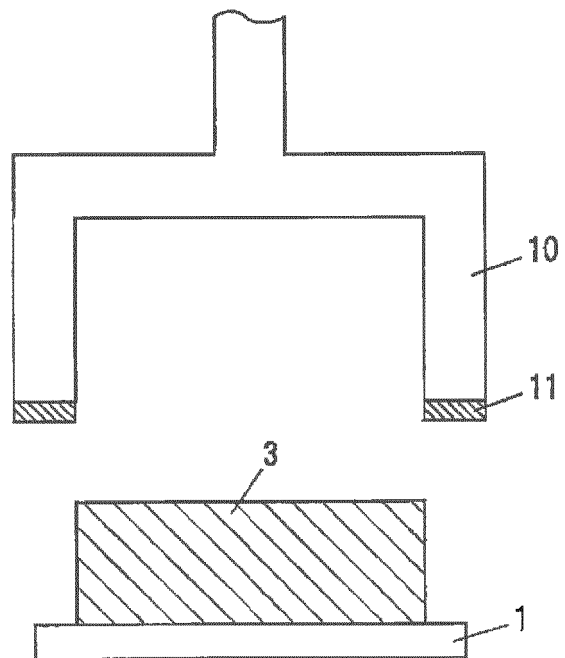


FIG. 6

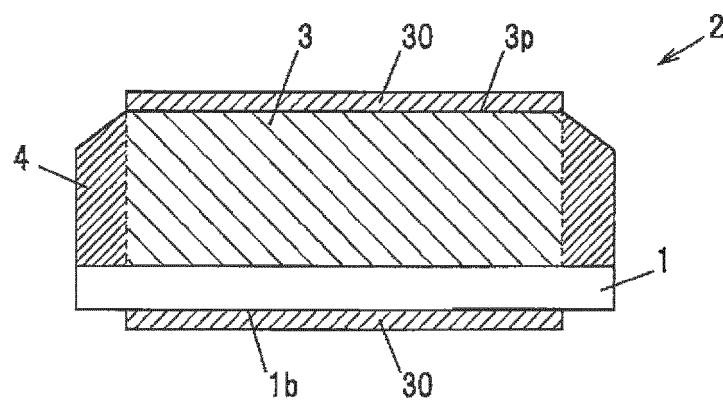


FIG. 7A

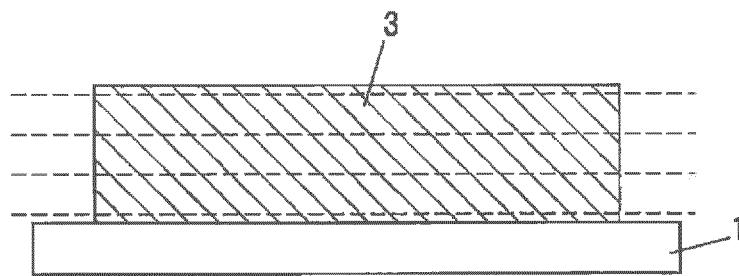


FIG. 7B

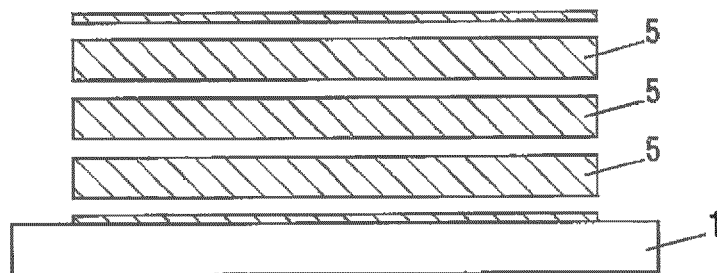


FIG. 8A

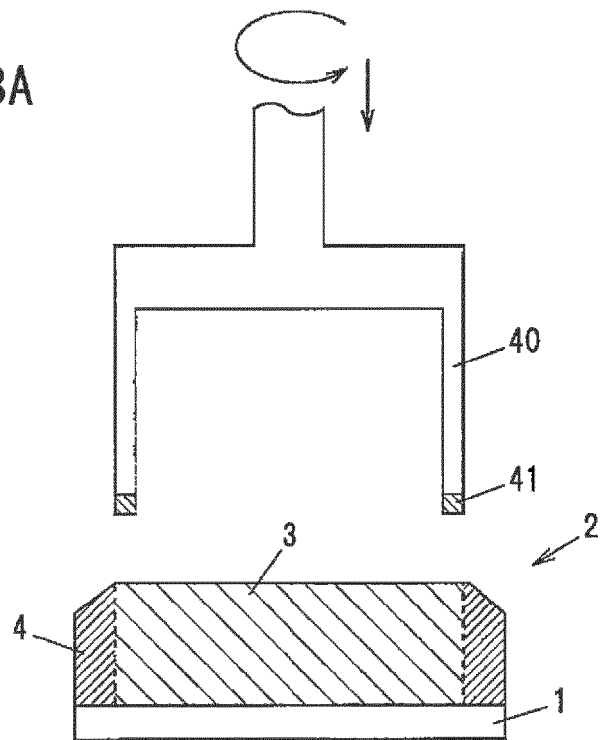


FIG. 8B

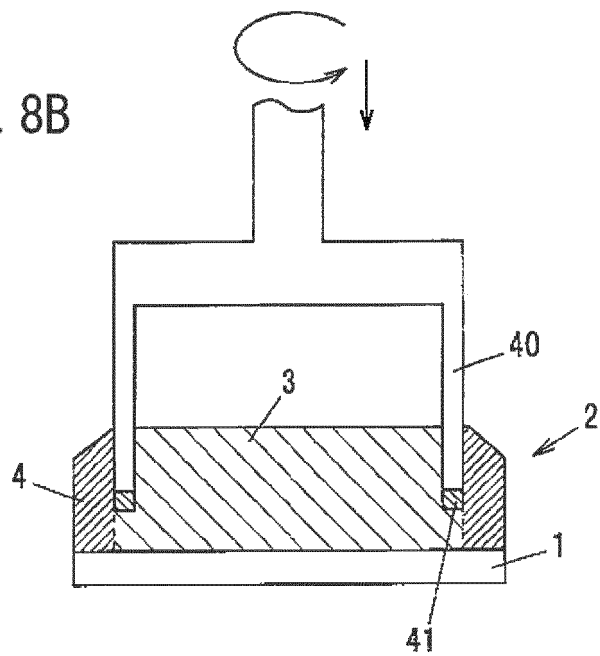


FIG. 9

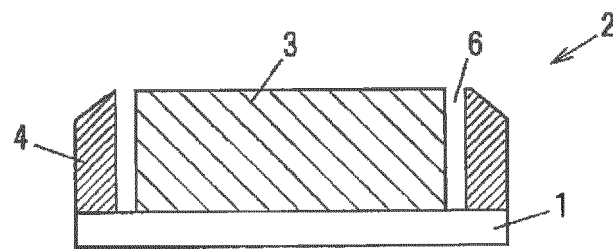
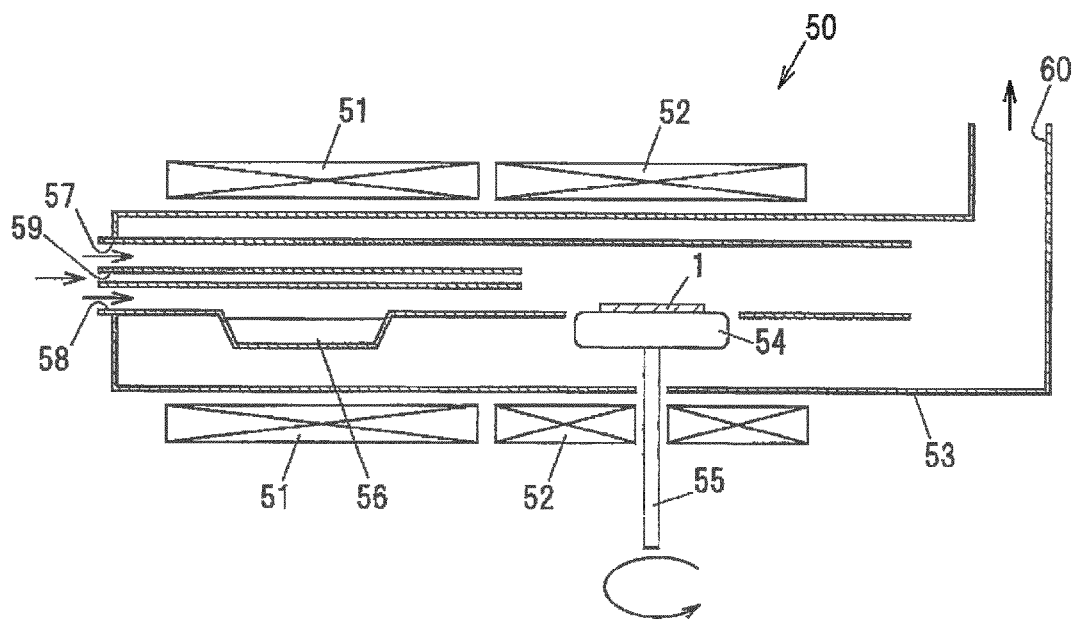


FIG. 10



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2014/051806

## A. CLASSIFICATION OF SUBJECT MATTER

C30B29/38(2006.01)i, H01L21/205(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C30B1/00-35/00, H01L21/205

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2014

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CAplus(STN), WPI, Science Direct, JSTPlus/JMEDPlus/JST7580(JDreamIII),  
CiNii

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2006-97058 A (Sumitomo Electric Industries, Ltd.), 13 April 2006 (13.04.2006), claims 1 to 5; paragraphs [0020] to [0035]; fig. 1 to 6 (Family: none)	1-3, 5-7, 9, 10 4, 8, 11 12-24
X Y A	JP 2009-161430 A (Sumitomo Electric Industries, Ltd.), 23 July 2009 (23.07.2009), claims 1 to 7; paragraphs [0022] to [0042]; fig. 1 to 7 (Family: none)	1-3, 5-7, 9-10 4, 8, 11 12-24

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

\* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

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"&amp;" document member of the same patent family

Date of the actual completion of the international search  
19 February, 2014 (19.02.14)Date of mailing of the international search report  
18 March, 2014 (18.03.14)Name and mailing address of the ISA/  
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2014/051806

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2013-60349 A (Hitachi Cable, Ltd.), 04 April 2013 (04.04.2013), paragraphs [0015], [0019], [0030] to [0034]; fig. 4, 5 & US 2013/0072005 A1	4, 8, 11
A	JP 2007-197240 A (Hitachi Cable, Ltd.), 09 August 2007 (09.08.2007), claims 1 to 4; paragraphs [0018] to [0030]; fig. 1, 2 (Family: none)	1-24
A	JP 2007-81372 A (Freiberger Compound Materials GmbH), 29 March 2007 (29.03.2007), paragraphs [0063], [0084] & US 2007/0012242 A1 & US 2009/0104423 A1 & EP 1739213 A1 & DE 102005030851 A	1-24
A	JP 2006-298744 A (Mitsubishi Chemical Corp.), 02 November 2006 (02.11.2006), paragraphs [0014] to [0069]; fig. 1, 2 & US 2008/0308812 A1 & EP 1790759 A1 & WO 2006/013957 A1 & KR 10-2007-0058465 A & CN 101035933 A	1-24
A	JP 2002-343728 A (NEC Corp.), 29 November 2002 (29.11.2002), claims 1 to 23 & US 2003/0017685 A1 & US 2005/0029507 A1 & EP 1271627 A2 & TW 544753 B & KR 10-2002-0089194 A & CN 1387231 A	1-24
A	JP 2003-178984 A (NEC Corp.), 27 June 2003 (27.06.2003), claims 1 to 27 & US 2002/0197825 A1 & EP 1246233 A2 & TW 533607 B & KR 10-2002-0076198 A & CN 1378237 A	1-24
A	E. RICHTER et al., Growth of GaN boules via vertical HVPE, Journal of Crystal Growth, 2011. 12.14, Vol.350, pp.89-92	1-24

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**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- JP 2013060349 A [0005]
- JP 3631724 B [0024]
- JP 3886341 B [0024]