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(54) **A GRAPHENE-BASED FIELD-EFFECT APPARATUS AND ASSOCIATED METHODS**

(57) A method comprising:
growing a layer of channel material (501), preferably graphene, on a growth wafer (512) to form a channel member, the growth wafer comprising a layer of catalyst material (511) separated from a carrier wafer (512) by a layer of release material (513), the catalyst material serving as a seed layer for growing the layer of channel material;
depositing a layer of polymeric material (502) over the formed channel member to form a supporting substrate for the layers of catalyst and channel material;
etching the layer of release material (513) to remove the release material and carrier wafer; and
patterning the layer of catalyst material (511) to form source and drain electrodes (516) configured to enable a flow of electrical current through the channel member.

Figure 5a

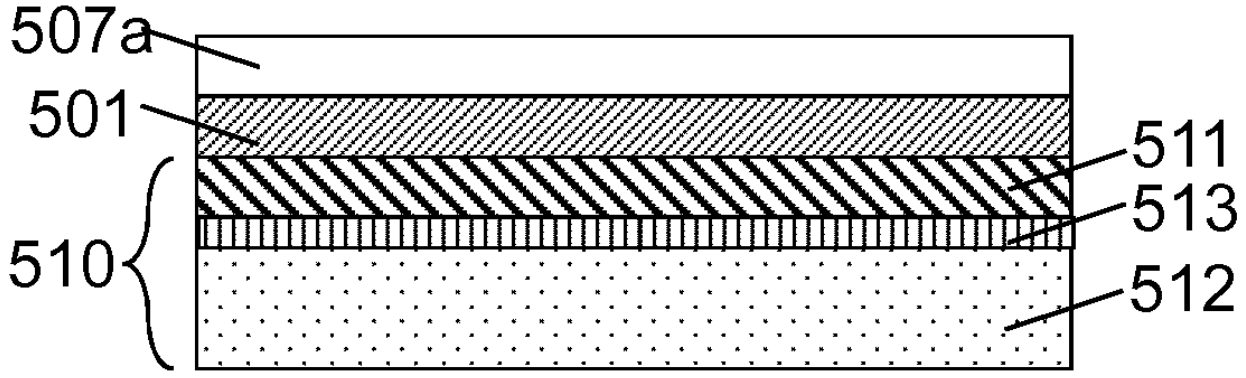

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Figure 5b

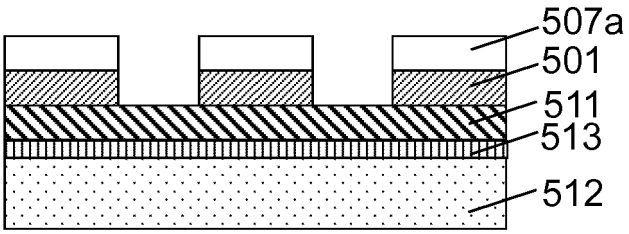

Figure 5c

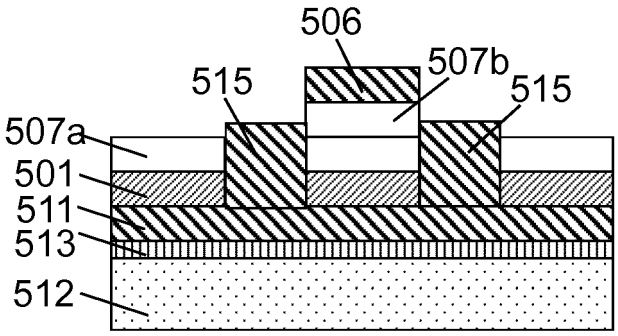

Figure 5d

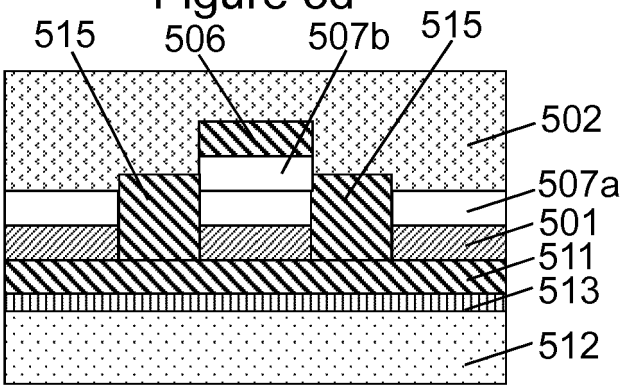

Figure 5e

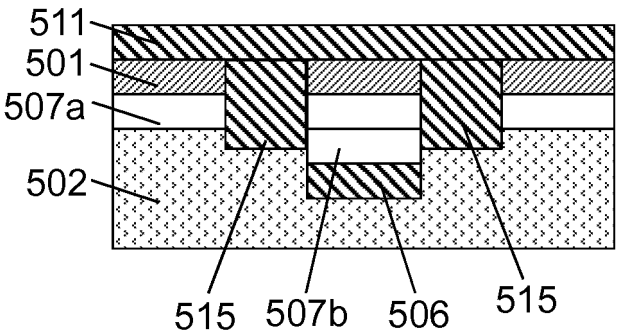

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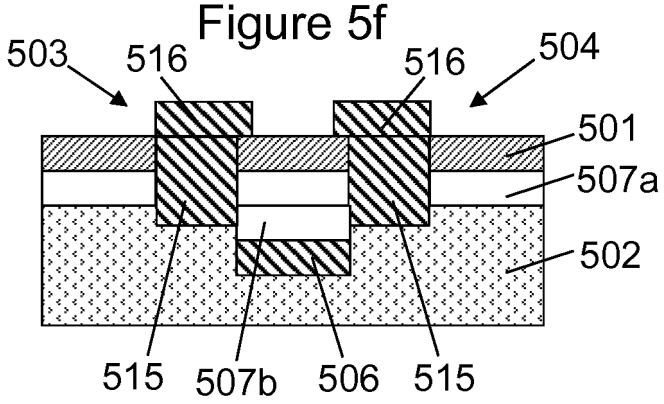
Figure 5f



Description

Technical Field

[0001] The present disclosure relates particularly to field-effect devices, associated methods and apparatus. Certain embodiments specifically concern a method of making a field-effect apparatus which results in less contamination in the end product than prior art methods. This reduction in contamination can provide an increase in charge carrier mobility and a reduction in contact resistance. Certain aspects/embodiments may relate to sensing (e.g. biosensing, optical sensing, deformation sensing, etc) for healthcare, automotive or wearable applications. Other aspects/embodiments may relate to field-effect transistors suitable for portable electronic devices, in particular, so-called hand-portable electronic devices which may be hand-held in use (although they may be placed in a cradle in use). Such hand-portable electronic devices include so-called Personal Digital Assistants (PDAs) and tablet PCs.

[0002] The portable electronic devices/apparatus according to one or more disclosed example aspects/embodiments may provide one or more audio/text/video communication functions (e.g. tele-communication, video-communication, and/or text transmission, Short Message Service (SMS)/ Multimedia Message Service (MMS)/emailing functions, interactive/non-interactive viewing functions (e.g. web-browsing, navigation, TV/program viewing functions), music recording/playing functions (e.g. MP3 or other format and/or (FM/AM) radio broadcast recording/playing), downloading/sending of data functions, image capture function (e.g. using a (e. g. in-built) digital camera), and gaming functions.

Background

[0003] Research is currently being done to develop new field-effect devices with improved physical and electrical properties for use in a variety of applications.

[0004] The listing or discussion of a prior-published document or any background in this specification should not necessarily be taken as an acknowledgement that the document or background is part of the state of the art or is common general knowledge.

Summary

[0005] According to a first aspect, there is provided a method comprising:

growing a layer of channel material on a growth wafer to form a channel member, the growth wafer comprising a layer of catalyst material separated from a carrier wafer by a layer of release material, the catalyst material serving as a seed layer for growing the layer of channel material;
depositing a layer of polymeric material over the formed channel member to form a supporting substrate for the layers of catalyst and channel material;
etching the layer of release material to remove the release material and carrier wafer; and
patterning the layer of catalyst material to form source and drain electrodes configured to enable a flow of electrical current through the channel member.

[0006] The method may comprise depositing respective layers of dielectric and conductive material on the channel member such that the layer of conductive material is separated from channel member by the layer of dielectric material, the layer of conductive material forming a gate electrode configured to enable the flow of electrical current through the channel member to be varied by a voltage applied to the gate electrode.

[0007] The method may comprise depositing the layers of dielectric and conductive material between the channel member and supporting substrate to form a back gate electrode.

[0008] The method may comprise depositing the layers of dielectric and conductive material such that the supporting substrate is separated from the layers of dielectric and conductive material by the channel member to form a top gate electrode.

[0009] The method may comprise patterning the layers of channel and conductive material to form a plurality of gated channel members.

[0010] The method may comprise patterning one or more of the layers of catalyst and conductive material to form at least one of a common source, common drain and common gate electrode for the plurality of gated channel members and/or at least one of a respective source, respective drain and respective gate electrode for each gated channel member.

[0011] Patterning the layer of channel material may comprise pre-patterning the layer of catalyst material before growing the layer of channel material to form the plurality of channel members by selective growth.

[0012] Patterning the layer of channel material may comprise:

depositing respective layers of dielectric material and photoresist on the layer of channel material such that the photoresist is separated from the layer of channel material by the layer of dielectric material;
patterning the layer of photoresist; and
etching the layers of channel and dielectric material through the patterned layer of photoresist.

[0013] Forming the source and drain electrodes may further comprise:

depositing respective layers of dielectric material and photoresist on the channel member such that the photoresist is separated from the channel member by the layer of dielectric material;

patterning the layer of photoresist;
etching the channel member and layer of dielectric material through the patterned layer of photoresist;
depositing a layer of conductive material onto the layer of catalyst material through the etched channel member and layer of dielectric material to form discrete regions of conductive material; and
patterning the layer of catalyst material to form electrical contacts overlying the channel member and respective discrete regions of conductive material, the electrical contacts and respective discrete regions of conductive material together forming the source and drain electrodes.

[0014] The method may comprise:

selectively depositing a further layer of dielectric material over the etched channel member; and
depositing the layer of conductive material onto the further layer of dielectric material such that the layer of conductive material is separated from the channel member by the further layer of dielectric material, the layer of conductive material forming a gate electrode configured to enable the flow of electrical current through the channel member to be varied by a voltage applied to the gate electrode.

[0015] The method may comprise depositing a layer of sensor material onto the channel member, the sensor material configured to vary the flow of electrical current through the channel member in response to an applied stimulus.

[0016] The layer of sensor material may be configured to vary the flow of electrical current in response to one or more of the following stimuli: electromagnetic radiation, temperature, mechanical stress, a chemical species and a biological species.

[0017] The polymeric material may be configured to form a supporting substrate that is one or more of substantially reversibly deformable, substantially reversibly stretchable, substantially reversibly flexible and substantially reversibly compressible.

[0018] The layer of channel material may be grown using chemical vapour deposition.

[0019] The layer of channel material may comprise one or more of graphene, a two-dimensional chalcogenide, MoS_2, WS_2, $MoSe_2$, WSe_2 and WTe_2.

[0020] One or more of the layers of catalyst and conductive material may comprise at least one of a metal, an alloy, gold, silver, aluminium, copper, nickel, platinum, germanium and indium tin oxide.

[0021] The layer of polymeric material may comprise one or more of PI-2545, PI-2610, PI-2525, polyimide, polyethylene naphthalate and polyethylene terephthalate.

[0022] The layer(s) of dielectric material may comprise one or more of Si_3N_4, Al_2O_3, hBN, SiO_2 and HfO_2.

[0023] The layer of release material may comprise one or more of a refractory metal, a ceramic, SiO, SiO_2, Mo, W, Al_2O_3 and Si_3N_4.

[0024] The carrier wafer may comprise one or more of silicon, quartz and sapphire.

[0025] The sensor material may comprise one or more of a quantum dot material, a pyroelectric material, a piezoelectric material, a chemical binding agent and a biological receptor.

[0026] The quantum dot material may comprise one or more of CdSe, CdS, PbSe, PbS, ZnO, ZnS, CZTS, Cu_2S, Bi_2S_3, Ag_2S, HgTe, CdSe, CdHgTe, InAs, InSb, Ge and CIS.

[0027] The pyroelectric material may comprise one or more of polyvinylidine fluoride, P(VDF-trifluoroethylene), lithium tantalate and gallium nitride.

[0028] The piezoelectric material may comprise one or more of polyvinylidene fluoride, lead zirconium titanate, barium titanate and zinc oxide.

[0029] The chemical binding agent may comprise one or more of an alkanethiol and an alkoxysilane.

[0030] The biological receptor may comprise an antibody.

[0031] According to a further aspect, there is provided an apparatus formed by any method described herein.

[0032] One or more of the source, drain and gate electrodes of the apparatus may be at least partially embedded within the polymeric material.

[0033] The apparatus may be one or more of an electronic device, a portable electronic device, a portable telecommunications device, a mobile phone, a personal digital assistant, a tablet, a phablet, a desktop computer, a laptop computer, a server, a smartphone, a smartwatch, smart eyewear, a sensor, a photodetector, a field-effect transistor, and a module for one or more of the same.

[0034] The steps of any method disclosed herein do not have to be performed in the exact order disclosed, unless explicitly stated or understood by the skilled person.

[0035] Throughout the present specification, descriptors relating to relative orientation and position, such as "top", "bottom", "upper", "lower", "above" and "below", as well as any adjective and adverb derivatives thereof, are used in the sense of the orientation of the apparatus as presented in the drawings. However, such descriptors are not intended to be in any way limiting to an intended use of the described or claimed invention.

[0036] Corresponding computer programs for implementing one or more steps of the methods disclosed herein are also within the present disclosure and are encompassed by one or more of the described example embodiments.

[0037] One or more of the computer programs may, when run on a computer, cause the computer to configure any apparatus, including a circuit, controller, or device disclosed herein or perform any method disclosed herein. One or more of the computer programs may be software implementations, and the computer may be considered as any appropriate hardware, including a digital signal

processor, a microcontroller, and an implementation in read only memory (ROM), erasable programmable read only memory (EPROM) or electronically erasable programmable read only memory (EEPROM), as non-limiting examples. The software may be an assembly program.

[0038] One or more of the computer programs may be provided on a computer readable medium, which may be a physical computer readable medium such as a disc or a memory device, or may be embodied as a transient signal. Such a transient signal may be a network download, including an internet download.

[0039] The present disclosure includes one or more corresponding aspects, example embodiments or features in isolation or in various combinations whether or not specifically stated (including claimed) in that combination or in isolation. Corresponding means for performing one or more of the discussed functions are also within the present disclosure.

[0040] The above summary is intended to be merely exemplary and non-limiting.

Brief Description of the Figures

[0041] A description is now given, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 shows a conventional field-effect transistor (cross-section);
Figures 2a-d show one method of forming a field-effect apparatus (cross-section);
Figures 3a-f show another method of forming a field-effect apparatus (cross-section);
Figures 4a-c show various embodiments of a field-effect apparatus comprising a plurality of gated graphene channels (plan view);
Figures 5a-f show another method of forming a field-effect apparatus (cross-section);
Figures 6a-c show a method of preventing contact between the gate electrode and channel member (cross-section);
Figures 7a-e show another method of forming a field-effect apparatus (cross-section);
Figure 8 shows one example of an apparatus described herein (schematic);
Figure 9 shows the main steps of a method described herein (flow chart);
Figure 10 shows a computer-readable medium comprising a computer program configured to perform, control or enable a method described herein (schematic); and Figures 11a-f show another method of forming a field-effect apparatus (cross-section).

Description of Specific Aspects/Embodiments

[0042] One or more disclosed embodiments of the present apparatus relate to field-effect transistors (FETs). An FET is a type of transistor in which an electrical current is passed through a channel, the conductance (or conductivity) of which can be controlled by a transverse electric field.

[0043] Figure 1 shows a conventional FET in cross-section. As shown in this figure, a semiconductor channel 101 (such as p-type silicon) is supported on a substrate 102 and connected to metal source 103 and drain 104 electrodes. A current enters and exits the channel via the source 103 and drain 104 electrodes, respectively, by applying a potential difference (V) 105 across the channel 101. The conductance of the channel 101 between the source 103 and drain 104 electrodes is switched on and off by a third electrode (the gate electrode 106) capacitively coupled through a thin dielectric layer 107. The conductance may be determined by measuring the current through the channel 101 (using an ammeter 108, for example) and dividing by the potential difference (V) 105. With p-type silicon (or another p-type semiconductor), application of a positive gate voltage (V_G) depletes the charge carriers (creating a depletion region 109 in the channel 101) and reduces the conductance, whilst applying a negative gate voltage (V_G) leads to an accumulation of charge carriers (creating a conductive region) and an increase in conductance.

[0044] Two factors which are important in defining the performance of FETs are the mobility of the charge carriers through the channel, and the contact resistance of the source and drain electrodes with the channel. It has been found, however, that the mobility and contact resistance are adversely affected by contamination at the surface of the channel where it can produce charge concentrations, scattering, locations for trapped water, and can inhibit physical and electrical contact. Contamination of the channel surface tends to increase with the number of processing steps performed on top of the channel (especially photolithography) and the transfer of the channel material from one substrate to another.

[0045] There will now be described a number of methods of forming a field-effect apparatus that may help to reduce the amount of contamination at the channel surface.

[0046] Figures 2a-d illustrate one method of forming a field-effect apparatus, shown as a series of cross-sectional process steps. First, a layer of channel material 201 is grown (e.g. via chemical vapour deposition) on a growth wafer 210 to form a channel member. The growth wafer 210 comprises a layer of catalyst material 211 separated from a carrier wafer 212 by a layer of release material 213, the catalyst material 211 serving as a seed layer for growing the layer of channel material 201. Respective layers of dielectric 207 and conductive 206 material are then deposited on the channel member 201 such that the layer of conductive material 206 is separated from the channel member 201 by the layer of dielectric material 207 to form a gate electrode. The layer of dielectric material 207 also acts as a barrier layer to protect the channel member 201 from water in humid

environments or solvents (which can result in p-type channel FETs requiring large gate voltage biases to reach their Dirac points). The layer of dielectric material 207 may be deposited using atomic layer deposition, and the layer of conductive material 206 may be deposited by evaporation or sputtering. After deposition of the layers of dielectric 207 and conductive 206 material, a layer of polymeric material 202 is deposited over the channel member 201 to form a supporting substrate for the layers of catalyst 211 and channel material 201 (Figure 2a). This may be performed via spin coating, bar coating or spray coating a liquid polymer and curing to cross-link, or by hot embossing a polymer foil (i.e. heating above the glass transition temperature and imprinting).

[0047] The layer of release material 213 is then etched (e.g. wet chemical etching using hydrofluoric acid if etching silicon oxide) to remove the release material 213 and carrier wafer 212, and the stack is turned upside down (e.g. using the polymeric supporting substrate 202 for handling) so that the layer of polymeric material 202 is at the bottom of the stack (Figure 2b). A photoresist mask 214 is then formed on top of the layer of catalyst material 211 to allow corresponding patterning of the catalyst material 211 (Figure 2c). The mask 214 may be formed by selectively exposing the photoresist to incident electromagnetic radiation and developing the exposed regions to remove the unwanted photoresist. The layer of catalyst material 211 is then etched through the photoresist mask 214 to form source 203 and drain 204 electrodes (Figure 2d).

[0048] This method addresses the above-mentioned contamination issue in a number of different ways. Firstly, by depositing the layer of polymeric material 202 on top of the stack and then removing the carrier wafer 212, there is no need to transfer the channel member 201 from the growth substrate 210 to the polymeric support substrate 202. Secondly, at no point in the process does the layer of channel material 201 come into contact with the photoresist 214. This is because the source 203 and drain 204 electrodes are formed by selectively etching the layer of catalyst material 211 through a resist mask 214 rather than by selectively depositing a layer of conductive material through the resist mask 214. Thirdly, since the source 203 and drain 204 electrodes are formed from the layer of catalyst material 211 on which the channel member 201 is grown, the source 203 and drain 204 electrodes are adhered more strongly to the channel member 201 than they would be if the electrodes 203, 204 had been deposited on top of a pre-grown channel member. The resulting apparatus therefore benefits from less contamination that existing field-effect devices which results in greater charge carrier mobility and lower contact resistance.

[0049] As mentioned with reference to Figure 1, the source 203 and drain 204 electrodes are configured to enable a flow of electrical current through the channel member 201, and the gate electrode 206 is configured to enable the flow of electrical current through the channel member 201 to be varied by a voltage applied to the gate electrode 206. In this example, the layers of dielectric 207 and conductive 206 material are deposited between the channel member 201 and supporting substrate 202 to form a back gate electrode 206. The back gate electrode 206 is formed as a continuous layer of conductive material which may facilitate control of the electrical current by generating electric fields which are able to interact with the full length of the channel member 201. It is, however, also possible to form a discrete back gate electrode by patterning the layer of conductive material 206 before deposition of the layer of polymeric material 202 (not shown).

[0050] Figures 3a-e show another method of forming a field-effect apparatus (cross-section), this time comprising a top gate electrode 306. To achieve this, the layer of polymeric material 302 is deposited without the prior deposition of the dielectric and conductive layers (Figure 3a). The release material 313 and carrier wafer 312 are then removed as before and the stack is turned upside down (Figure 3b). Once the photoresist mask 314 has been formed on top of the layer of catalyst material 311 (Figure 3c), and the catalyst material 311 etched through the photoresist mask 314 to form source 303 and drain 304 electrodes (Figure 3d), a layer of dielectric material 307 can be deposited onto the channel 301 and source 303 and drain 304 electrodes to form a gate insulator (Figure 3e). A layer of conductive material 306 can then be deposited on top of the dielectric layer 307 to form a gate electrode (Figure 3f). In this example, the gate electrode 306 is localised to the channel region between the source 303 and drain 304 electrodes (e.g. by deposition through a mask), but a continuous layer covering the complete dielectric layer 307 could also be used for ease of fabrication without adversely affecting operation of the apparatus. With this method, therefore, the layers of dielectric 307 and conductive 306 material are deposited such that the supporting substrate 302 is separated from the layers of dielectric 307 and conductive 306 material by the channel member 301 to form a top gate electrode 306.

[0051] Figures 4a-c show various embodiments of a field-effect apparatus (in plan-view) comprising a plurality of channel members 401a-c rather than a single channel member 401. This may form the basis of an electronic device which requires a high density of transistors or a sensor which is capable of detecting multiple stimuli, and can be fabricated by suitable patterning of the layer of channel material. For example, the layer of catalyst material may be pre-patterned before growing the layer of channel material to form the plurality of channel members 401a-c by selective growth. Alternatively, a continuous layer of channel material may be patterned after growth. The latter may be performed by depositing respective layers of dielectric material and photoresist on the layer of channel material such that the photoresist is separated from the layer of channel material by the layer of dielectric material, patterning the layer of photoresist, and etching

the layers of channel and dielectric material through the patterned layer of photoresist. Here, the layer of dielectric material is used to prevent contact between the photoresist and the channel member 401 in order to reduce contamination at the surface of the channel member 401.

[0052] In the example shown in Figure 4a, the layers of catalyst and conductive material have been patterned to form a respective source electrode 403a-c, a respective drain electrode 404a-c and a respective gate electrode 406a-c for each channel member 401 a-c. In some scenarios, however, it may be acceptable to use the same source 403, drain 404 or gate 406 electrode for multiple channel members 401a-c. Using the same electrode for multiple channel members 401a-c can simplify the fabrication process and device complexity and can also reduce material costs. In the example shown in Figure 4b, the layers of catalyst and conductive material have been patterned to form a common source electrode 403, a common drain electrode 404 and a common gate electrode 406 for the plurality of channel members 401a-c. In other examples, some of the source 403a-c, drain 404a-c and/or gate 406a-c electrodes may be associated with respective channel members and some may be associated with multiple channel members. Figure 4c is one such example, which comprises two channel members 401 a,b formed from a single strip of channel material (in contrast to the examples of Figures 4a and 4b which comprise separate strips of channel material). In this example, the channel members 401 a,b have their own source 403a,b and gate 406a,b electrodes but share a common drain electrode 404. As a result, the electrical currents flowing through each channel member 401a,b are in opposite directions (as indicated by the arrows). In the examples of Figures 4a and 4b, on the other hand, the current flow is in the same direction for each channel member 401a-c.

[0053] Figures 5a-f illustrate another method of forming a field-effect apparatus (in cross-section). First, a layer of channel material 501 is grown on a growth wafer 510 followed by the deposition of a layer of dielectric material 507a (Figure 5a). The layers of channel 501 and dielectric 507a material are then patterned (e.g. by selectively etching the channel 501 and dielectric 507a materials through a photoresist mask) to define the channel member (Figure 5b). A layer of conductive material is then deposited onto the layer of catalyst material 511 through the patterned layers of channel 501 and dielectric 507a material to form discrete regions of conductive material 515. After this, a further layer of dielectric material 507b is selectively deposited over the channel member 501 followed by a layer of conductive material to form a gate electrode 506 (Figure 5c). The further layer of dielectric material 507b helps to prevent contact between the gate electrode 506 and the underlying channel member 501 (described in more detail with reference to Figures 6a-c), as well as between the gate electrode 506 and the discrete regions of conductive material 515. It also allows the thickness of the dielectric material 507b forming the gate insulator to be independent of the thickness of the dielectric material 507a elsewhere.

[0054] A layer of polymeric material 502 is then deposited on top of the stack (Figure 5d), the release material 513 and carrier wafer 512 are removed as before and the stack is turned upside down (Figure 5e). As mentioned previously, the polymeric material 502 may be deposited as a liquid polymer and cured, or as a polymer foil and embossed. Either way, the layer of polymeric material 502 encapsulates the gate electrode 506 and exposed regions of conductive material 515. Finally, the layer of catalyst material 511 is patterned to form electrical contacts 516 overlying the channel member 501 and respective discrete regions of conductive material 515 (Figure 5f). In this way, the electrical contacts 516 and respective discrete regions of conductive material 515 together form source 503 and drain 504 electrodes.

[0055] If the process illustrated in Figures 5a-f is to be used to form a plurality of gated channel members, any channel material 501 which is not used to form the channel members may be removed to help prevent short circuits between adjacent channel members or their respective electrodes 503, 504.

[0056] Figures 11a-f show a modified version of the process of Figures 5a-f in which the excess channel material 1101 is etched away before formation of the source 1103, drain 1104 and gate 1106 electrodes. As with the previous process, the layers of channel 1101 and dielectric 1107a material are patterned to define the channel member (e.g. by etching through a photoresist mask). This time, however, the layers of channel 1101 and dielectric 1107a material are patterned such that all material outside the channel region is removed by the etching step (Figure 11 b). The further layer of dielectric material 1107b is then selectively deposited over the channel member (e.g. using a photoresist mask on top of the layer of catalyst material 1111) followed by the deposition of a layer of conductive material to form the gate electrode 1106. Once the mask is removed, a further mask (e.g. photoresist) can then be used to selectively deposit discrete regions of conductive material 1115 for the source 1103 and drain 1104 electrodes (Figure 11c). In some cases, the same layer of conductive material may be used for the source 1103, drain 1104 and gate 1106 electrodes. To achieve this, the mask used during deposition of the further layer of dielectric material 1107b is removed before selective deposition of the conductive material. The remaining steps of the process (e.g. Figures 11d-f) are the same as those described with reference to Figures 5d-f.

[0057] Figures 6a-c show how the further layer of dielectric material 507b is Figure 5c can help to prevent contact between the gate electrode 506 and the underlying channel member 501. These figures are cross-sectional views of the corresponding layers of Figure 5c perpendicular to the cross-section of Figure 5c (i.e. into the page). As illustrated in Figure 6a, deposition of the layer of conductive material 606 on top of the channel member

601 and layer of dielectric material 607a can result in contact between the conductive material 606 and the channel material 601 at the edges of the channel member which may create a short circuit. The reason for extending the layer of conductive material 606 down the edges of the channel member 601 is to enable connection of the gate electrode 606 to a power supply for provision of a gate voltage. By depositing a further layer of dielectric material 607b on top of the first layer of dielectric material 607a (Figure 6b), however, the edges of the channel member 601 can be insulated from the layer of subsequently deposited conductive material 606 (Figure 6c). In some cases, the further layer of dielectric material 607b may be deposited at the edges of the channel member 601 only so as not to increase the distance between the gate electrode 606 and the channel member 601.

[0058] Figures 7a-e show a further method of forming a field-effect apparatus. As can be seen from these figures, steps 7a-d are identical to steps 3a-d of the method described with reference to Figure 3. This time, however, instead of depositing respective layers of dielectric and conductive material onto the channel member 701, the method comprises depositing a layer of sensor material 717 (e.g. by spin casting, inkjet printing or stamping) configured to vary the flow of electrical current through the channel member 701 in response to an applied stimulus. The layer of sensor material 717 functionalises or activates the channel member 701 such that the applied stimulus is able to gate the channel member 701 instead of a gate electrode, thus enabling detection of the stimulus based on the variation in electrical current. In practice, the sensor material 717 may be configured to enable detection of any stimulus provided that the interaction of that stimulus with the sensor material 717 results in a change in electrical current through the channel member. For example, the sensor material 717 may comprise one or more of a quantum dot material for sensing electromagnetic radiation, a pyroelectric material for sensing temperature, a piezoelectric material for sensing mechanical stress, a chemical binding agent for sensing a chemical species, and a biological receptor for sensing a biological species. In the example shown in Figure 7e, the layer of sensor material 717 comprises an antibody configured to bind to a charged species 718 in the surrounding environment such that the charged species 718 is in sufficient proximity to the channel member 701 to cause a variation in electrical current.

[0059] Although the applied stimulus gates the channel member instead of a gate electrode in this example, a bottom gate electrode could be used to tune the conductance/conductivity of the channel member 701. In this respect, it is also possible to incorporate the layer of sensor material 717 of Figure 7 into the methods of Figures 2 and 5.

[0060] A number of different materials may be used in the above-mentioned processes. One particular example involves the use of a graphene channel member grown on a silicon carrier wafer using copper as the catalyst material and silicon oxide as the release material. In this example, the dielectric material may comprise aluminium oxide, the conductive material may comprise copper, the polymeric material may comprise polyimide, and the sensor material may comprise PbS quantum dots. This example benefits from the high mobility of graphene, the quantum efficiency of PbS quantum dots and the mechanical resilience of polyimide, thus rendering it suitable for use as a reversibly deformable (e.g. flexible, stretchable and/or compressible) graphene field-effect transistor (GFET) photodetector.

[0061] The present methods and resulting field-effect apparatus are not limited to these specific materials. For example, the channel material may comprise one or more of graphene, a two-dimensional chalcogenide, MoS_2, WS_2, $MoSe_2$, WSe_2 and WTe_2; the catalyst and conductive materials may comprise one or more of a metal, an alloy, gold, silver, aluminium, copper, nickel, platinum, germanium and indium tin oxide (the catalyst material should be electrically conductive to enable its use as source and drain electrodes); the polymeric material may comprise one or more of HD Microsystems™ PI-2545, PI-2610 or PI-2525, polyimide, polyethylene naphthalate and polyethylene terephthalate; the dielectric material may comprise one or more of Si_3N_4, Al_2O_3, hBN, SiO_2 and HfO_2; the release material may comprise one or more of a refractory metal, a ceramic, SiO, SiO_2, Mo, W, Al_2O_3 and Si_3N_4 (the release material should be resistant to the high temperatures that are possible during growth of the channel material, should not form compounds with the catalyst material and should have etch selectivity against the catalyst and polymeric materials); and the carrier wafer may comprise one or more of silicon, quartz and sapphire.

[0062] Also, as mentioned above, a number of different types of sensor material may be used depending on the specific stimuli being detected. These include, but are not limited to, one or more of: a quantum dot material (e.g. CdSe, CdS, PbSe, PbS, ZnO, ZnS, CZTS, Cu_2S, Bi_2S_3, Ag_2S, HgTe, CdSe, CdHgTe, InAs, InSb, Ge or CIS); a pyroelectric material (e.g. polyvinylidine fluoride, P(VDF-trifluoroethylene), lithium tantalate and gallium nitride); a piezoelectric material (e.g. polyvinylidene fluoride, lead zirconium titanate, barium titanate and zinc oxide); a chemical binding agent (e.g. an alkanethiol and an alkoxysilane); and a biological receptor (e.g. an antibody).

[0063] Figure 8 shows one example of an apparatus 819 at least partly formed using a method described herein. The apparatus 819 may be one or more of an electronic device, a portable electronic device, a portable telecommunications device, a mobile phone, a personal digital assistant, a tablet, a phablet, a desktop computer, a laptop computer, a server, a smartphone, a smartwatch, smart eyewear, a sensor, a photodetector, a field-effect transistor, and a module for one or more of the same. In the example shown, the apparatus 819 comprises the various components described previously (de-

noted collectively by reference numeral 820), a power source 821, a processor 822 and a storage medium 823, which are electrically connected to one another by a data bus 824.

[0064] The processor 822 is configured for general operation of the apparatus 819 by providing signalling to, and receiving signalling from, the other components to manage their operation. The storage medium 823 is configured to store computer code configured to perform, control or enable operation of the apparatus 819. The storage medium 823 may also be configured to store settings for the other components. The processor 822 may access the storage medium 823 to retrieve the component settings in order to manage the operation of the other components.

[0065] Under the control of the processor 822, the power source 821 is configured to apply a voltage between the source and drain electrodes to enable a flow of electrical current through the channel member, and apply a gate voltage to the gate electrode to cause a detectable change in the flow of electrical current. In this way, the components 820 may act as an electronic switch within the circuitry of the apparatus 819.

[0066] The processor 822 may be a microprocessor, including an Application Specific Integrated Circuit (ASIC). The storage medium 823 may be a temporary storage medium such as a volatile random access memory. On the other hand, the storage medium 823 may be a permanent storage medium 823 such as a hard disk drive, a flash memory, or a non-volatile random access memory. The power source 821 may comprise one or more of a primary battery, a secondary battery, a capacitor, a supercapacitor and a battery-capacitor hybrid.

[0067] Figure 9 shows schematically the main steps 925-928 of a method of making a field-effect apparatus. The method generally comprises: growing a layer of channel material on a growth wafer to form a channel member, the growth wafer comprising a layer of catalyst material separated from a carrier wafer by a layer of release material 925; depositing a layer of polymeric material over the formed channel member to form a supporting substrate 926; etching the layer of release material to remove the release material and carrier wafer 927; and patterning the layer of catalyst material to form source and drain electrodes 928.

[0068] Figure 10 illustrates schematically a computer/processor readable medium 1029 providing a computer program according to one embodiment. The computer program may comprise computer code configured to perform, control or enable one or more of the method steps 925-928 of Figure 9. Additionally or alternatively, the computer program may comprise computer code configured to apply a voltage between the source and drain electrodes to enable a flow of electrical current through the channel member; and apply a gate voltage to the gate electrode to cause a detectable change in the flow of electrical current.

[0069] In this example, the computer/processor readable medium 1029 is a disc such as a digital versatile disc (DVD) or a compact disc (CD). In other embodiments, the computer/processor readable medium 1029 may be any medium that has been programmed in such a way as to carry out an inventive function. The computer/processor readable medium 1029 may be a removable memory device such as a memory stick or memory card (SD, mini SD, micro SD or nano SD).

[0070] Other embodiments depicted in the figures have been provided with reference numerals that correspond to similar features of earlier described embodiments. For example, feature number 1 can also correspond to numbers 101, 201, 301 etc. These numbered features may appear in the figures but may not have been directly referred to within the description of these particular embodiments. These have still been provided in the figures to aid understanding of the further embodiments, particularly in relation to the features of similar earlier described embodiments.

[0071] It will be appreciated to the skilled reader that any mentioned apparatus/device and/or other features of particular mentioned apparatus/device may be provided by apparatus arranged such that they become configured to carry out the desired operations only when enabled, e.g. switched on, or the like. In such cases, they may not necessarily have the appropriate software loaded into the active memory in the non-enabled (e.g. switched off state) and only load the appropriate software in the enabled (e.g. on state). The apparatus may comprise hardware circuitry and/or firmware. The apparatus may comprise software loaded onto memory. Such software/computer programs may be recorded on the same memory/processor/functional units and/or on one or more memories/processors/functional units.

[0072] In some embodiments, a particular mentioned apparatus/device may be pre-programmed with the appropriate software to carry out desired operations, and wherein the appropriate software can be enabled for use by a user downloading a "key", for example, to unlock/enable the software and its associated functionality. Advantages associated with such embodiments can include a reduced requirement to download data when further functionality is required for a device, and this can be useful in examples where a device is perceived to have sufficient capacity to store such pre-programmed software for functionality that may not be enabled by a user.

[0073] It will be appreciated that any mentioned apparatus/circuitry/elements/processor may have other functions in addition to the mentioned functions, and that these functions may be performed by the same apparatus/circuitry/elements/processor. One or more disclosed aspects may encompass the electronic distribution of associated computer programs and computer programs (which may be source/transport encoded) recorded on an appropriate carrier (e.g. memory, signal).

[0074] It will be appreciated that any "computer" described herein can comprise a collection of one or more individual processors/processing elements that may or

may not be located on the same circuit board, or the same region/position of a circuit board or even the same device. In some embodiments one or more of any mentioned processors may be distributed over a plurality of devices. The same or different processor/processing elements may perform one or more functions described herein.

[0075] It will be appreciated that the term "signalling" may refer to one or more signals transmitted as a series of transmitted and/or received signals. The series of signals may comprise one, two, three, four or even more individual signal components or distinct signals to make up said signalling. Some or all of these individual signals may be transmitted/received simultaneously, in sequence, and/or such that they temporally overlap one another.

[0076] With reference to any discussion of any mentioned computer and/or processor and memory (e.g. including ROM, CD-ROM etc), these may comprise a computer processor, Application Specific Integrated Circuit (ASIC), field-programmable gate array (FPGA), and/or other hardware components that have been programmed in such a way to carry out the inventive function.

[0077] The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole, in the light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that the disclosed aspects/embodiments may consist of any such individual feature or combination of features. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the disclosure.

[0078] While there have been shown and described and pointed out fundamental novel features as applied to different embodiments thereof, it will be understood that various omissions and substitutions and changes in the form and details of the devices and methods described may be made by those skilled in the art without departing from the spirit of the invention. For example, it is expressly intended that all combinations of those elements and/or method steps which perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Moreover, it should be recognized that structures and/or elements and/or method steps shown and/or described in connection with any disclosed form or embodiment may be incorporated in any other disclosed or described or suggested form or embodiment as a general matter of design choice. Furthermore, in the claims means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents, but also equivalent structures. Thus although a nail and a screw may not be structural equivalents in that a nail employs a cylindrical surface to secure wooden parts together, whereas a screw employs a helical surface, in the environment of fastening wooden parts, a nail and a screw may be equivalent structures.

Claims

1. A method comprising:

   growing a layer of channel material on a growth wafer to form a channel member, the growth wafer comprising a layer of catalyst material separated from a carrier wafer by a layer of release material, the catalyst material serving as a seed layer for growing the layer of channel material;
   depositing a layer of polymeric material over the formed channel member to form a supporting substrate for the layers of catalyst and channel material;
   etching the layer of release material to remove the release material and carrier wafer; and
   patterning the layer of catalyst material to form source and drain electrodes configured to enable a flow of electrical current through the channel member.

2. The method of claim 1, wherein the method comprises depositing respective layers of dielectric and conductive material on the channel member such that the layer of conductive material is separated from channel member by the layer of dielectric material, the layer of conductive material forming a gate electrode configured to enable the flow of electrical current through the channel member to be varied by a voltage applied to the gate electrode.

3. The method of claim 2, wherein the method comprises depositing the layers of dielectric and conductive material between the channel member and supporting substrate to form a back gate electrode.

4. The method of claim 2, wherein the method comprises depositing the layers of dielectric and conductive material such that the supporting substrate is separated from the layers of dielectric and conductive material by the channel member to form a top gate electrode.

5. The method of any of claims 2 to 4, wherein the method comprises patterning the layers of channel and conductive material to form a plurality of gated channel members.

6. The method of claim 5, wherein the method comprises patterning one or more of the layers of catalyst and conductive material to form at least one of a

common source, common drain and common gate electrode for the plurality of gated channel members and/or at least one of a respective source, respective drain and respective gate electrode for each gated channel member.

7. The method of claim 5 or 6, wherein patterning the layer of channel material comprises pre-patterning the layer of catalyst material before growing the layer of channel material to form the plurality of channel members by selective growth.

8. The method of claim 5 or 6, wherein patterning the layer of channel material comprises:

depositing respective layers of dielectric material and photoresist on the layer of channel material such that the photoresist is separated from the layer of channel material by the layer of dielectric material;
patterning the layer of photoresist; and
etching the layers of channel and dielectric material through the patterned layer of photoresist.

9. The method of any preceding claim, wherein forming the source and drain electrodes further comprises:

depositing respective layers of dielectric material and photoresist on the channel member such that the photoresist is separated from the channel member by the layer of dielectric material;
patterning the layer of photoresist;
etching the channel member and layer of dielectric material through the patterned layer of photoresist;
depositing a layer of conductive material onto the layer of catalyst material through the etched channel member and layer of dielectric material to form discrete regions of conductive material; and
patterning the layer of catalyst material to form electrical contacts overlying the channel member and respective discrete regions of conductive material, the electrical contacts and respective discrete regions of conductive material together forming the source and drain electrodes.

10. The method of claim 9, wherein the method comprises:

selectively depositing a further layer of dielectric material over the etched channel member; and
depositing the layer of conductive material onto the further layer of dielectric material such that the layer of conductive material is separated from the channel member by the further layer of dielectric material, the layer of conductive material forming a gate electrode configured to enable the flow of electrical current through the channel member to be varied by a voltage applied to the gate electrode.

11. The method of any preceding claim, wherein the method comprises depositing a layer of sensor material onto the channel member, the sensor material configured to vary the flow of electrical current through the channel member in response to an applied stimulus.

12. The method of claim 11, wherein the layer of sensor material is configured to vary the flow of electrical current in response to one or more of the following stimuli:

electromagnetic radiation, temperature, mechanical stress, a chemical species and a biological species.

13. A computer program comprising computer code configured to perform the method of any preceding claim.

14. An apparatus formed by the method of any preceding method claim.

15. The apparatus of claim 14, wherein one or more of the source, drain and gate electrodes are at least partially embedded within the polymeric material.

Figure 1

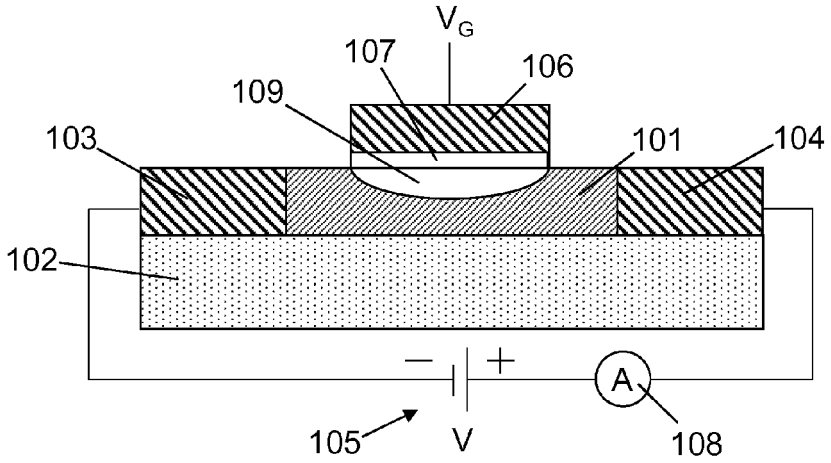


Figure 2a

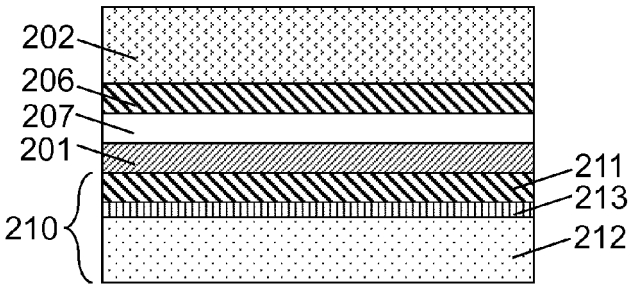


Figure 2b

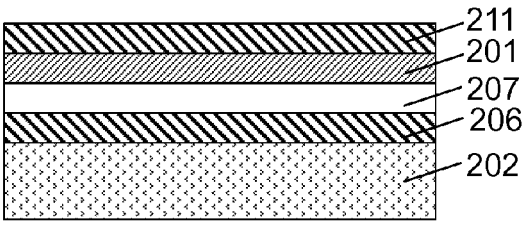


Figure 2c

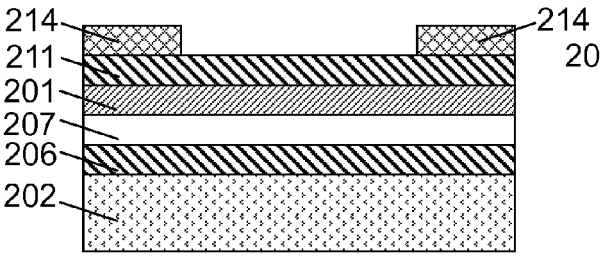


Figure 2d

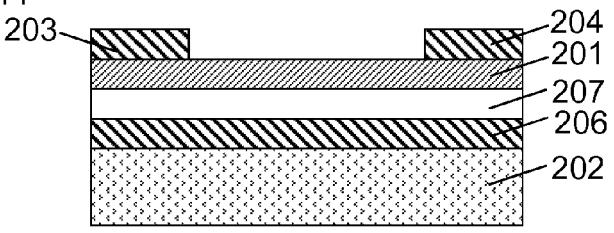


Figure 3a

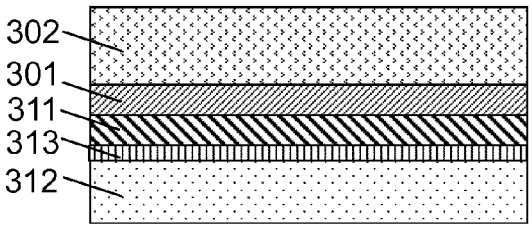


Figure 3b

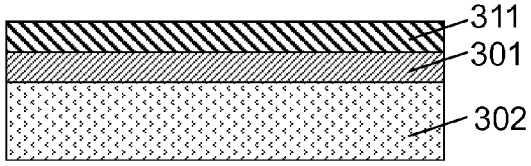


Figure 3c

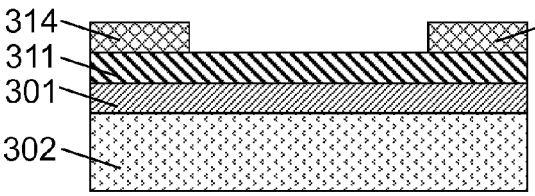


Figure 3d

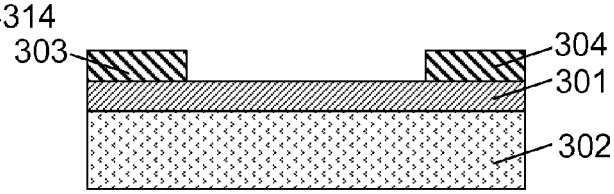


Figure 3e

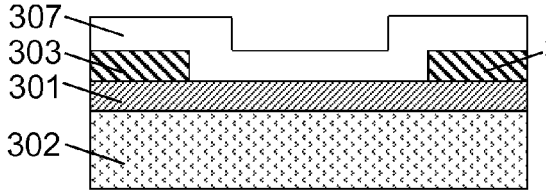


Figure 3f

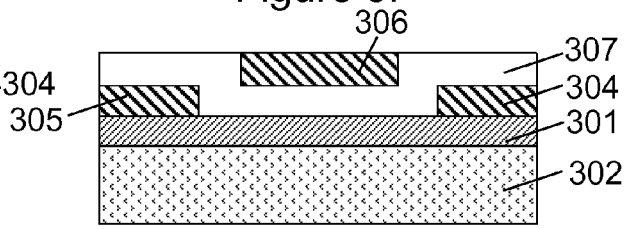


Figure 4a

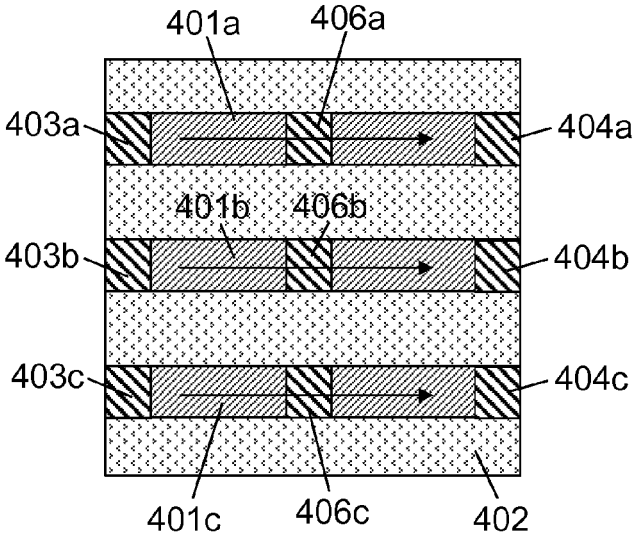


Figure 4b

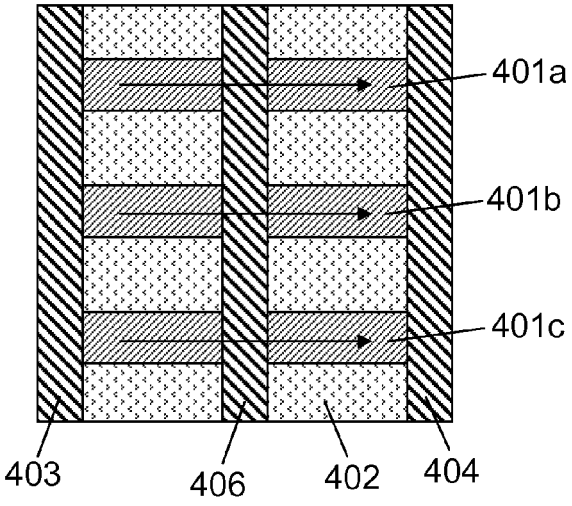


Figure 4c

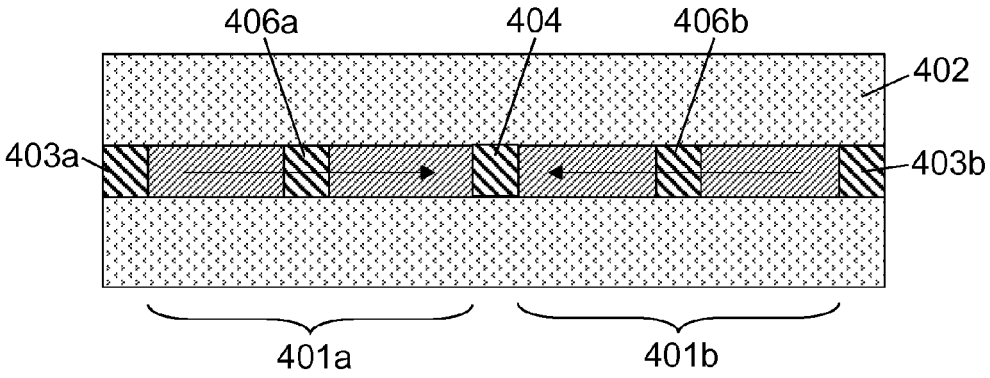


Figure 5a

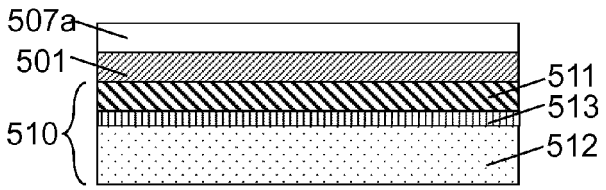


Figure 5b

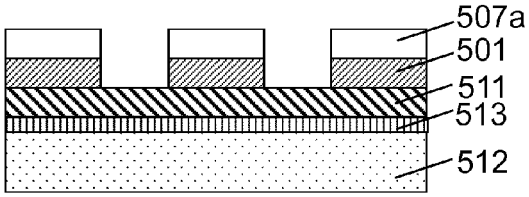


Figure 5c

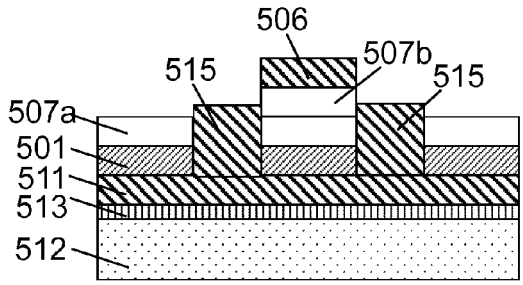


Figure 5d

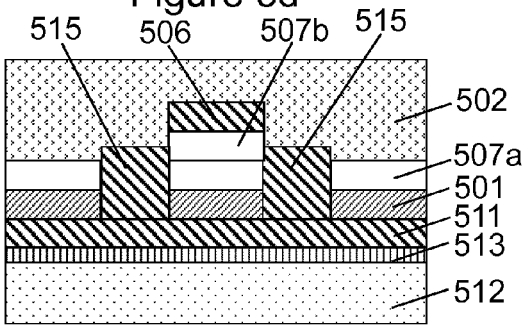


Figure 5e

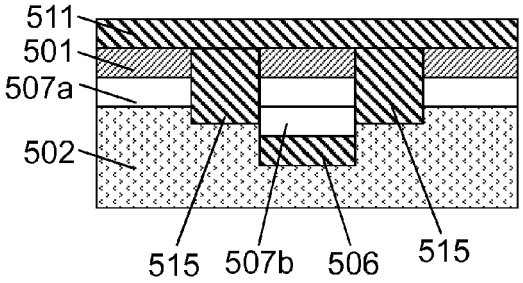


Figure 5f

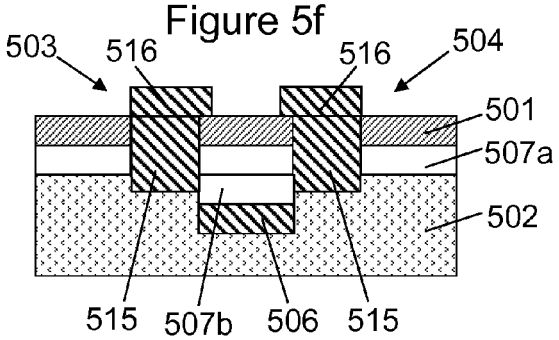


Figure 6a

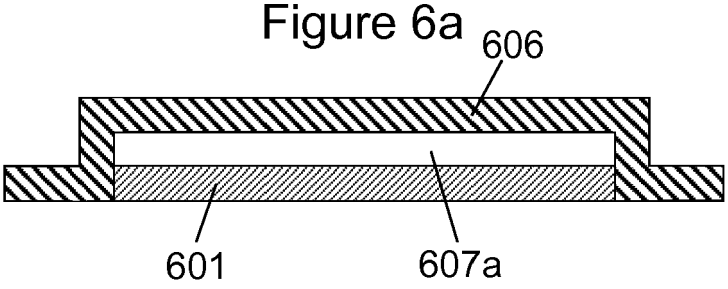


Figure 6b

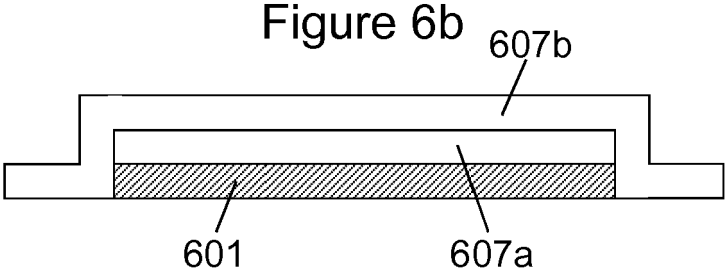


Figure 6c

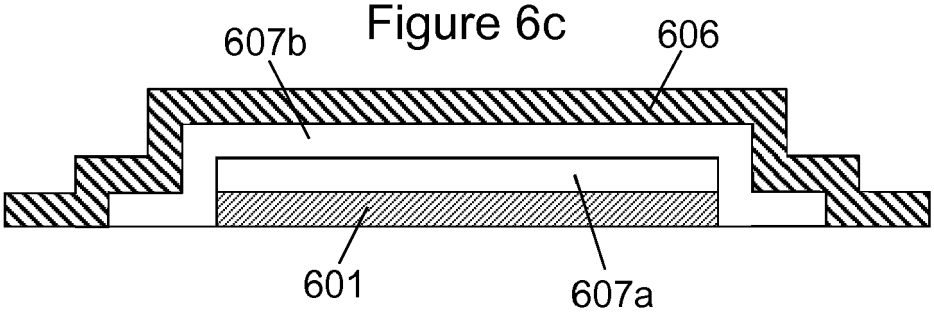


Figure 7a

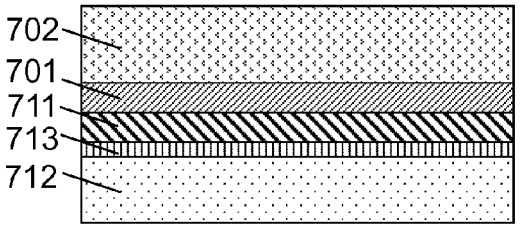


Figure 7b

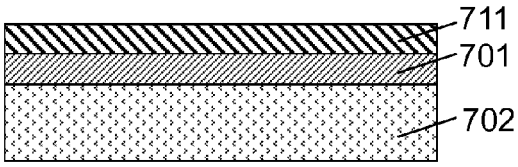


Figure 7c

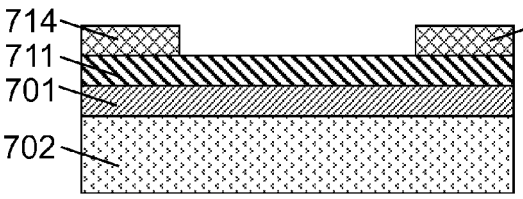


Figure 7d

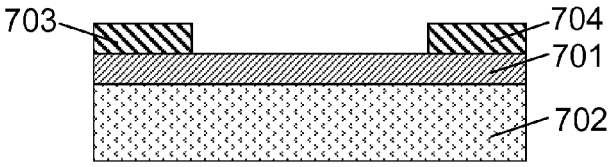


Figure 7e

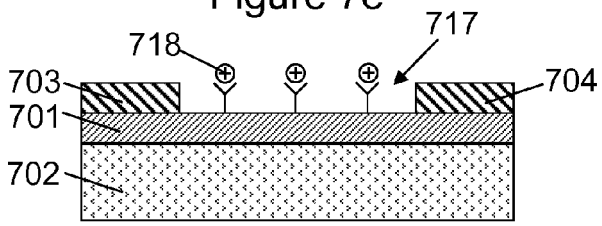


Figure 8

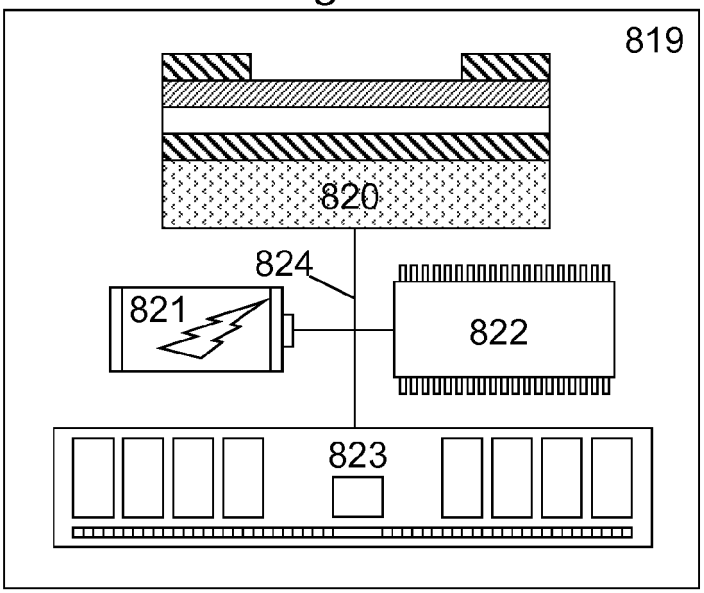


Figure 9

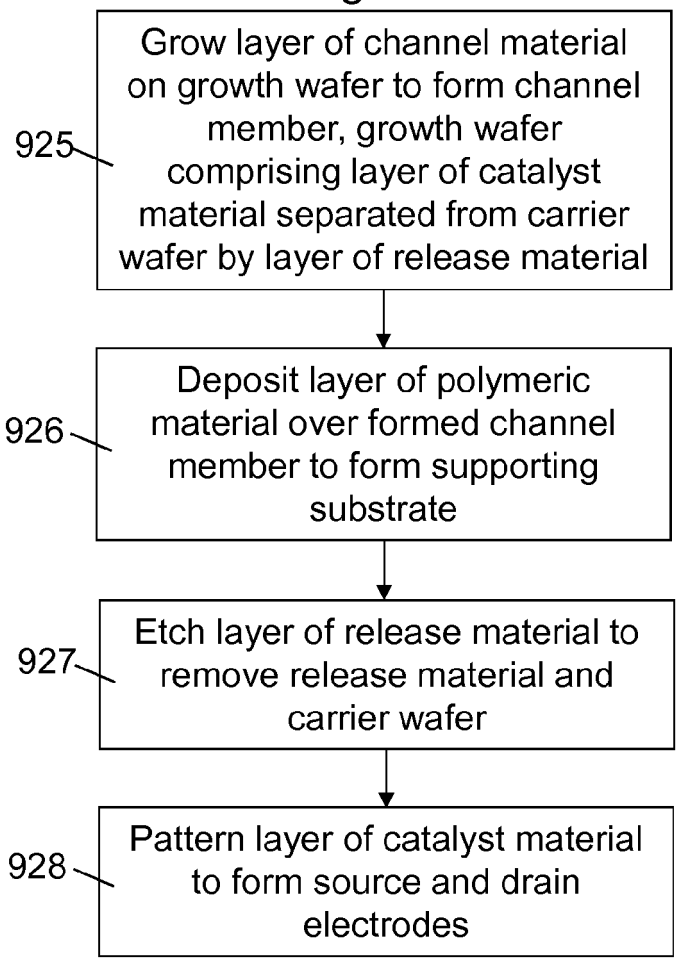


Figure 10

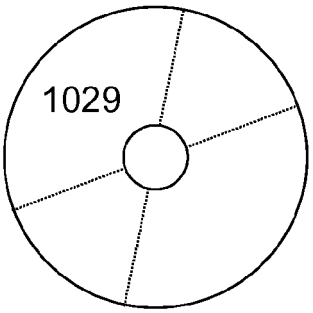


Figure 11a

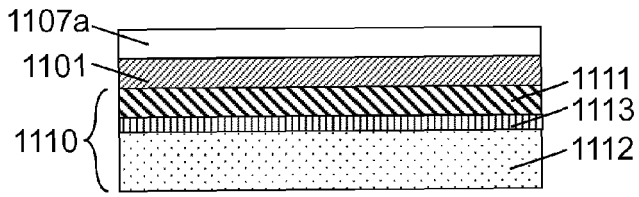


Figure 11b

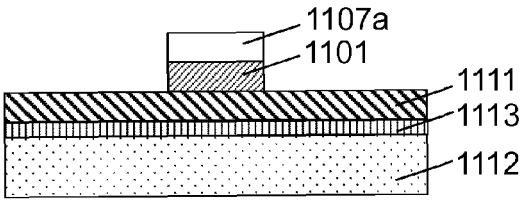


Figure 11c

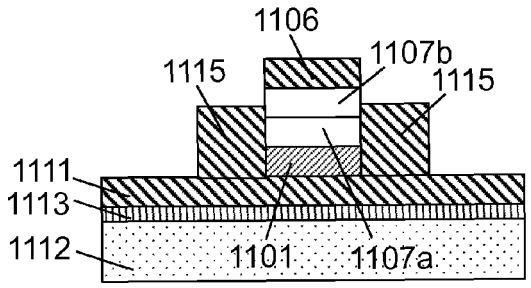


Figure 11d

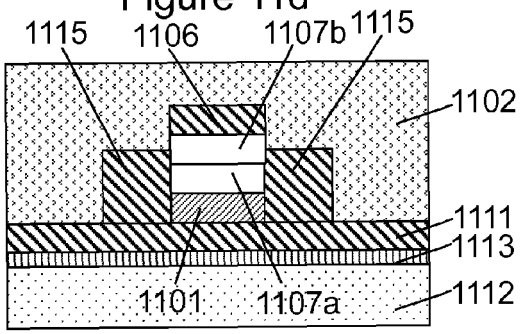


Figure 11e

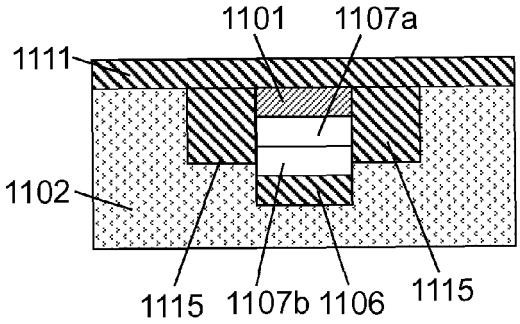
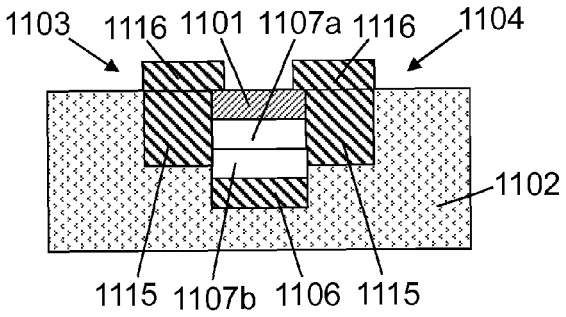


Figure 11f



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Application Number
EP 15 18 0829

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Place of search	Date of completion of the search	Examiner
Munich	18 February 2016	Dauw, Xavier

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