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(54) ORGANIC THIN FILM TRANSISTOR AND PREPARATION METHOD THEREOF, ARRAY SUBSTRATE AND PREPARATION METHOD THEREOF, DISPLAY DEVICE

(57) An organic thin film transistor and a preparation method thereof, an array substrate and a preparation method thereof, and a display device; and the preparation method of the organic thin film transistor comprises: forming a source-drain metal layer including a source electrode (12a) and a drain electrode (12b), and forming an organic semiconductor active layer (13) in contact with the source electrode (12a) and the drain electrode (12b); and forming an organic insulating thin film (140) on a substrate (10) where the source-drain metal layer and the organic semiconductor active layer (13) have been formed, thinning the organic insulating thin film (140) and curing the thinned organic insulating thin film (140), or curing the organic insulating thin film (140) and thinning the cured organic insulating thin film (140), to form an organic insulating layer (14). The method can be used to form a thin and uniform organic insulating layer, so a technical difficulty in forming a via hole is reduced.

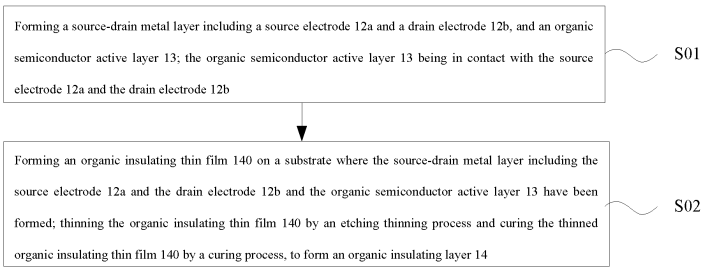

FIG. 1

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Description

TECHNICAL FIELD

[0001] At least one embodiment of the invention relates to an organic thin film transistor and a preparation method thereof, an array substrate and a preparation method thereof, and a display device.

BACKGROUND

[0002] Since organic thin film transistors (OTFTs) appeared in mid-80s of the 20th century, they show excellent application prospect in various display devices and storage units, especially in E-paper and flexible display field due to advantages such as light weight, low price, good flexibility and so on, so they have been valued by researchers, and developed rapidly.

[0003] The key structure of an OTFT is an organic semiconductor active layer made of an organic semiconductor material, and due to strong activity, most organic semiconductor materials are prepared under low temperature condition (less than 200 °C). Therefore, it is necessary to select a right insulating layer material to cover the organic semiconductor active layer, so that the organic semiconductor active layer is well packaged and protected, thus ensuring that stability of various performances of the organic semiconductor active layer are not affected by other preparation processes.

SUMMARY

[0004] At least one embodiment of the invention provides an organic thin film transistor and a preparation method thereof, an array substrate and a preparation method thereof, and a display device, in order to form a thin and uniform organic insulating layer, reduce a technical difficulty in forming a via hole on the organic insulating layer, and improve a technical reliability while effectively packaging and protecting an organic semiconductor active layer.

[0005] In one aspect, at least one embodiment of the invention provides a preparation method of an organic thin film transistor, the preparation method comprising: forming a source-drain metal layer including a source electrode and a drain electrode, and an organic semiconductor active layer, the organic semiconductor active layer being in contact with the source electrode and the drain electrode; forming an organic insulating thin film on a substrate where the source-drain metal layer including the source electrode and the drain electrode and the organic semiconductor active layer have been formed; thinning the organic insulating thin film by an etching process and curing the thinned organic insulating thin film by a curing process, or curing the organic insulating thin film by a curing process and thinning the cured organic insulating thin film by an etching thinning process, to form an organic insulating layer; and the preparation method further comprises forming a gate electrode.

[0006] In another aspect, at least one embodiment of the invention provides a preparation method of an array substrate, the preparation method comprising: forming an organic thin film transistor, the organic thin film transistor being prepared by the preparation method described above.

[0007] In still another aspect, at least one embodiment of the invention provides an organic thin film transistor prepared by the preparation method described above; the organic thin film transistor includes an organic insulating layer located above an organic semiconductor active layer, and the organic insulating layer has a thickness from 300 nm to 500 nm.

[0008] In yet another aspect, at least one embodiment of the invention provides an array substrate, the array substrate comprising the organic thin film transistor described above.

[0009] In a further aspect, at least one embodiment of the invention further provides a display device, the display device comprising the organic thin film transistor described above or the array substrate described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In order to clearly illustrate the technical solution of the embodiments of the invention, the drawings of the embodiments will be briefly described in the following; it is obvious that the described drawings are only related to some embodiments of the invention and thus are not limitative of the invention.

FIG. 1 is a schematic diagram of a preparation process of an organic thin film transistor provided by an embodiment of the invention;

FIG. 2(a) is a structural schematic diagram of a bottom-gate bottom-contact type provided by an embodiment of the invention;

FIG. 2(b) is a structural schematic diagram of a bottom-gate top-contact type provided by the embodiment of the invention;

FIG. 3(a) is a structural schematic diagram of a top-gate bottom-contact type provided by an embodiment of the invention;

FIG. 3(b) is a structural schematic diagram of a top-gate top-contact type provided by the embodiment of the invention;

FIG. 4(a) and FIG. 4(b) are schematic diagram I and schematic diagram II of forming an organic semiconductor thin film and an organic photosensitive thin film on a substrate where a source electrode and a drain electrode have been formed for an organic thin film transistor of bottom-contact type, sequentially;

FIG. 5(a) is a schematic diagram of forming a completely-retained portion and a completely-removed portion of the organic photosensitive thin film on the basis of FIG. 4(a);

FIG. 5(b) is a schematic diagram of forming a com-

pletely-retained portion and a completely-removed portion of the organic photosensitive thin film on the basis of FIG. 4(b);

FIG. 6(a) is a schematic diagram of forming an organic semiconductor active layer on the basis of FIG. 5(a);

FIG. 6(b) is a schematic diagram of forming an organic semiconductor active layer on the basis of FIG. 5(b);

FIG. 7(a) is a schematic diagram of forming an organic etching blocking layer on the basis of FIG. 6(a);

FIG. 7(b) is a schematic diagram of forming an organic etching blocking layer on the basis of FIG. 6(b);

FIGs. 8(a) and 8(b) are schematic diagram I and schematic diagram II of forming an organic semiconductor thin film and an organic photosensitive thin film on a substrate for an organic thin film transistor of top-contact type, sequentially;

FIG. 9(a) is a schematic diagram of forming a completely-retained portion, a completely-removed portion, and a half-retained portion of the organic photosensitive thin film on the basis of FIG. 8 (a);

FIG. 9(b) is a schematic diagram of forming a completely-retained portion, a completely-removed portion, and a half-retained portion of the organic photosensitive thin film on the basis of FIG. 8(b);

FIG. 10(a) is a schematic diagram of forming an organic semiconductor active layer on the basis of FIG. 9 (a);

FIG. 10(b) is a schematic diagram of forming an organic semiconductor active layer on the basis of FIG. 9(b);

FIG. 11 (a) is a schematic diagram of removing the half-retained portion of the organic photosensitive thin film to expose the organic semiconductor active layer on the basis of FIG. 10(a);

FIG. 11(b) is a schematic diagram of removing the half-retained portion of the organic photosensitive thin film to expose the organic semiconductor active layer on the basis of FIG. 10(b);

FIG. 12(a) is a schematic diagram of forming an organic etching blocking layer on the basis of FIG. 11 (a);

FIG. 12(b) is a schematic diagram of forming an organic etching blocking layer on the basis of FIG. 11(b);

FIG. 13(a) is a schematic diagram of forming a source electrode and a drain electrode on the basis of FIG. 12(a);

FIG. 13(b) is a schematic diagram of forming a source electrode and a drain electrode on the basis of FIG. 12(b);

FIG. 14(a) is a schematic diagram of forming an organic insulating thin film on the basis of FIG. 7(a);

FIG. 14 (b) is a schematic diagram of forming an organic insulating thin film on the basis of FIG. 7(b);

FIG. 14(c) is a schematic diagram of forming an organic insulating thin film on the basis of FIG. 13(a);

FIG. 14(d) is a schematic diagram of forming an organic insulating thin film on the basis of FIG. 13(b);

FIG. 15(a) is a schematic diagram of thinning the organic insulating thin film by a first etching thinning process on the basis of FIG. 14(a);

FIG. 15(b) is a schematic diagram of thinning the organic insulating thin film by a first etching thinning process on the basis of FIG. 14(b);

FIG. 15(c) is a schematic diagram of thinning the organic insulating thin film by a first etching thinning process on the basis of FIG. 14(c);

FIG. 15(d) is a schematic diagram of thinning the organic insulating thin film by a first etching thinning process on the basis of FIG. 14(d);

FIG. 16(a) is a schematic diagram of curing first regions which have completed step S34 on the basis of FIG. 15(a);

FIG. 16(b) is a schematic diagram of curing first regions which has completed step S34 on the basis of FIG. 15(b);

FIG. 16(c) is a schematic diagram of curing first regions which has completed step S34 on the basis of FIG. 15(c);

FIG. 16(d) is a schematic diagram of curing first regions which has completed step S34 on the basis of FIG. 15(d);

FIG. 17(a) is a schematic diagram of thinning second regions on the basis of FIG. 16 (a);

FIG. 17(b) is a schematic diagram of thinning second regions on the basis of FIG. 16(b);

FIG. 17(c) is a schematic diagram of thinning second regions on the basis of FIG. 16(c);

FIG. 17(d) is a schematic diagram of thinning second regions on the basis of FIG. 16(d);

FIG. 18(a) is a schematic diagram of forming an organic insulating layer on the basis of FIG. 17 (a);

FIG. 18(b) is a schematic diagram of forming an organic insulating layer on the basis of FIG. 17 (b);

FIG. 18(c) is a schematic diagram of forming an organic insulating layer on the basis of FIG. 17(c);

FIG. 18(d) is a schematic diagram of forming an organic insulating layer on the basis of FIG. 17(d);

FIG. 19(a), FIG. 19(b), FIG. 19(c) and FIG. 19(d) are structural schematic diagrams I, II, III and IV of an array substrate provided by an embodiment of the present invention, sequentially.

Reference signs:

[0011] 01-organic thin film transistor; 10-base substrate; 11-gate electrode; 12a-source electrode; 12b-drain electrode; 13-organic semiconductor active layer; 130-organic semiconductor thin film; 14-organic insulating layer; 140-organic insulating thin film; 15-gate insulating layer; 16-organic etching blocking layer; 160-organic photosensitive thin film; 160a-completely-retained portion of the organic photosensitive thin film; 160b-completely-removed portion of the organic photosensitive

thin film; 160c- half-retained portion of the organic photosensitive thin film; 02-array substrate; 20-planarization layer; 21-via hole; 22-pixel electrode.

DETAILED DESCRIPTION

[0012] In order to make objects, technical details and advantages of the embodiments of the invention apparent, the technical solutions of the embodiment will be described in a clearly and fully understandable way in connection with the drawings related to the embodiments of the invention. It is obvious that the described embodiments are just a part but not all of the embodiments of the invention. Based on the described embodiments herein, those skilled in the art can obtain other embodiment(s), without any inventive work, which should be within the scope of the invention.

[0013] The inventors of the application have noted that, in a preparation process of an OTFT, there are mainly two difficulties in adopting an insulating layer material to cover an organic semiconductor active layer for well packaging and protecting the organic semiconductor active layer.

[0014] Firstly, an insulating layer made of an inorganic material such as silicon nitride (SiNx), silicon oxide (SiOx) and the like, usually requires higher preparation temperature (e.g., 200°C-400°c) and needs to use a kind of corrosive gas in a process of film forming, and activity of organic semiconductor material will be damaged by high temperature and corrosive gas; and therefore, an insulating layer made of inorganic material is not applicable to the OTFT.

[0015] Secondly, for an insulating layer made of an organic material such as polyvinyl alcohol (PVA), polyvinyl pyrrolidone (PVP) and the like, its thickness is usually at a micron scale (1 μm - 2 μm); after an organic semiconductor active layer is packaged by the insulating layer, when the OTFT is applied to an array substrate, a via hole is required to be formed in the insulating layer for electrically connecting a drain electrode of the OTFT and a pixel electrode, and the insulating layer is quite different from the source and drain electrodes of OTFT in thickness and size, so that a technical difficulty in forming a via hole is increased, and it tends to generate fracture the via hole, thus reducing a technical reliability of the OTFT when applied in the array substrate.

[0016] For the above second problem, the inventors of the application have found that, if a thinner insulating layer made of an organic material is directly formed on an organic semiconductor active layer, it is hard to guarantee uniformity and continuity in forming the insulating layer thin film, resulting in decrease of coverage of the insulating layer on the organic semiconductor active layer or short of coverage on an edge of a gap between the source electrode and the drain electrode, thus affecting efficiency of the insulating layer for packaging and protecting the organic semiconductor active layer; moreover, if a thinner insulating layer made of an organic material is directly formed, problems such as too rough surface may appear, resulting in decrease of flatness of the insulating layer, and affecting the following film forming process(es).

[0017] Therefore, how to form a thin and uniform organic insulating layer, to reduce the technical difficulty in forming a via hole in the organic insulating layer while effectively packaging and protecting an organic semiconductor active layer, has become a urgent problem to be solved by a person of skill in the art.

[0018] At least one embodiment of the invention provides a preparation method of an organic thin film transistor 01, the preparation method comprising: forming a source-drain metal layer including a source electrode and a drain electrode, and forming an organic semiconductor active layer being in contact with the source electrode and the drain electrode; forming an organic insulating thin film on a substrate where the source-drain metal layer including the source electrode and the drain electrode and the organic semiconductor active layer have been formed; thinning the organic insulating thin film by an etching thinning process and curing the thinned organic insulating thin film by a curing process, or curing the organic insulating thin film by a curing process and thinning the cured organic insulating thin film by an etching thinning process, to form an organic insulating layer. The following embodiments are illustrated by taking an example of thinning the organic insulating thin film by an etching thinning process and curing the thinned organic insulating thin film by a curing process to form an organic insulating layer.

[0019] As shown in FIG. 1, the preparation method comprises steps of:

Step S01: forming a source-drain metal layer including a source electrode 12a and a drain electrode 12b, and forming an organic semiconductor active layer 13; the organic semiconductor active layer 13 is in contact with the source electrode 12a and the drain electrode 12b, as shown in FIG. 4(a) to FIG. 13(b).

Step S02: forming an organic insulating thin film 140 on a substrate where the source-drain metal layer including the source electrode 12a and the drain electrode 12b and the organic semiconductor active layer 13 have been formed; thinning the organic insulating thin film 140 by an etching thinning process, and curing the thinned organic insulating thin film 140 for a curing process, to form an organic insulating layer 14, as shown in FIG. 14(a) to FIG. 18(d).

[0020] In the above embodiment, the preparation method further comprises forming a gate electrode 11.

[0021] It should be noted that, firstly, the organic thin film transistor 01 can be divided into different types according to different classification standards. For example, according to different depositing sequences of the source electrode 12a, the drain electrode 12b and the

gate electrode 11 in the organic thin film transistor 01, the organic thin film transistor 01 can be divided into a bottom-gate type and a top-gate type.

[0022] For example, as shown in FIG. 2(a) and FIG. 2(b), in a case where the organic thin film transistor 01 to be formed is of a bottom-gate type, the source-drain metal layer including the source electrode 12a and the drain electrode 12b and the organic semiconductor active layer 13 are formed on a base substrate 10 including the gate electrode 11 and the gate insulating layer 15 formed thereon.

[0023] For example, as shown in FIG. 3(a) and FIG. 3(b), in a case where the organic thin film transistor 01 to be formed is of a top-gate type, the source-drain metal layer including the source electrode 12a and the drain electrode 12b and the organic semiconductor active layer 13 are formed on a base substrate 10; in that case, the gate electrode 11 is formed on a substrate including the organic insulating layer 14.

[0024] In addition, according to different depositing sequences of the source electrode 12a, the drain electrode 12b and the organic semiconductor active layer 13 in the organic thin film transistor 01, the organic thin film transistor 01 can be divided into a bottom-contact type and a top-contact type. If the source electrode 12a and the drain electrode 12b are below the organic semiconductor active layer 13, it is called a bottom-contact type, as shown in FIG. 2(a) and FIG. 3(a); on the contrary, if the source electrode 12a and the drain electrode 12b are above the organic semiconductor active layer 13, it is called a top-contact type, as shown in FIG. 2(b) and FIG. 3(b).

[0025] The preparation method provided by the embodiment of the present invention is applicable to various types of organic thin film transistors, i.e., a bottom-gate bottom-contact type shown in FIG. 2(a), a bottom-gate top-contact type shown in FIG. 2(b), a top-gate bottom-contact type shown in FIG. 3(a) and a top-gate top-contact type shown in FIG. 3(b).

[0026] Secondly, in the above step S01, in a case where the organic thin film transistor 01 is of a bottom-contact type, as shown in FIG. 2(a) and FIG. 3(a), when the organic semiconductor active layer 13 is in contact with the source electrode 12a and the drain electrode 12b, part of the drain electrode 12b may be exposed, i.e., if the organic thin film transistor 01 is applied in an array substrate, and the drain electrode 12b is electrically connected with the pixel electrode through a via hole, when the via hole passing though the organic insulating layer 14 is formed, it is not necessary for the via hole to run through the organic semiconductor active layer 13, which avoids damage to the organic semiconductor active layer 13 by the etching process.

[0027] Thirdly, in the above step S02, the etching thinning process is to thin the organic insulating thin film 140, for example, the organic insulating thin film 140 can be directly thinned to a corresponding thickness in a one-step thinning manner, or the organic insulating thin film 140 is thinned in a multi-step gradually thinning manner, and finally thinned to the corresponding thickness; the process can be flexibly adjusted according to thickness and material of the organic insulating thin film 140 to be formed, which is not limited by the embodiment of the present invention.

[0028] Fourthly, also in the above step S02, the etching thinning process, for example, may be a wet etching process, or a plasma dry etching process (e.g., O_2 plasma); the curing process, for example, may be a hot curing process by baking, or an ultraviolet curing process, or a combination thereof; suitable etching thinning process and curing process can be selected according to thickness and material of the organic insulating thin film 140 to be formed, which is not limited by the embodiment of the present invention.

[0029] Fifthly, as shown in FIG. 3(a) and FIG. 3(b), in a case where the organic thin film transistor 01 is of a top-contact type, the organic insulating layer 14 plays a role of insulating the gate electrode 11 from the organic semiconductor active layer 13, the source electrode 12a and the drain electrode 12b, while packaging and protecting the organic semiconductor active layer 13, the source electrode 12a and the drain electrode 12b.

[0030] At least one embodiment of the invention provides a preparation method of an organic thin film transistor 01, the preparation method comprising: forming a source-drain metal layer including a source electrode 12a and a drain electrode 12b, and forming an organic semiconductor active layer 13, the organic semiconductor active layer 13 being in contact with the source electrode 12a and the drain electrode 12b; forming an organic insulating thin film 140 on a substrate where the source-drain metal layer including the source electrode 12a and the drain electrode 12b and the organic semiconductor active layer 13 have been formed; thinning the organic insulating thin film 140 by an etching thinning process and curing the organic insulating thin film 140 by a curing process, to form an organic insulating layer 14. In the embodiment of the present invention, the preparation method further comprises forming a gate electrode 11.

[0031] When the preparation method provided by the embodiment of the present invention is used, because the organic insulating thin film 140 with a larger film thickness is formed at first, it can be ensured that the formed organic insulating thin film 140 has good uniformity and continuity in film formation, avoiding decrease in coverage on the organic semiconductor active layer 13 due to smaller film thickness or short of coverage on an edge of a gap between the source electrode 12a and the drain electrode 12b. Later, the organic insulating thin film 140 which has been already deposited is subjected to an etching thinning process, so the organic insulating layer 14 with a smaller film thickness can be obtained.

[0032] On such basis, the preparation method overcomes a shortcoming that it is hard to form a uniform and continuous thin film when an organic insulating layer with smaller film thickness is directly formed, so that a thin

and uniform organic insulating layer 14 is formed, while effectively packaging and protecting the organic semiconductor active layer 13; when the organic thin film transistor 01 is applied in an array substrate, because the pixel electrode is electrically connected with the drain electrode 12b of the organic thin film transistor 01, and the organic insulating layer 14 between the pixel electrode and the drain electrode 12b has a smaller film thickness, the technical difficulty of forming a via hole in the organic insulating layer 14 is reduced, the technical reliability is improved, and the method has very important value in actual applications.

[0033] In one embodiment, before forming the organic insulating thin film 140, the above step S01 further includes: forming an organic etching blocking layer 16. The organic etching blocking layer 16 is located above the organic semiconductor active layer 13, and the organic etching blocking layer 16 corresponds to a gap between the source electrode 12a and the drain electrode 12b.

[0034] Herein, the "above" in connection with the organic semiconductor active layer 13 refers to the side of the organic semiconductor active layer 13 away from the base substrate 10, and the organic etching blocking layer 16 is used for protecting the surface of a region of the organic semiconductor active layer 13 corresponding to the gap between the source electrode 12a and the drain electrode 12b.

[0035] On this basis, according to different depositing sequences of the source electrode 12a, the drain electrode 12b and the organic semiconductor active layer 13 in the organic thin film transistor, the above step S01, for example, may include two cases, which are described in detail hereinafter.

[0036] In a first case contained in the above step S01, for an organic thin film transistor of bottom-contact type, the above step S01, for example, may include four substeps, which are described one by one hereinafter.

[0037] Step S11: as shown in FIG. 4(a) and FIG. 4(b), forming an organic semiconductor thin film 130 and an organic photosensitive thin film 160 sequentially on a substrate where the source-drain metal layer including the source electrode 12a and the drain electrode 12b have been formed.

[0038] It should be noted that, firstly, referring to FIG. 4(a), in a case where the organic thin film transistor 01 to be formed is of a bottom-gate bottom-contact type, the substrate where the source-drain metal layer including source electrode 12a and the drain electrode 12b are formed is a base substrate 10 including a gate electrode 11 and a gate insulating layer 15. The gate insulating layer 15 can be made of an insulating material such as metal oxide, metal nitride, an organic material or the like, and may have a thickness, for example, from 30 nm to 1000 nm. Referring to FIG. 4(b), in a case where the organic thin film transistor 01 to be formed is of a top-gate bottom-contact type, the source-drain metal layer including source electrode 12a and the drain electrode 12b is formed on the base substrate 10. After a gate electrode is formed on a substrate of FIG. 4(b), the situation is shown in FIG. 3(a), at that time the gate electrode 11, for example, can be made of a metal material, an indium tin oxide (ITO) material, a doped silicon material, or an organic conductive material, and may have a thickness of, for example, 20nm-200nm; the source electrode 12a and the drain electrode 12b, for example, can be made of metal material (such as Au, Ag, Mo, Al, Cu, etc.) or ITO, and may have a thickness, for example, from 20 nm to 300 nm.

[0039] Secondly, the organic semiconductor thin film 130, for example, can be made of an organic semiconductor material such as pentacene, metallo phthalocyanine compounds, thienyl-polymers or polycyclic aromatic polymers and so on, and the depositing method can still use a technology known by a person of skill in the art, which is not limited here.

[0040] Thirdly, the organic photosensitive thin film, for example, can be made of a photoresist material, or can be made of a photosensitive polymer material which will undergo a photochemical reaction (e.g., a photo-crosslinking or photo-degrading) under light irradiation.

[0041] Step S12: as shown in FIG. 5(a) or FIG. 5(b), exposing and developing the substrate, on which the organic photosensitive thin film 160 has been formed, by using a common mask plate, and forming a completely-retained portion 160a of the organic photosensitive thin film and a completely-removed portion 160b of the organic photosensitive thin film.

[0042] In the step, the completely-retained portion 160a of the organic photosensitive thin film corresponds to a region of an organic semiconductor active layer 13 to be formed, while the completely-removed portion 160b of the organic photosensitive thin film corresponds to the rest regions.

[0043] Step S13: as shown in FIG. 6(a) or FIG. 6(b), removing the organic semiconductor thin film 130 (not shown) exposed by the completely-removed portion 160b (not shown) of the organic photosensitive thin film by an etching process, to form the organic semiconductor active layer 13.

[0044] In the step, the formed organic semiconductor active layer 13 exposes part of the drain electrode 12b and part of the source electrode 12a.

[0045] Step S14: as shown in FIG. 7(a) or FIG. 7(b), curing the completely-retained portion 160a (not shown) of the organic photosensitive thin film formed on the organic semiconductor active layer 13 by a curing process, to form the organic etching blocking layer 16.

[0046] It should be noted that, an organic semiconductor active layer with a certain pattern is often formed by a patterning process, and a typical patterning process refers to a process of etching and removing photoresist through exposure and development by using a mask plate for one time; since a magnitude of thickness of the organic semiconductor active layer (usually 10 nm - 200 nm) is less than a magnitude of thickness of the photoresist (usually 500 nm - 1000 nm), when the retained pho-

toresist on the surface of the organic semiconductor active layer are removed by an ashing process (e.g., dry etching) or stripping (e.g., wet etching), the organic semiconductor active layer may be possibly stripped together, or in the process of removing the photoresist, the surface of the organic semiconductor active layer corresponding to the gap between the source electrode and the drain electrode may be damaged, affecting performance of the organic thin film transistor.

[0047] Therefore, by using the above step S14, not only the step for removing the retained photoresist from the surface of the organic semiconductor active layer is saved, but the cured organic etching blocking layer 16 can protect the surface of the organic semiconductor active layer 13 from being damaged.

[0048] In a second case included in the above step S01, for an organic thin film transistor of top-contact type, the above step S01, for example, may include six sub-steps, which are described one by one hereinafter.

[0049] Step S21: as shown in FIG. 8(a) and FIG. 8(b), forming an organic semiconductor thin film 130 and an organic photosensitive thin film 160 sequentially.

[0050] It should be noted that, firstly, referring to FIG. 8(a), in a case where the organic thin film transistor 01 to be formed is of a bottom-gate top-contact type, the organic semiconductor thin film 130 and the organic photosensitive thin film 160 are sequentially formed on a base substrate 10 including the gate electrode 11 and the gate insulating layer 15 formed thereon. Referring to FIG. 8(b), in a case where the organic thin film transistor 01 to be formed is of a top-gate top-contact type, the organic semiconductor thin film 130 and the organic photosensitive thin film 160 are sequentially formed on the base substrate 10.

[0051] Secondly, the materials of the organic semiconductor thin film 130 and the organic photosensitive thin film 160 can be referred to step 11, which will be not repeated herein.

[0052] Step S22: as shown in FIG. 9(a) and FIG.9(b), after exposing and developing the substrate where the organic photosensitive thin film 160 has been formed by using a half-tone mask plate or a gray-tone mask plate, forming a completely-retained portion 160a of the organic photosensitive thin film, a completely-removed portion 160b of the organic photosensitive thin film, and a half-retained portion 160c of the organic photosensitive thin film.

[0053] In the step, the completely-retained portion 160a of the organic photosensitive thin film corresponds to a region of an organic etching blocking layer 16 to be formed, the half-retained portion 160c of the organic photosensitive thin film corresponds to a region of an organic semiconductor active layer 13 to be formed, where is not covered by the organic etching blocking layer 16, and the completely-removed portion 160b of the organic photosensitive thin film corresponds to the rest regions.

[0054] Step S23: as shown in FIG. 10(a) or FIG. 10(b), removing the organic semiconductor thin film 130 exposed the completely-retained portion 160b (not shown) of the organic photosensitive thin film by an etching process, to form the organic semiconductor active layer 13.

[0055] Step S24: as shown in FIG. 11(a) or FIG. 11(b), removing the organic photosensitive thin film 160 in the half-retained portion 160c (not shown) of the organic photosensitive thin film by an ashing process, to expose a region of the organic semiconductor active layer 13 corresponding to the half-retained portion 160c of the organic photosensitive thin film.

[0056] Step S25: as shown in FIG. 12(a) or FIG. 12(b), curing the completely-retained portion 160a (not shown) of the organic photosensitive thin film formed on the organic semiconductor active layer 13 by a curing process, to form the organic etching blocking layer 16.

[0057] Step S26: as shown in FIG. 13(a) or FIG. 13(b), forming a source-drain metal layer including the source electrode 12a and the drain electrode 12b on a substrate where the organic semiconductor active layer 13 and the organic etching blocking layer 16 are formed.

[0058] Based on the above description, both step S14 and step S25 include two sub-steps, i.e., firstly, curing the completely-retained portion 160a of the organic photosensitive thin film formed on the organic semiconductor active layer 13 by a curing process; secondly, thinning the cured completely-retained portion 160a of the organic photosensitive thin film by an etching thinning process, to form the organic etching blocking layer 16. Or, the above step S14 and step S25 may include: before curing the completely-retained portion 160a of the organic photosensitive thin film formed on the organic semiconductor active layer by a curing process, thinning the completely-retained portion of the organic photosensitive thin film by an etching thinning process, to form the organic etching blocking layer.

[0059] The formed organic etching blocking layer 16 is thinned by the etching thinning process, to provide a more flat substrate for the following film forming process, and avoid forming non-uniform film.

[0060] Here, considering that the wet etching process has poor control in forming a pattern with a smaller feature size, the etching thinning process is preferably a plasma etching process, for example, an oxygen plasma etching, to more accurately control a speed of etching.

[0061] Herein, for example, the completely-retained portion 160a of the organic photosensitive thin film formed on the organic semiconductor active layer 13 can be cured by way of baking.

[0062] Herein, in comprehensive consideration of preparation costs of the organic photosensitive thin film and an appropriate thickness of the organic etching blocking layer 16 finally formed, in at least one embodiment, the completely-retained portion 160a of the organic photosensitive thin film formed on the organic semiconductor active layer 13 may have a thickness of 500 nm - 1000 nm. Thereafter, in at least one embodiment, the completely-retained portion 160a of the organic photosensitive thin film thinned by the etching thinning process

may have a thickness of 300 nm - 500 nm.

[0063] Base on that the liquid organic photosensitive material has better surface covering capability, to get better contact with the organic semiconductor thin film 130, in at least one embodiment, in step S11 and step S21 described above, the organic photosensitive thin film 160 can be formed through a solution coating process.

[0064] Her "solution coating" refers to a technology of depositing a thin film on a substrate surface by using a chemical method such as chemical reaction or electrochemical reaction in solution. For example, the solution coating process may involve a chemical coating process, a sol-gel method process, an electroplating process, a coating process, a spin-coating process, a Langmuir-Blodgett (LB) process, and the like. The solution coating process does not need a vacuum condition, requires simple instruments, can form a film on surfaces of various substrates, and raw materials are easy to get, so the solution coating has a much wider prospect in application.

[0065] Based on the above, the above step S02, for example, may include seven sub-steps, which are described one by one hereinafter.

[0066] S31: as shown in FIG. 14(a), or FIG. 14(b), or FIG. 14(c), or FIG. 14(d), forming an organic insulating thin film 140 on a substrate where the source-drain metal layer including the source electrode 12a and the drain electrode 12b, the organic semiconductor active layer 13 and the organic etching blocking layer have been formed thereon.

[0067] The organic insulating thin film 140, for example, may be photosensitive high-molecular compound (e.g., UV curing adhesive), or polyvinyl chloride (PVC), or polyethylene terephthalate (PET), or polyethylene naphthalate (PEN), or polyimide (PI), or polyvinyl chloride (PVC) or polytetrafluoroethylene (PTFE), etc.

[0068] S32: pre-baking the formed organic insulating thin film 140 at a first temperature. For example, the first temperature can be 110 °C - 150 °C.

[0069] S33: as shown in FIG. 15(a), or FIG. 15(b), or FIG. 15(c), or FIG. 15(d), thinning the organic insulating thin film 140 pre-baked at the first temperature, by a first etching thinning process.

[0070] S34: pre-baking the thinned organic insulating thin film 140 at a second temperature. For example, the second temperature can be 150 °C - 200 °C.

[0071] S35: as shown in FIG. 16(a), or FIG. 16(b), or FIG. 16(c), or FIG. 16(d), curing first regions (marked as Si in the diagrams) of the organic insulating thin film 140 pre-baked at the second temperature, by a first curing process.

[0072] In the step, the first regions S_1 are the rest regions of the organic insulating thin film 140 except regions above the source electrode 12a, above the drain electrode 12b, and above the gap between the source electrode 12a and the drain electrode 12b.

[0073] S36: as shown in FIG. 17(a), or FIG. 17(b), or FIG. 17(c), or FIG. 17(d), thinning second regions (marked as S_2 in the diagrams) of the organic insulating thin film 140 processed by the first curing process, by a second etching thinning process.

[0074] In the step, the second regions S_2 are the regions of the organic insulating thin film 140 above the source electrode 12a, above the drain electrode 12b, and above the gap between the source electrode 12a and the drain electrode 12b.

[0075] S37: as shown in FIG. 18(a), or FIG. 18(b), or FIG. 18(c), or FIG. 18(d), curing the second regions S_2 of the organic insulating thin film 140 processed by the second etching thinning process, by a second curing process, to form an organic insulating layer 14.

[0076] Gradually curing and thinning in the above steps S32 to S37, can flexibly control technical parameters of thinning, also can avoid deformation and cracking of organic materials due to fast heating when the organic materials are directly cured after thinning.

[0077] Herein, in comprehensive consideration of the preparation costs of the organic insulating thin film and the appropriate thickness of the organic insulating layer 14 finally formed, in at least one embodiment, the formed organic insulating thin film 140 may have a thickness from 500 nm to 1000 nm. In at least one embodiment, the thinned organic insulating layer 14 may have a thickness from 300 nm to 500 nm.

[0078] Based on the above, considering that the liquid organic insulating material has greater surface covering capability, to better protect a side surface of the formed organic semiconductor active layer 13 perpendicular to the base substrate 10, in at least one embodiment, the organic insulating thin film 140 can be formed by a solution coating process.

[0079] In at least one embodiment, as shown in FIG. 16(a), or FIG. 16(b), or FIG. 16(c), or FIG. 16(d), the above step S35, for example, may include steps of: by using an ultraviolet curing process, making ultraviolet light irradiate from the side of the base substrate 10 away from the source electrode 12a, the drain electrode 12b and the gate electrode 11, or away from the source electrode 12a, the drain electrode 12b and the organic semiconductor active layer 13, i.e., from the back side of the base substrate 10, to the first regions S_1 of the organic insulating thin film 140 pre-baked at the second temperature, so as to cure the first regions S_1 of the organic insulating thin film 140.

[0080] Herein, because the source electrode 12a, the drain electrode 12b and the gate electrode 11 or the organic semiconductor active layer 13 are used as a structure for blocking the ultraviolet light, a mask process is saved, further simplifying the preparation process.

[0081] In at least one embodiment, as shown in FIG. 18(a), or FIG. 18(b), or FIG. 18(c), or FIG. 18(d), the above step S37, for example, may include steps of: by using an ultraviolet curing process, making the ultraviolet light irradiate from the side of the base substrate 10 close to the source electrode 12a, the drain electrode 12b and the gate electrode 11, or close to the source electrode

12a, the drain electrode 12b and the organic semiconductor active layer 13, i.e., from the front side of the base substrate 10 where respective film layers have been deposited to the second regions S_2 of the organic insulating thin film 140 processed by the second etching thinning process, so as to cure the second regions S_2 of the organic insulating thin film 140, to form the organic insulating layer 14.

[0082] Based on the above, the etching thinning process, for example, may be a plasma etching process.

[0083] On the basis of the above, at least one embodiment of the present invention provides an organic thin film transistor 01 prepared by the above preparation method, the organic thin film transistor 01 comprising an organic insulating layer 14 above an organic semiconductor active layer 13; the organic insulating layer 14 is thin and uniform, and its thickness ranges from 300 nm to 500 nm. The term "above the organic semiconductor active layer 13" refers to be on a side of the organic semiconductor active layer 13 away from the base substrate 10.

[0084] At least one embodiment of the present invention further provides a preparation method of the array substrate 02 shown in FIG. 19(a), or FIG. 19(b), or FIG. 19(c), or FIG. 19(d), and the preparation method includes steps S41 to S43, which are described one by one hereinafter.

[0085] S41: forming an organic thin film transistor, the organic thin film transistor 01 being prepared by using the above preparation method.

[0086] S42: forming a planarization layer 20 on an organic insulating layer 14 of the organic thin film transistor, and at least forming a via hole 21 passing through the planarization layer 20 and the organic insulating layer 14, wherein the via hole 21 exposes a drain electrode 12b of the organic thin film transistor.

[0087] In the case where the organic semiconductor active layer 13 of the organic thin film transistor covers the drain electrode 12b, the via hole 21 will pass though the organic semiconductor active layer to expose the drain electrode 12b.

[0088] Herein, the planarization layer 20, for example, may be made of a photoresist material, a PI (polyimide) material; and its thickness, for example, can be from 500 nm to 2000 nm.

[0089] S43: forming a pixel electrode 22 on the planarization layer 20, and the pixel electrode 22 is electrically connected with the drain electrode 12b through the via hole 21.

[0090] In the step, the organic thin film transistor in FIG. 19(a) is of a bottom-gate bottom-contact type, the organic thin film transistor in FIG. 19(b) is of a top-gate bottom-contact type, the organic thin film transistor in FIG. 19(c) is of a bottom-gate top-contact type, and the organic thin film transistor in FIG. 19(d) is of a top-gate top-contact type.

[0091] Because the organic insulating layer 14 between the pixel electrode 22 and the drain electrode 12b is small in film thickness, the technical difficulty in forming a via hole on the organic insulating layer 14 is reduced, the technical reliability is improved, and the method has important value in actual application.

[0092] Based on the above, the preparation method of the array substrate 02 may further include forming a common electrode.

[0093] On such basis, at least one embodiment of the present invention provides an array substrate 02 prepared by the above preparation method, and the array substrate 02 includes the organic thin film transistor 01 described above. In at least one embodiment, the array substrate further includes a planarization layer 20 located on the organic insulating layer 14 of the organic thin film transistor, and a pixel electrode 22 located on the planarization layer 20; the pixel electrode 22 is electrically connected with the drain electrode 12b through a via hole 21 passing through the planarization layer 20 and the organic insulating layer 14.

[0094] At least one embodiment of the present invention further provides a display device, the display device comprising the organic thin film transistor 01 or the array substrate 02.

[0095] The display device, for example, may be a liquid crystal panel, a liquid crystal display, a liquid crystal television, an organic light emitting display (OLED) panel, an OLED display, an OLED television or E-paper and other display devices.

[0096] It should be noted that, all the drawings of the invention are schematic diagrams/views of the organic thin film transistor and the array substrate, merely to clearly describe the structure reflected in the technical solution related with the invention; other structures unrelated with the invention are the existing structure, which are not or only partially reflected in the drawings.

[0097] The above-mentioned is merely an exemplary embodiment of the present invention, which does not intend to restrict the protection scope of the present invention. The protection scope of the present invention is determined by the attached claims.

[0098] The present application claims priority of Chinese Patent Application No. 201410319179.7 filed on July 4, 2014, the disclosure of which is incorporated herein by reference in its entirety as part of the present application.

Claims

1. A preparation method of an organic thin film transistor, comprising:

   forming a source-drain metal layer including a source electrode and a drain electrode, and forming an organic semiconductor active layer, wherein the organic semiconductor active layer is in contact with the source electrode and the drain electrode;

forming an organic insulating thin film on a substrate where the source-drain metal layer including the source electrode and the drain electrode and the organic semiconductor active layer have been formed;
thinning the organic insulating thin film by an etching thinning process and curing the thinned organic insulating thin film by a curing process, or curing the organic insulating thin film by a curing process and thinning the cured organic insulating thin film by an etching thinning process, to form an organic insulating layer;
wherein the preparation method further comprises forming a gate electrode.

2. The preparation method according to claim 1, before forming the organic insulating thin film, further comprising: forming an organic etching blocking layer;
wherein the organic etching blocking layer is located above the organic semiconductor active layer, and the organic etching blocking layer corresponds to a gap between the source electrode and the drain electrode.

3. The preparation method according to claim 2, wherein the process of forming a source-drain metal layer including a source electrode and a drain electrode, an organic semiconductor active layer, and an organic etching blocking layer includes:

forming an organic semiconductor thin film and an organic photosensitive thin film sequentially on a substrate where the source-drain metal layer including the source electrode and the drain electrode has been formed;
after exposing and developing the substrate where the organic photosensitive thin film has been formed by using a common mask plate, forming a completely-retained portion of the organic photosensitive thin film and a completely-removed portion of the organic photosensitive thin film; wherein the completely-retained portion of the organic photosensitive thin film corresponds to a region of an organic semiconductor active layer to be formed, and the completely-removed portion of the organic photosensitive thin film corresponds to rest regions;
removing the organic semiconductor thin film exposed in the completely-removed portion of the organic photosensitive thin film by an etching process, to form the organic semiconductor active layer; wherein the formed organic semiconductor active layer exposes part of the drain electrode and part of the source electrode; and
curing the completely-retained portion of the organic photosensitive thin film formed on the organic semiconductor active layer by a curing process, to form the organic etching blocking layer.

4. The preparation method according to claim 2, wherein the process of forming a source-drain metal layer including a source electrode and a drain electrode, an organic semiconductor active layer, and an organic etching blocking layer, includes:

forming an organic semiconductor thin film and an organic photosensitive thin film sequentially;
after exposing and developing the substrate where the organic photosensitive thin film has been formed by using a half-tone mask or a gray-tone mask, forming a completely-retained portion of the organic photosensitive thin film, a completely-removed portion of the organic photosensitive thin film, and a half-retained portion of the organic photosensitive thin film, wherein the completely-retained portion of the organic photosensitive thin film corresponds to a region of an organic etching blocking layer to be formed, the half-retained portion of the organic photosensitive thin film corresponds to a region of an organic semiconductor active layer to be formed, where is not covered by the organic etching blocking layer, and the completely-removed portion of the organic photosensitive thin film corresponds to rest regions;
removing the organic semiconductor thin film exposed in the completely-removed portion of the organic photosensitive thin film by an etching process, to form the organic semiconductor active layer;
removing the organic photosensitive thin film in the half-retained portion of the organic photosensitive thin film by an ashing process, to expose a region of the organic semiconductor active layer corresponding to the half-retained portion of the organic photosensitive thin film;
curing the completely-retained portion of the organic photosensitive thin film formed on the organic semiconductor active layer by a curing process, to form the organic etching blocking layer; and
forming the source-drain metal layer including the source electrode and the drain electrode on the substrate where the organic semiconductor active layer and the organic etching blocking layer have been formed.

5. The preparation method according to claim 3 or 4, wherein,
after curing the completely-retained portion of the organic photosensitive thin film on the organic semiconductor active layer by the curing process, thinning the cured completely-retained portion of the organic photosensitive thin film by an etching thinning process, to form the organic etching blocking layer;

or
before curing the completely-retained portion of the organic photosensitive thin film on the organic semiconductor active layer by the curing process, thinning the completely-retained portion of the organic photosensitive thin film by an etching thinning process, to form the organic etching blocking layer.

6. The preparation method according to claim 5, wherein the completely-retained portion of the organic photosensitive thin film thinned by the etching thinning process has a thickness from 300 nm - 500 nm.

7. The preparation method according to any one of claims 3 to 6, wherein the completely-retained portion of the organic photosensitive thin film formed on the organic semiconductor active layer has a thickness from 500 nm to 1000 nm.

8. The preparation method according to any one of claims 3 to 7, wherein the organic photosensitive thin film is formed by a solution coating process.

9. The preparation method according to any one of claims 1 to 8, wherein the process of forming an organic insulating layer includes:

forming an organic insulating thin film on a substrate where the source-drain metal layer including the source electrode and the drain electrode and the organic semiconductor active layer have been formed;
pre-baking the formed organic insulating thin film at a first temperature;
thinning the organic insulating thin film pre-baked at the first temperature, by a first etching thinning process;
pre-baking the thinned organic insulating thin film at a second temperature;
curing first regions of the organic insulating thin film pre-baked at the second temperature, by a first curing process; wherein the first regions are rest regions of the organic insulating thin film except regions above the source electrode, above the drain electrode, and above the gap between the source electrode and the drain electrode;
thinning second regions of the organic insulating thin film processed by the first curing process, by a second etching thinning process; wherein the second regions are the regions of the organic insulating thin film above the source electrode, above the drain electrode, and above the gap between the source electrode and the drain electrode; and
curing the second regions of the organic insulating thin film processed by the second etching thinning process, by a second curing process, to form an organic insulating layer.

10. The preparation method according to claim 9, wherein the first temperature is 110 °C - 150 °C.

11. The preparation method according to claim 9 or 10, wherein the second temperature is 150 °C - 200 °C.

12. The preparation method according to any one of claims 1 to 11, wherein the formed organic insulating thin film has a thickness from 500 nm - 1000 nm.

13. The preparation method according to any one of claims 1 to 12, wherein the formed organic insulating thin film has a thickness from 300 nm - 500 nm.

14. The preparation method according to any one of claims 1 to 13, wherein the organic insulating thin film is formed by a solution coating process.

15. A preparation method of an array substrate, comprising:

forming an organic thin film transistor, wherein the organic thin film transistor is prepared by the preparation method according to any one of claims 1 to 14 described above.

16. The preparation method according to claim 15, further comprising:

forming a planarization layer on an organic insulating layer of the organic thin film transistor, and forming a via hole passing through the planarization layer and the organic insulating layer, wherein the via hole exposes the drain electrode of the organic thin film transistor; and forming a pixel electrode on the planarization layer, wherein the pixel electrode is electrically connected with the drain electrode through the via hole.

17. An organic thin film transistor, wherein the organic thin film transistor is prepared by the preparation method according to any one of claims 1 to 14 described above;
wherein the organic thin film transistor includes an organic insulating layer located above the organic semiconductor active layer, the organic insulating layer having a thickness from 300 nm - 500 nm.

18. An array substrate comprising the organic thin film transistor according to claim 17.

19. The array substrate according to claim 18, further comprising: a planarization layer located on an organic insulating layer of the organic thin film transistor, and a pixel electrode located on the planarization

layer;
wherein the pixel electrode is at least electrically connected with the drain electrode through a via hole passing through the planarization layer and the organic insulating layer.

20. A display device comprising the organic thin film transistor according to claim 17, or the array substrate according to claim 18 to 19.

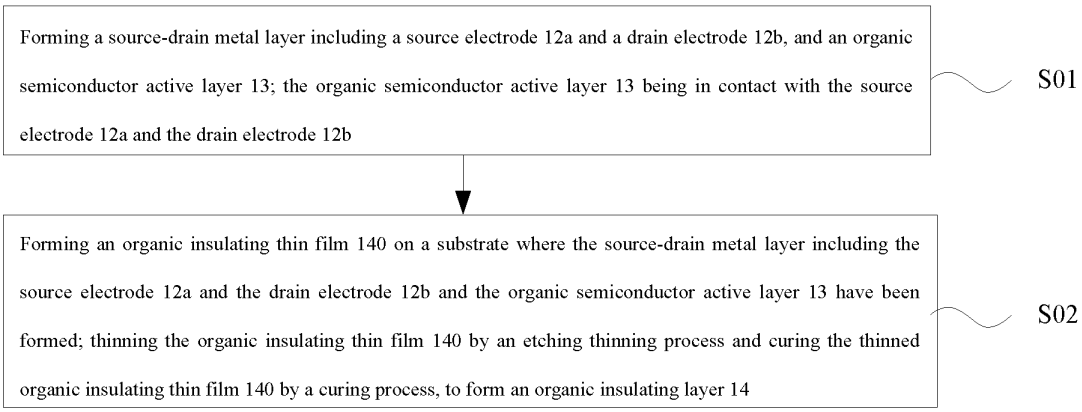

FIG. 1

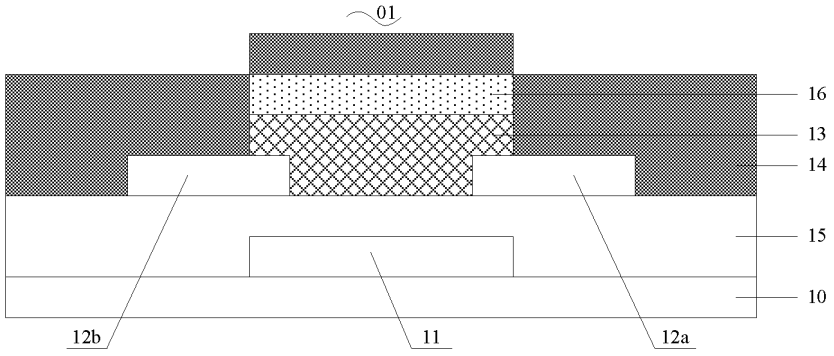

FIG.2(a)

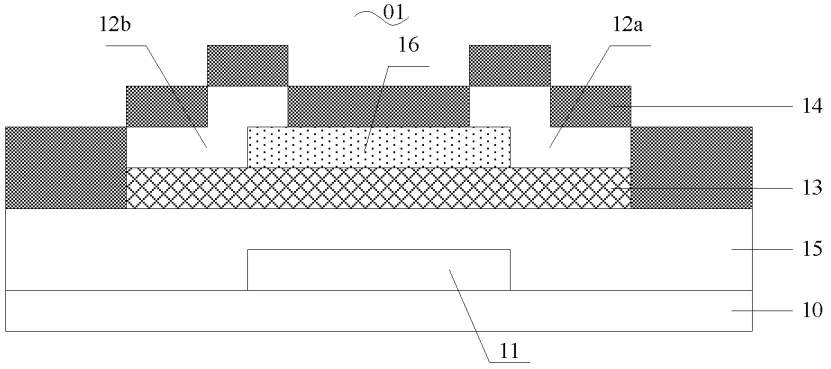

FIG. 2(b)

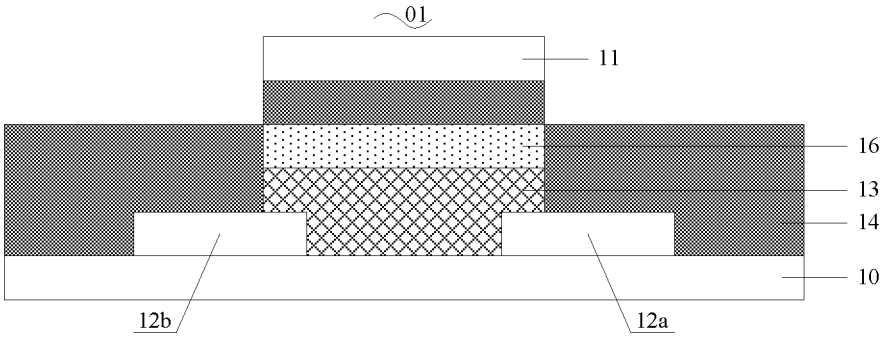

FIG. 3(a)

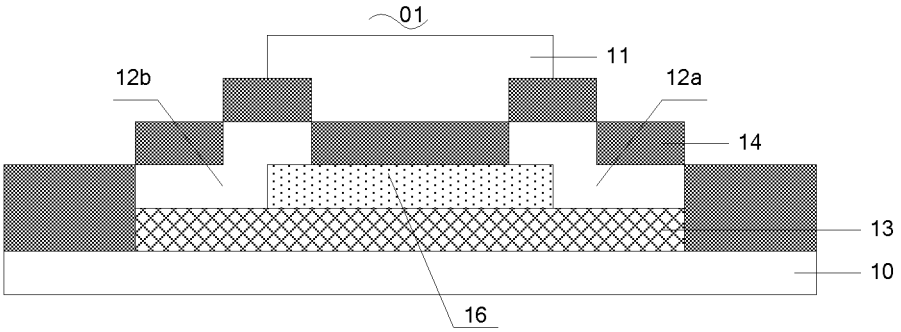

FIG. 3(b)

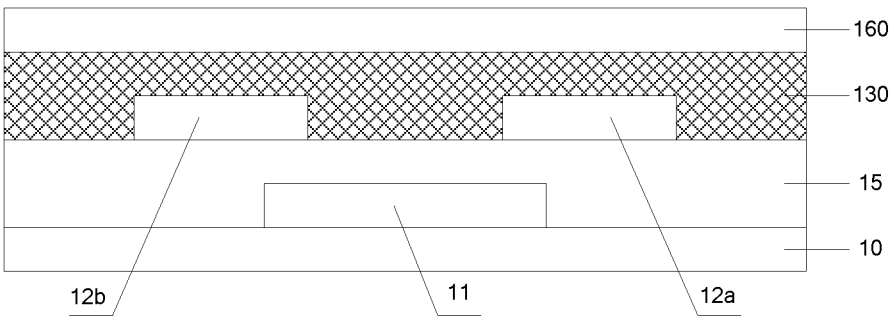

FIG. 4(a)

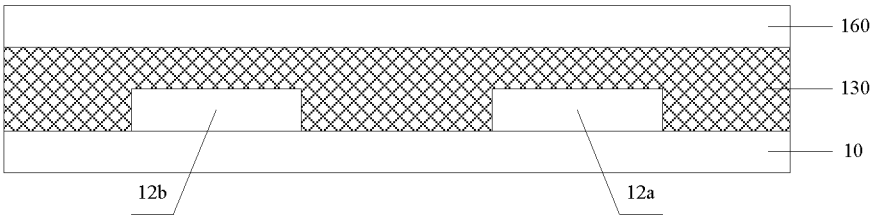

FIG. 4(b)

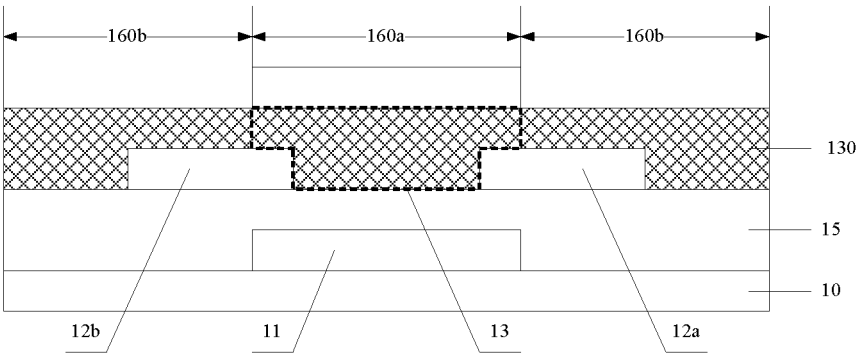

FIG. 5(a)

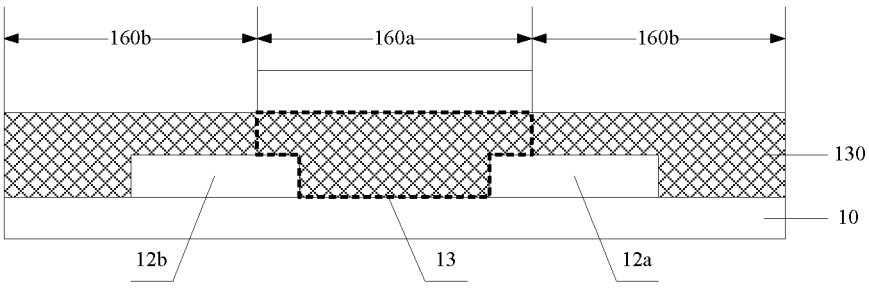

FIG. 5(b)

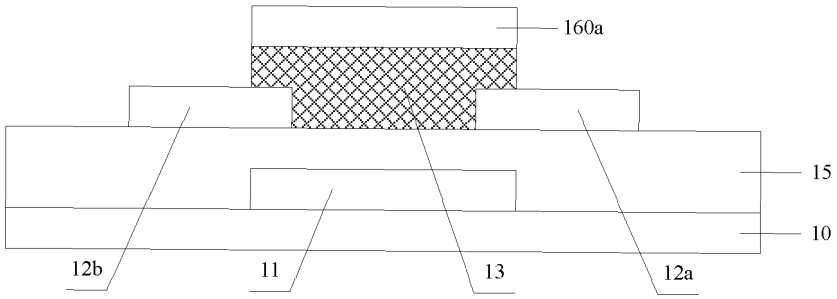

FIG. 6(a)

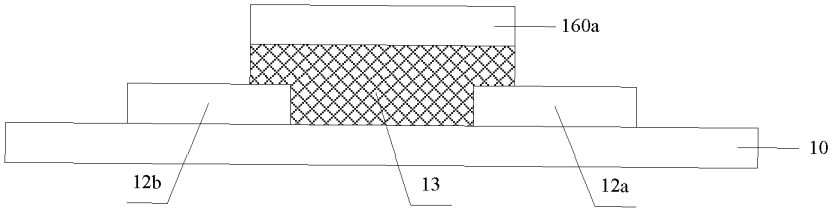

FIG. 6(b)

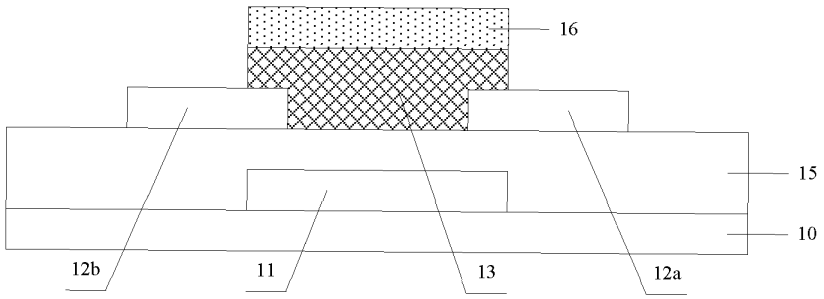

FIG. 7(a)

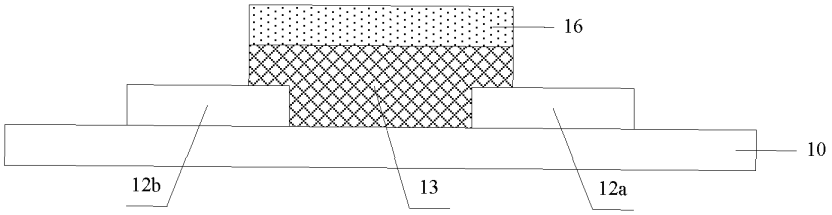

FIG. 7(b)

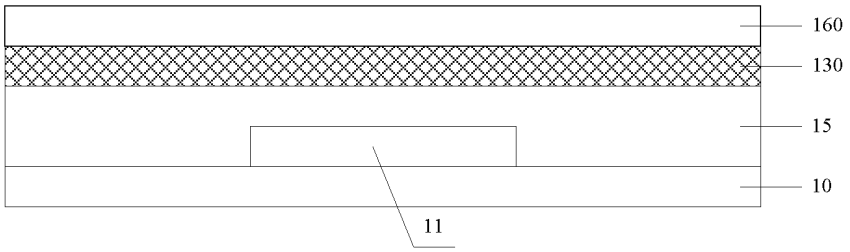

FIG. 8(a)

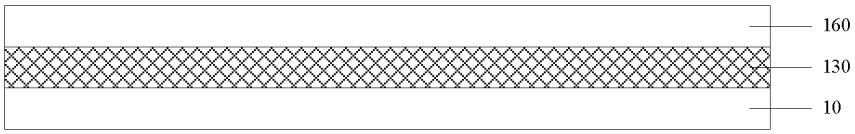

FIG. 8(b)

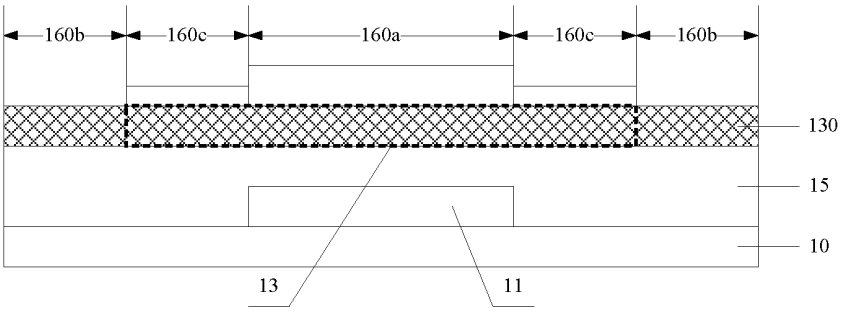

FIG. 9(a)

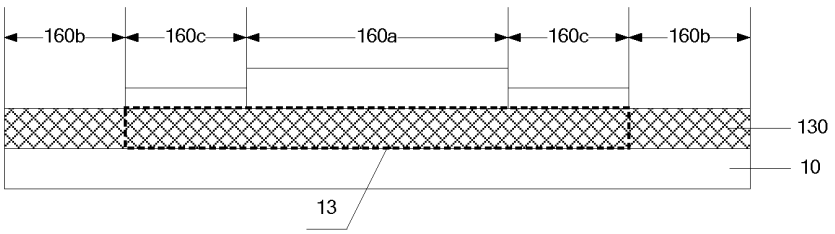

FIG. 9(b)

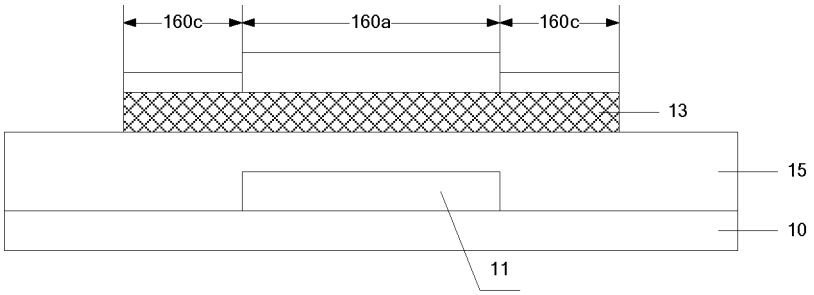

FIG. 10(a)

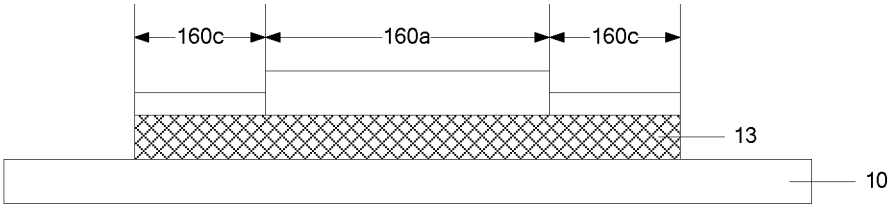

FIG. 10(b)

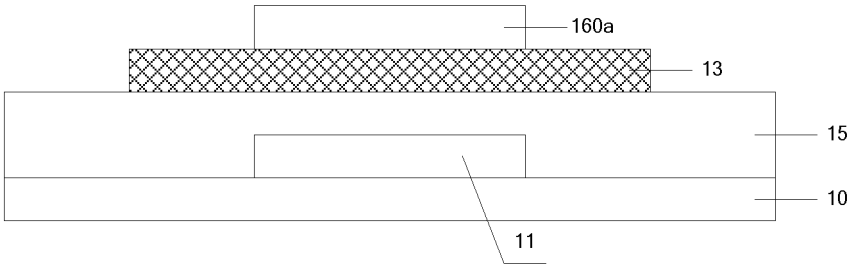

FIG. 11(a)

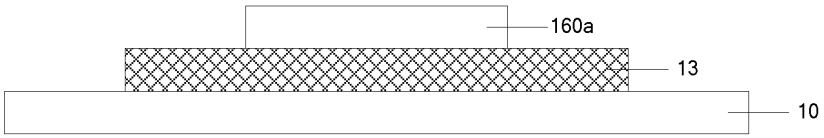

FIG. 11(b)

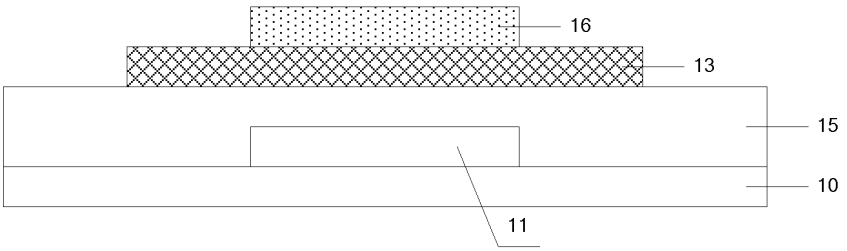

FIG. 12(a)

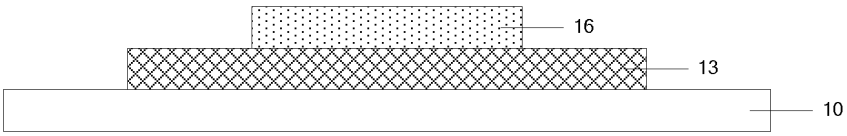

FIG. 12(b)

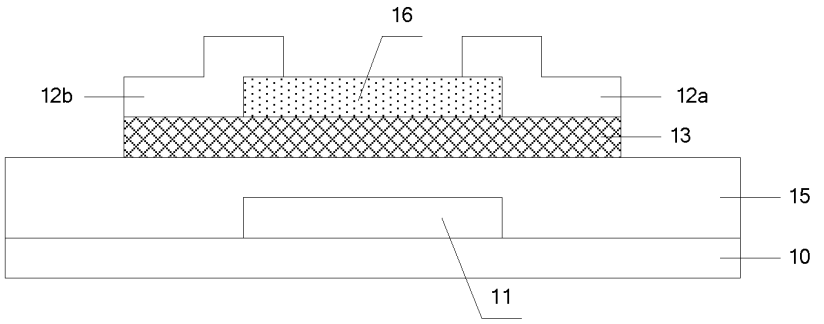

FIG. 13(a)

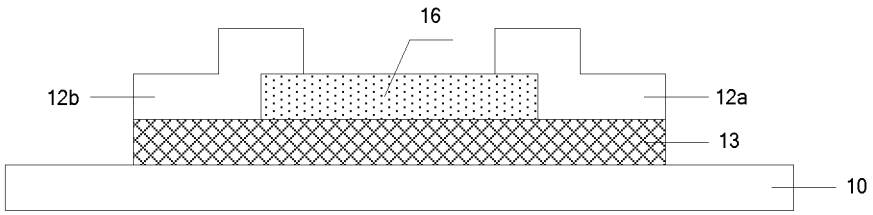

FIG. 13(b)

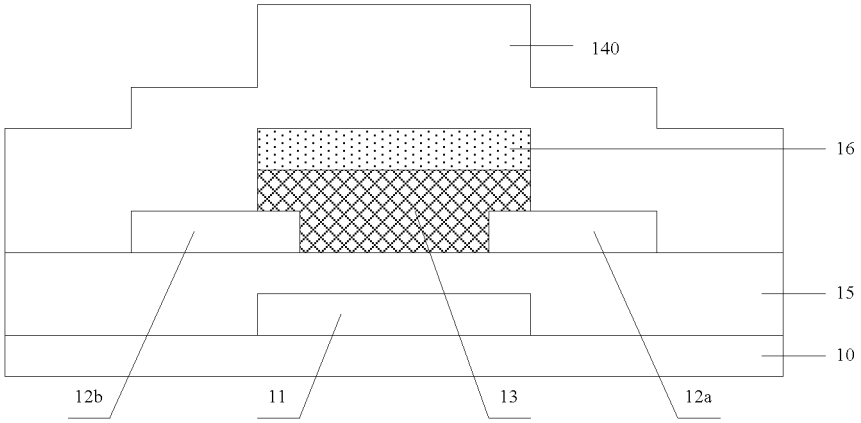

FIG. 14(a)

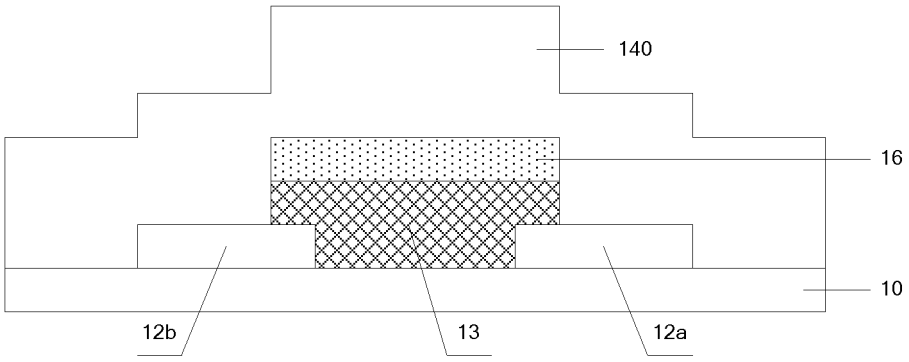

FIG. 14(b)

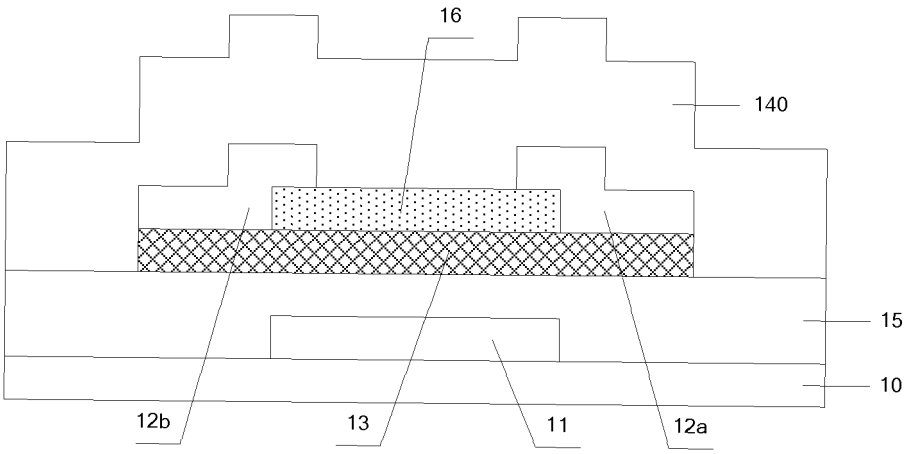

FIG. 14(c)

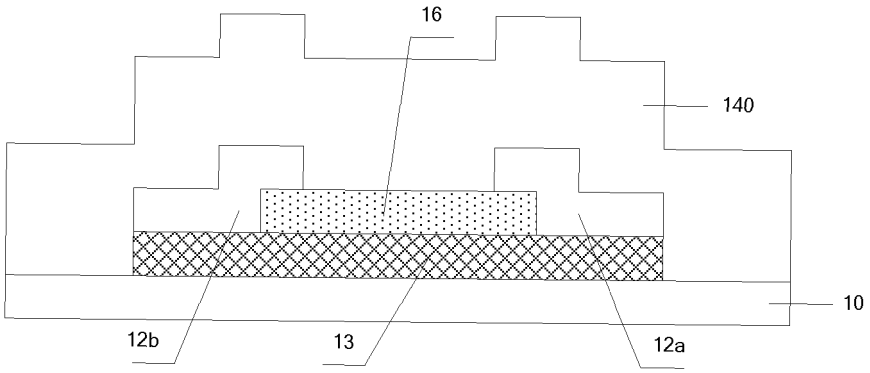

FIG. 14(d)

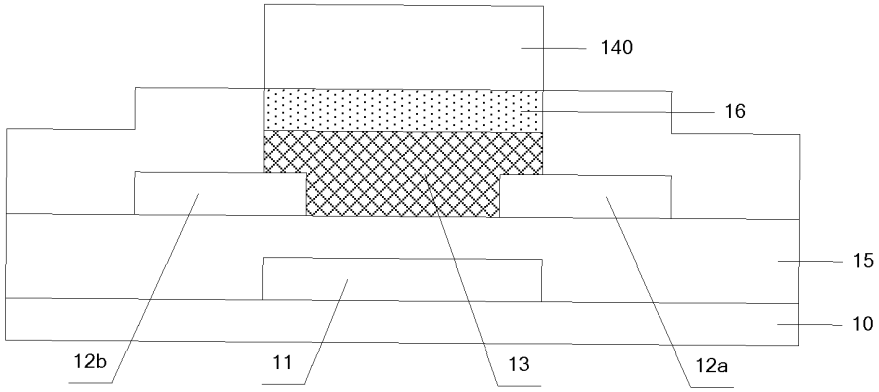

FIG. 15(a)

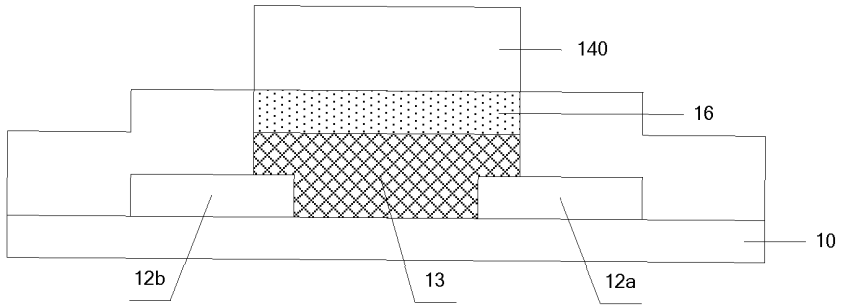

FIG. 15(b)

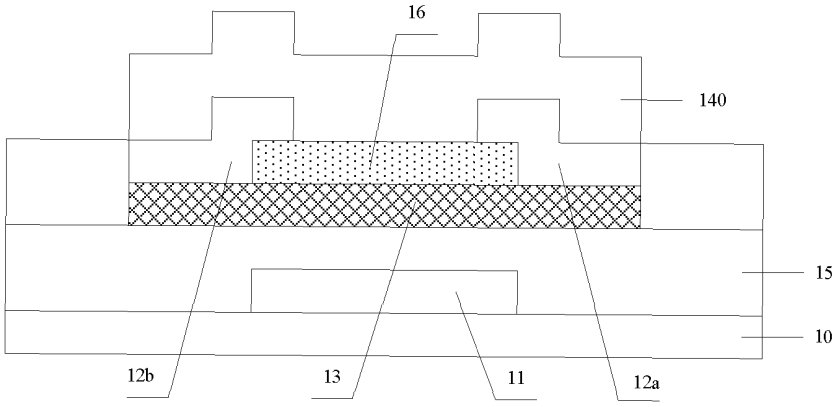

FIG. 15(c)

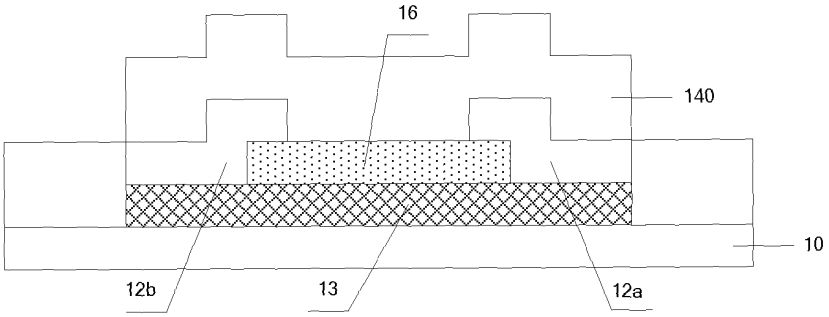

FIG. 15(d)

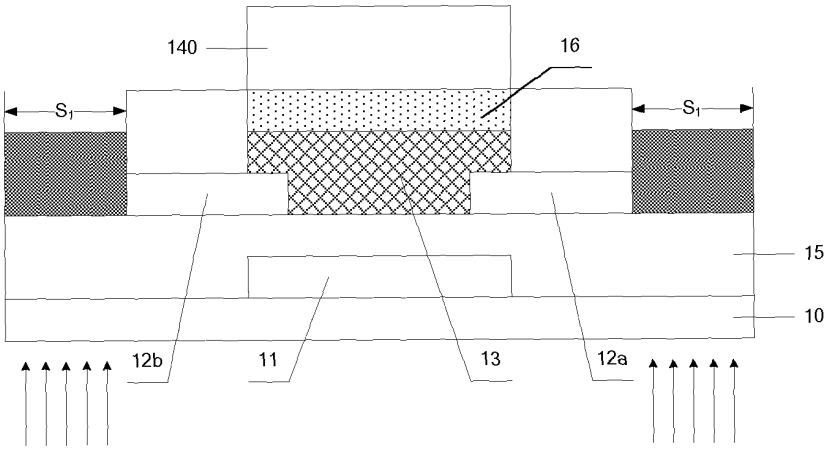

FIG. 16(a)

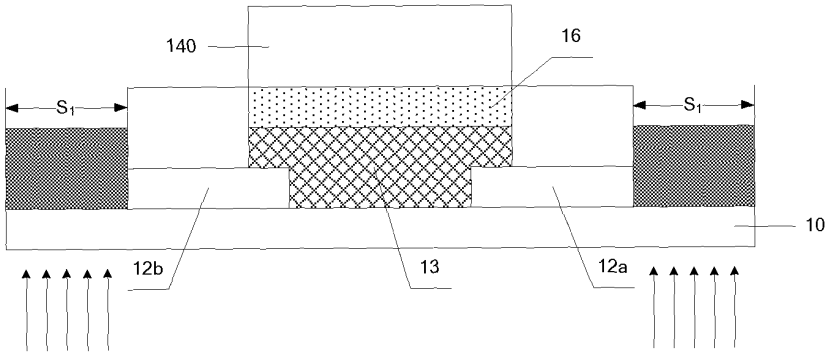

FIG. 16(b)

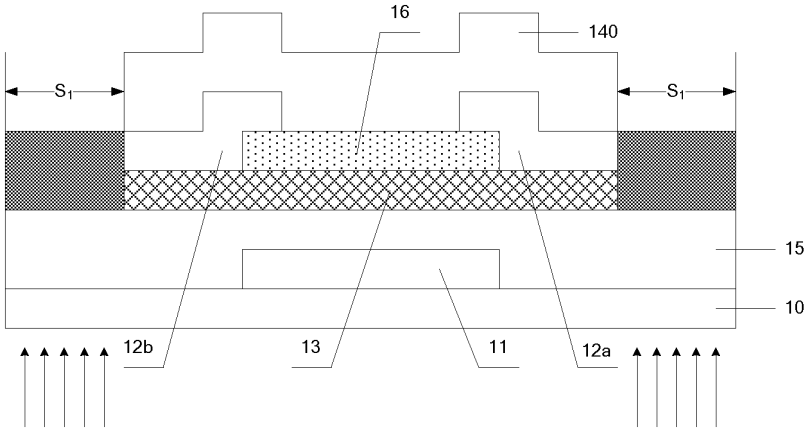

FIG. 16(c)

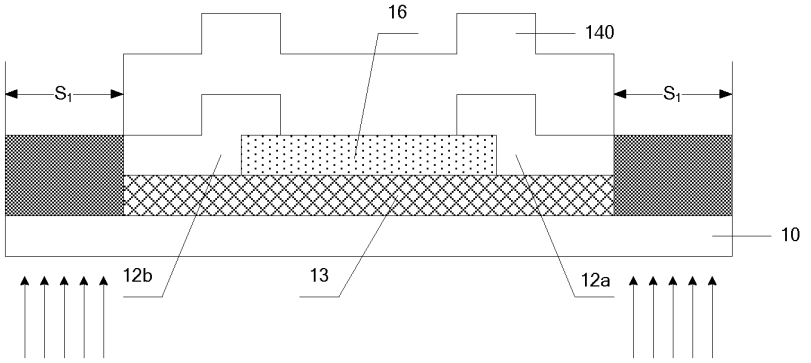

FIG. 16(d)

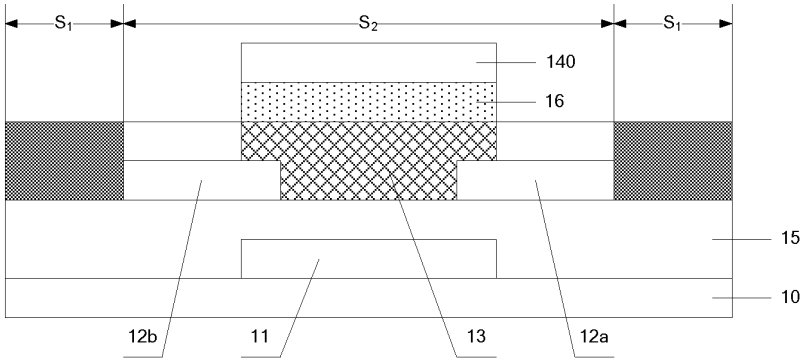

FIG. 17(a)

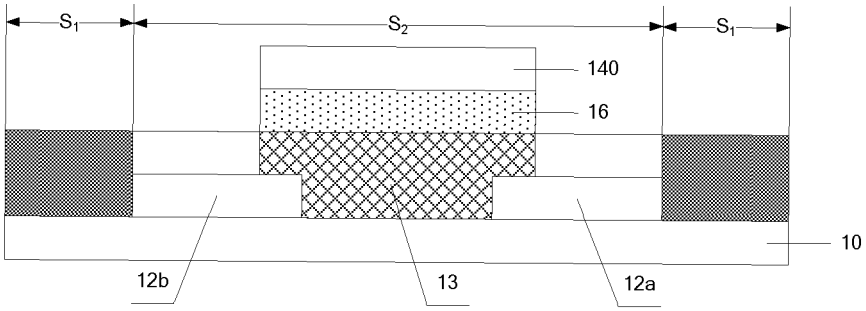

FIG. 17(b)

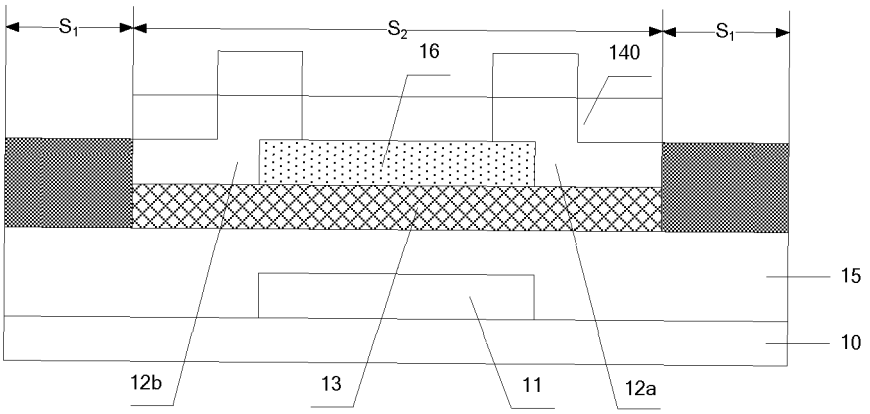

FIG. 17(c)

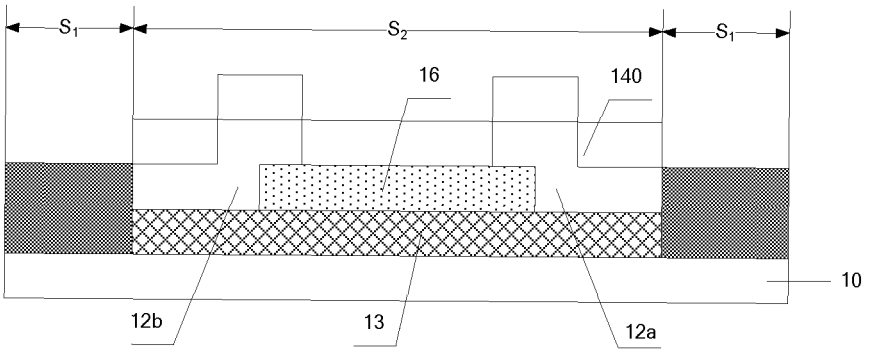

FIG. 17(d)

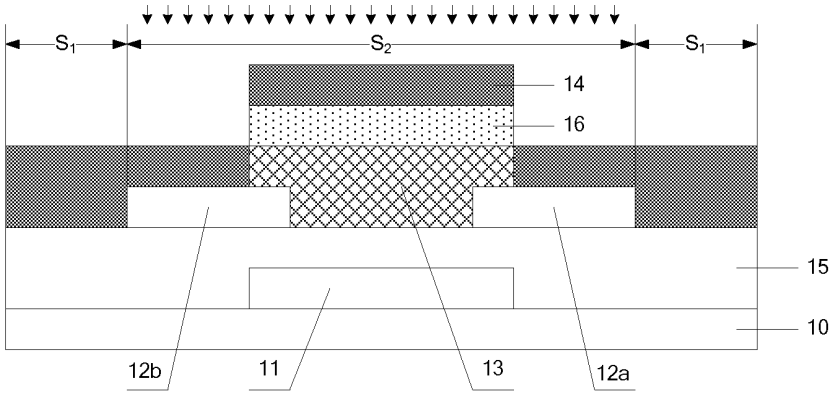

FIG. 18(a)

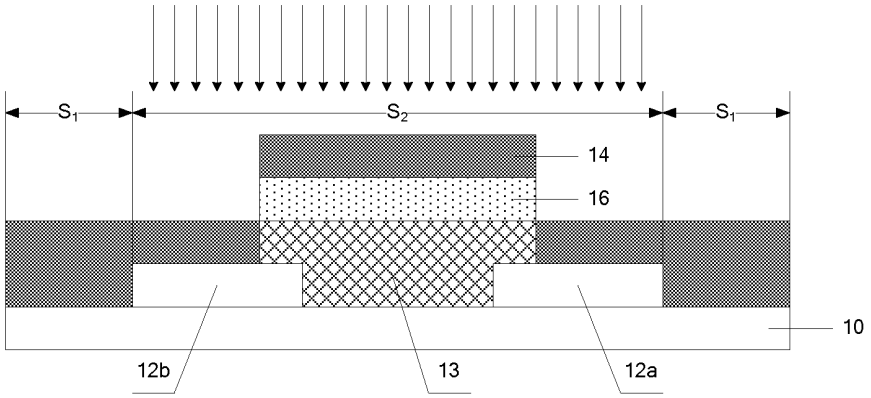

FIG. 18(b)

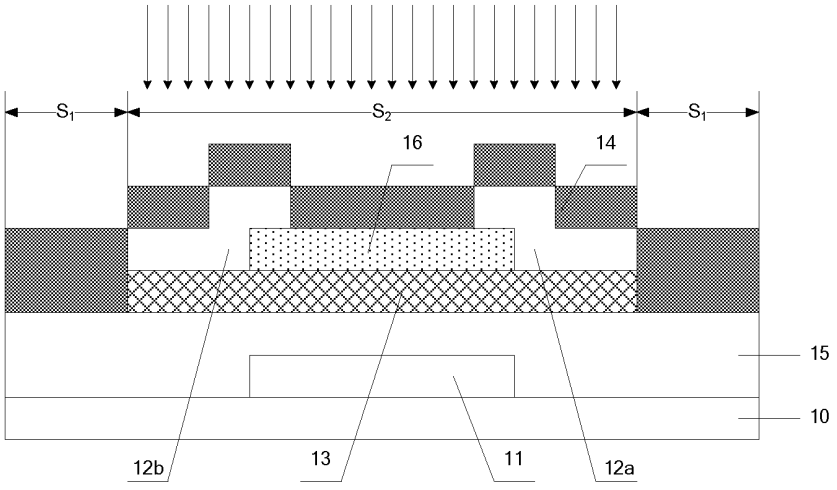

FIG. 18(c)

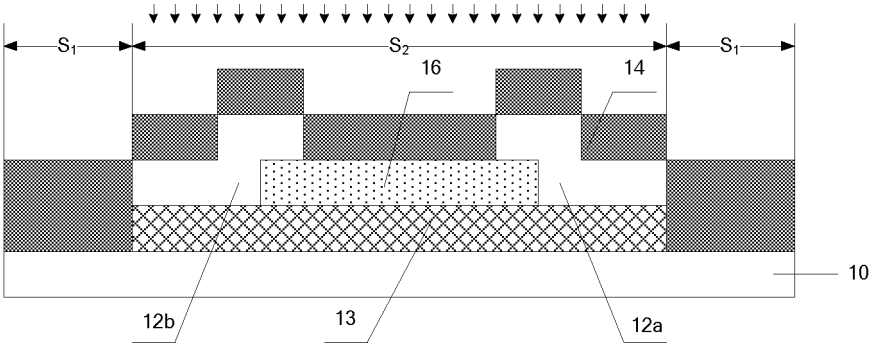

FIG. 18(d)

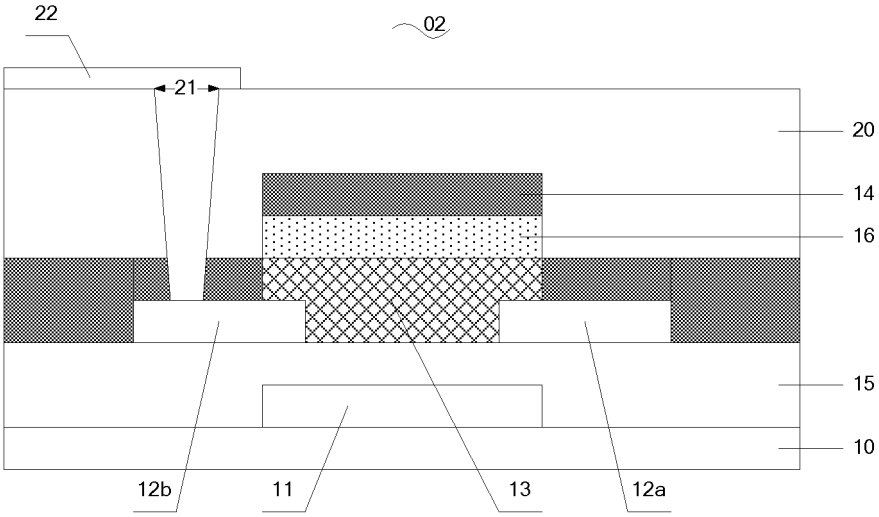

FIG. 19(a)

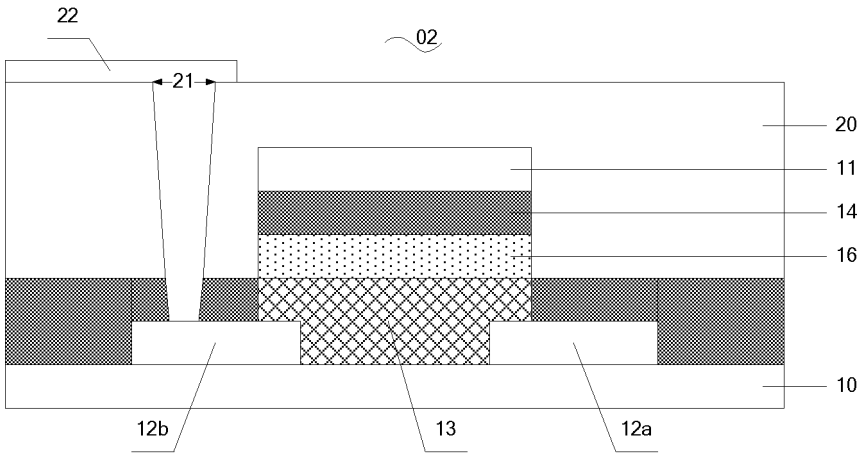

FIG. 19(b)

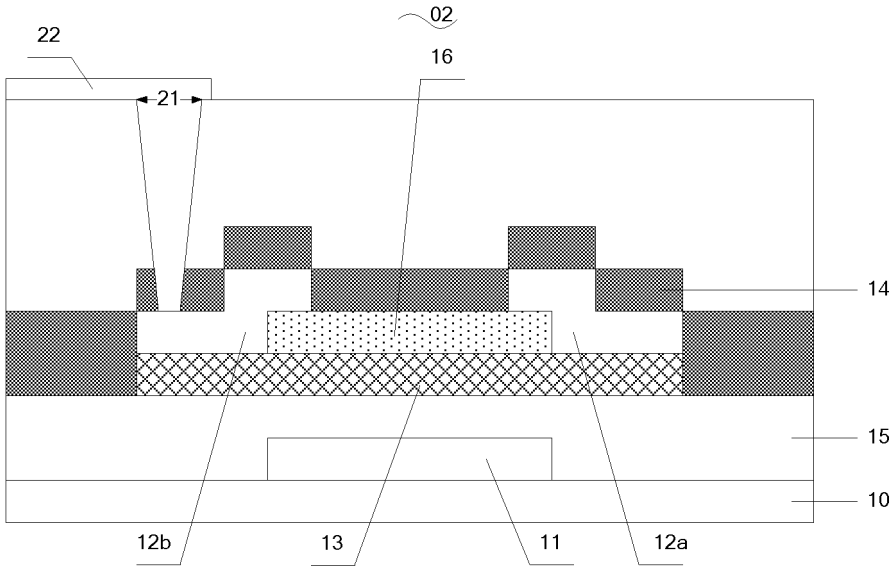

FIG. 19(c)

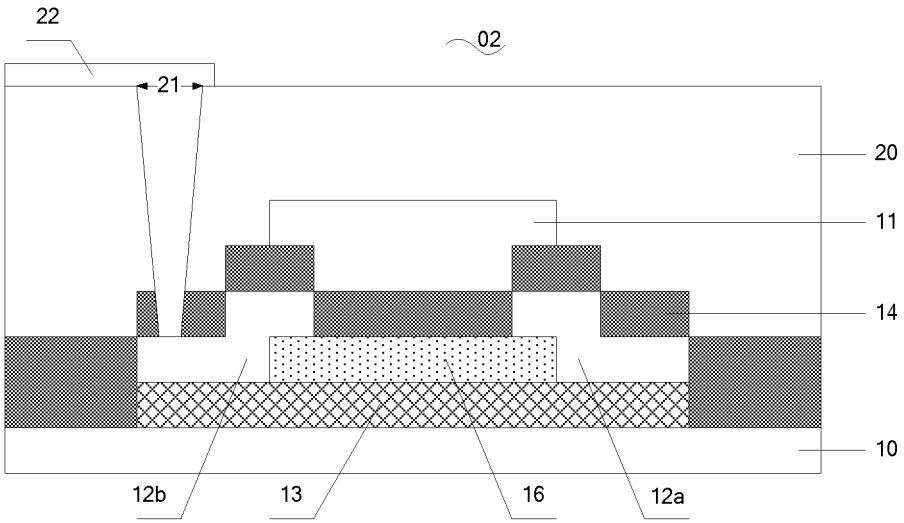

FIG. 19(d)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2014/093052

A. CLASSIFICATION OF SUBJECT MATTER

H01L 51/05 (2006.01) i; H01L 51/40 (2006.01) i; H01L 51/10 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 51/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USTXT; CNTXT; CNABS; DWPI; VEN: OTFT, organic, insulation layer, insulation film, dielectric film, dielectric layer, protective layer, protective film, passivation layer, passivation film, interlayer insulation film, thinning, uniform, curing, organic thin film transistor, organic TFT, etch, etching, insulation, dielectric, film, layer, protective, passivation, thin, thickness

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104091886 A (BOE TECHNOLOGY GROUP CO., LTD.), 08 October 2014 (08.10.2014), the whole document	1-20
A	CN 101971348 A (SONY CORPORATION), 09 February 2011 (09.02.2011), description, paragraphs 0030-0035 and 0108, and figure 10	1-20
A	CN 101059631 A (LG. PHILIPS LCD CO., LTD.), 24 October 2007 (24.10.2007), description, page 7, line 6 to page 8, line 15, and figure 6	1-20
A	CN 103210698 A (PANASONIC CORPORATION), 17 July 2013 (17.07.2013), description, paragraphs 0049-0065, and figure 7	1-20
A	US 2007252142 A1 (YOON), 01 November 2007 (01.11.2007), the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 March 2015 (25.03.2015)	**03 April 2015 (03.04.2015)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **XU, Xiaoling** Telephone No.: (86-10) **62089121**

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2014/093052

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		KR 1261608 B1	06 May 2013

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 201410319179 **[0098]**