(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 3 178 083 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
07.10.2026 Bulletin 2026/41

(21) Application number: **15828956.1**

(22) Date of filing: **15.07.2015**

(51) International Patent Classification (IPC):
G09G 3/20 *(2006.01)* ***G09G 3/36*** *(2006.01)*

(52) Cooperative Patent Classification (CPC):
G09G 3/3611; G09G 3/32; G09G 2310/04; G09G 2320/0247; G09G 2320/103; G09G 2340/0435

(86) International application number:
PCT/US2015/040632

(87) International publication number:
WO 2016/022265 (11.02.2016 Gazette 2016/06)

(54) CONCURRENTLY REFRESHING MULTIPLE AREAS OF A DISPLAY DEVICE USING MULTIPLE DIFFERENT REFRESH RATES

GLEICHZEITIGE AKTUALISIERUNG MEHRERER BEREICHE EINER ANZEIGEVORRICHTUNG MIT MEHREREN VERSCHIEDENEN AKTUALISIERUNGSRATEN

RAFRAÎCHISSEMENT SIMULTANÉ DE ZONES MULTIPLES D'UN DISPOSITIF D'AFFICHAGE EN UTILISANT DES FRÉQUENCES DE RAFRAÎCHISSEMENT MULTIPLES DIFFÉRENTES

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **05.08.2014 US 201462033586 P**
28.08.2014 US 201414472272
02.12.2014 US 201414558663

(43) Date of publication of application:
14.06.2017 Bulletin 2017/24

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(56) References cited:
EP-A1- 2 924 682
WO-A1-2014/080731
KR-A- 20060 066 424
KR-A- 20130 079 623
US-A1- 2008 001 863
US-A1- 2009 251 445
US-A1- 2011 032 231
US-A1- 2013 208 189
US-A1- 2013 265 294
US-A1- 2014 002 465
US-A1- 2014 085 276

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Description

FIELD

[0001] The described embodiments relate generally to modifying refresh rates of a display device. More particularly, the present embodiments relate to methods and apparatus for concurrently refreshing multiple areas of a display device at different rates.

BACKGROUND

[0002] Recent advances in computing devices have allowed for visually stunning graphics on many light, and often portable, computing devices. The graphics can be provided through a variety of systems that incorporate a graphics processor and a display monitor. Many graphics processors can interact with a display monitor to provide images and video that can update or refresh without any interruption being perceived by the user of the display monitor. However, both the transmission of data and the emissions of light from the display monitor for prolonged periods necessitate quantities of energy typically not available when implemented in portable computing devices. Often times this energy is devoted to transitions between colors and brightness levels of the display, and therefore designing a display that does not provide as optimal of transitions can degrade the user experience with the computing device. As a result, manufacturers must often make a choice between providing a more impressive visual display or conserving energy in order to provide a longer battery life for the computing device.

[0003] Many computing devices are primarily used for internet browsing, which can often require a variety of graphics to be displayed. For instance, some web pages are devoted to streaming videos and therefore can demand a lot of effort from the graphics processor of a computing device. In order to provide smooth streams of videos, the display monitor should be refreshed at a rate that allows for the video to be smoothly presented on the display monitor. However, maintaining a high refresh rate can be inefficient with respect to energy consumption because often times the entire area of the display monitor is refreshed without regards to the size of the video being displayed. Therefore, even if the user of the computing device is streaming a small video on a large display monitor, the refresh rate will be dynamic with respect to the dimensions of the video. Because the hardware of many computing devices is not designed to adjust refresh rates according to the application being executed, the user is often left with a device that cannot maintain charge during periods of frequent media playback. The user is therefore often discouraged from displaying media streams until the user can plug their computing device into a charging port, or until the user knows that they will not need the battery life for other applications at certain points in the day. Additionally, idle screens displaying animations for various applications can also consume energy in a wasteful manner despite many processes of the application occurring on a cloud server rather than the computing device. In this way, an application can in some cases consume more energy merely for aesthetics rather than the primary purpose of the application.

[0004] Document US2014/0085276 discloses a method for driving a display device that involves driving motion picture and still image display pixel rows with motion picture frequency and with still image display frequency, respectively, such that different parts of the display are concurrently refreshed at different refresh rates.

[0005] Document US 2013/0 208 189 A1 discloses a method of displaying a video of a scene on a display with reduced motion blur that includes: providing the video of a scene having first subframes that have a first input rate and second subframes that have a second input rate, wherein the first subframes correspond to a first region of the display and the second subframes correspond to a second region of the display; and selectively providing the first and second subframes to corresponding regions in the display, and providing the first region of the display with a first update rate and the second region of the display with a second update rate, wherein the first update rate is greater than the second update rate, so that the displayed image has reduced motion blur.

SUMMARY

[0006] The invention provides methods and display devices according to the independent claims. Further embodiments are provided in the dependent claims. This paper describes various embodiments that relate to methods and apparatus for controlling the refresh rate of display devices.

[0007] Other aspects and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings which illustrate, by way of example, the principles of the described embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements.

FIG. 1 illustrates a computing device having a display with multiple areas where the displayed graphics are either static or dynamic.

FIG. 2 illustrates a system diagram for controlling a display device according to some embodiments discussed herein.

FIG. 3 illustrates a diagram of the display device having a light emitting diode (LED) array connected to a gate driver and data driver.

FIGS. 4A-4B illustrate a gate driver circuit having a unit circuit and an output selector circuit.

FIG. 5 illustrates a diagram setting forth how multiple rows and areas of an LED array can be refreshed at different rates based on the operation of the gate driver circuit.

FIGS. 6A-6B illustrate issues and solutions associated with providing multiple refresh rates to the LED array.

FIG. 7 illustrates a diagram for performing multiple bank and multiple parameter gamma distribution in order to mitigate flickering and ripple issues at the refresh boundary.

FIG. 8 illustrates a method for modifying a refresh rate of a row or group of rows based on differences between frames provided to the LED array.

FIG. 9 illustrates a method for adjusting a refresh rate of one or more rows of and LED array based on flicker content of one or more frames, or images to be displayed by the LED array.

FIG. 10 illustrates a method for refreshing one or more rows of the LED array according to the amount of time one or more rows has remained static or unchanged.

FIG. 11 is a block diagram of a computing device that can represent the components of the various embodiments discussed herein.

DETAILED DESCRIPTION

[0009] Representative applications of methods and apparatus according to the present application are described in this section. These examples are being provided solely to add context and aid in the understanding of the described embodiments. It will thus be apparent to one skilled in the art that the described embodiments may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order to avoid unnecessarily obscuring the described embodiments. Other applications are possible, such that the following examples should not be taken as limiting.

[0010] In the following detailed description, references are made to the accompanying drawings, which form a part of the description and in which are shown, by way of illustration, specific embodiments in accordance with the described embodiments.

[0011] The embodiments discussed herein relate to display devices configured to refresh at different rates based on the content to be displayed by the display devices. Many computing devices have displays that often display static and dynamic images over various periods of usage. The static and dynamic images can often be displayed concurrently over the display of the computing device. According to the embodiments discussed here, a lower refresh rate can be assigned to portions of the display that are displaying a static image, while a normal refresh rate can be assigned to portions of the display that are displaying a dynamic image. These differences in refresh rates can be accomplished in part by an output selector circuit that can prevent the updating of one or more rows of the display. Specifically, the display can include an LED array having multiple rows, and each row can be connected to a gate driver that can be prevented from allowing a refresh of a respective row based on actions of the output selector circuit. In some instances, a data driver provides updated frame data to the LED array, and if the updated frame data is the same for two or more refreshes the gate driver can prevent the refresh of one or more rows of the LED array. For example, when the LED array is outputting a static image at a portion of the LED array, a control signal can be provided to the output selector that prevents that portion of the LED array from being refreshed at a rate equal to other portions of the LED array. Single rows or groups of rows can be refreshed differently than other portions of the LED array such that at least two refresh rates are being used to provide output from the LED array. In some embodiments, the refresh rate assigned to a portion of the LED array can be based on the flicker content of the image or images to be output by the LED array. For example, when the images contain high flicker content, the corresponding portion of the LED array can be assigned a low refresh rate. Moreover, when the images contain low flicker content, the corresponding portion of the LED array can be assigned an extremely low refresh rate. Additionally, during each refresh a polarity alteration can be performed in order to mitigate wear of the LED's of the LED array.

[0012] When multiple refresh rates are concurrently used on a display device, a ripple may be visible by a user of the computing device on which the display device is attached. The ripple can be caused by a boundary between two adjacent portions of the display that are operating at different refresh rates. In order to mitigate and prevent the occurrences of ripples, methods of compensation are discussed herein. In one embodiment, a digital compensation method is used. The digital compensation method allows for at least a 2-bit spatial dithering to be performed on the data presented at the display boundary at issue. In another example, an interpolation process is used, which interpolates at least two gamma curves based on the refresh rate of one or more rows at issue. The result of the interpolation is output to the one or more rows at issue in order to adjust the gamma of the images to be displayed at the one or more rows, for rendering any ripple effect imperceptible.

[0013] These and other embodiments are discussed below with reference to FIGS. 1 - 11; however, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes only and should not be construed as limiting.

[0014] FIG. 1 illustrates a computing device 100 having a display 102 with multiple areas where the displayed graphics are either static or dynamic. Specifically, the display 102 of the computing device 100 includes a header row 104 and a dynamic icon row 106 that con-

stantly update according to a cycle or period programmed within the computing device 100. The display 102 also includes static area 108, which do not constantly update but rather remain static until input is received from the user, a network connection, or other suitable source of input for the computing device 100. The header row 104 can include an indicator for wireless signal strength, clock time, and battery life, which typically can change at any given moment in time. For this reason, the header row 104 must display different values and adjust according to the dynamic changes occurring. The dynamic icon row 106 can also be modified according to updates occurring at the dynamic icons 110. The dynamic icons 110 can display the current date and clock time, which changes and updates constantly. In this way, the dynamic icons 110 should be refreshed more frequently than the static areas 108 in order to reduce energy consumption, as further discussed herein. For example, during the operation of an application on the computing device 100, a display manager stored in the computing device 100 can determine whether one or more rows currently presented on the display 102 include dynamic data. Thereafter, and as further discussed herein, the rows that include dynamic data can be assigned, by the display manager, a refresh rate that is higher than the rows that do not include dynamic data.

[0015] FIG. 2 illustrates a system diagram 200 for controlling a display device 210 according to some embodiments discussed herein. Specifically, FIG. 2 illustrates how the computing device 202 disclosed herein interacts with the display device 210 in order to simultaneously assign different refresh rates to various areas of the display device 210 in order to save battery life of the computing device 202. The computing device 202 can include a memory 204 storing a display manager 206 for transmitting display data between the processor 208 and display device 210. The display device 210 can include a data driver 216 for providing the display data to a light emitting diode (LED) array 214. The LED array 214 can include any suitable type of LED for displaying at a display device 210. For example, the LED array 214 can be an array of organic light emitting diodes. A gate driver 212 can be responsible for providing power to the individual LED's of the display device 210 and scanning rows and/or columns of the LED array 214 according to a refresh rate provided from the display manager 206. The display device can include multiple gate drivers 212, multiple data drivers 216, and multiple LED arrays 214, arranged in any suitable manner for operating a display device 210. The data drivers 216 and the gate drivers 212 can be configured to control the luminance of each LED pixel on the display device 210. Additionally, the display device 210 can be any suitable display monitor for use by a computing device such as a desktop computer, mobile device, media player, or any other computer-related device. In some embodiments, the display device 210 is a liquid crystal display (LCD) with an LED backlight. The LED backlight can be decoupled from the gate drivers 212 and data drivers 216, and the gate drivers 212 and data drivers 216 can be used to control the transmittance of the liquid crystals for passing through LED light from the LED backlight. In this way, the liquid crystals, or the LED's of the LED array discussed herein, can act as a pixel array to provide a channel or source for light to be projected from the display device 210.

[0016] FIG. 3 illustrates a diagram 300 of the display device 210 having an LED array 214 connected to a gate driver 212 and data driver 216. As further discussed herein, the gate driver 212 can include multiple gate output controllers that provide power to each row and/or column of the LED array and scan for data outputs. Each gate output 302 can be limited by a refresh rate for each individual row or group of rows, according to embodiments discussed herein. In this way, one or more gate outputs 302 can refresh at a different rate than one or more other gate outputs 302. Additionally, the data driver 216 can include multiple data outputs 304 for updating and transmitting signals to the LED array 214. In some embodiments, the one or more data outputs 304 can be stopped or transitioned into a low output state in order to reduce power consumption when the LED array 214 is displaying static images on the screen. Additionally, when the data outputs 304 are stopped or in a low state, the refresh rate corresponding to the gate outputs 302 can be reduced in areas affecting the portions of the LED array 214 displaying a static image.

[0017] FIGS. 4A-4B illustrate a gate driver circuit 400 having a unit circuit 410 and an output selector 412. The gate driver circuit 400 includes a control circuit 408 connected to multiple transistors and inputs for allowing the control circuit 408 to scan for updates from the data driver 216. One or more of the multiple transistors can be oxide transistors (e.g., oxide thin-film transistors), which provide for extremely low off-state currents, thereby allowing for less power consumption when a low refresh rate is applied to the LED array 214, as further discussed herein. Additionally, by using oxide transistors in combination with an LED array 214 of organic LED's, a significant reduction in power consumption can be achieved as compared to displays using low temperature polysilicon. Therefore, the apparatus and methods discussed herein can be implemented using a gate driver circuit 400 having one or more oxide thin-film transistors connected to an LED array 214 of organic LED's. Furthermore, in some embodiments, the gate drive circuit 400 can be incorporated into each gate output 302 in order to scan one or more rows concurrently based on one or more clock signals provided to the gate driver circuit 400. The output selector 412 is incorporated into the gate driver circuit 400 in order to prevent scanning based on the control input 402. For example, as shown in FIG. 4A, a scan signal 414 can be provided to the output selector 412 and prevented from being output from the selector output 404 by the absence of a control input 402. When a control input 402 is not provided to the output selector 412, either

no signal or a low voltage signal can be output from the selector output 404. FIG. 4B illustrates an example of when a control signal 416 is received at the control input 402 of the output selector 412. As a result of the control signal 416, a conductive pathway is formed at a transistor between the control input 402 and selector output 404, thereby allowing the scan signal 414 to be output from the selector output 404. The scan signal 414 can be a high voltage, in the context of a logical circuit to which the scan signal is provided, in order to indicate an "on" or "high" state of operation. Therefore, although the scan signal 414 can be constantly applied throughout the gate driver circuit 400, the scan signal 414 will not be output from the selector output 404 until the control signal 416 is received at the control input 402. In this way, because the gate driver circuit 400 can be incorporated at each gate output 302, one or more rows of gate outputs can be prevented from outputting a scan signal 414, or caused to output an "off" or "low" signal, simply by applying the control signal 416 to one or more gate driver circuits 400.

[0018] FIG. 5 illustrates a diagram 500 setting forth how multiple rows and areas of an LED array 214 can be refreshed at different rates based on the operation of the gate driver circuit 400. Specifically, FIG. 5 sets forth an example of when a first refresh rate is assigned to a first area 508 of the LED array 214 that is greater than a second refresh rate that is assigned to a second area 510 of the LED array 214. At the 1st frame, both the first area 508 and the second area 510 are refreshed based on a scan performed on all rows of the LED array 214 as a result of both the first refresh rate and the second refresh rate. For purposes of explanation, the first area 508 can be a streaming video and the second area 510 can be a static image bordering the streaming video. From the second frame to the "N+3" frame, the first refresh rate causes the rows corresponding to the first area 508 to be refreshed at each frame in order to allow the streaming video to be updated at each frame. However, the second refresh rate causes the rows corresponding to the second area 510 to not be refreshed and remain static as a result of the second refresh rate being lower than the first refresh rate. At the "N+4" frame, the first area 508 and second area 510 refresh concurrently again after the second area 510 has remained unrefreshed for multiple consecutive frames. In this way, energy is saved by refreshing portions of the LED array 214 at different refresh rates as opposed to refreshing the entire LED array 214 at the same rate. In some embodiments, any suitable number of refresh rates can be applied to the LED array 214. For example, at least three different refresh rates can be applied to the LED array 214. Additionally, a minimum refresh rate can be determined for one or more rows of the LED array 214. The minimum refresh rate can be the lowest refresh rate that prevents flickering of an image being displayed by the LED array 214. Moreover, polarity alteration can be performed during each refresh that is performed at a respective area or row of the LED array 214.

[0019] FIGS. 6A-6B illustrate issues and solutions associated with providing multiple refresh rates to the LED array 214. Specifically, FIG. 6A illustrates a representation of a refresh boundary 608 that can be visible to a user when the refresh rate of a first area 508 is greater than the refresh rate of a second area 510. A representation of the refresh boundary 608 can be seen in FIG. 6A where an average refresh line 606 is illustrated. The average refresh line 606 is an example of when a first refresh rate 602 is greater than a second refresh rate 604, and both refresh rates are concurrently exhibited adjacent to a refresh boundary 608. As a result of the average refresh line 606, a flicker or luminance ripple will be visible unless the refresh boundary 608 is compensated. In order to resolve the issues of flicker and ripple, solutions are set forth in FIG. 6B and 7. Specifically, FIG. 6B illustrates how compensation for the refresh boundary 608 can be performed in the digital domain using a set of pixels 610 that can be interchanged over the refresh boundary 608 based on the refresh rate. For example, for each set of at least 2-by-2 pixels traversing the refresh boundary 608, each block of pixels 612 illustrated in the set of pixels 610 can be sequenced and/or alternated. This technique, sometimes referred to as spatial dithering, can be performed in order to provide a visually smooth transition between two areas having different refresh rates.

[0020] FIG. 7 illustrates a system diagram 700 for performing multiple bank and multiple parameter gamma distribution in order to mitigate flickering and ripple issues at the refresh boundary 608. Specifically, FIG. 7 illustrates an analog solution for applying gamma switching to a row or block of rows in order to correct flickering and ripple. The system diagram 700 includes a first bank 702 that stores a first gamma curve and a second bank 704 that stores a second gamma curve. Each of the first gamma curve and second gamma curve are associated with one of the two refresh rates that can be applied to the LED array 214 respectively. During a compensation operation using gamma switching, the first gamma curve and second gamma curve are input into an interpolation module 708 along with a row block refresh rate 706. The first gamma curve and second gamma curve are thereafter interpolated. The method of interpolation can be any suitable form of interpolating image data. The result of an interpolation of the first gamma curve and second gamma curve can be scaled or otherwise modified according to the row block refresh rate 706 provided to the interpolation module 708. As a result, the row block gamma 710 is output as a curve from the interpolation module 708 in order to provide an analog solution that hides the refresh boundary 608. The row block gamma 710 can be applied to one or more rows of the LED array 214 concurrently depending on the severity of the flickering and rippling occurring at the refresh boundary 608.

[0021] FIG. 8 illustrates a method 800 for modifying a refresh rate of a row or group of rows based on differences between frames provided to the LED array 214.

Specifically, the method 800 includes a step 802 of generating, by a display manager 206, a first frame of data and a second frame of data. The first and second frames of data can be generated at the computing device 202 or the display device 210, by one or more software modules within either or both respective devices. At step 804, the display manager 206 compares each first frame row (i.e. a row of the first frame of data) and each second frame row (i.e. a row of the second frame of data). The comparison of step 804 can be done consecutively or one at a time for each row, or the comparison of all the rows can be performed concurrently. At step 806, the display manager 206 determines whether a first frame row is different than a second frame row. If the first frame row is different than the second frame row, the display manager 206, at step 808, causes an array row associated with the second frame row to refresh according to a normal refresh rate. If the first frame row is not different than the second frame row, the display manager 206, at step 810, causes an array row associated with the second frame row to refresh according to a low refresh rate. In this way, rows of a frame that remain static over multiple consecutive frames can be kept at a low refresh rate in order to save energy. For example, a normal refresh rate can be 30 Hertz or 60 Hertz, a low refresh rate can be 10 Hertz or 2 Hertz, and an extremely low refresh rate can be 1 Hz. The normal refresh rate, low refresh rate, and extremely low refresh rate can be any suitable value or values for a given display device. The normal refresh rate can be greater than the low refresh rate, and the low refresh rate can be greater than an extremely low refresh rate, as further discussed herein.

[0022] FIG. 9 illustrates a method 900 for adjusting a refresh rate of one or more rows of an LED array 214 based on flicker content of one or more frames, or images to be displayed by the LED array 214. Flicker content or flickering refers to the amount or severity of noticeable transitions from frame to frame a user can perceive when viewing a display of a computing device. The method 900 includes a step 902 where the display manager 206 generates a first frame of data and a second frame of data. Each of the first frame and second frame of data include one or more rows of data to be provided to the LED array 214. The display manager 206, at step 904, compares each first frame row of the first frame and each second frame row of the second frame. Thereafter, at step 906, the display manager 206 determines whether a first frame row is different than a second frame, for one or more of the first frame rows of the first frame and for one or more of the second frame rows of the second frame. If any of the first frame rows are different than a corresponding second frame row, the display manager 206, at step 908, can refresh the respective second frame row or rows according to a normal refresh rate. If any of the first frame rows are the same as a corresponding second frame row, the display manager 206 can proceed to step 910. At step 910, the display manager 206 can determine whether the any of the second frame rows include high flicker content. If any of the second frame rows include high flicker content (e.g., content that would cause a user to notice flickering from the LED array 214), the display manager 206, at step 912, can refresh the second frame row according to a low refresh rate. The refresh rates provided herein can be assigned to one or more transitions between frames such that the next transition can be delayed according to the respective refresh rate. If the any of the second frame rows do not contain high flicker content, the display manager 205, at step 914, can refresh the respective second frame rows according to an extremely low refresh rate. In this way, the row or rows assigned the extremely low refresh rate can remain static longer in order to conserve energy. Any of the methods discussed herein can iteratively analyze a single row at a time or multiple rows concurrently in order to efficiently determine a suitable refresh rate for one or more rows of the LED array 214.

[0023] FIG. 10 illustrates a method 1000 for refreshing one or more rows of the LED array 214 according to the amount of time one or more rows has remained static or unchanged. The method 1000 includes a step 1002 where the display manager 206 determines how long a row, or rows, of the LED array 214 has been static. At step 1004, the display manager 206 compares a static time, or the time the row or rows has remained static or unchanged, to a predetermined threshold time. The threshold time can be a value set by a user or manufacturer that remains constant throughout the life of the LED array 214 or changes based on hardware changes to the computing device associated with the LED array 214. At step 1006, the display manager 206 determines whether the static time is greater than the threshold time. If the static time is greater than the threshold time, the display manager 206, at step 1010, can prevent the row or rows from being refreshed. In this way, the refresh rate of one or more rows of the LED array 214 will be based on an amount of time the one or more rows has been static. If the static time is less than or equal to the threshold time, the display manager 206, at step 1008, can allow the row or rows to be refreshed. Following steps 1008 and 1010, the display manager 206, at step 1012, can analyze the next row or rows of a current frame or proceeding frame. For example, the method 1000 can be performed on each frame of data provided to the LED array 214, and for each row of each frame. When the all of the frames have been analyzed according to the method 1000, the display manager 206 can proceed to the next frame to be provided to the LED array 214. It should be noted that any method or embodiment discussed herein can be combined and performed in any order or arrangement suitable for mitigating energy consumption of a display device.

[0024] The FIG. 11 is a block diagram of a computing device 1100 that can represent the components of the computing device 100 and/or the computing device 202. It will be appreciated that the components, devices or elements illustrated in and described with respect to FIG. 11 may not be mandatory and thus some may be omitted

in certain embodiments. The computing device 1100 can include a processor 1102 that represents a microprocessor, a coprocessor, circuitry and/or a controller for controlling the overall operation of computing device 1100. Although illustrated as a single processor, it can be appreciated that the processor 1102 can include a plurality of processors. The plurality of processors can be in operative communication with each other and can be collectively configured to perform one or more functionalities of the computing device 1100 as described herein. In some embodiments, the processor 1102 can be configured to execute instructions that can be stored at the computing device 1100 and/or that can be otherwise accessible to the processor 1102. As such, whether configured by hardware or by a combination of hardware and software, the processor 1102 can be capable of performing operations and actions in accordance with embodiments described herein.

[0025] The computing device 1100 can also include user input device 1104 that allows a user of the computing device 1100 to interact with the computing device 1100. For example, user input device 1104 can take a variety of forms, such as a button, keypad, dial, touch screen, audio input interface, visual/image capture input interface, input in the form of sensor data, etc. Still further, the computing device 1100 can include a display 1108 (screen display) that can be controlled by processor 1102 to display information to a user. Controller 1110 can be used to interface with and control different equipment through equipment control bus 1112. The computing device 1100 can also include a network/bus interface 1114 that couples to data link 1116. Data link 1116 can allow the computing device 1100 to couple to a host computer or to accessory devices. The data link 1116 can be provided over a wired connection or a wireless connection. In the case of a wireless connection, network/bus interface 1114 can include a wireless transceiver.

[0026] The computing device 1100 can also include a storage device 1118, which can have a single disk or a plurality of disks (e.g., hard drives) and a storage management module that manages one or more partitions (also referred to herein as "logical volumes") within the storage device 1118. In some embodiments, the storage device 1120 can include flash memory, semiconductor (solid state) memory or the like. Still further, the computing device 1100 can include Read-Only Memory (ROM) 1122 and Random Access Memory (RAM) 1124 and. The ROM 1122 can store programs, code, instructions, utilities or processes to be executed in a non-volatile manner. The RAM 1124 can provide volatile data storage, and stores instructions related to components of the storage management module that are configured to carry out the various techniques described herein. The computing device can further include data bus 1126. Data bus 1126 can facilitate data and signal transfer between at least processor 1102, controller 1110, network interface 1114, storage device 1118, ROM 1122, and RAM 1124.

[0027] The various aspects, embodiments, implementations or features of the described embodiments can be used separately or in any combination. Various aspects of the described embodiments can be implemented by software, hardware or a combination of hardware and software. The described embodiments can also be embodied as computer readable code on a computer readable medium for controlling manufacturing operations or as computer readable code on a computer readable medium for controlling a manufacturing line. The computer readable storage medium is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable storage medium include read-only memory, random-access memory, CD-ROMs, HDDs, DVDs, magnetic tape, and optical data storage devices. The computer readable storage medium can also be distributed over network-coupled computer systems so that the computer readable code is stored and executed in a distributed fashion. In some embodiments, the computer readable storage medium can be non-transitory.

[0028] The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the described embodiments. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the described embodiments. Thus, the foregoing descriptions of specific embodiments are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the described embodiments to the precise forms disclosed. It will be apparent to one of ordinary skill in the art that many modifications and variations are possible in view of the above teachings.

Claims

1. A method (800) for refreshing multiple rows of a display device comprising a pixel array concurrently at different refresh rates, the method comprising:

generating (802) a first data frame and a second data frame corresponding to image data to be displayed on the display device;

comparing (804) each frame row of the first data frame to its corresponding frame row in the immediately subsequent second data frame;

determining (806) based on the comparing, whether each first frame row is different than its corresponding second frame row;

based on the determining that any first frame row is different than its corresponding second frame row, causing (808) an array row of the pixel array associated with this particular second frame row to be refreshed with the pixel data of the second frame row according to a normal refresh rate; or

based on the determining that any first frame

row is not different than its corresponding second frame row, causing (810) the array row of the pixel array associated with the second frame row to be refreshed with the pixel data of the second frame row according to a low refresh rate, wherein
the normal refresh rate is 30 Hertz or 60 Hertz, and the low refresh rate is 10 Hertz or 2 Hertz; and
characterised in that the method further comprises:
performing a spatial dithering process on data presented at a refresh boundary between the first frame row and the second frame row by interchanging a set of pixels (610) over the refresh boundary.

2. The method of claim 1, wherein the set of pixels (610) comprises a plurality of blocks of pixels (612), and wherein the interchanging comprises, for each of a plurality of sets of pixels that traverse the refresh boundary, sequencing and/or alternating each block of pixels (612) in the plurality of blocks of pixels.

3. A computing device (202) comprising:

a display manager (206); and
a display device (210) comprising:

a pixel array (214);
a plurality of gate drivers (400) each operatively coupled to a row of the pixel array; and
a data driver (216) operatively coupled to the pixel array to provide frame data to the pixel array;

wherein the display manager (206) is operatively coupled to each of the plurality of gate drivers, wherein the display manager is configured to implement the method according to claim 1.

4. The computing device of claim 3,
wherein the pixel array includes:

multiple liquid crystals configured to control a transmittance of light from a light emitting diode, LED, backlight, or
multiple organic LEDs.

5. The computing device of claim 4, wherein the set of pixels (610) comprises a plurality of blocks of pixels (612), and
wherein the interchanging comprises, for each of a plurality of sets of pixels that traverse the refresh boundary, sequencing and/or alternating each block of pixels (612) in the plurality of blocks of pixels.

Patentansprüche

1. Verfahren (800) zum gleichzeitigen Aktualisieren mehrerer Zeilen einer Anzeigevorrichtung, die eine Pixelanordnung aufweist, mit unterschiedlichen Aktualisierungsraten, wobei das Verfahren Folgendes aufweist:

Erzeugen (802) eines ersten Datenrahmens und eines zweiten Datenrahmens, die Bilddaten entsprechen, die auf der Anzeigevorrichtung angezeigt werden sollen;
Vergleichen (804) jeder Rahmenzeile des ersten Datenrahmens mit ihrer entsprechenden Rahmenzeile in dem unmittelbar nachfolgenden zweiten Datenrahmen;
Bestimmen (806), basierend auf dem Vergleichen, ob sich jede erste Rahmenzeile von ihrer entsprechenden zweiten Rahmenzeile unterscheidet;
basierend auf dem Bestimmen, dass sich jede erste Rahmenzeile von ihrer entsprechenden zweiten Rahmenzeile unterscheidet, Veranlassen (808), dass eine Anordnungszeile der Pixelanordnung, die dieser bestimmten zweiten Rahmenzeile zugeordnet ist, mit den Pixeldaten der zweiten Rahmenzeile gemäß einer normalen Aktualisierungsrate aktualisiert wird; oder
basierend auf dem Bestimmen, dass sich jede erste Rahmenzeile nicht von ihrer entsprechenden zweiten Rahmenzeile unterscheidet, Veranlassen (810), dass die Anordnungszeile der Pixelanordnung, die der zweiten Rahmenzeile zugeordnet ist, mit den Pixeldaten der zweiten Rahmenzeile gemäß einer niedrigen Aktualisierungsrate aktualisiert wird, wobei
die normale Aktualisierungsrate 30 Hertz oder 60 Hertz beträgt und die niedrige Aktualisierungsrate 10 Hertz oder 2 Hertz beträgt; und
dadurch gekennzeichnet, dass das Verfahren ferner Folgendes aufweist:
Durchführen eines räumlichen Dithering-Prozesses an Daten, die an einer Aktualisierungsgrenze zwischen der ersten Rahmenzeile und der zweiten Rahmenzeile dargestellt werden, durch Austauschen eines Satzes von Pixeln (610) über die Aktualisierungsgrenze.

2. Verfahren nach Anspruch 1, wobei der Satz von Pixeln (610) eine Vielzahl von Blöcken von Pixeln (612) aufweist, und
wobei das Austauschen für jeden einer Vielzahl von Sätzen von Pixeln, die die Aktualisierungsgrenze durchlaufen, ein Sequenzieren und/oder Abwechseln jedes Blocks von Pixeln (612) in der Vielzahl von Blöcken von Pixeln aufweist.

3. Rechenvorrichtung (202), die Folgendes aufweist:

einen Anzeigemanager (206); und
eine Anzeigevorrichtung (210), die Folgendes aufweist:

eine Pixelanordnung (214);
eine Vielzahl von Gate-Treibern (400), die jeweils operativ mit einer Zeile der Pixelanordnung gekoppelt sind; und
einen Datentreiber (216), der operativ mit der Pixelanordnung gekoppelt ist, um Rahmendaten für die Pixelanordnung bereitzustellen;

wobei der Anzeigemanager (206) operativ mit jedem der Vielzahl von Gate-Treibern gekoppelt ist, wobei der Anzeigemanager konfiguriert ist, um das Verfahren nach Anspruch 1 zu implementieren.

4. Rechenvorrichtung nach Anspruch 3,
wobei die Pixelanordnung Folgendes beinhaltet:

mehrere Flüssigkristalle, die konfiguriert sind, um eine Durchlässigkeit von Licht von einer Leuchtdioden-, LED-, Hintergrundbeleuchtung zu steuern, oder
mehrere organische LEDs.

5. Rechenvorrichtung nach Anspruch 4, wobei der Satz von Pixeln (610) eine Vielzahl von Blöcken von Pixeln (612) aufweist, und
wobei das Austauschen für jeden einer Vielzahl von Sätzen von Pixeln, die die Aktualisierungsgrenze durchlaufen, ein Sequenzieren und/oder Abwechseln jedes Blocks von Pixeln (612) in der Vielzahl von Blöcken von Pixeln aufweist.

Revendications

1. Un procédé (800) pour rafraîchir en même temps à des cadences de rafraîchissement différentes des rangées multiples d'un dispositif afficheur comprenant un réseau de pixels, le procédé comprenant :

la génération (802) d'une première trame de données et d'une seconde trame de données correspondant à des données d'image à afficher sur le dispositif afficheur ;
la comparaison (804) de chaque rangée de trame de la première trame de données à sa rangée de trame correspondante de la seconde trame de données qui la suit immédiatement ;
la détermination (806), sur la base de la comparaison, si chaque première rangée de trame est ou non différente de sa seconde rangée de trame ;
sur la base de la détermination qu'une quelconque première rangée de trame est différente de sa seconde rangée de trame correspondante, faire en sorte (808) qu'une rangée de réseau du réseau de pixels associée à cette seconde rangée de trame particulière soit rafraîchie avec les données de pixels de la seconde rangée de trame selon une cadence de rafraîchissement normale ; ou
sur la base de la détermination qu'aucune première rangée de trame n'est différente de sa seconde rangée de trame correspondante, faire en sorte (810) que la rangée de réseau de pixels associée à la seconde rangée de trame soit rafraîchie avec les données de pixels de la seconde rangée de trame selon une cadence de rafraîchissement réduite, dans lequel
la cadence de rafraîchissement normale est de 30 hertz ou 60 hertz, et la cadence de rafraîchissement réduite est de 10 hertz ou 2 hertz ; et
caractérisé en ce que le procédé comprend en outre :
l'exécution d'un processus de dithering spatial sur les données présentées à une frontière de rafraîchissement entre la première rangée de trame et la seconde rangée de trame, par interversion d'un ensemble de pixels (610) au-dessus de la frontière de rafraîchissement.

2. Le procédé de la revendication 1, dans lequel l'ensemble de pixels (610) comprend une pluralité de blocs de pixels (612), et
dans lequel l'interversion comprend, pour chacun d'une pluralité d'ensembles de pixels qui traversent la frontière de rafraîchissement, le séquencement et/ou l'alternance de chaque bloc de pixels (612) de la pluralité de blocs de pixels.

3. Un dispositif informatique (202) comprenant :

un gestionnaire d'afficheur (206) ; et
un dispositif afficheur (210) comprenant :

un réseau de pixels (214) ;

une pluralité de pilotes de grille (40) couplés chacun de manière opérante à une rangée du réseau de pixels ; et
un pilote de données (216) couplé de manière opérante au réseau de pixels pour délivrer des données de trame au réseau de pixels ;

dans lequel le gestionnaire d'afficheur (206) est couplé de manière opérante à chacun de la pluralité de pilotes de grille, le gestionnaire d'afficheur étant configuré pour implémenter le procédé selon la revendication 1.

4. Le dispositif informatique de la revendication 3, dans lequel le réseau de pixels comprend :

des cristaux liquides multiples configurés pour contrôler un facteur de transmission de la lumière provenant d'un rétroéclairage à diodes émettrices de lumière, LED, ou
des LED organiques multiples.

5. Le dispositif informatique de la revendication 4, dans lequel l'ensemble de pixels (610) comprend une pluralité de blocs de pixels (612), et
dans lequel l'interversion comprend, pour chacun d'une pluralité d'ensembles de pixels qui traversent la frontière de rafraîchissement, le séquencement et/ou l'alternance de chaque bloc de pixels (612) de la pluralité de blocs de pixels.

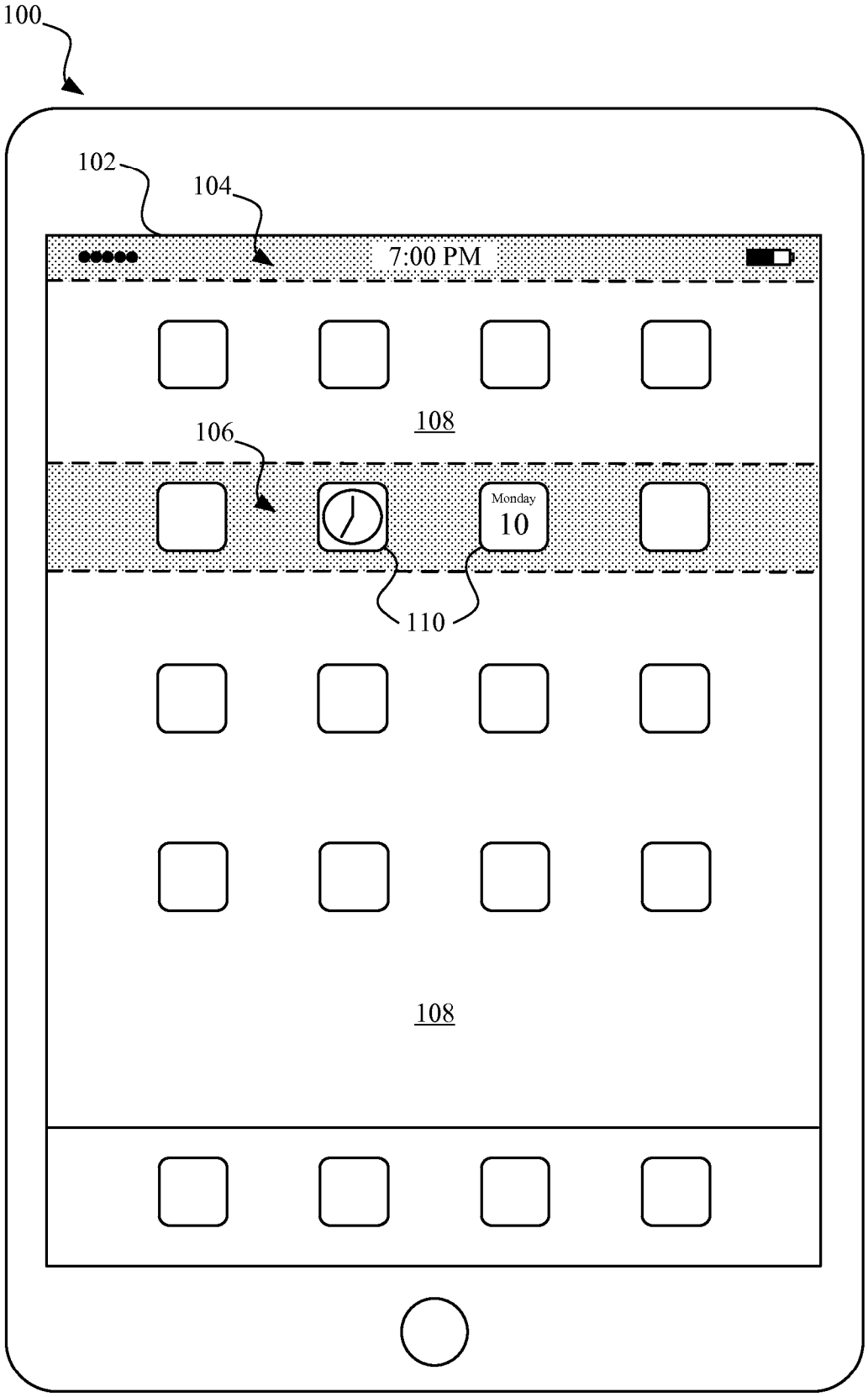


FIG. 1

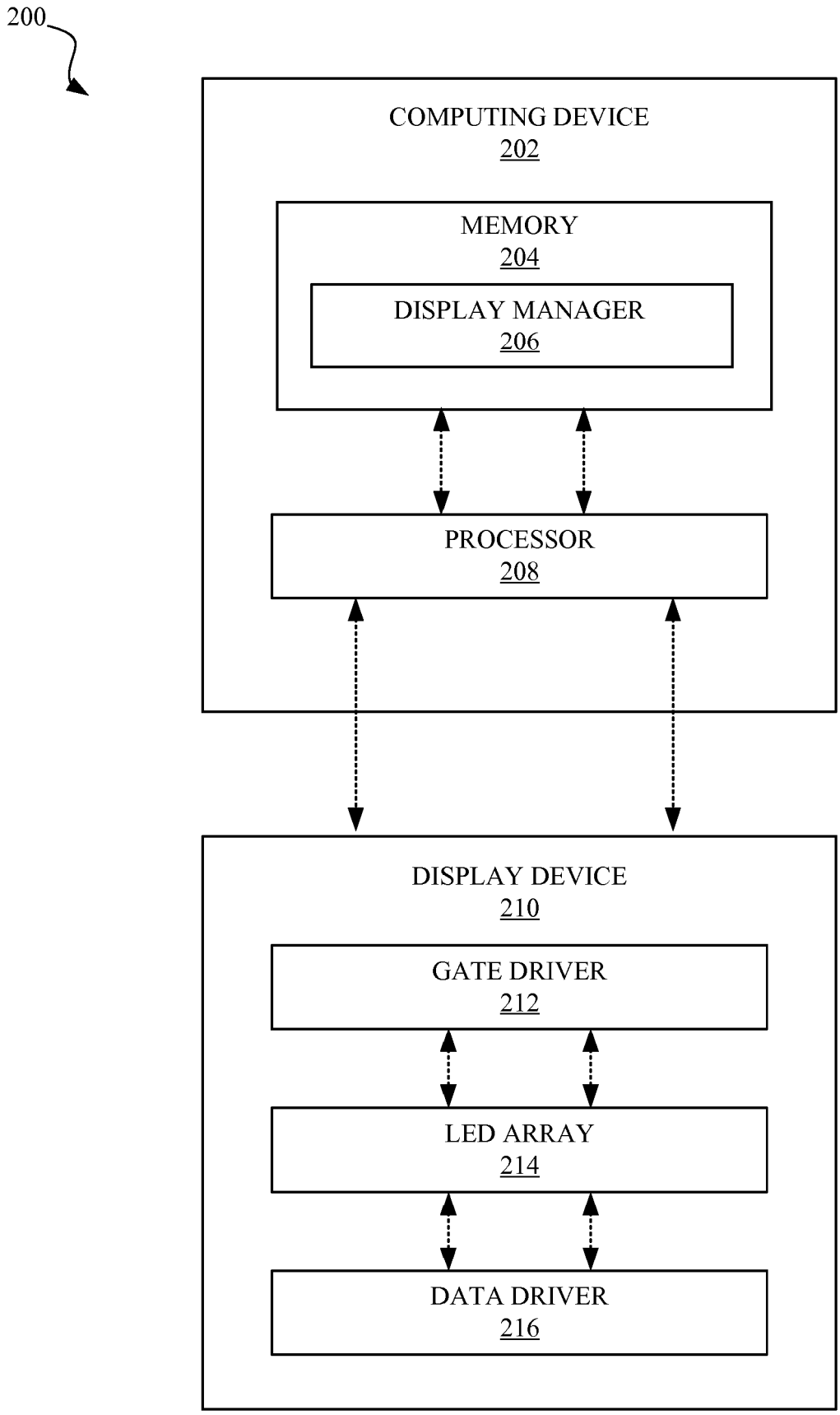

200
COMPUTING DEVICE
202
MEMORY
204
DISPLAY MANAGER
206
PROCESSOR
208
DISPLAY DEVICE
210
GATE DRIVER
212
LED ARRAY
214
DATA DRIVER
216

FIG. 2

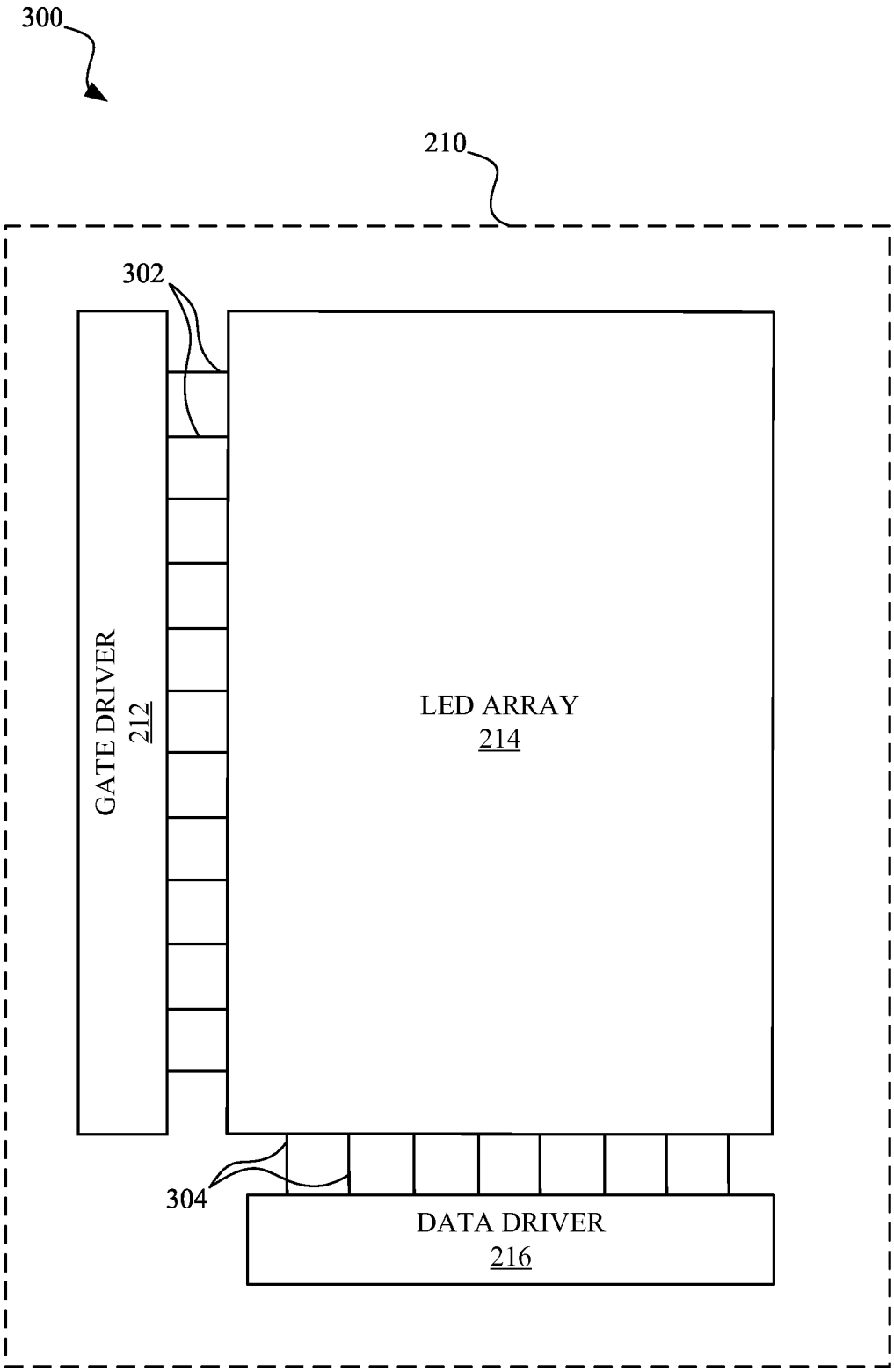


FIG. 3

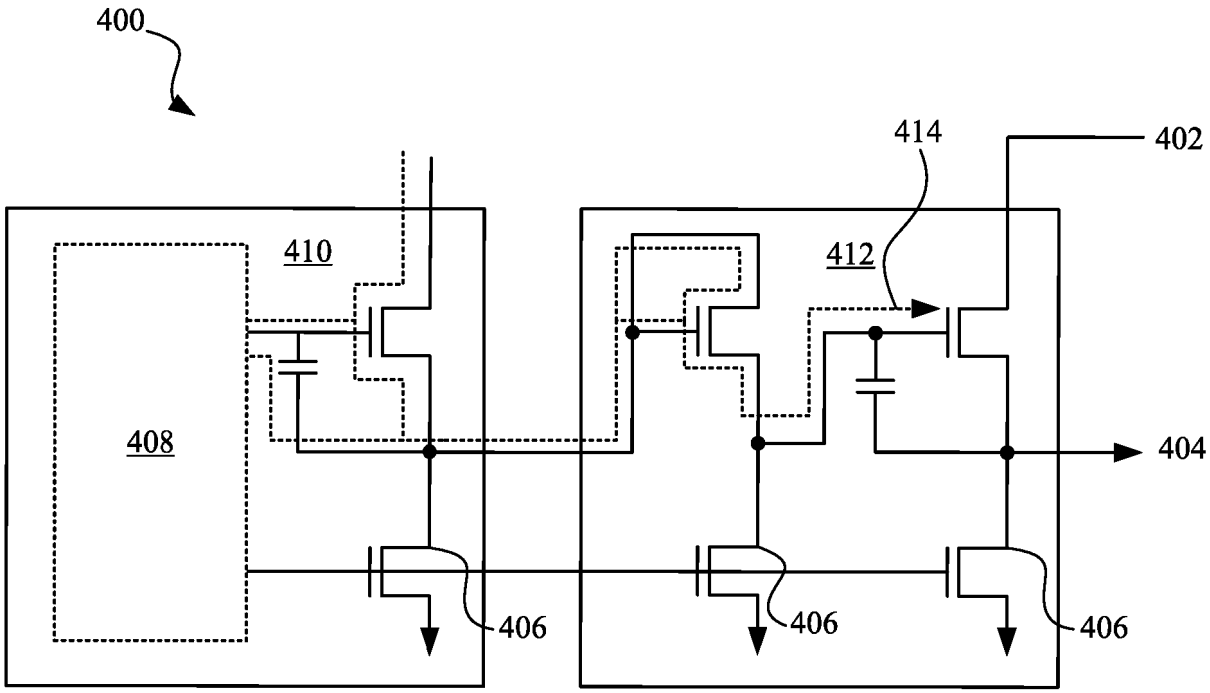

400
414
402
410
412
408
404
406
406
406

FIG. 4A

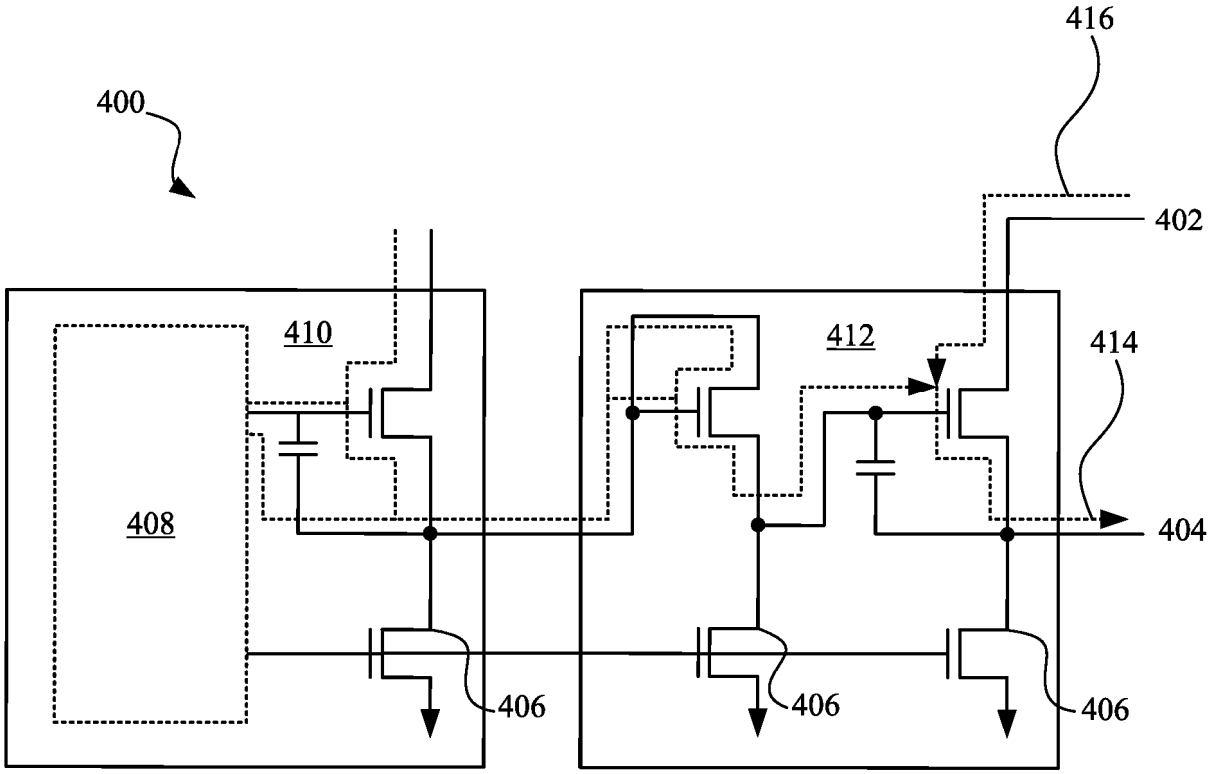

416
400
402
410
412
414
408
404
406
406
406

FIG. 4B

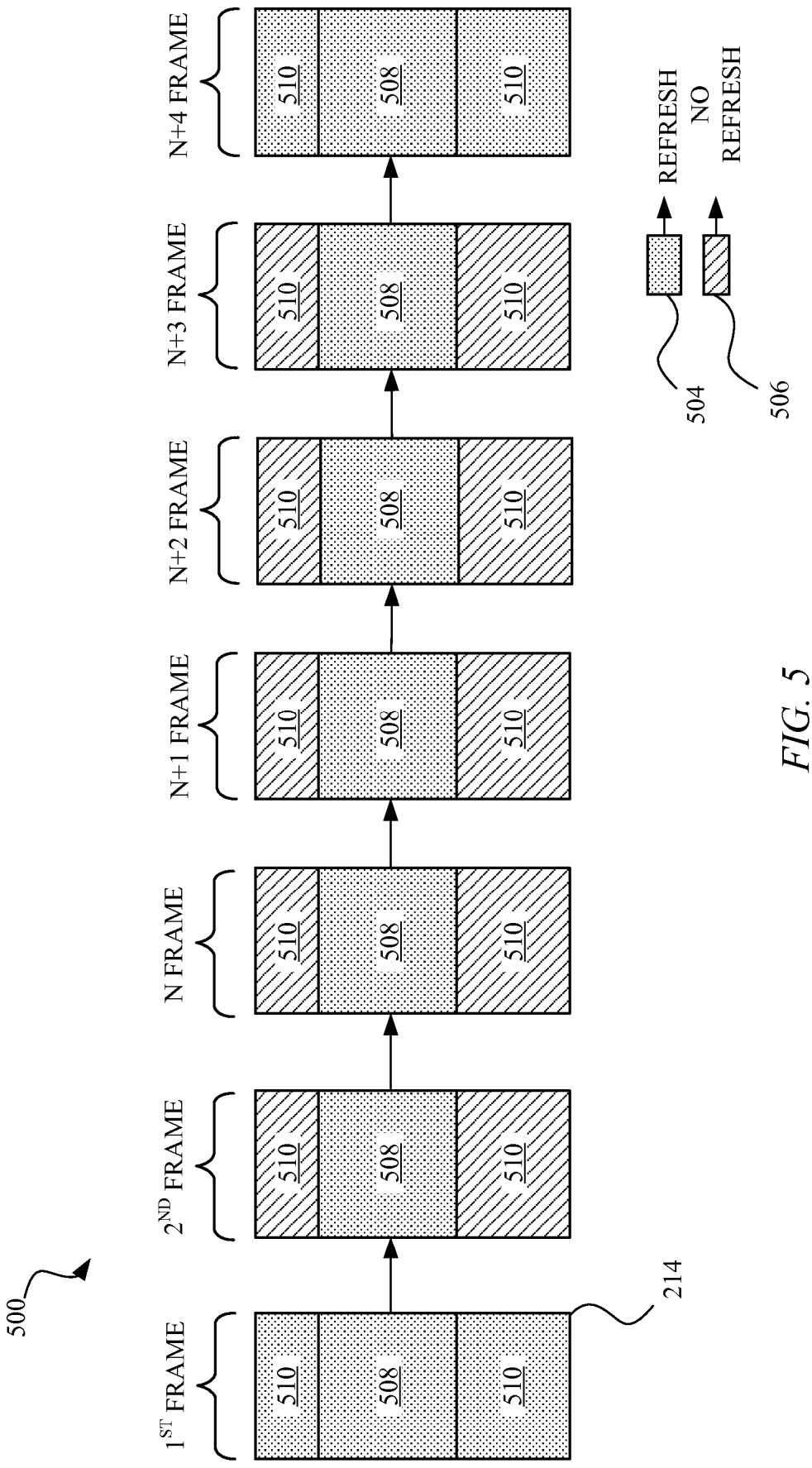

500
1ST FRAME
2ND FRAME
N FRAME
N+1 FRAME
N+2 FRAME
N+3 FRAME
N+4 FRAME
510
508
214
REFRESH
NO REFRESH
504
506

FIG. 5

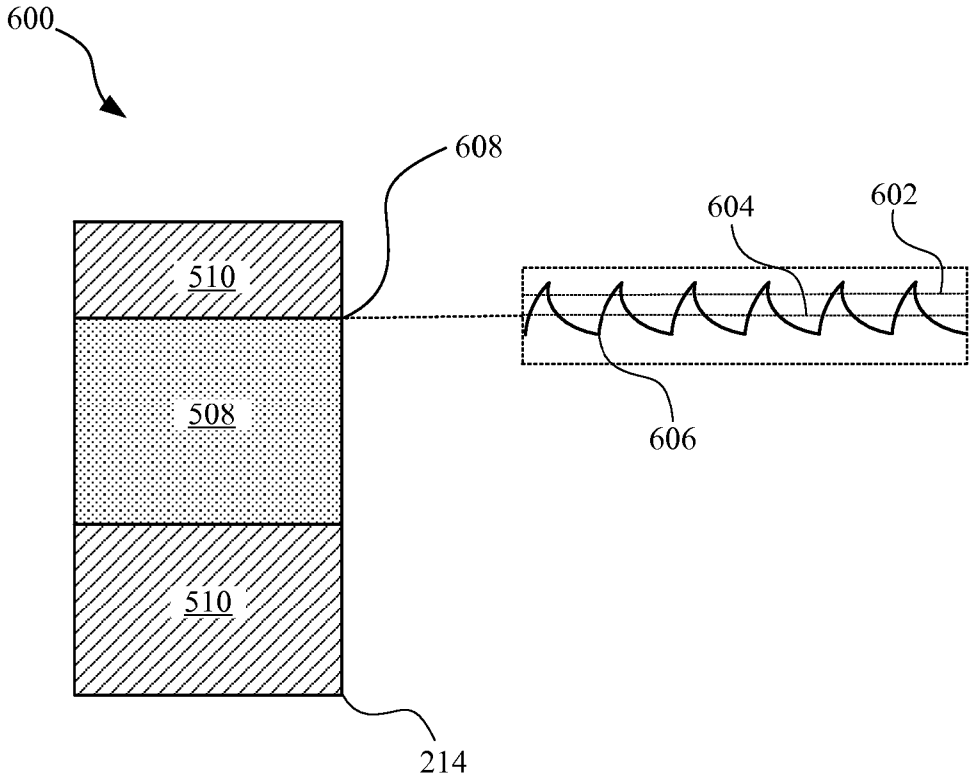


FIG. 6A

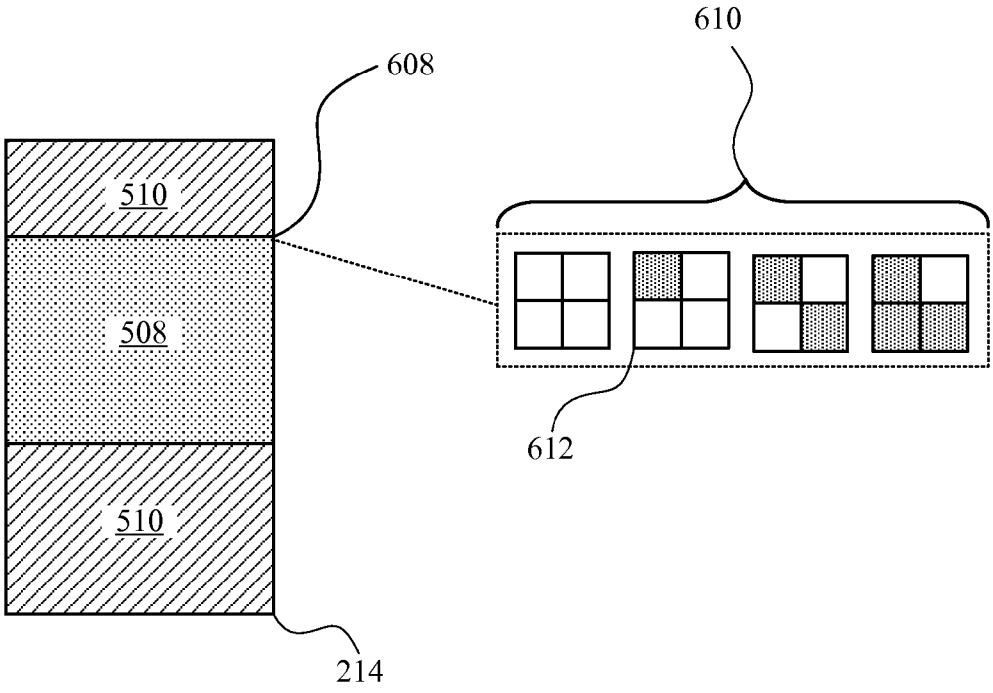


FIG. 6B

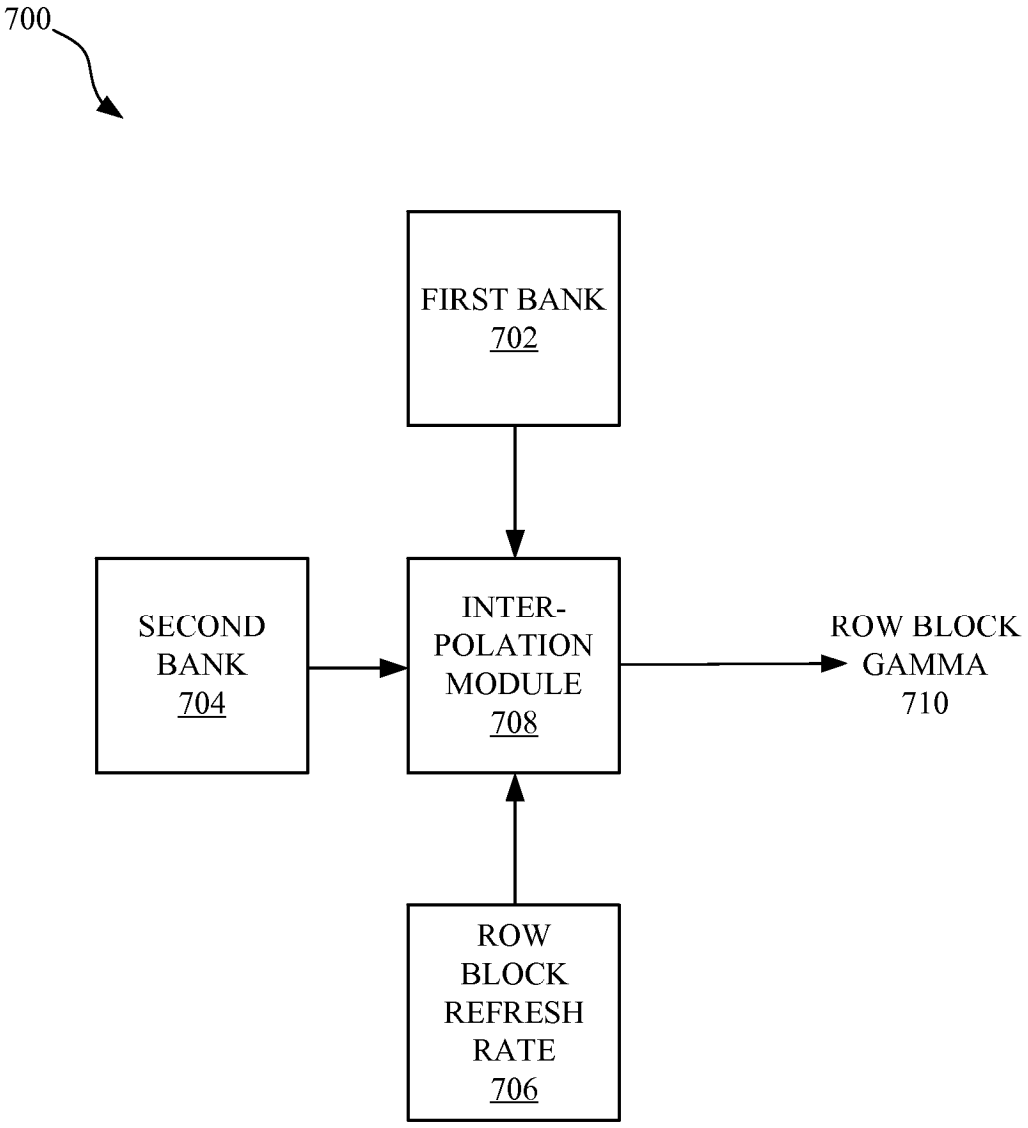

700
FIRST BANK
702
SECOND
BANK
704
INTER-
POLATION
MODULE
708
ROW BLOCK
GAMMA
710
ROW
BLOCK
REFRESH
RATE
706

FIG. 7

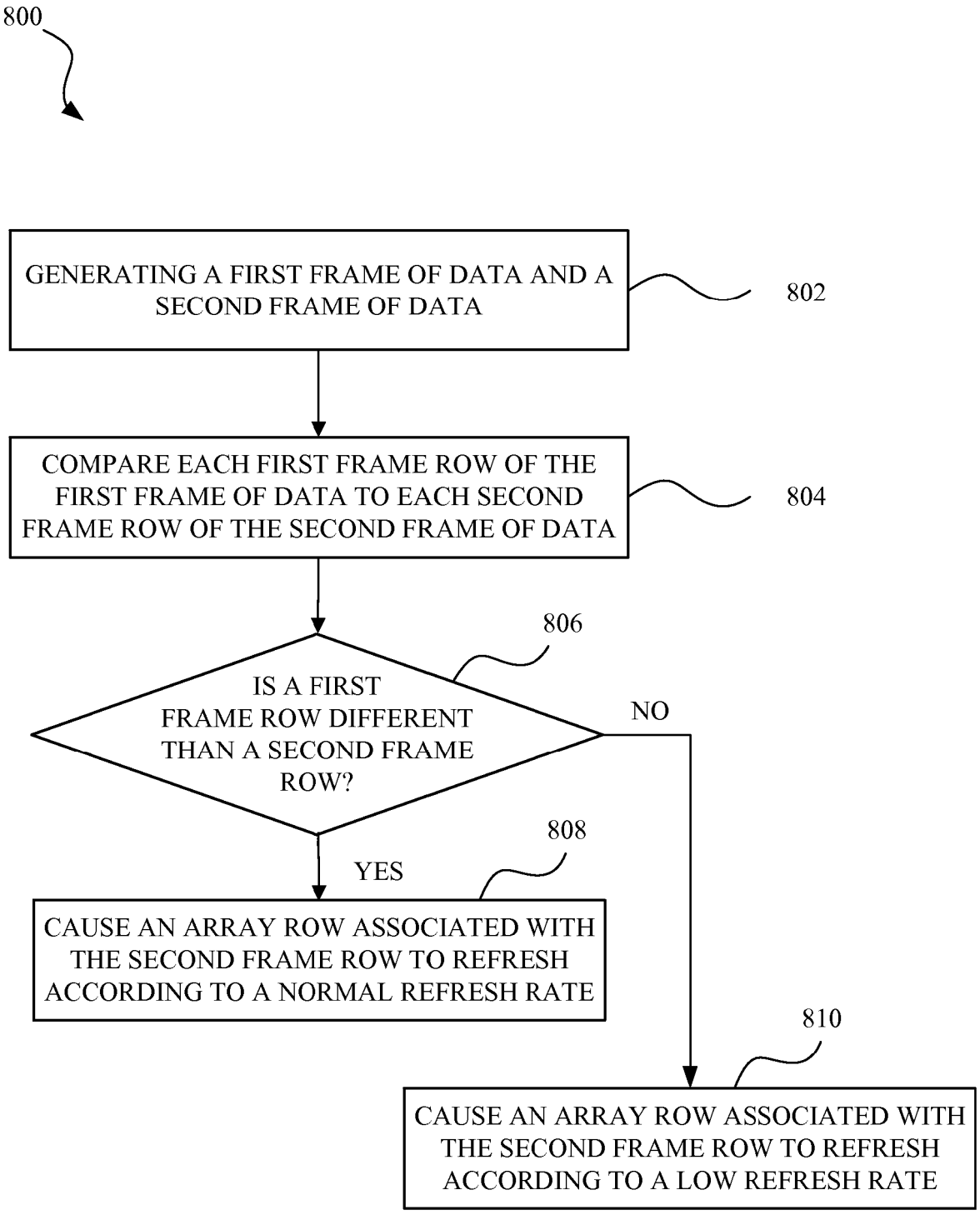

800
GENERATING A FIRST FRAME OF DATA AND A SECOND FRAME OF DATA
802
COMPARE EACH FIRST FRAME ROW OF THE FIRST FRAME OF DATA TO EACH SECOND FRAME ROW OF THE SECOND FRAME OF DATA
804
806
IS A FIRST FRAME ROW DIFFERENT THAN A SECOND FRAME ROW?
NO
YES
808
CAUSE AN ARRAY ROW ASSOCIATED WITH THE SECOND FRAME ROW TO REFRESH ACCORDING TO A NORMAL REFRESH RATE
810
CAUSE AN ARRAY ROW ASSOCIATED WITH THE SECOND FRAME ROW TO REFRESH ACCORDING TO A LOW REFRESH RATE

FIG. 8

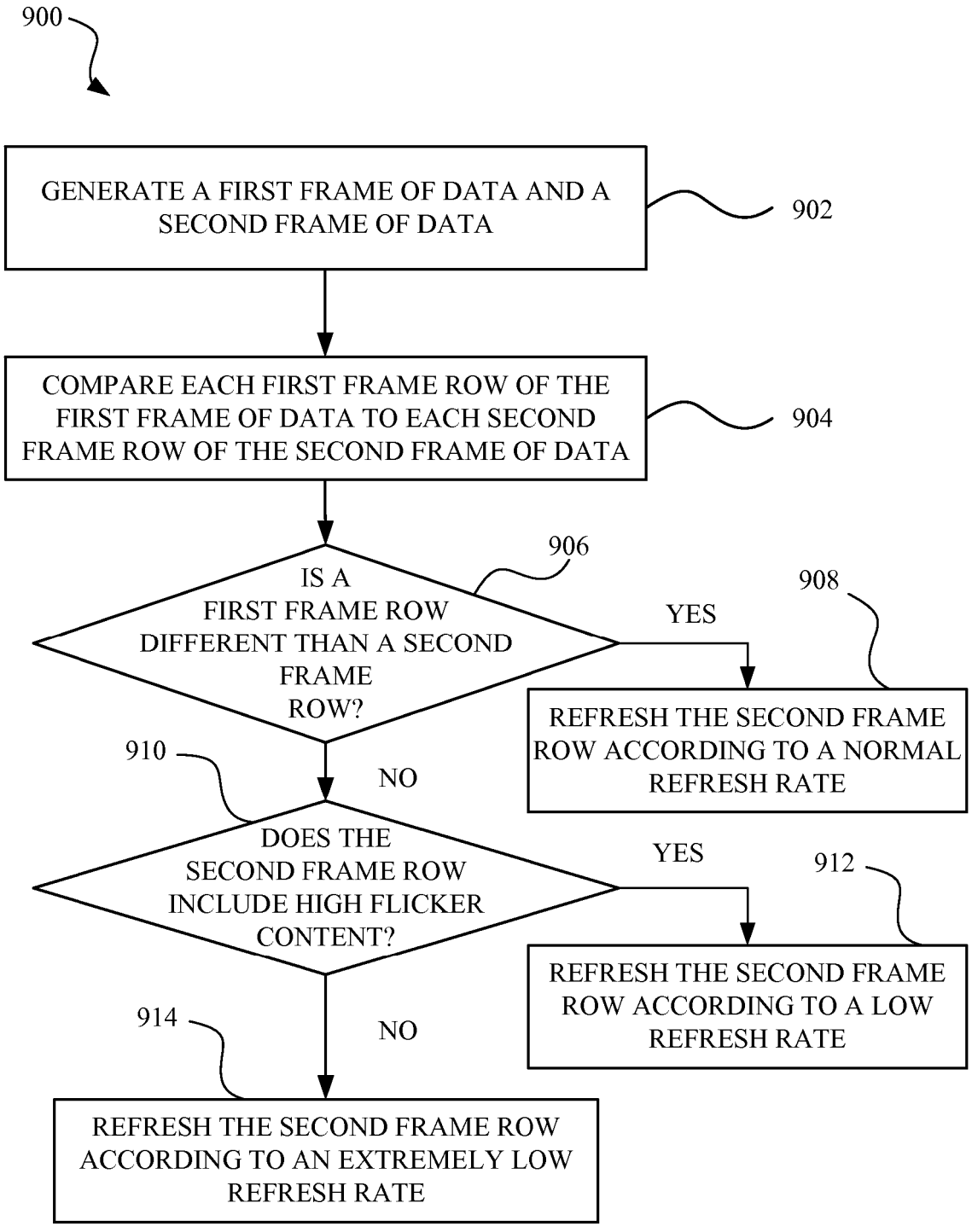

900
GENERATE A FIRST FRAME OF DATA AND A SECOND FRAME OF DATA
902
COMPARE EACH FIRST FRAME ROW OF THE FIRST FRAME OF DATA TO EACH SECOND FRAME ROW OF THE SECOND FRAME OF DATA
904
906
IS A FIRST FRAME ROW DIFFERENT THAN A SECOND FRAME ROW?
YES
908
REFRESH THE SECOND FRAME ROW ACCORDING TO A NORMAL REFRESH RATE
NO
910
DOES THE SECOND FRAME ROW INCLUDE HIGH FLICKER CONTENT?
YES
912
REFRESH THE SECOND FRAME ROW ACCORDING TO A LOW REFRESH RATE
NO
914
REFRESH THE SECOND FRAME ROW ACCORDING TO AN EXTREMELY LOW REFRESH RATE

FIG. 9

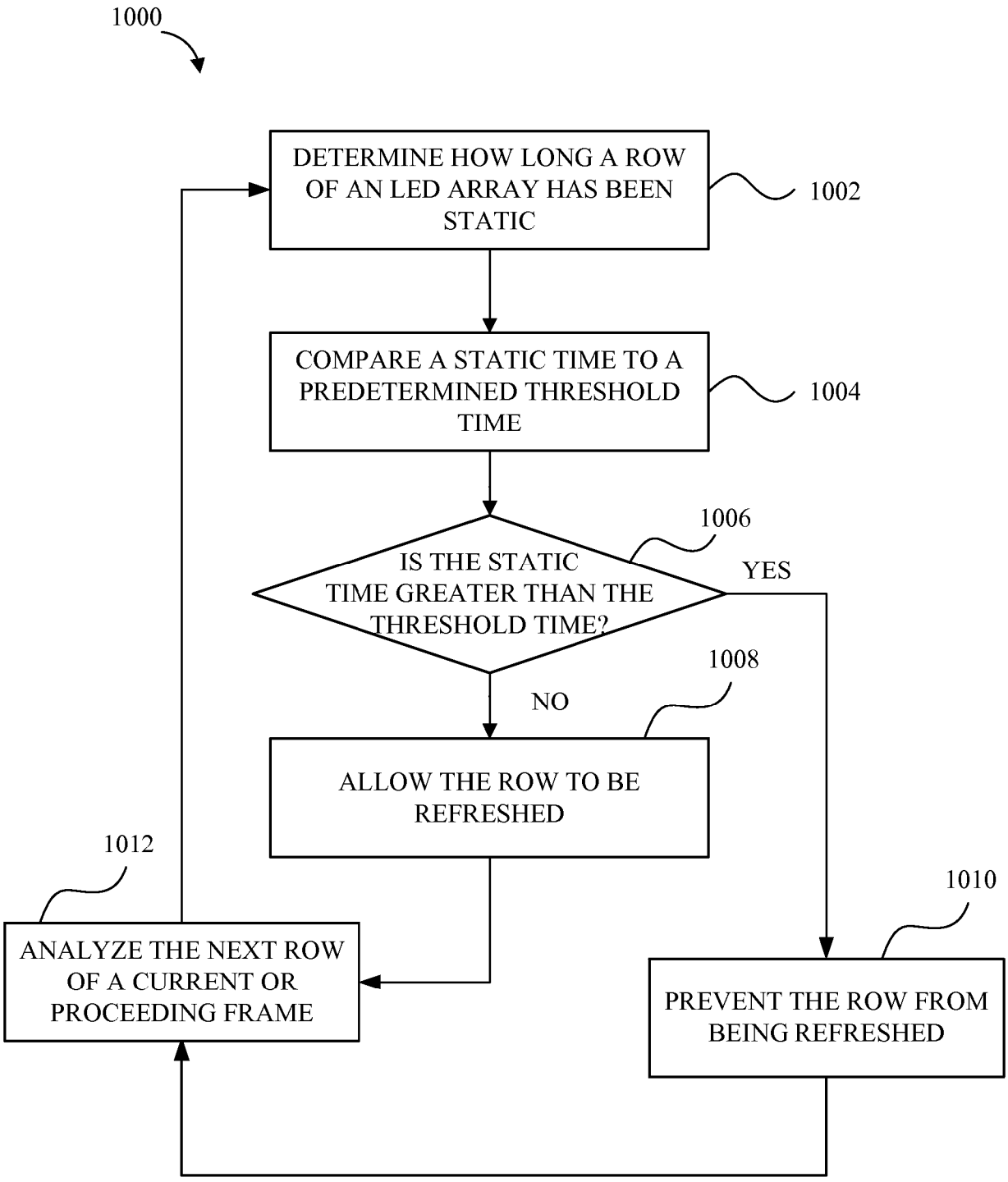

1000
DETERMINE HOW LONG A ROW OF AN LED ARRAY HAS BEEN STATIC
1002
COMPARE A STATIC TIME TO A PREDETERMINED THRESHOLD TIME
1004
1006
IS THE STATIC TIME GREATER THAN THE THRESHOLD TIME?
YES
NO
1008
ALLOW THE ROW TO BE REFRESHED
1012
ANALYZE THE NEXT ROW OF A CURRENT OR PROCEEDING FRAME
1010
PREVENT THE ROW FROM BEING REFRESHED

FIG. 10

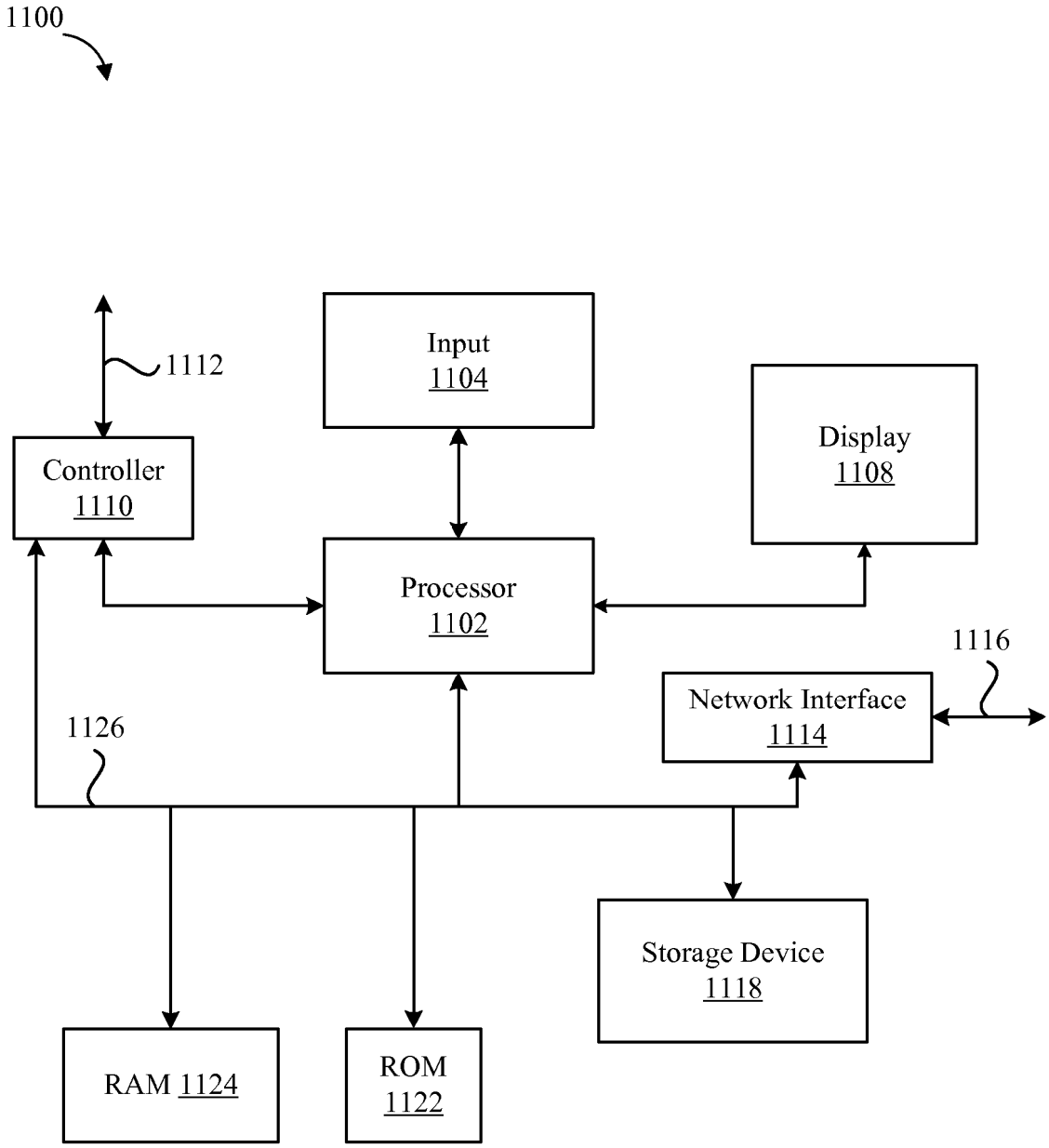

1100
1112
Input
1104
Display
1108
Controller
1110
Processor
1102
1116
Network Interface
1114
1126
Storage Device
1118
RAM 1124
ROM
1122

FIG. 11

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20140085276 A **[0004]**
- US 20130208189 A1 **[0005]**